DRAM DIE

16 MEG DRAM

MT4LC4M4B1D24A, MT4LC4M4E8D24A,
MT4LC1M16C3D24A, MT4LC1M16E5D24A

FEATURES

- Single 3.3V (x4, x16) power supply
- Industry-standard x4, x16 timing and functions
- High-performance CMOS silicon-gate process
- All inputs and outputs are TTL-compatible
- 5V-tolerant I/Os
- Refresh modes: $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$(CBR), and HIDDEN
- FAST PAGE MODE or Extended Data-Out (EDO) access cycle
- 2,048 cycle refresh (32ms) on x4
- 1,024 cycle refresh (16ms) on x16

GENERAL PHYSICAL SPECIFICATIONS

- Wafer thickness = 18.5 mil ±0.5 mil for x4
- Wafer thickness = 12.0 mil ±0.5 mil for x16
- Backside wafer surface of polished bare silicon
- Typical lower level metal thickness is 5.7K angstroms
- Typical top level metal thickness is 10.5K angstroms
- Metalization composition: 99.5% Al and 0.5% Cu over Titanium
- Typical topside passivation: 4K angstroms nitride over 10K angstroms of undoped oxide
- Typical passivation openings: 4.5 x 4.5 mil (114 x 114 µm)
- Product is a lead-over chip (LOC) design; bond pads are in the center of the die

OPTIONS — ORDER NUMBER

- Speed probing*
  - 70ns access — -7**
  - 80ns access — -8
- Form
  - Die — D
  - Wafer (6" wafer) — W
- Testing levels†
  - Standard Probe — C1
  - Speed Probe — C2

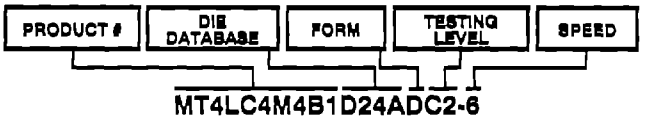
*Refer to "Speed Probing" section of this data sheet. Speed designator should not be included in die part number for C1 level product.
**Available as C2 level product only.
†Refer to "Die Testing Procedures" section of this data sheet.

DIE DATA BASE D24A
DIE OUTLINE (see page 4)

Die Size: 262 x 569 mil
6,655 x 14,453 µm
See Bond Pad Location and Identification Table.

ORDER INFORMATION

- FAST PAGE MODE
  - 4 Meg x 4 — MT4LC4M4B1D24A
- EDO
  - 4 Meg x 4 — MT4LC4M4E8D24A
- FAST PAGE MODE
  - 1 Meg x 16 — MT4LC1M16C3D24A
- EDO
  - 1 Meg x 16 — MT4LC1M16E5D24A



GENERAL DESCRIPTION

Micron DRAMs are fabricated using an advanced CMOS process. The MT4LC1M16 and MT4LC4M4 are randomly accessed solid-state memories organized in a 1 Meg x 16 or 4 Meg x 4 configuration.

DIE TESTING PROCEDURES

Most Micron products are tested to Standard Probe (C1) level. Selected products are available as Speed Probe (C2) level.

STANDARD PROBE (C1)

Micron probes wafers at a temperature with limits guardbanded to assure product performance from 0°C to 70°C in Micron's standard package. Since the package environment is not within Micron's control, the user must determine the necessary heat sinking requirements to ensure that the die junction temperature remains within specified limits. A high voltage functional stress test will be performed at probe to assure minimum junction break-

DIE TESTING PROCEDURES (continued)

down integrity. V_{BB} (substrate bias voltage) is a forced condition at wafer probe.

Wafer probe consists of various functional and parametric tests of each die. Test patterns, timing, voltage margins, limits and test sequence are determined by individual product yields and reliability data.

Micron retains a wafer map of each wafer as part of the probe records along with a lot summary of wafer yields for each lot probed. Micron reserves the right to change the probe program at any time to improve the reliability, packaged device yield or performance of the product.

Die users may experience differences in performance relative to our data sheets. This is due to differences in package capacitance, inductance, resistance and trace length.

SPEED PROBE (C2)

In addition to the testing performed at Standard Probe (C1), Micron also offers Speed Probe (C2). Micron's Hot Chuck Speed Probe assures the speed performance of die products for the fastest speed grades. Speed Probe tests for most data sheet parameters, and may increase the yield over C1-level. C2-level die have not received burn-in, and are still subject to infant mortality failures.

FUNCTIONAL SPECIFICATIONS

Please refer to the packaged product data sheets found in the applicable Micron data book, for functional and parametric specifications. The specifications are provided for reference only on C1- and C2-level die product. On C2 product ^{t}RAC and ^{t}CAC are guaranteed.

DIE AND WAFER LEVEL CONSIDERATIONS

C2-level wafers are shipped with a user's wafer map indicating speed. Users should be aware that there may be multiple speed grades on wafers shipped with a C2 level.

BONDING INSTRUCTIONS

The D24A DRAM die has 57 bond pads. Refer to the bond pad location and identification table for a complete list of bond pads and coordinates.

The D24A DRAM die is available in two separate configurations: 4 Meg x 4 or 1 Meg x 16. Each of these configurations can operate through a bonding option, in either FAST PAGE MODE (FPM) or Extended Data-Out (EDO). Connecting bond pad 5 (OPT) to Vcc allows the device to operate with EDO access cycles. Leaving bind pad 5 open (not bonded) allows the device to operate with FPM access cycles.

The D24A DRAM die has an internal substrate bias generator for normal operation. Bond pad 57 V_{BB} is used for manufacturing tests only, and is to be left open (not bonded). All Vcc and Vss pads must be bonded. It is important that the back of the die be kept isolated from any other devices sharing a common package or substrate, since the die substrate is internally driven to a negative voltage.

The die also has several pads defined as "Do Not Use." These pads are used for engineering purposes and should NOT be used. Bonding these pads could result in nonfunctional die.

WAFER SAW

Standard wafer saw cuts the die 100 percent through. Micron holds die dimensions to a maximum tolerance of +0/-1 mil of each cut, as measured from the vertical cut. For clarification purposes, the die size provided is measured from center to center of the die street. A finished die is approximately 1.5 mils smaller on each side due to the sawing operation. As an example, a 262 mil x 569 mil die is approximately 260.5 mil x 567.5 mil after sawing.

PACKAGING

For packaging, Micron utilizes Gel-Pak®. Additional information can be found in technical note TN-00-03, "Using Gel-Pak Trays with Micron Die." We package all die with the top metalization consistently oriented (refer to Figure 1). External packaging is suitable for electrostatic discharge protection. Each tray is individually self-locking or closed with a conductive clip and labeled with the following information:

- Generic device type and data base (Example: MT4LC4M4B1D24A)
- Micron fabrication lot number
- Speed grade of the die (optional)
- Quantity of die in package

STORAGE REQUIREMENTS

Micron die products are packaged in a cleanroom environment for shipping. Upon receipt, the customer should transfer the Gel-Pak to a similar environment for storage. Micron recommends the die be maintained in a filtered nitrogen atmosphere until removed for assembly. The moisture content of the storage facility should be maintained at 30% ±10% relative humidity. ESD damage precautions are necessary during handling. The die must be in an ESD-protected environment at all times for inspection and assembly.

PRODUCT RELIABILITY MONITORS

Reliability of all packaged products is monitored by ongoing QA reliability evaluations. Micron's QA department samples product families on a continuous basis for reliability studies. These studies include high temperature operating life (HTOL) tests for failure in time (FIT) calculations and high temperature steady state (HTSS) tests to monitor electromigration reliability. A summary of these product family evaluations is published on a regular basis.

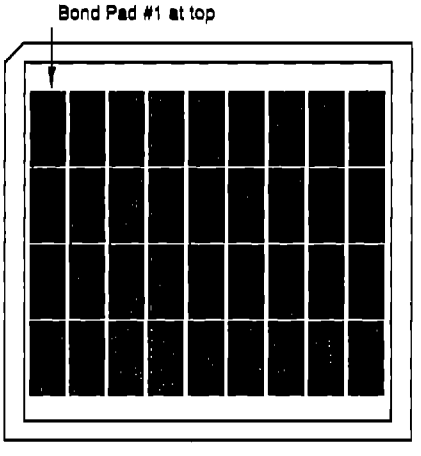
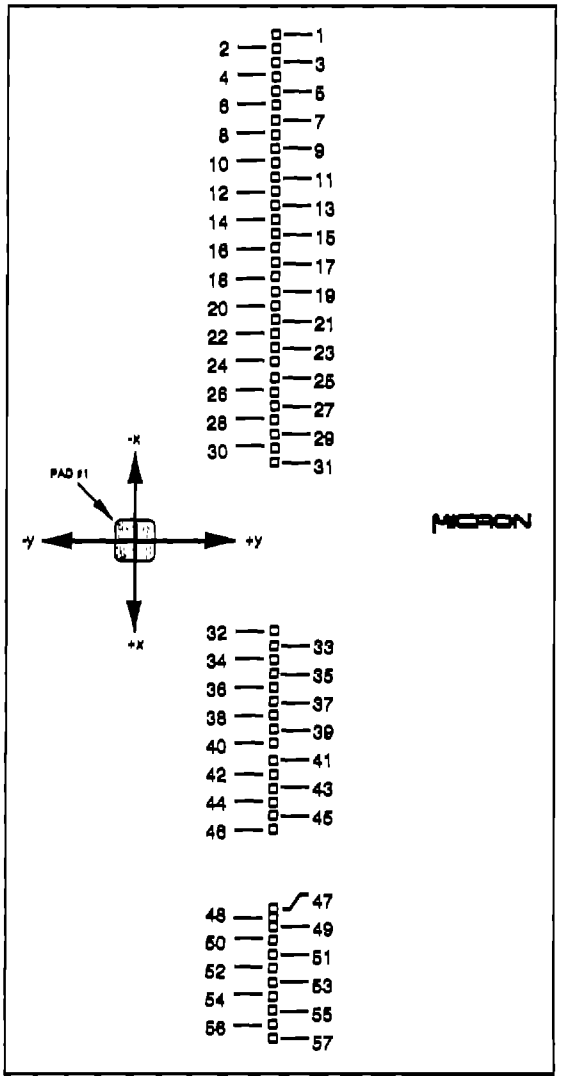


Figure 1
ORIENTATION OF DIE IN GEL-PAK

BOND PAD LOCATION AND IDENTIFICATION TABLE

			FROM CENTER OF #1			
PAD #	4 MEG x 4	1MEG x 16	"X"[1] INCHES	"Y"[1] INCHES	"X"[1] MICRONS	"Y"[1] MICRONS
1	Vss	Vss	0.000000	0.000000	0.0	0.0
2	Vss	Vss	0.007998	0.000000	203.1	0.0
3	Vcc	Vcc	0.016004	0.000000	406.5	0.0
4	Vcc	Vcc	0.024019	0.000000	610.1	0.0
5	OPT[2]	OPT	0.033447	0.000000	849.6	0.0
6	DNU[3]	DNU	0.041693	0.000000	1,059.0	0.0
7	DNU	DNU	0.049700	0.000000	1,262.4	0.0
8	DNU	DQ16	0.059992	0.000000	1,523.8	0.0
9	DQ4	DQ15	0.067836	0.000000	1,723.0	0.0
10	DQ1	DQ1	0.075971	0.000000	1,929.7	0.0
11	DNU	DQ2	0.083815	0.000000	2,128.9	0.0
12	DNU	DQ14	0.091949	0.000000	2,335.5	0.0
13	DQ3	DQ13	0.099793	0.000000	2,534.8	0.0
14	DQ2	DQ3	0.107928	0.000000	2,741.4	0.0
15	DNU	DQ4	0.115772	0.000000	2,940.6	0.0
16	$\overline{WE}$	Vss	0.124086	0.000000	3,151.8	0.0
17	$\overline{CAS}$	Vcc	0.132364	0.000000	3,362.6	0.0
18	$\overline{OE}$	DNU	0.140887	0.000000	3,578.5	0.0
19	DNU	DQ12	0.149467	0.000000	3,796.5	0.0
20	DNU	DQ11	0.157311	0.000000	3,995.7	0.0
21	DNU	DQ5	0.165446	0.000000	4,202.3	0.0
22	DNU	DQ6	0.173289	0.000000	4,401.8	0.0
23	DNU	DQ10	0.181424	0.000000	4,608.2	0.0
24	DNU	DQ9	0.189268	0.000000	4,807.4	0.0
25	DNU	DQ7	0.197403	0.000000	5,014.0	0.0
26	DNU	DQ8	0.205246	0.000000	5,213.3	0.0
27	$\overline{RAS}$	DNU	0.213561	0.000000	5,424.5	0.0
28	A9	$\overline{CASL}$	0.221807	0.000000	5,633.9	0.0
29	DNU	DNU	0.230053	0.000000	5,843.4	0.0
30	DNU	$\overline{CASH}$	0.238300	0.000000	6,052.8	0.0
31	DNU	$\overline{WE}$	0.246546	0.000000	6,262.3	0.0
32	DNU	DNU	0.324075	0.000283	8,231.5	7.2
33	DNU	$\overline{OE}$	0.332321	0.000283	8,441.0	7.2
34	DNU	$\overline{RAS}$	0.340567	0.000283	8,650.4	7.2
35	DNU	A9	0.348813	0.000283	8,859.9	7.2
36	DNU	DNU	0.357060	0.000283	9,069.3	7.2
37	A8	A8	0.365306	0.000283	9,278.8	7.2
38	A10	DNU	0.373552	0.000283	9,488.2	7.2
39	A7	A7	0.381798	0.000283	9,697.7	7.2
40	A0	A0	0.390044	0.000283	9,907.1	7.2
41	A6	A6	0.398290	0.000283	10,116.6	7.2
42	A1	A1	0.406537	0.000283	10,326.0	7.2
43	A5	A5	0.414783	0.000283	10,535.5	7.2
44	A2	A2	0.423029	0.000283	10,744.9	7.2
45	A4	A4	0.431275	0.000283	10,954.4	7.2
46	A3	A3	0.439521	0.000283	11,163.8	7.2
47	DNU	DNU	0.467068	-0.000017	11,863.5	-0.4
48	DNU	DNU	0.472138	-0.000017	11,992.3	-0.4
49	DNU	DNU	0.477207	-0.000017	12,121.1	-0.4
50	DNU	DNU	0.482816	0.000283	12,263.5	7.2
51	DNU	DNU	0.490831	0.000283	12,467.1	7.2
52	DNU	DNU	0.499308	0.000283	12,682.4	7.2
53	Vss	Vss	0.507323	0.000283	12,886.0	7.2
54	Vss	Vss	0.515338	0.000283	13,089.6	7.2
55	Vcc	Vcc	0.523353	0.000283	13,293.2	7.2
56	Vcc	Vcc	0.531368	0.000283	13,496.7	7.2
57	Vss	Vss	0.539383	0.000283	13,700.3	7.2

DIE OUTLINE (Top View)



Wafer diameter: 150mm

Wafer thickness: 18.5 mil ±0.5 mil for x4
12.0 mil ±0.5 mil for x16

Die size: 262 x 569 mil
(stepping interval) 6,655 x 14,453 µm

Bond pad size: 5.3 x 5.3 mil
134 x 134 µm

Passivation Openings: 4.5 x 4.5 mil
(typical) 114 x 114 µm

NOTE: 1. Reference to center of each bond pad from center of bond pad #1.
2. Option pin: EDO = Vcc, FPM = OPEN.
3. DNU stands for "do not use."