Four Digit Counter / Display Drivers

FEATURES

- Minimum interface required to drive most common types of LED, fluorescent, seven segment displays
- Large output current capability on seven segment outputs, typically 25mA with 1V drop
- Fully synchronous up/down counting operation
- Look ahead carry for error free outputs when reversing count direction
- Internal oscillator needing no external components for operating the digit select counter
- Four digit select outputs with inversion control for display driving flexibility
- Multiplexed BCD outputs and serial output from storage register is available
- TTL/DTL compatible on inputs and outputs
- Blanking action of Reset Input
- Counting rate up to 600 kHz

DESCRIPTION

The Four Digit Counter Display Driver is an LSI subsystem designed for application in counting display systems such as frequency counters, digital voltmeters, digital timers, event counters using 7 segment numeric displays. It contains a 4 decade up/down synchronous BCD counter, a storage register, multiplexing circuits, internal oscillator for digit selection and 7 segment decoder to count and display up to 9999.

Built-in control circuits provide flexibility of use with a minimum of external components.

The device is constructed on a single monolithic chip using MTNS P-channel enhancement mode transistors.

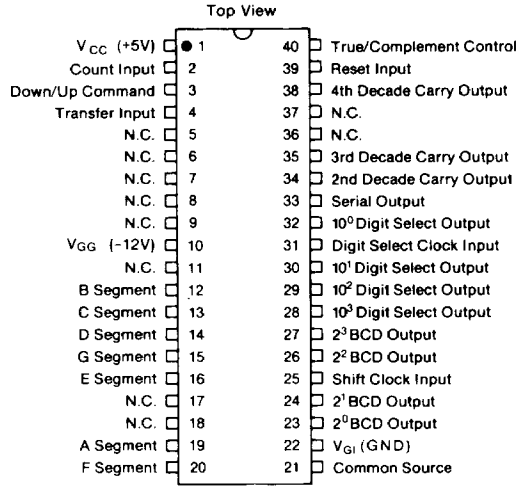
AY-5-4007A, available in 40 Lead Dual In Line package, allows for all available functions.

The AY-5-4007 and AY-5-4007D incorporate the most commonly used features in 24 Lead Dual In Line packages.

PIN CONFIGURATION

40 LEAD DUAL IN LINE
AY-5-4007A

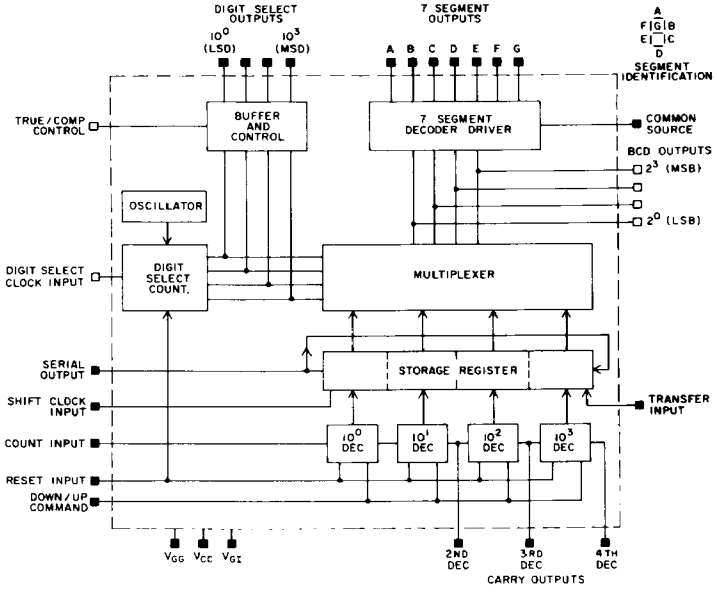
Top View



BLOCK DIAGRAM

AY-5-4007A shown:

■ indicates functions available with the AY-5-4007D.

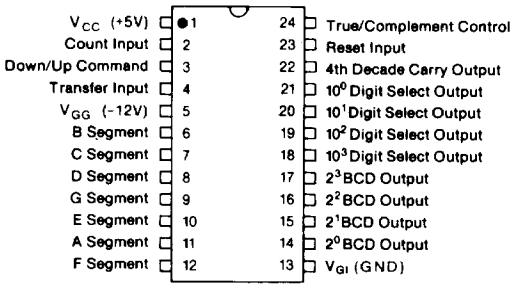


CONSUMER

PIN CONFIGURATIONS

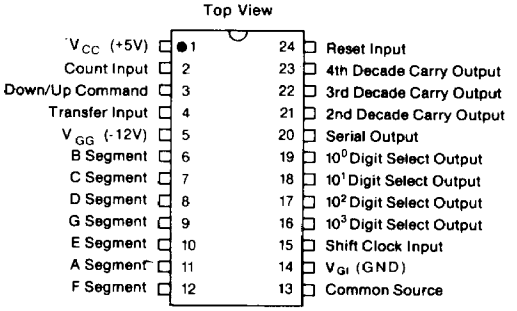
24 LEAD DUAL IN LINE
AY-5-4007

Top View



24 LEAD DUAL IN LINE
AY-5-4007D

Top View



NOTE: For AY-5-4007D, True/Complement control is internally connected to logic "0" level.

PIN FUNCTIONS

Name	Function
COUNT INPUT	Count Input operates the decade counters synchronously on the positive going edges (logic '0' to '1' transitions).
RESET INPUT	When this input goes to a logic '1' it resets the decade counters to 0000, forces the digit select counter to the MSD position and the Digit Select Outputs to 'not active' logic levels to blank the display. It must be present for a minimum of 10 μsec.
DOWN/UP COMMAND	The count direction depends upon the logic level on the DOWN/UP Command input. Logic '0' = Count UP. Logic '1' = Count DOWN.
2ND DECADE CARRY OUTPUT **3RD DECADE CARRY OUTPUT** **4TH DECADE CARRY OUTPUT**	Normally the Carry Outputs are at a logic '0' level; when activated a positive pulse is generated on the output line, which is identical with the Count Input causing the carry.
TRANSFER INPUT	Placing the Transfer Input at a logic '1' allows transfer of data from the decade counters to the storage register.
SHIFT CLOCK INPUT	This input is used to apply clock pulses to the storage register for serial shift operation. Normally Shift Clock is maintained at a Logic '1' and negative pulses are necessary to perform shift operation. Actual shifting of storage register data is done on the second edge (positive going) of each clock pulse. A Pull-up resistor is internally provided for the Shift Clock Input so that this line, if not used, may be left floating. Since the storage register is quasi-static in serial shift operation the width of negative pulses (at logic '0') has to be limited to 20 μsec. During serial shift operation the Transfer input must be at a logic '0'.
SERIAL OUTPUT	This is the serial output of the storage register. When serial shift operation is not performed the Serial Output is the least significant bit of the least significant digit of the storage register.
10^0 DIGIT SELECT OUTPUT (LSD) **10^1 DIGIT SELECT OUTPUT** **10^2 DIGIT SELECT OUTPUT** **10^3 DIGIT SELECT OUTPUT (MSD)**	These outputs provide sequentially an active logic level (logic '1' if the True/Complement Control is at a logic '1'; logic '0' if the True/Comlement Control is at a logic '0'), to specify which of the corresponding digits is selected and displayed, the remaining 3 Outputs being 'not active'. All the Digit Select Outputs are forced to a 'not active' logic level as long as the Reset Input is active.
2^0 BCD OUTPUT(LSB) **2^1 BCD OUTPUT** **2^2 BCD OUTPUT** **2^3 BCD OUTPUT(MSB)**	These outputs provide the Binary Coded Decimal representation of the digit being selected and displayed by the multiplexer. The truth table shows BCD Codification of these outputs.
"A" TO "G" SEGMENT	These outputs are programmed according to the truth table. Each output terminal is actually connected to the drain of the corresponding output transistor.
COMMON SOURCE	This is the common of the seven segment output transistors. When not externally available the corresponding terminal is internally tied to VGI (0V) line. It may be connected to any voltage between VSS and VDD according to requirements.
TRUE/COMPLEMENT CONTROL	This input controls the polarity of the Digit Select Outputs active logic level. When the TRUE/COMPLEMENT Control is at a logic '1', active level for the Digit Select Outputs is a logic '1', when at a logic '0' active level is a logic '0'.
DIGIT SELECT CLOCK INPUT	An external signal applied to this terminal overrides the internal oscillator. When the internal oscillator is used, this terminal must be left floating.

CONSUMER

ELECTRICAL CHARACTERISTICS

Maximum Ratings *

Voltage on any pin with respect to V_{CC} . . . . . −20 to +0.3V
Storage temperature range . . . . . −65°C to +150°C
Ambient operating temperature range . . . . . 0°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions is not implied—operating ranges are specified below.

Standard Conditions (unless otherwise noted)

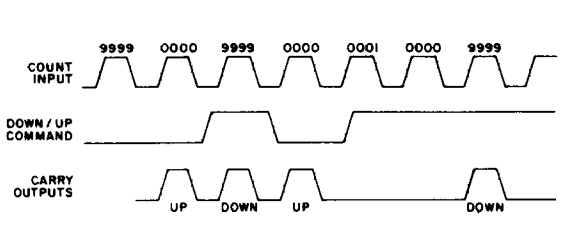
V_{CC} = +5.0 ±0.5V V_{GG} = −12V ±1V OR −7.0V ±0.5V
V_{GI} = 0V Operating Temperature (T_A) 0°C to +70°C

Characteristic	V_{GG} = −12V ±1V			V_{GG} = −7V ±0.5V			Units	Conditions
	Min	Typ**	Max	Min	Typ**	Max		
Inputs								
Logic '0'	V_{GG}	-	+0.8	V_{GG}	-	+0.8	Volts	See Fig. 4.
Logic '1'	V_{CC}−1.5	-	V_{CC}+0.3	V_{CC}−1.5	-	V_{CC}+0.3	Volts	
Capacitance	-	-	10.0	-	-	10.0	pF	V_{IN} = V_{CC} f= 1MHz
Leakage	-	-	5.0	-	-	5.0	µA	V_{IN} − V_{CC} = −10V at 25°C
Repetition Rate	D.C.	-	600	D.C.	-	350	kHz	Square Wave
Pulse Width	0.7	-	-	1.0	-	-	µsec	Pulse either high or low
Tr & Tf	-	-	100			100	µsec	
True/Complement/ Control Input								
Input Current	10	40	100	10	-	50	µA	V_{IN} = V_{CC}
	10	25	50	10	-	25	µA	V_{IN} = V_{GI} See Fig. 5
Digit Select Clock								
Input Current	10	60	150	5	25	75	µA	V_{IN} = V_{CC} (Sink)
	50	250	1600	50	150	1000	µA	V_{IN} = V_{GI} (Source) See Fig. 3.
Internal Freq.	1.0	2.0	4.0	1.0	2.0	4.0	kHz	
External Freq.—Data only	D.C.	-	100	D.C.	-	50	kHz	
Display	D.C.	-	15	D.C.	-	7	kHz	Display Duty Cycle 25%
Shift Clock								
Frequency	D.C.	-	1	D.C.	-	0.8	MHz	
Pulse Width	0.4	-	1000	0.5	-	1000	µsec	See functional description
Input Current	20	100	400	10	30	200	µA	V_{IN} = V_{GI} (See Fig. 6)
Outputs—7 Segment (See Note 2)								
Leakage Current	-	-	10	-	-	10	µA	V_{OUT}—V_{CC} = −10V at 25°C
Device on Current	15	25	45	12	20	35	mA	V_{CS}—V_{OUT} = +1.0V at 25°C, V_{CS} = V_{CC}
Device on Current	12	18	27	7	11	17	mA	V_{CS}—V_{OUT} = −1.0V at 25°C, V_{CS} = V_{GI}
Power Dissipation (per segment at 25°C)	-	-	200	-	-	200	mW	See Note 1 & Fig. 1
Other Outputs								
Logic '0'	-	0.2	0.4	-	0.3	0.4	Volts	I_{OL} = 1.6mA with 10pF load
Logic '1'	V_{CC} −1.0	V_{CC} −0.65	-	V_{CC} −1.0	V_{CC} −0.65	-	Volts	I_{OL} = 50µA
Propagation Delay	-	-	1.0	-	-	1.5	µsec	Carry Output } See Fig. 2
			1.5	-	-	2.0	µsec	Serial Output }
Tr, Tf Rise, Fall Times	-	0.15	0.3	-	0.3	0.6	µsec	
Power								
I_{GG}	-	25	40	-	13	20	mA	(V_{CC} to V_{GG})

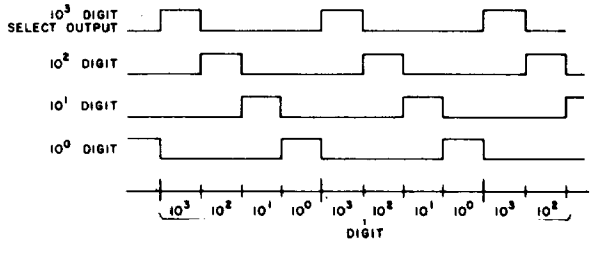
**Typical values are at +25°C and nominal voltages.

NOTES:
1. Derate Power Linearly to 100mW at 70°C.
2. See also Typical 7-Segment Output Curves, Figs. 9, 11, & 13 (−12V ±1V)
   See also Typical 7-Segment Output Curves, Figs. 10, 12, & 14 (−7V ±0.5V)

TIMING DIAGRAMS



CARRY OPERATION



DIGIT SELECT OPERATION
(True/Complement Control is at logic '1' level)

CONSUMER

OPERATION

Decade Counters

The four decade counters are synchronously operated on the positive going edges of the Count Input; a single DOWN/UP Command controls the direction of counting. The edge-triggered structure of the master-slave flip-flops allows the count direction to be changed between count pulses at either Count Input level. A Reset Input resets decade counters to 0000.

Carry outputs are provided at the 2nd, 3rd and 4th decade; these outputs are activated when an overflow (in counting up) or an underflow (in counting down) condition exists in the corresponding decade counter. The carry output pulse is the same as the Count Input pulse causing the carry.

The look ahead design of the carry stages gives error free outputs when reversing the count direction.

Storage Register

Data in the decade counters is transferred to the storage register under control of the Transfer Input signal. The Transfer Input may be connected to a logic '1' for a continuous transfer and display operation.

The Storage register may also be operated as a parallel-in serial-out shift register. In this case clock pulses are to be provided to Shift Clock Input, the serial content of storage register is available on the Serial Output line, and recirculated back to the first stage input. A train of 16 clock pulses is needed to extract the full content of the register, least significant bit of least significant digit first. When operating the storage register serially, Transfer input is to be kept at a logic '0'.

Digit Select Counter and Multiplexer

The digit select counter is driven by a built in oscillator which requires no external components. The internal oscillator can be overridden by applying an external signal to the Digit Select Clock Input.

The digit select counter controls the multiplexer to route information from storage register to the 7 segment decoder drivers and to the BCD Outputs.

The counter scans from MSD (10^3 digit) to LSD (10^0 digit). Each of the four Digit Select Outputs is sequentially activated when the corresponding digit is selected and displayed.

The Digit Select counter is forced to MSD position and Digit Select Outputs are forced to 'not active' logic levels as long as Reset Input is active. This feature blanks the display when the device is being reset. The True/Complement Control inverts the Digit Select Outputs active logic level for flexibility of output interface circuitry.

Internal delay logic ensures that both 7 segment outputs and BCD outputs are valid before activation of the corresponding Digit Select Output to avoid "ghost images".

7 Segment Decoder Driver

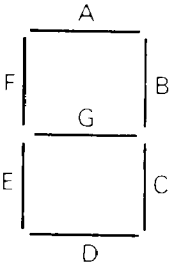
The 7 segment decoder drivers consist of very low impedance output transistors (typically 40 ohms) to minimize external interface components when driving 7 segment displays such as LEDs, fluorescents, incandescents, etc.

The 7 Segment Outputs are the drains of the corresponding output transistors, these outputs are programmed according to the truth table below. A Common Source terminal is also available to increase flexibility of use.

DIGIT	7 SEGMENT OUTPUT TRANSISTOR							BCD OUTPUT			
	A	B	C	D	E	F	G	MSB 2^3	2^2	2^1	LSB 2^0
0	*	*	*	*	*	*	–	0	0	0	0
1	–	*	*	–	–	–	–	0	0	0	1
2	*	*	–	*	*	–	*	0	0	1	0
3	*	*	*	*	–	–	*	0	0	1	1
4	–	*	*	–	–	*	*	0	1	0	0
5	*	–	*	*	–	*	*	0	1	0	1
6	*	–	*	*	*	*	*	0	1	1	0
7	*	*	*	–	–	–	–	0	1	1	1
8	*	*	*	*	*	*	*	1	0	0	0
9	*	*	*	*	–	*	*	1	0	0	1

LEGEND:
* output transistor ON
– output transistor OFF
0 logic '0'
1 logic '1'

SEGMENT IDENTIFICATION



7 SEGMENT AND BCD OUTPUTS TRUTH TABLE

CONSUMER

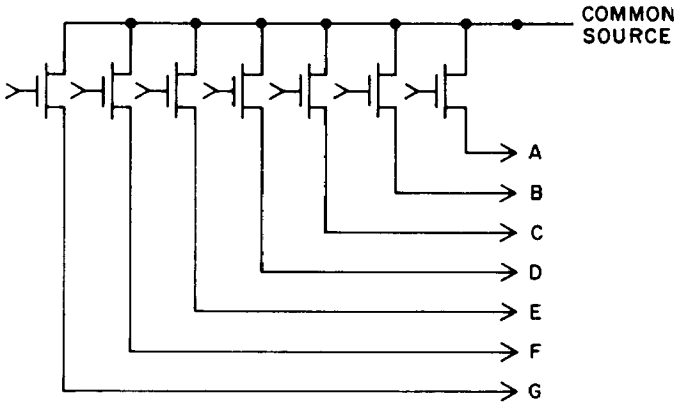


Fig.1 7-SEGMENT OUTPUTS

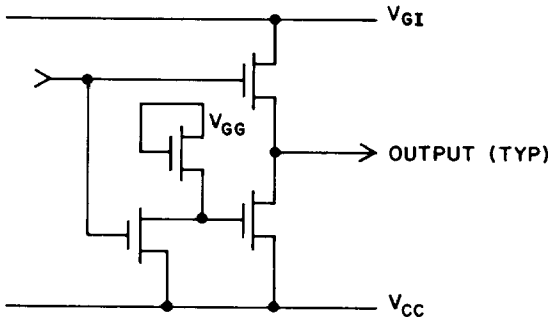


Fig.2 ALL OTHER OUTPUTS

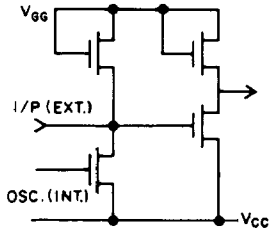


Fig.3 DIGIT SELECT CLOCK INPUT

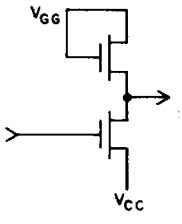


Fig.4 TYPICAL INPUT

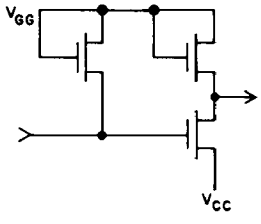


Fig.5 TRUE/COMPLEMENT INPUT

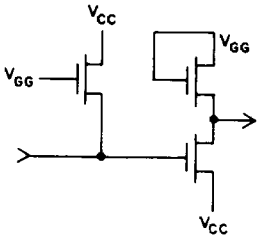


Fig.6 SHIFT CLOCK INPUT

CIRCUIT DIAGRAMS

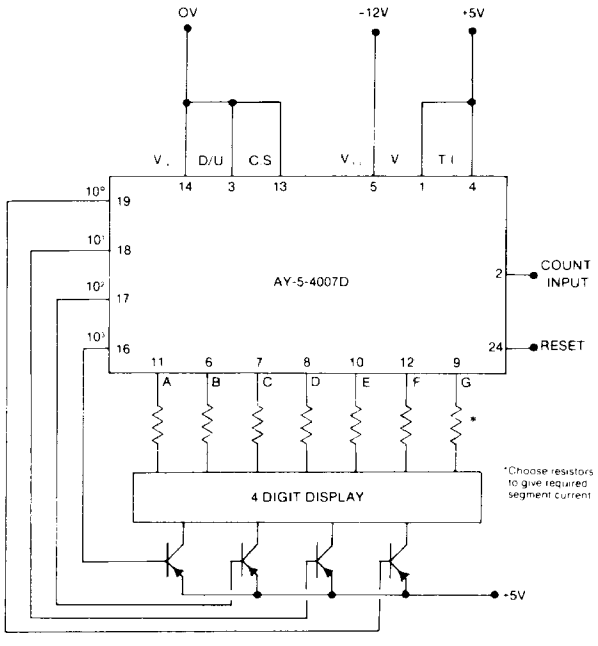


Fig.7 COMMON CATHODE LED DISPLAY

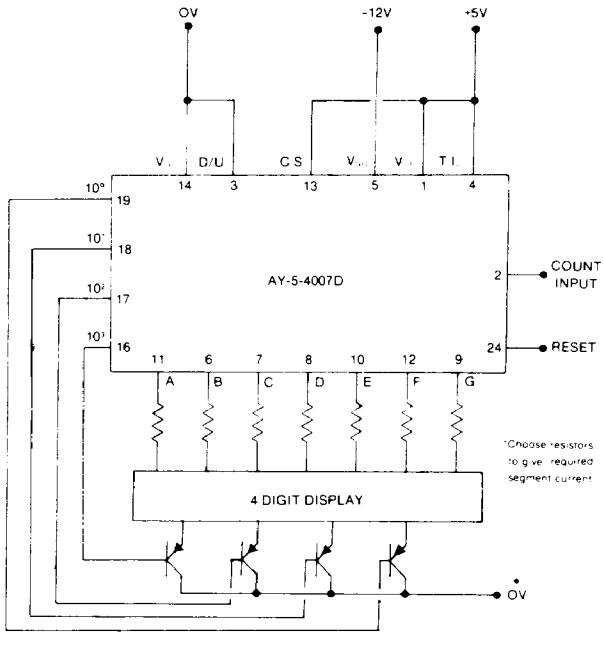


Fig.8 COMMON ANODE LED DISPLAY

CONSUMER

TYPICAL CHARACTERISTIC CURVES

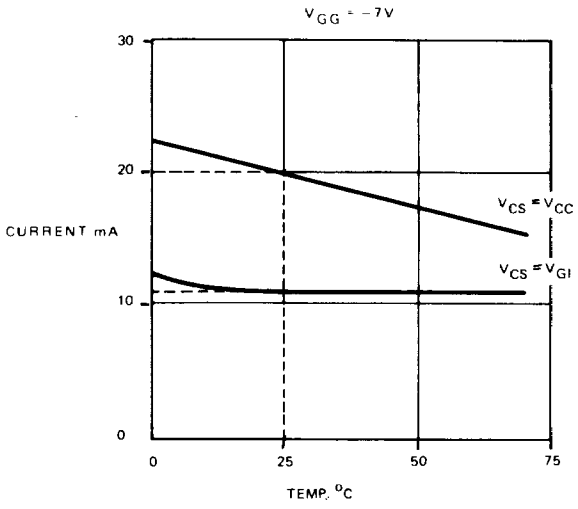


Fig.9

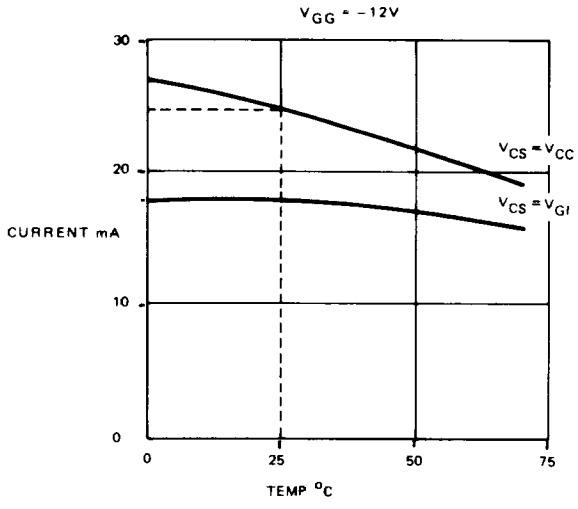


Fig.10

TYPICAL CURVES OF SEGMENT CURRENT VS. TEMPERATURE AT 1V ACROSS OUTPUT DEVICE

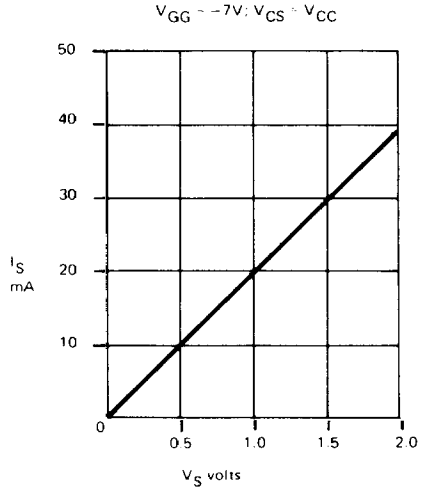


Fig.11

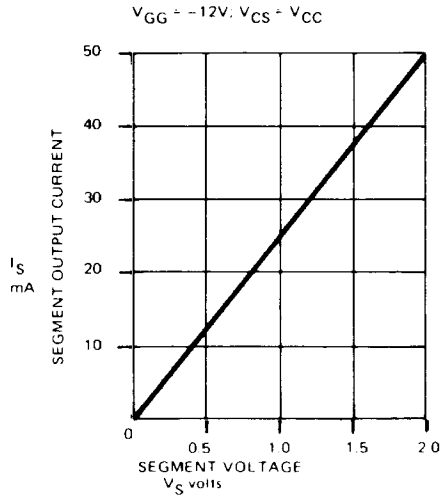


Fig.12

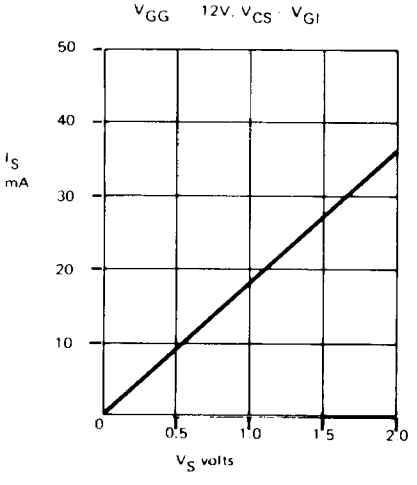


Fig.13

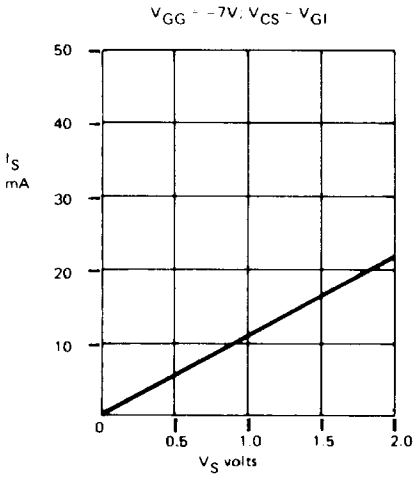


Fig.14

TYPICAL SEGMENT OUTPUT CURRENT VS. OUTPUT VOLTAGE AT +25°C

CONSUMER