

LPR200/201

16-bit Multilevel Pipeline Register

FEATURES

- Pipeline Registers — Eight 16-bit High-Speed (LPR200) or Seven 16-bit High-Speed with a Direct Feed-Through Path (LPR201)
- Programmable Multilevel Register Configurations
- Access time of 12 ns
- Hold, Shift, and Load Instructions
- Replaces IDT73200 and IDT73201
- Available 100% Screened to MIL-STD-883, Class B
- Package Styles Available:
 - 48-pin Plastic DIP
 - 48-pin Sidebraze, Hermetic DIP
 - 52-pin Plastic LCC, J-Lead
 - 52-pin Ceramic LCC

DESCRIPTION

The LPR200 and LPR201 are programmable multilevel pipeline registers. Both devices are pin-for-pin compatible with the IDT73200 and IDT73201.

The LPR200 contains eight 16-bit high-speed pipeline registers which can be configured as eight independent, 1-level pipelines; four independent, 2-level pipelines; two independent, 4-level pipelines; or as one 8-level pipeline.

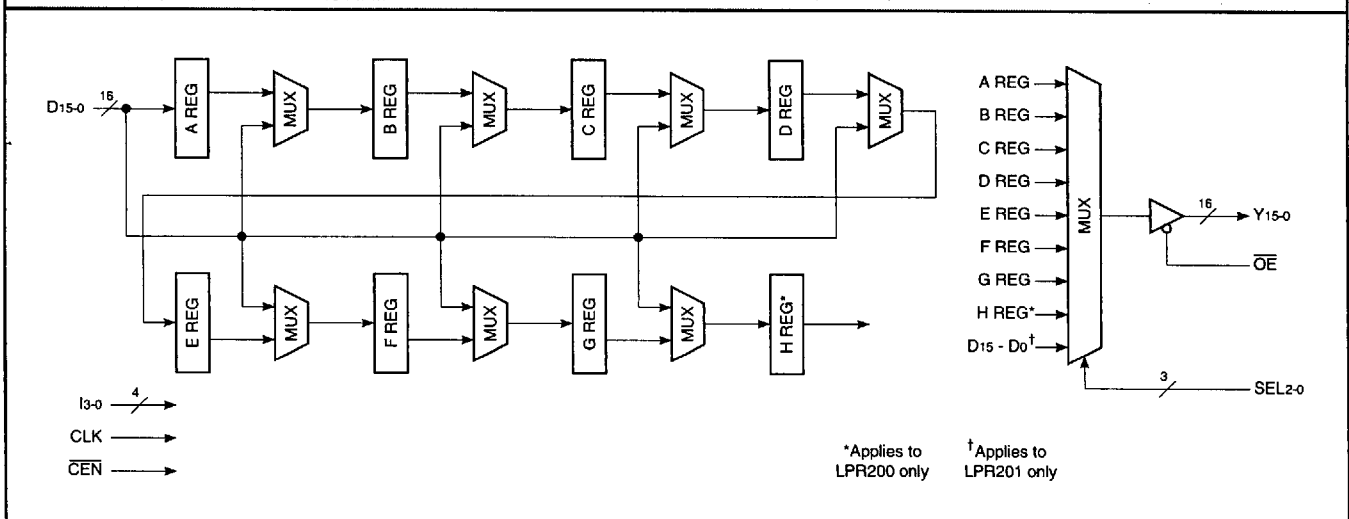
The LPR201 contains seven 16-bit high-speed pipeline registers which can be configured as seven independent, 1-level pipelines; three independent, 2-level plus one 1-level pipelines; one 4-level plus one 3-level pipeline; or as one 7-level pipeline.

The Instruction pins, I3-0, control the loading of the registers. The registers can be configured as a seven-stage delay line (eight-stage in the case of the LPR200) with data loaded into A

and shifted sequentially through B, C, D, E, F, and G (and H in the case of the LPR200) as shown in Table 1. The Instruction pins may also be set to prevent any register from changing.

The Select lines, S2-0, control an 8-to-1 multiplexer which routes the contents of any of the registers to the Y output pins. The independence of the I and S controls allow simultaneous write and read operations on different registers.

LPR200/201 BLOCK DIAGRAM



16-bit Multilevel Pipeline Register

SIGNAL DEFINITIONS

Power

VCC and GND

+5 V power supply. All pins must be connected.

Clock

CLK — Master Clock

The rising edge of CLK strobes all registers.

Inputs

D15-0 — Data Input

16-bit data input port. Data is latched into the registers on the rising edge of CLK.

Outputs

Y15-0 — Data Output

16-bit data output port.

Controls

I3-0 — Instruction Control

The instruction control pins select which register operation will be carried out. Refer to Tables 2 and 3.

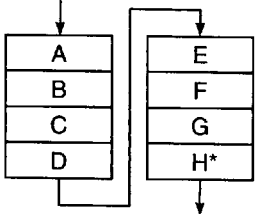
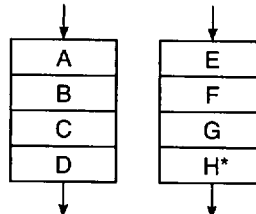
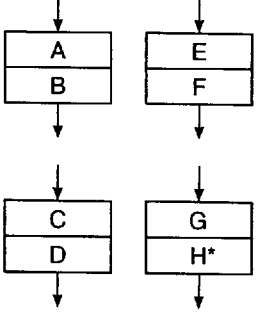
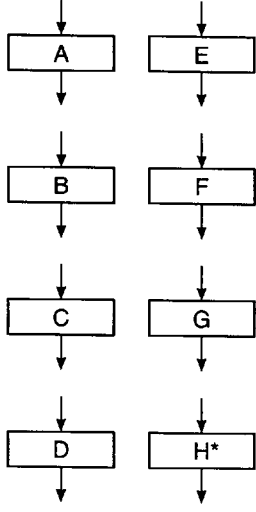
SEL2-0 — Output Select

The output select pins control which register contents will appear at the Y15-0 output pins. Refer to Tables 4 and 5.

\overline{CEN} — Clock Enable

When \overline{CEN} is LOW, the instruction designated by I3-0 is performed on the registers. When \overline{CEN} is HIGH, no register operations are performed.

TABLE 1. REGISTER LOAD OPERATIONS

<p>Single 8-Level (LPR200) Single 7-Level (LPR201)</p> 	<p>Two 4-Level (LPR200) One 4 Level, One 3-Level (LPR201)</p> 
<p>Four 2-Level (LPR200) Three 2-Level, One 1-Level (LPR201)</p> 	<p>Eight 1-Level (LPR200) Seven 1-Level (LPR201)</p> 

*Applies to LPR200 only

\overline{OE} — Output Enable

When \overline{OE} is LOW, the register data specified by SEL2-0 is available on the Y15-0 output pins. When \overline{OE} is HIGH, the output port is in a high-impedance state.

16-bit Multilevel Pipeline Register

TABLE 2. LPR200 INSTRUCTION TABLE

Mnemonics	Inputs				Description
	I ₃	I ₂	I ₁	I ₀	
LDA	0	0	0	0	D ₁₅₋₀ →A
LDB	0	0	0	1	D ₁₅₋₀ →B
LDC	0	0	1	0	D ₁₅₋₀ →C
LDD	0	0	1	1	D ₁₅₋₀ →D
LDE	0	1	0	0	D ₁₅₋₀ →E
LDF	0	1	0	1	D ₁₅₋₀ →F
LDG	0	1	1	0	D ₁₅₋₀ →G
LDH	0	1	1	1	D ₁₅₋₀ →H
LSHAH	1	0	0	0	D ₁₅₋₀ →A A→B B→C C→D D→E E→F F→G G→H
LSHAD	1	0	0	1	D ₁₅₋₀ →A A→B B→C C→D
LSHEH	1	0	1	0	D ₁₅₋₀ →E E→F F→G G→H
LSHAB	1	0	1	1	D ₁₅₋₀ →A A→B
LSHCD	1	1	0	0	D ₁₅₋₀ →C C→D
LSHEF	1	1	0	1	D ₁₅₋₀ →E E→F
LSHGH	1	1	1	0	D ₁₅₋₀ →G G→H
HOLD	1	1	1	1	ALL REGISTERS ON HOLD

TABLE 4. LPR200 OUTPUT SELECT

SEL ₂	SEL ₁	SEL ₀	Y ₁₅₋₀
0	0	0	A
0	0	1	B
0	1	0	C
0	1	1	D
1	0	0	E
1	0	1	F
1	1	0	G
1	1	1	H

TABLE 3. LPR201 INSTRUCTION TABLE

Mnemonics	Inputs				Description
	I ₃	I ₂	I ₁	I ₀	
LDA	0	0	0	0	D ₁₅₋₀ →A
LDB	0	0	0	1	D ₁₅₋₀ →B
LDC	0	0	1	0	D ₁₅₋₀ →C
LDD	0	0	1	1	D ₁₅₋₀ →D
LDE	0	1	0	0	D ₁₅₋₀ →E
LDF	0	1	0	1	D ₁₅₋₀ →F
LDG	0	1	1	0	D ₁₅₋₀ →G
HOLD	0	1	1	1	ALL REGISTERS ON HOLD
LSHAG	1	0	0	0	D ₁₅₋₀ →A A→B B→C C→D D→E E→F F→G
LSHAD	1	0	0	1	D ₁₅₋₀ →A A→B B→C C→D
LSHEG	1	0	1	0	D ₁₅₋₀ →E E→F F→G
LSHAB	1	0	1	1	D ₁₅₋₀ →A A→B
LSHCD	1	1	0	0	D ₁₅₋₀ →C C→D
LSHEF	1	1	0	1	D ₁₅₋₀ →E E→F
LDG	1	1	1	0	D ₁₅₋₀ →G
HOLD	1	1	1	1	ALL REGISTERS ON HOLD

TABLE 5. LPR201 OUTPUT SELECT

SEL ₂	SEL ₁	SEL ₀	Y ₁₅₋₀
0	0	0	A
0	0	1	B
0	1	0	C
0	1	1	D
1	0	0	E
1	0	1	F
1	1	0	G
1	1	1	D ₁₅₋₀

16-bit Multilevel Pipeline Register

MAXIMUM RATINGS <i>Above which useful life may be impaired (Notes 1, 2, 3, 8)</i>	
Storage temperature	-65°C to +155°C
Operating ambient temperature	-55°C to +125°C
V _{CC} supply voltage with respect to ground	-0.5 V to +7.0 V
Input signal with respect to ground	-0.5 V to V _{CC} + 0.5 V
Signal applied to high impedance output	-0.5 V to V _{CC} + 0.5 V
Output current into low outputs	50 mA
Latchup current	> 400 m

OPERATING CONDITIONS <i>To meet specified electrical and switching characteristics</i>		
Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V _{CC} ≤ 5.25 V
Active Operation, Military	-55°C to +125°C	4.50 V ≤ V _{CC} ≤ 5.50 V

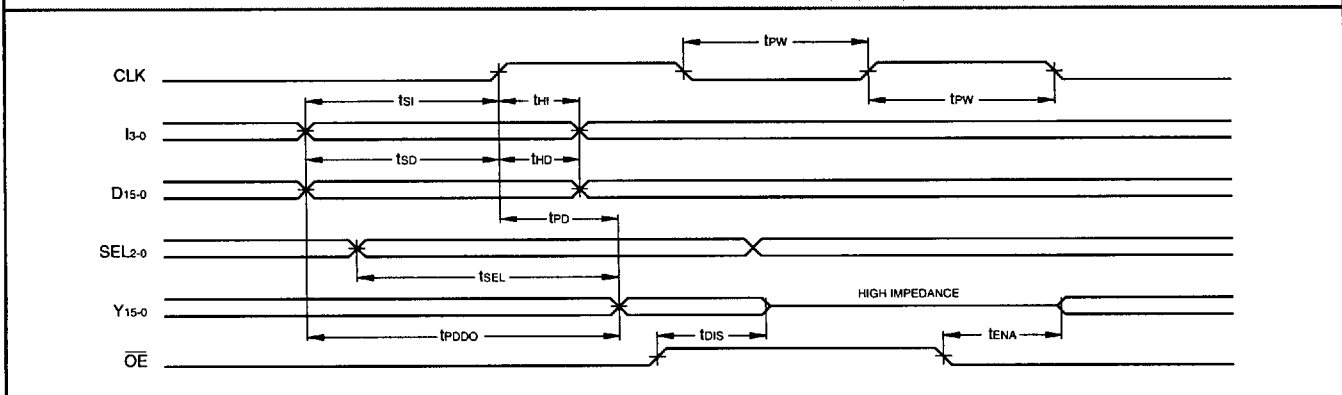
ELECTRICAL CHARACTERISTICS <i>Over Operating Conditions (Note 4)</i>						
Symbol	Parameter	Test Condition	Min	Typ	Max	Uni
V _{OH}	Output High Voltage	V _{CC} = Min., I _{OH} = -8.0 mA	2.4			V
V _{OL}	Output Low Voltage	V _{CC} = Min., I _{OL} = 16 mA			0.4	V
V _{IH}	Input High Voltage		2.0		V _{CC}	V
V _{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I _{Ix}	Input Current	Ground ≤ V _{IN} ≤ V _{CC} (Note 12)			±20	μA
I _{OZ}	Output Leakage Current	(Note 12)			±20	μA
I _{CC1}	V _{CC} Current, Dynamic	(Notes 5, 6)		10	30	mA
I _{CC2}	V _{CC} Current, Quiescent	(Note 7)		2.0	10	mA
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz			10	pF
C _{OUT}	Output Capacitance	T _A = 25°C, f = 1 MHz			12	pF

SWITCHING CHARACTERISTICS

COMMERCIAL OPERATING RANGE (0°C to +70°C) Notes 9, 10 (ns)

Symbol	Parameter	LPR200/201-					
		20		15		12	
		Min	Max	Min	Max	Min	Max
t _{CYC}	Cycle Time	20		15		12	
t _{PW}	Clock Pulse Width	5		5		5	
t _{PD}	Clock to Output Delay		20		15		12
t _{SEL}	Select to Output Delay		20		15		12
t _{PDDO}	Data In to Data Out Flowthrough Delay (LPR201)		20		15		12
t _{SI}	Instruction Setup Time	5		5		4	
t _{HI}	Instruction Hold Time	2		2		2	
t _{SD}	Data Setup Time	4		4		3	
t _{HD}	Data Hold Time	2		2		1	
t _{SC}	Clock Enable Setup Time	5		5		5	
t _{HC}	Clock Enable Hold Time	2		2		2	
t _{DIS}	Three-State Output Disable Delay (Note 11)		10		9		8
t _{ENA}	Three-State Output Enable Delay (Note 11)		15		10		9

SWITCHING WAVEFORMS

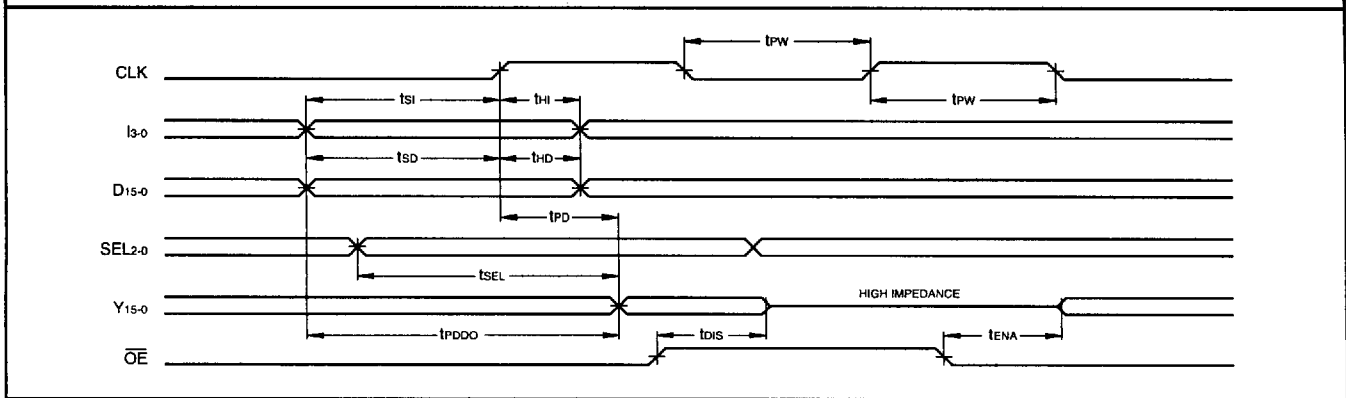


SWITCHING CHARACTERISTICS

MILITARY OPERATING RANGE (-55°C to +125°C) Notes 9, 10 (ns)

Symbol	Parameter	LPR200/201-			
		20		15	
		Min	Max	Min	Max
t _{CYC}	Cycle Time	20		15	
t _{PW}	Clock Pulse Width	6		5	
t _{PD}	Clock to Output Delay		20		15
t _{SEL}	Select to Output Delay		20		15
t _{PDDO}	Data In to Data Out Flowthrough Delay (LPR201)		20		15
t _{SI}	Instruction Setup Time	6		5	
t _{HI}	Instruction Hold Time	3		2	
t _{SD}	Data Setup Time	5		4	
t _{HD}	Data Hold Time	3		2	
t _{SC}	Clock Enable Setup Time	6		5	
t _{HC}	Clock Enable Hold Time	2		2	
t _{DIS}	Three-State Output Disable Delay (Note 11)		13		9
t _{ENA}	Three-State Output Enable Delay (Note 11)		13		10

SWITCHING WAVEFORMS



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above VCC will be clamped beginning at -0.6 V and VCC + 0.6 V. The device can withstand indefinite operation with inputs in the range of -0.5 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

4

- N = total number of device outputs
- C = capacitive load per output
- V = supply voltage
- F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 10 MHz clock rate.

7. Tested with all inputs within 0.1 V of VCC or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except tENA/tDIS test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified IOH and IOL at an output voltage of VOH min and VOL max respectively. Alternatively, a diode bridge with upper and lower current sources of IOH and IOL respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed. For tENABLE and tDISABLE measurements, the load current is increased to 10 mA to reduce the RC delay component of the measurement.

This device has high-speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

- a. A 0.1 μF ceramic capacitor should be installed between VCC and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device VCC and the tester common, and device ground and tester common.
- b. Ground and VCC supply planes must be brought directly to the DUT socket or contactor fingers.
- c. Input voltages should be adjusted to compensate for inductive ground and VCC noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from

the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. Transition is measured ±200 mV from steady-state voltage with specified loading.

12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

FIGURE 1. INPUT CIRCUIT

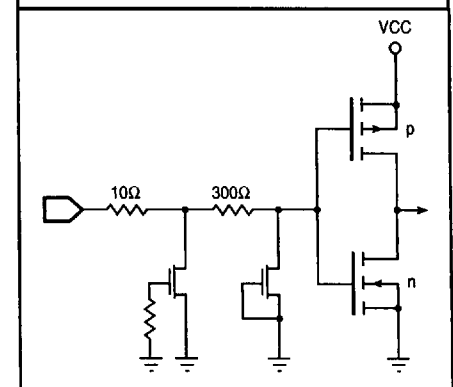


FIGURE 2. OUTPUT CIRCUIT

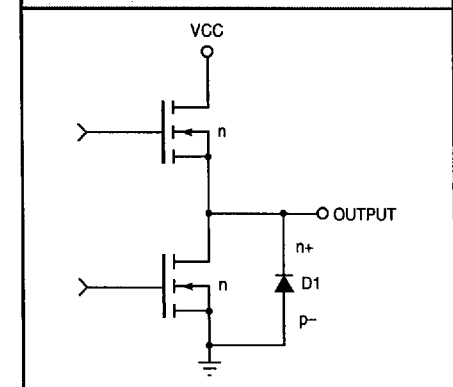
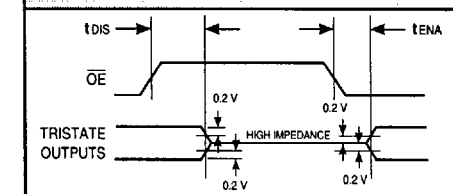
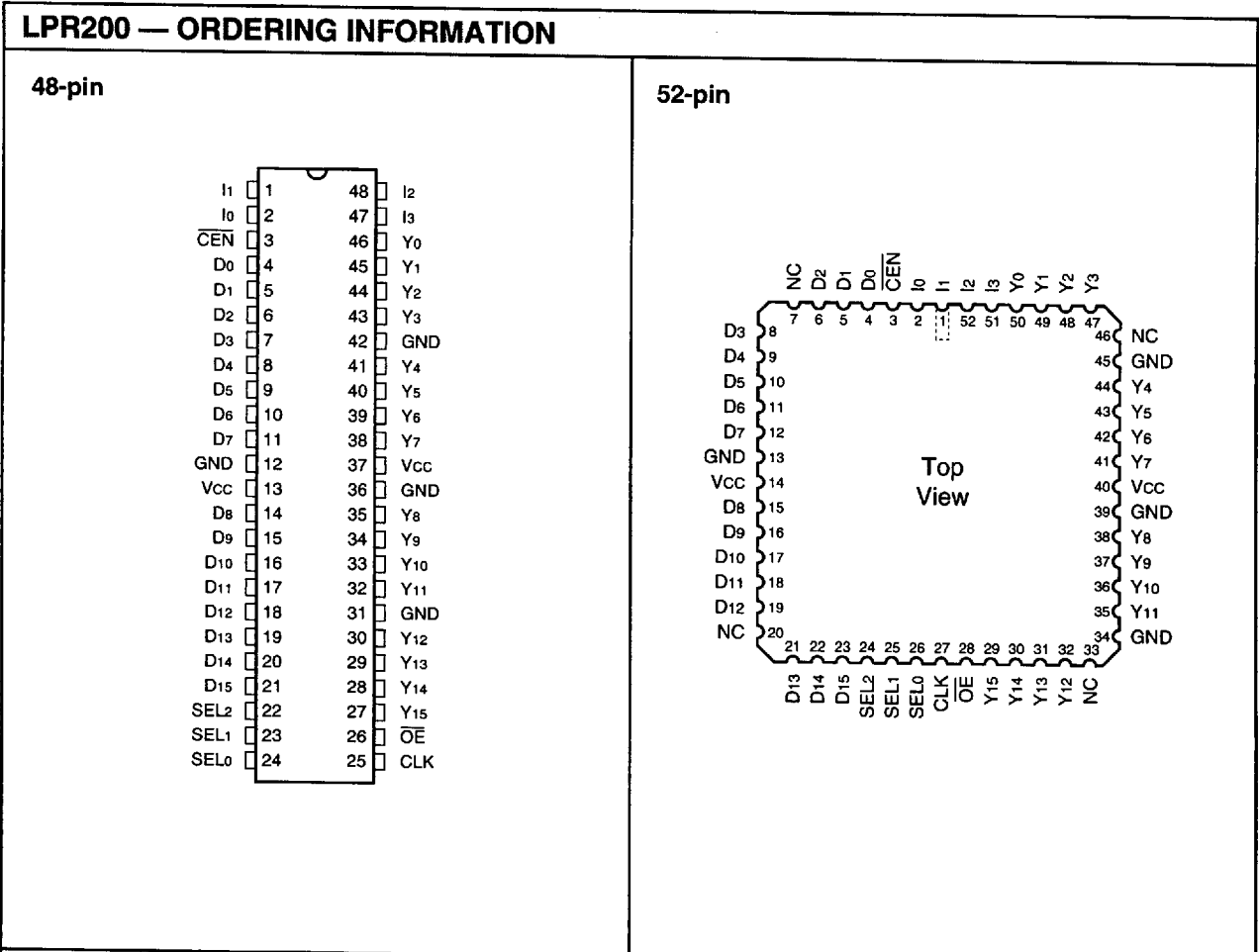


FIGURE 3. THRESHOLD LEVELS

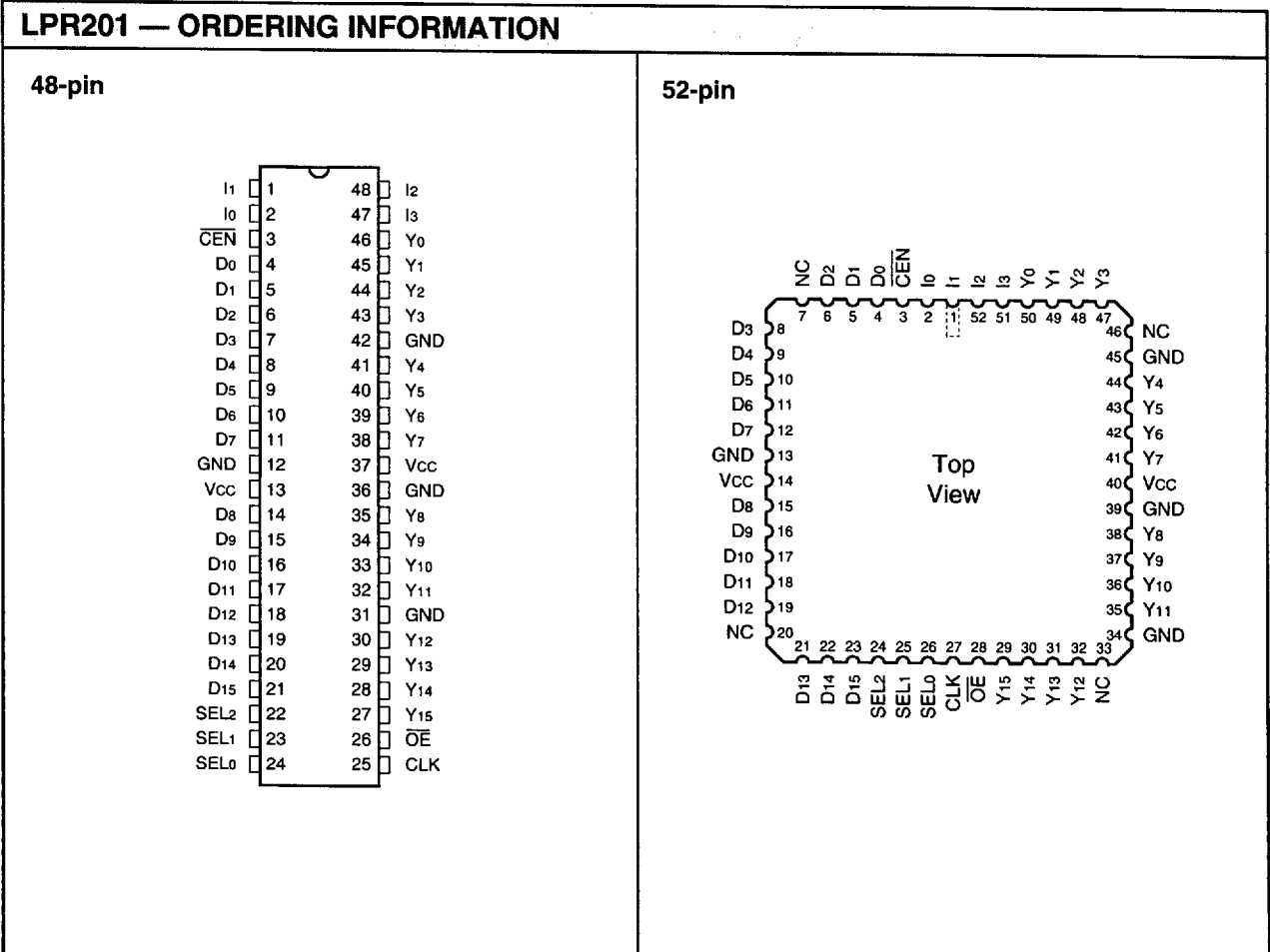


16-bit Multilevel Pipeline Register



Speed	Plastic DIP (P5)	Sidebraze Hermetic DIP (D5)	Plastic Leaded Chip Carrier (J5)	Ceramic Leadless Chip Carrier (K10)
0°C to +70°C — COMMERCIAL SCREENING				
20 ns 15 ns 12 ns 10 ns	LPR200PC20 LPR200PC15 LPR200PC12 LPR200PC10		LPR200JC20 LPR200JC15 LPR200JC12 LPR200JC10	
-55°C to +125°C — COMMERCIAL SCREENING				
-55°C to +125°C — MIL-STD-883 COMPLIANT				
20 ns 15 ns 12 ns		LPR200DMB20 LPR200DMB15 LPR200DMB12		LPR200KMB20 LPR200KMB15 LPR200KMB12

16-bit Multilevel Pipeline Register



Speed	Plastic DIP (P5)	Sidebrazed Hermetic DIP (D5)	Plastic Leaded Chip Carrier (J5)	Ceramic Leadless Chip Carrier (K10)
0°C to +70°C — COMMERCIAL SCREENING				
20 ns	LPR201PC20		LPR201JC20	
15 ns	LPR201PC15		LPR201JC15	
12 ns	LPR201PC12		LPR201JC12	
10 ns	LPR201PC10		LPR201JC10	
-55°C to +125°C — COMMERCIAL SCREENING				
-55°C to +125°C — MIL-STD-883 COMPLIANT				
20 ns		LPR201DMB20		LPR201KMB20
15 ns		LPR201DMB15		LPR201KMB15
12 ns		LPR201DMB12		LPR201KMB12