Section 15 Electrical Characteristics (5V Version)

15.1 Absolute Maximum Ratings

Table 15.1 shows the absolute maximum ratings.

Table 15.1 Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Power supply voltage	V_{CC}	–0.3 to +7.0	V
Input voltage	Vin	–0.3 to V_{CC} + 0.3	V
Operating temperature	Topr	–20 to +75	°C
Storage temperature	Tstg	–55 to +125	°C

Caution: Operating the chip in excess of the absolute maximum rating may result in permanent damage.

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15.2 DC Characteristics

Tables 15.2 and 15.3 list DC characteristics.

Table 15.2 DC Characteristics (Condition V_{CC} = 5.0 V ± 10%, Ta = –20 to +75° C)

Item		Symbol	Min	Typ	Max	Unit	Measurement Conditions
Input high-level voltage	$\overline{RES}$, NMI, MD5–MD0	V_{IH}	V_{CC} – 0.5	—	V_{CC} + 0.3	V	During standby
	MD0		V_{CC} – 0.7	—	V_{CC} + 0.3	V	Normal operation
	EXTAL, CKIO		V_{CC} – 0.7	—	V_{CC} + 0.3	V	
	Other input pins		2.2	—	V_{CC} + 0.3	V	
Input low-level voltage	$\overline{RES}$, NMI, MD5–MD0	V_{IL}	–0.3	—	0.5	V	During standby
	MD0		–0.3	—	0.8	V	Normal operation
	Other input pins		–0.3	—	0.8	V	
Input leak current	$\overline{RES}$	|Iin|	—	—	1.0	µA	Vin = 0.5 to V_{CC} – 0.5 V
	NMI, MD5–MD0		—	—	1.0	µA	Vin = 0.5 to V_{CC} – 0.5 V
	Other input pins		—	—	1.0	µA	Vin = 0.5 to V_{CC} – 0.5 V
3-state leak current (while off)	A26–A0, D31–D0, $\overline{BS}$, $\overline{CS3}$–$\overline{CS0}$, RD/$\overline{WR}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE3}$-$\overline{WE0}$, $\overline{RD}$, $\overline{IVECF}$	$\|I_{STI}\|$	—	—	1.0	µA	Vin = 0.5 to V_{CC} – 0.5 V
Output high-level voltage	All output pins	V_{OH}	V_{CC} – 0.5	—	—	V	I_{OH} = –200 µA
			3.5	—	—	V	I_{OH} = –1 mA
Output low level voltage	All output pins	V_{OL}	—	—	0.4	V	I_{OL} = 1.6 mA
Input capacitance	$\overline{RES}$	Cin	—	—	15	pF	Vin = 0 V f = 1 MHz Ta = 25°C
	NMI		—	—	15	pF	
	All other input pins (D31–D0)		—	—	15	pF	

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Table 15.2 DC Characteristics (Condition V_{CC} = 5.0 V ± 10%, Ta = –20 to +75° C) (cont)

Item		Symbol	Min	Typ	Max	Unit	Measurement Conditions
Current consumption	Ordinary operation	I_{CC}	—	60	80	mA	f = 8 MHz
			—	80	100	mA	f = 16 MHz
			—	110	160	mA	f = 28.7 MHz
	Sleep		—	30	55	mA	f = 8 MHz
			—	50	70	mA	f = 16 MHz
			—	80	100	mA	f = 28.7 MHz
	Standby		—	1	15	µA	Ta ≤ 50°C
			—	—	60	µA	50°C < Ta

Notes: 1. When no PLL is used, do not release the $PLLV_{CC}$ and $PLLV_{SS}$ pins. Connect $PLLV_{CC}$ to V_{CC} and $PLLV_{SS}$ to V_{SS}.
2. Current consumption values shown are the values at which all output pins are without load under conditions of V_{IH} min = V_{CC} - 0.5 V, V_{IL} max = 0.5 V.

Table 15.3 Permitted Output Current Values (V_{CC} = 5.0 V ± 10%, Ta = –20 to +75°C)

Item	Symbol	Min	Typ	Max	Unit
Output low-level permissible current (per pin)	I_{OL}	—	—	2.0	mA
Output low-level permissible current (total)	ΣI_{OL}	—	—	80	mA
Output high-level permissible current (per pin)	$-I_{OH}$	—	—	2.0	mA
Output high-level permissible current (total)	$-\Sigma I_{OH}$	—	—	25	mA

Caution: To ensure LSI reliability, do not exceed the value for output current given in table 15.3.

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15.3 AC Characteristics

15.3.1 Clock Timing

Table 15.4 Clock Timing (V_{CC} = 5.0 V ± 10%, Ta = –20 to +75°C)

Item	Symbol	Min	Max	Unit	Figures
Operating frequency	f_{OP}	4	28.7	MHz	15.1
Clock cycle time	t_{cyc}	35	143*1 or 250*2	ns	
Clock high pulse width	t_{CH}	8*1 or 15*2	—	ns	
Clock low pulse width	t_{CL}	8*1 or 15*2	—	ns	
Clock rise time	t_{CR}	—	5	ns	
Clock fall time	t_{CF}	—	5	ns	
EXTAL clock input frequency	f_{EX}	4	8	MHz	15.2
EXTAL clock input cycle time	t_{EXcyc}	125	250	ns	
EXTAL clock input low level pulse width	t_{EXL}	50	—	ns	
EXTAL clock input high level pulse width	t_{EXH}	50	—	ns	
EXTAL clock input rise time	t_{EXR}	—	5	ns	
EXTAL clock input clock fall time	t_{EXF}	—	5	ns	
Power-on oscillation settling time	t_{OSC1}	10	—	ms	15.3
Software standby oscillation settling time 1	t_{OSC2}	10	—	ms	15.4
Software standby oscillation settling time 2	t_{OSC3}	10	—	ms	15.5
PLL synchronization settling time	t_{PLL}	1	—	µs	15.6

Notes: 1. With PLL circuit 1 operating.
2. With PLL circuit 1 not used.

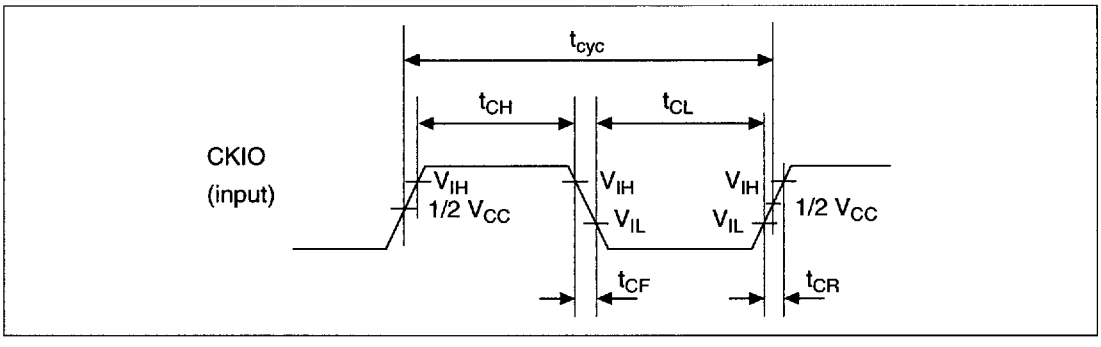

Figure 15.1 CKIO Input Timing

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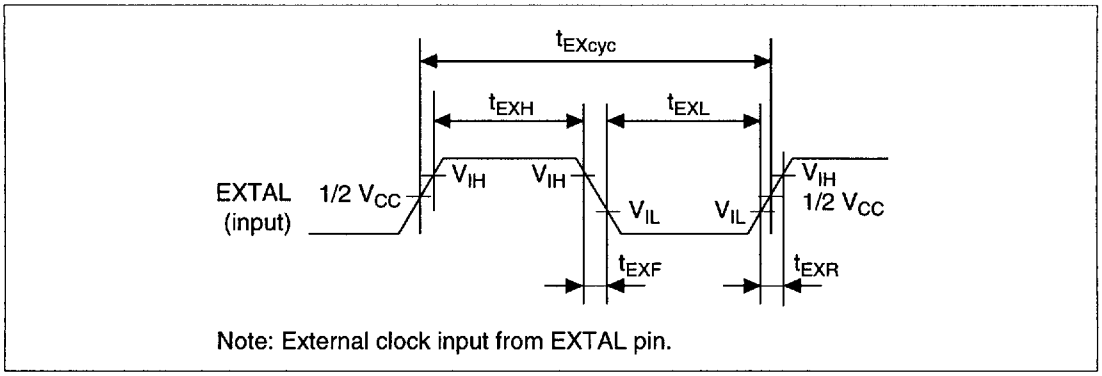

Figure 15.2 EXTAL Clock Input Timing

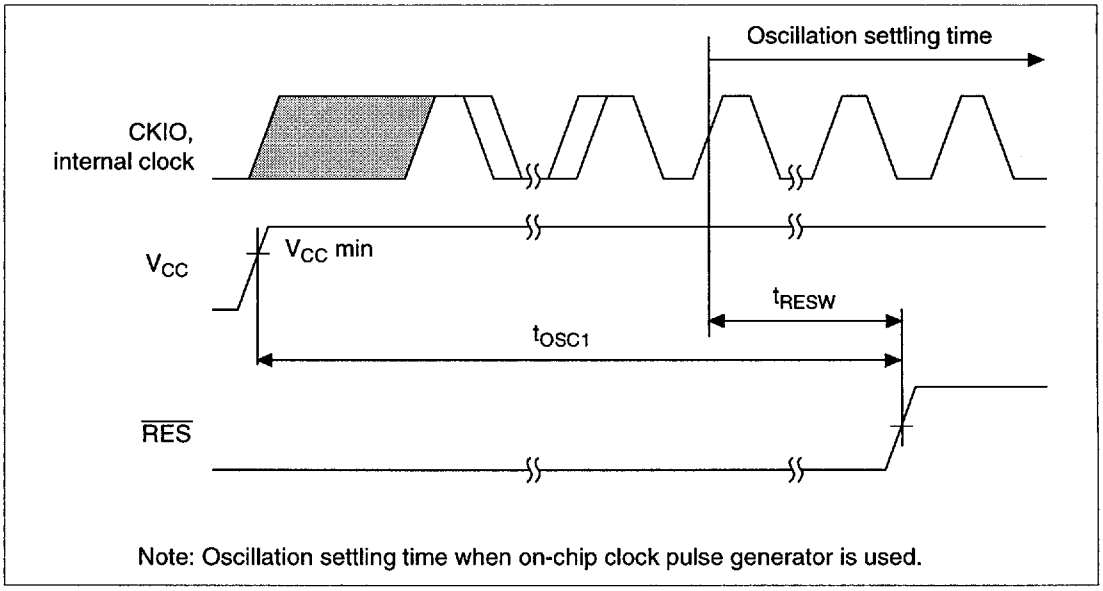

Figure 15.3 Oscillation Settling Time at Power-On

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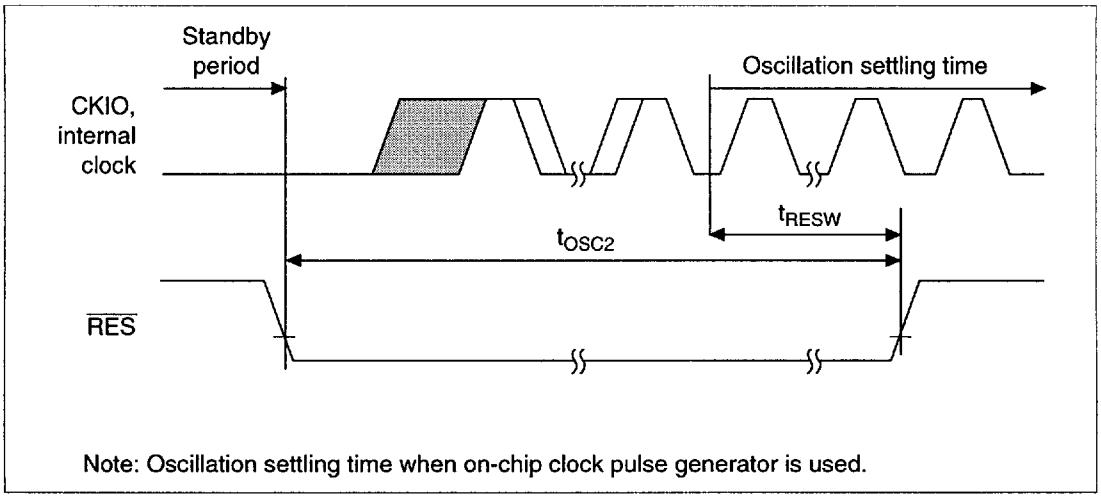

Figure 15.4 Oscillation Settling Timing at Standby Return (via RES)

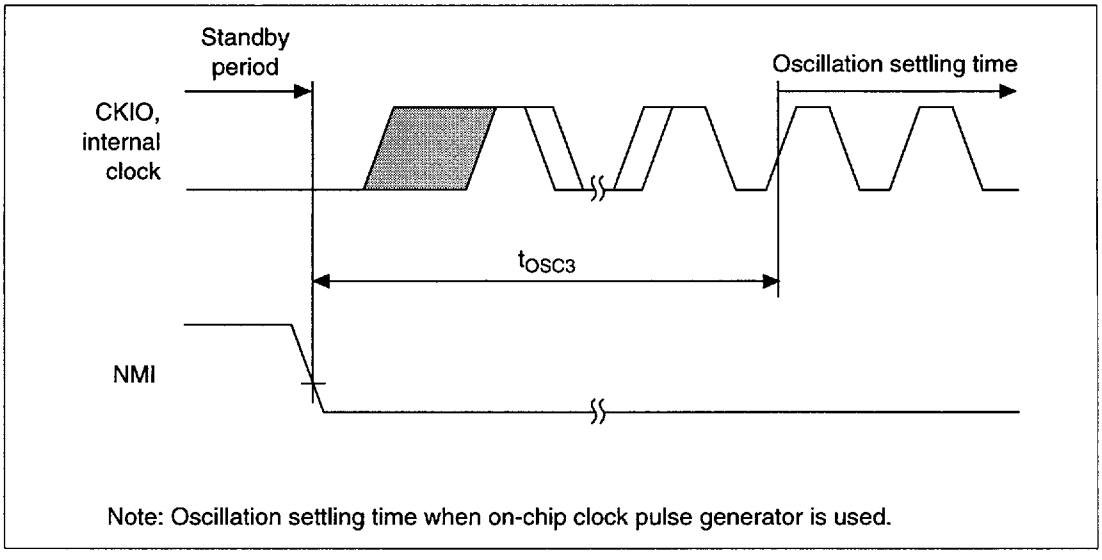

Figure 15.5 Oscillation Settling Timing at Standby Return (via NMI)

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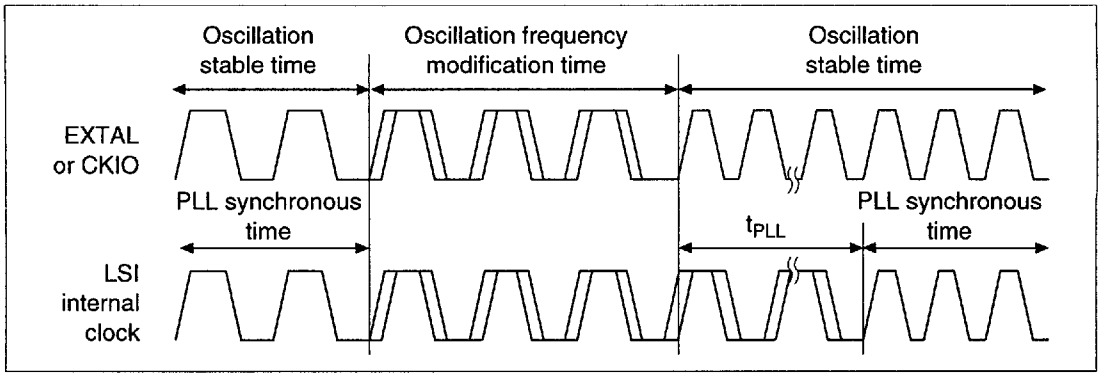

Figure 15.6 PLL Synchronization Settling Timing

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15.3.2 Control Signal Timing

Table 15.5 Control Signal (V_{CC} = 5.0 V ± 10%, Ta = –20 to +75°C)

Item	Symbol	Min	Max	Unit	Figure
$\overline{RES}$ rise, fall	t_{RESr}, t_{RESf}	—	200	ns	15.7
$\overline{RES}$ pulse width	t_{RESW}	20	—	t_{cyc}	
NMI reset setup time	t_{NMIRS}	tcyc + 10	—	ns	
NMI reset hold time	t_{NMIRH}	tcyc + 10	—	ns	
NMI rise, fall	t_{NMIr}, t_{NMIf}	—	200	ns	
NMI minimum pulse width	t_{IRQES}	3	—	tcyc	
$\overline{RES}$ setup time*	t_{RESS}	30	—	ns	15.8, 15.9
NMI setup time*	t_{NMIS}	30	—	ns	
$\overline{IRL3}$–$\overline{IRL0}$ setup time*	t_{IRLS}	30	—	ns	
$\overline{RES}$ hold time	t_{RESH}	10	—	ns	15.8, 15.9
NMI hold time	t_{NMIH}	10	—	ns	
$\overline{IRL3}$–$\overline{IRL0}$ hold time	t_{IRLH}	10	—	ns	
$\overline{BRLS}$ setup time 1 (PLL on)	t_{BLSS1}	1/2 tcyc+9	—	ns	15.10
$\overline{BRLS}$ hold time 1 (PLL on)	t_{BLSH1}	9–1/2 tcyc	—	ns	
$\overline{BGR}$ delay time 1 (PLL on)	t_{BGRD1}	—	1/2 tcyc+18	ns	
$\overline{BRLS}$ setup time 1 (PLL on, 1/4 cycle delay)	t_{BLSS1}	1/4 tcyc+9	—	ns	15.10
$\overline{BRLS}$ hold time 1 (PLL on, 1/4 cycle delay)	t_{BLSH1}	9–1/4 tcyc	—	ns	
$\overline{BGR}$ delay time 1 (PLL on, 1/4 cycle delay)	t_{BGRD1}	—	3/4 tcyc+18	ns	
$\overline{BRLS}$ setup time 2 (PLL off)	t_{BLSS2}	9	—	ns	15.11
$\overline{BRLS}$ hold time 2 (PLL off)	t_{BLSH2}	19	—	ns	
$\overline{BGR}$ delay time 2 (PLL off)	t_{BGRD2}	—	28	ns	

Note The $\overline{RES}$, NMI, and $\overline{IRL3}$-$\overline{IRL0}$ signals are asynchronous inputs, but when the setup times shown here are provided, the signals are considered to have produced changes at clock fall. If the setup times are not provided, recognition is delayed until the next clock fall.

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Table 15.5 Control Signal Timing (V_{CC} = 5.0 V ± 10%, Ta = –20 to +75°C)(cont)

Item	Symbol	Min	Max	Unit	Figure
$\overline{BREQ}$ delay time 1 (PLL on)	t_{BRQD1}	—	1/2 tcyc+18	ns	15.12
$\overline{BACK}$ setup time 1 (PLL on)	t_{BAKS1}	1/2 tcyc+9	—	ns	
$\overline{BACK}$ hold time 1 (PLL on)	t_{BAKH1}	9–1/2 tcyc	—	ns	
$\overline{BREQ}$ delay time 1 (PLL on, 1/4 cycle delay)	t_{BRQD1}	—	3/4 tcyc+18	ns	15.12
$\overline{BACK}$ setup time 1 (PLL on, 1/4 cycle delay)	t_{BAKS1}	1/4t cyc+9	—	ns	
$\overline{BACK}$ hold time 1 (PLL on, 1/4 cycle delay)	t_{BAKH1}	9–1/4 tcyc	—	ns	
$\overline{BREQ}$ delay time 2 (PLL off)	t_{BRQD2}	—	28	ns	15.13
$\overline{BACK}$ setup time 2 (PLL off)	t_{BAKS2}	9	—	ns	
$\overline{BACK}$ hold time 2 (PLL off)	t_{BAKH2}	19	—	ns	
Bus tri-state delay time 1 (PLL on)	t_{BOFF1}	0	25	ns	15.10,
Bus buffer on time 1 (PLL on)	t_{BON1}	0	18	ns	15.12
Bus tri-state delay time 1 (PLL on, 1/4 cycle delay)	t_{BOFF1}	1/4 tcyc	1/4 tcyc+25	ns	15.10,
Bus buffer on time 1 (PLL on, 1/4 cycle delay)	t_{BON1}	1/4 tcyc	1/4 tcyc+18	ns	15.12
Bus tri-state delay time 1 (PLL off)	t_{BOFF1}	0	30	ns	15.11,
Bus buffer on time 1 (PLL off)	t_{BON1}	0	25	ns	15.13
Bus tri-state delay time 2 (PLL on)	t_{BOFF2}	1/2 tcyc	1/2 tcyc+25	ns	15.10,
Bus buffer on time 2 (PLL on)	t_{BON2}	1/2 tcyc	1/2 tcyc+18	ns	15.12
Bus tri-state delay time 2 (PLL on, 1/4 cycle delay)	t_{BOFF2}	3/4 tcyc	3/4 tcyc+25	ns	15.10,
Bus buffer on time 2 (PLL on, 1/4 cycle delay)	t_{BON2}	3/4 tcyc	3/4 tcyc+18	ns	15.12
Bus tri-state delay time 3 (PLL off)	t_{BOFF3}	0	30	ns	15.11,
Bus buffer on time 3 (PLL off)	t_{BON3}	0	25	ns	15.13

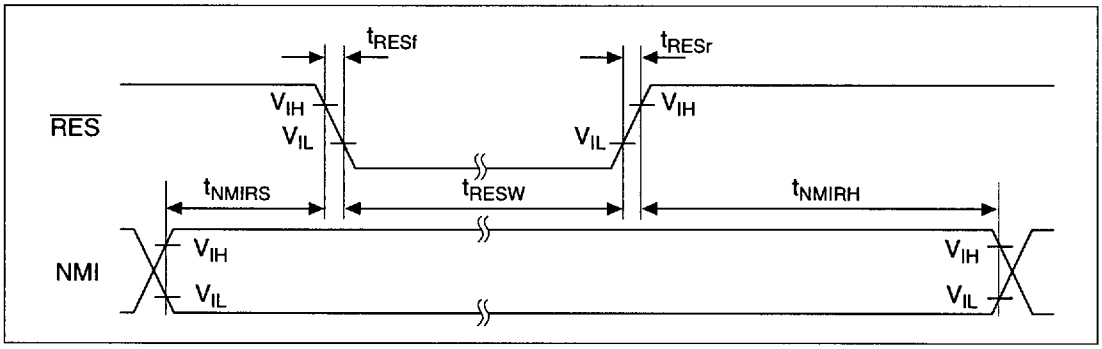

Figure 15.7 Reset Input Timing

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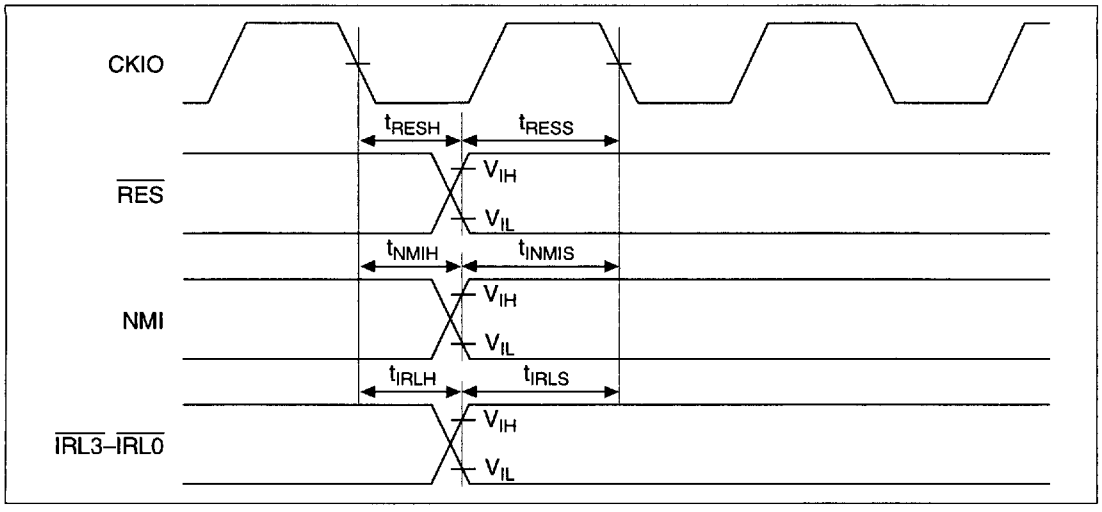

Figure 15.8 Interrupt Signal Input Timing (With PLL1 Off)

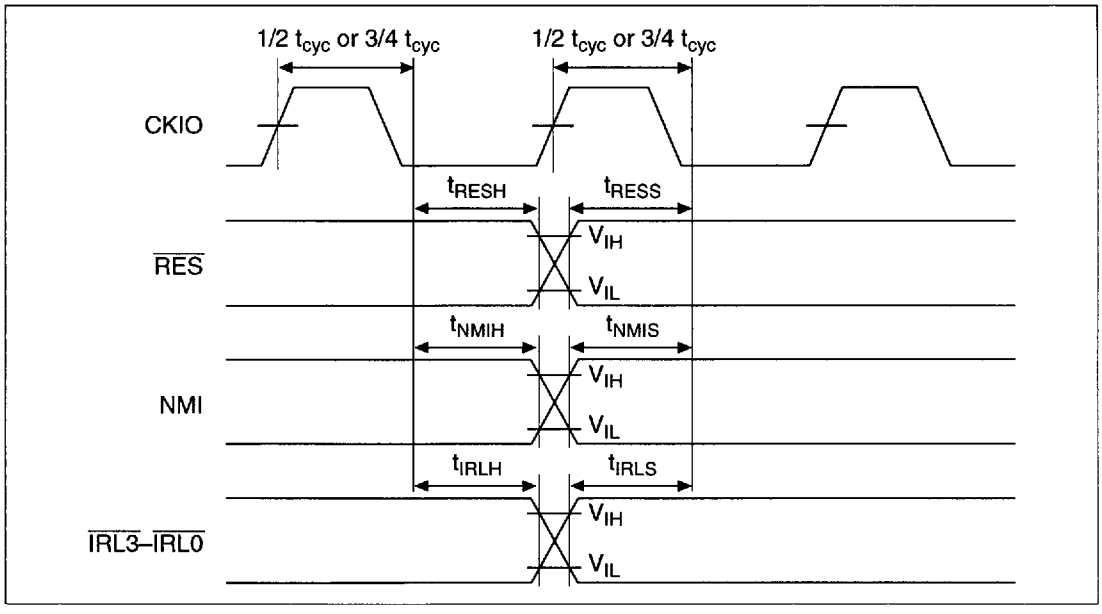

Figure 15.9 Interrupt Signal Input Timing (With PLL1 On)

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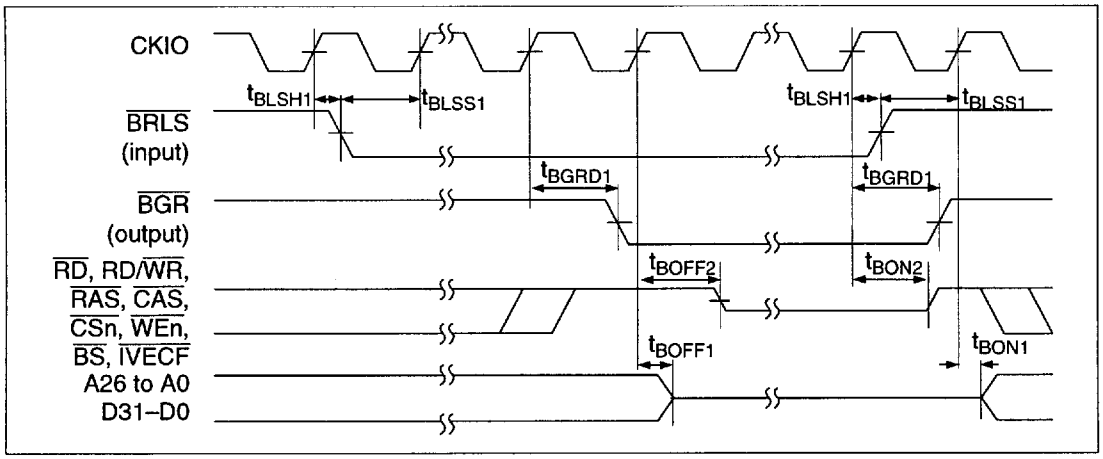

Figure 15.10 Bus Release Timing (Master Mode With PLL1 On)

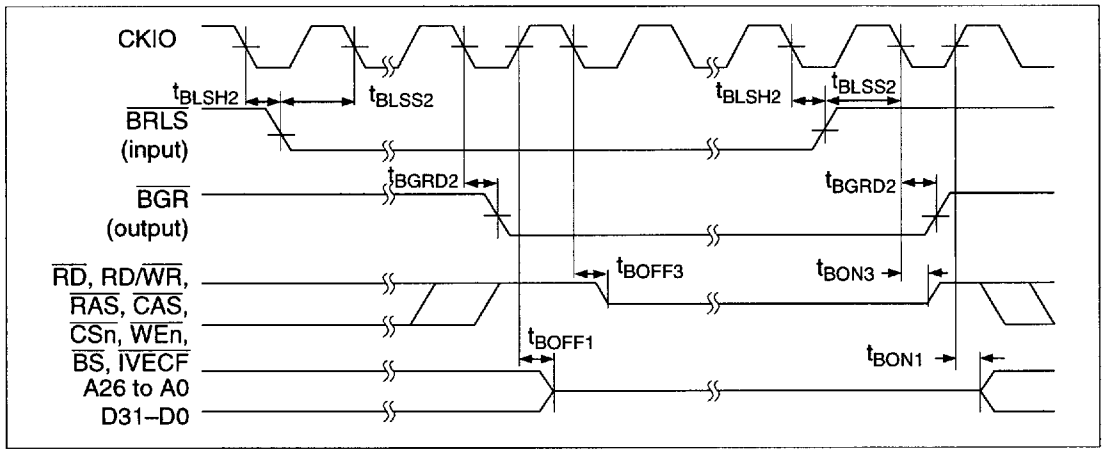

Figure 15.11 Bus Release Timing (Master Mode With PLL1 Off)

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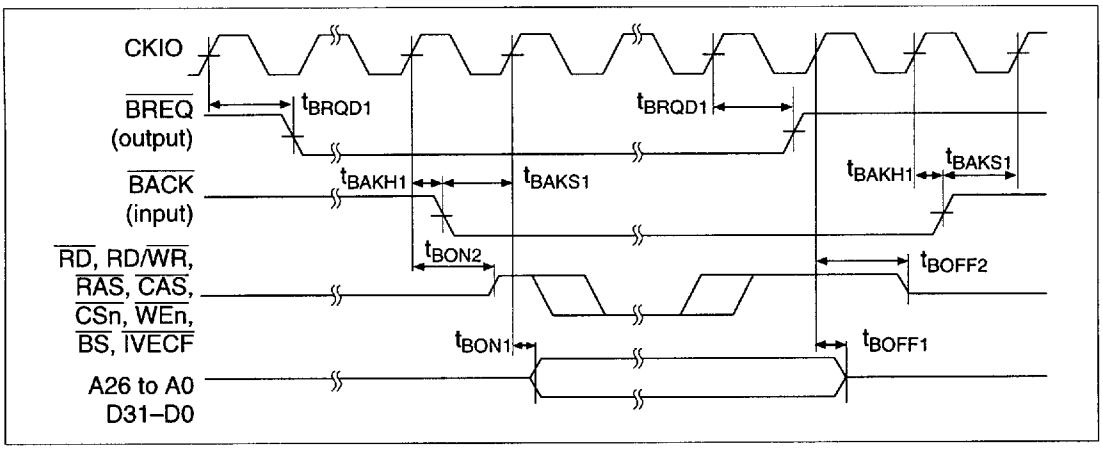

Figure 15.12 Bus Release Timing (Slave Mode, With PLL1 On)

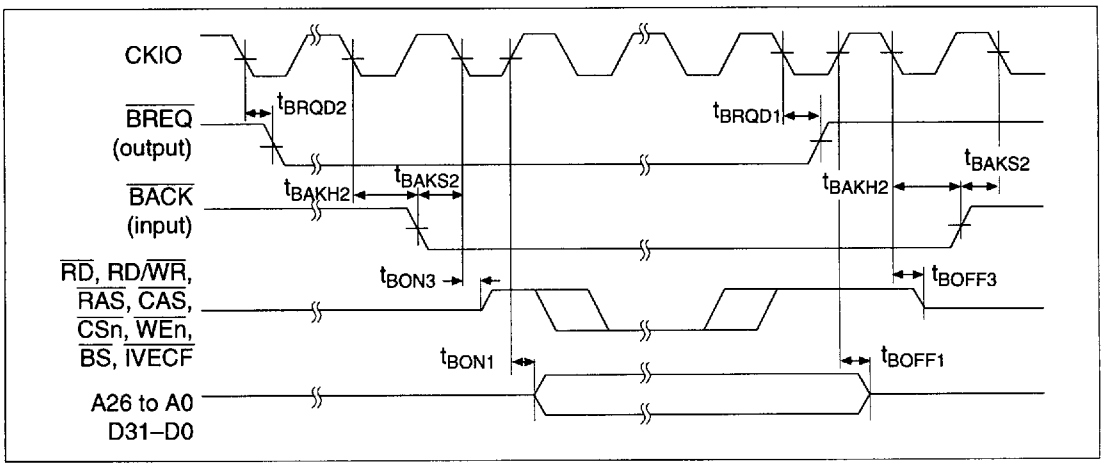

Figure 15.13 Bus Release Timing (Slave Mode, With PLL1 Off)

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15.3.3 Bus Timing

Table 15.6 Bus Timing With PLL On [mode 0, 4] (Condition: V_{CC} = 5.0 V ±10%, Ta = –20 to +75°C)

Item	Symbol	Min	Max	Unit	Figures
Address delay time	t_{AD}	3	18	ns	15.14, 15.20, 15.40, 15.52, 15.66, 15.68
$\overline{BS}$ delay time	t_{BSD}	—	21	ns	15.14, 15.20, 15.40, 15.52, 15.66
$\overline{CS}$ delay time 1	t_{CSD1}	—	21	ns	15.14, 15.20, 15.40, 15.52, 15.66
$\overline{CS}$ delay time 2	t_{CSD2}	—	1/2 tcyc + 21	ns	15.14, 15.66
Read write delay time	t_{RWD}	3	18	ns	15.14, 15.20, 15.40, 15.52, 15.66
Read strobe delay time 1	t_{RSD1}	—	1/2 tcyc + 16	ns	15.14, 15.40, 15.52, 15.66, 15.68
Read data setup time 1	t_{RDS1}	1/2 tcyc + 10	—	ns	15.14, 15.40, 15.52, 15.66, 15.68
Read data setup time 3 (SDRAM)	t_{RDS3}	1/2 tcyc + 8	—	ns	15.20
Read data hold time 2	t_{RDH2}	0	—	ns	15.14, 15.66
Read data hold time 4 (SDRAM)	t_{RDH4}	0	—	ns	15.20
Read data hold time 5 (DRAM)	t_{RDH5}	0	—	ns	15.40
Read data hold time 6 (PSRAM)	t_{RDH6}	0	—	ns	15.52
Read data hold time 7 (interrupt vector)	t_{RDH7}	0	—	ns	15.68
Write enable delay time	t_{WED1}	1/2 tcyc + 3	1/2 tcyc + 18	ns	15.14, 15.15, 15.52, 15.53
Write data delay time 1	t_{WDD}	3	18	ns	15.15, 15.27, 15.41, 15.53
Write data hold time 1	t_{WDH1}	3	—	ns	15.15, 15.27, 15.41, 15.53
Data buffer on time	t_{DON}	—	18	ns	15.15, 15.27, 15.41, 15.53
Data buffer off time	t_{DOF}	—	18	ns	15.15, 15.27, 15.41, 15.53

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Table 15.6 Bus Timing With PLL On [mode 0, 4] (Condition: V_{CC} = 5.0 V ±10%, Ta = –20 to +75°C) (cont)

Item	Symbol	Min	Max	Unit	Figures
DACK delay time 1	t_{DACD1}	—	18	ns	15.14, 15.20, 15.40, 15.52, 15.66
DACK delay time 2	t_{DACD2}	—	1/2 tcyc + 18	ns	15.14, 15.20, 15.40, 15.52, 15.66
$\overline{WAIT}$ setup time	t_{WTS}	20	—	ns	15.19, 15.43, 15.55, 15.66, 15.70
$\overline{WAIT}$ hold time	t_{WTH}	5	—	ns	15.19, 15.43, 15.55, 15.66, 15.70
$\overline{RAS}$ delay time 1 (SDRAM)	t_{RASD1}	—	18	ns	15.20
$\overline{RAS}$ delay time 2 (DRAM)	t_{RASD2}	1/2 tcyc + 3	1/2 tcyc + 18	ns	15.40
$\overline{CAS}$ delay time 1 (SDRAM)	t_{CASD1}	—	18	ns	15.20
$\overline{CAS}$ delay time 2 (DRAM)	t_{CASD2}	1/2 tcyc + 3	1/2 tcyc + 18	ns	15.40
DQM delay time	t_{DQMD}	—	18	ns	15.20
CKE delay time	t_{CKED}	—	21	ns	15.37
$\overline{CE}$ delay time 1	t_{CED1}	1/2 tcyc + 3	1/2 tcyc + 18	ns	15.52
$\overline{OE}$ delay time 1	t_{OED1}	—	1/2 tcyc + 18	ns	15.52
$\overline{IVECF}$ delay time	t_{IVD}	—	18	ns	15.68
Address input setup time	t_{ASIN}	14	—	ns	15.71
Address input hold time	t_{AHIN}	3	—	ns	15.71
$\overline{BS}$ input setup time	t_{BSS}	15	—	ns	15.71
$\overline{BS}$ input hold time	t_{BSH}	3	—	ns	15.71
Read write input setup time	t_{RWS}	15	—	ns	15.71
Read write input hold time	t_{RWH}	3	—	ns	15.71
Address hold time 1	t_{AH1}	5	—	ns	15.15

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Table 15.7 Bus Timing With PLL On and 1/4 Cycle Delay [mode 1, 5] (Condition: V_{CC} = 5.0 V ±10%, Ta = –20 to +75°C)

Item	Symbol	Min	Max	Unit	Figures
Address delay time	t_{AD}	1/4 tcyc + 3	1/4 tcyc + 18	ns	15.14, 15.20, 15.40, 15.52, 15.66, 15.68
$\overline{BS}$ delay time	t_{BSD}	—	1/4 tcyc + 21	ns	15.14, 15.20, 15.40, 15.52, 15.66
$\overline{CS}$ delay time 1	t_{CSD1}	—	1/4 tcyc + 21	ns	15.14, 15.20, 15.40, 15.52, 15.66
$\overline{CS}$ delay time 2	t_{CSD2}	—	3/4 tcyc + 21	ns	15.14, 15.66
Read write delay time	t_{RWD}	1/4 tcyc + 3	1/4 tcyc + 18	ns	15.14, 15.20, 15.40, 15.52, 15.66
Read strobe delay time 1	t_{RSD1}	—	3/4 tcyc + 16	ns	15.14, 15.40, 15.52, 15.66, 15.68
Read data setup time 1	t_{RDS1}	1/4 tcyc + 10	—	ns	15.14, 15.40, 15.52, 15.66, 15.68
Read data setup time 3 (SDRAM)	t_{RDS3}	1/4 tcyc + 8	—	ns	15.20
Read data hold time 2	t_{RDH2}	0	—	ns	15.14, 15.66
Read data hold time 4 (SDRAM)	t_{RDH4}	0	—	ns	15.20
Read data hold time 5 (DRAM)	t_{RDH5}	0	—	ns	15.40
Read data hold time 6 (PSRAM)	t_{RDH6}	0	—	ns	15.52
Read data hold time 7 (interrupt vector)	t_{RDH7}	0	—	ns	15.68
Write enable delay time	t_{WED1}	3/4 tcyc + 3	3/4 tcyc + 18	ns	15.14, 15.15, 15.52, 15.53
Write data delay time 1	t_{WDD}	1/4 tcyc + 3	1/4 tcyc + 18	ns	15.15, 15.27, 15.41, 15.53
Write data hold time 1	t_{WDH1}	1/4 tcyc + 3	—	ns	15.15, 15.27, 15.41, 15.53
Data buffer on time	t_{DON}	—	1/4 tcyc + 18	ns	15.15, 15.27, 15.41, 15.53
Data buffer off time	t_{DOF}	—	1/4 tcyc + 18	ns	15.15, 15.27, 15.41, 15.53

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Table 15.7 Bus Timing With PLL On and 1/4 Cycle Delay [mode 1, 5] (Condition: V_{CC} = 5.0 V ±10%, Ta = –20 to +75°C) (cont)

Item	Symbol	Min	Max	Unit	Figures
DACK delay time 1	t_{DACD1}	—	1/4 tcyc + 18	ns	15.14, 15.20, 15.40, 15.52, 15.66
DACK delay time 2	t_{DACD2}	—	3/4 tcyc + 18	ns	15.14, 15.20, 15.40, 15.52, 15.66
$\overline{WAIT}$ setup time	t_{WTS}	20 – 1/4 tcyc	—	ns	15.19, 15.43, 15.55, 15.66, 15.70
$\overline{WAIT}$ hold time	t_{WTH}	1/4 tcyc + 5	—	ns	15.19, 15.43, 15.55, 15.66, 15.70
$\overline{RAS}$ delay time 1 (SDRAM)	t_{RASD1}	—	1/4 tcyc + 18	ns	15.20
$\overline{RAS}$ delay time 2 (DRAM)	t_{RASD2}	3/4 tcyc + 3	3/4 tcyc + 18	ns	15.40
$\overline{CAS}$ delay time 1 (SDRAM)	t_{CASD1}	—	1/4 tcyc + 18	ns	15.20
$\overline{CAS}$ delay time 2 (DRAM)	t_{CASD2}	3/4 tcyc + 3	3/4 tcyc + 18	ns	15.40
DQM delay time	t_{DQMD}	—	1/4 tcyc + 18	ns	15.20
CKE delay time	t_{CKED}	—	1/4 tcyc + 21	ns	15.37
$\overline{CE}$ delay time 1	t_{CED1}	3/4 tcyc + 3	3/4 tcyc + 18	ns	15.52
$\overline{OE}$ delay time 1	t_{OED1}	—	3/4 tcyc + 18	ns	15.52
$\overline{IVECF}$ delay time	t_{IVD}	—	1/4 tcyc + 18	ns	15.68
Address input setup time	t_{ASIN}	14 - 1/4 tcyc	—	ns	15.71
Address input hold time	t_{AHIN}	1/4 tcyc + 3	—	ns	15.71
$\overline{BS}$ input setup time	t_{BSS}	15 - 1/4 tcyc	—	ns	15.71
$\overline{BS}$ input hold time	t_{BSH}	1/4 tcyc + 3	—	ns	15.71
Read write input setup time	t_{RWS}	15 - 1/4 tcyc	—	ns	15.71
Read write input hold time	t_{RWH}	1/4 tcyc + 3	—	ns	15.71
Address hold time 1	t_{AH1}	5	—	ns	15.15

4496204 0054356 325

Table 15.8 Bus Timing With PLL Off (CKIO input) [mode 6] (Condition: V_{CC} = 5.0 V ±10%, Ta = –20 to +75°C)

Item	Symbol	Min	Max	Unit	Figures
Address delay time	t_{AD}	13	28	ns	15.16, 15.38, 15.47, 15.60, 15.67, 15.69
$\overline{BS}$ delay time	t_{BSD}	—	30	ns	15.16, 15.38, 15.47, 15.60, 15.67
$\overline{CS}$ delay time 1	t_{CSD1}	—	30	ns	15.16, 15.38, 15.47, 15.60, 15.67
$\overline{CS}$ delay time 3	t_{CSD3}	—	28	ns	15.16, 15.67
Read write delay time	t_{RWD}	13	28	ns	15.16, 15.38, 15.47, 15.60, 15.67
Read strobe delay time 2	t_{RSD2}	—	26	ns	15.16, 15.47, 15.60, 15.67, 15.69
Read data setup time 2	t_{RDS2}	10	—	ns	15.16, 15.38, 15.47, 15.60, 15.67, 15.69
Read data hold time 2	t_{RDH2}	0	—	ns	15.16, 15.67
Read data hold time 3	t_{RDH3}	15	—	ns	15.38
Read data hold time 5 (DRAM)	t_{RDH5}	0	—	ns	15.47
Read data hold time 6 (PSRAM)	t_{RDH6}	0	—	ns	15.60
Read data hold time 7 (interrupt vector)	t_{RDH7}	0	—	ns	15.69
Write enable delay time 2	t_{WED2}	10	25	ns	15.17, 15.61
Write data delay time	t_{WDD}	10	25	ns	15.17, 15.39, 15.48, 15.61
Write data hold time 1	t_{WDH1}	3		ns	15.17, 15.39, 15.48, 15.61
Write data hold time 2	t_{WDH2}	5		ns	15.17
Write data hold time 3	t_{WDH3}	3		ns	15.61
DACK delay time 1	t_{DACD1}	—	25	ns	15.16, 15.38, 15.47, 15.60, 15.67
DACK delay time 3	t_{DACD3}	—	25	ns	15.16, 15.38, 15.47, 15.60, 15.67

4496204 0054357 261

Table 15.8 Bus Timing With PLL Off (CKIO input) [mode 6] (Condition: V_{CC} = 5.0 V ±10%, Ta = –20 to +75°C) (cont)

Item	Symbol	Min	Max	Unit	Figures
$\overline{\text{WAIT}}$ setup time	t_{WTS}	20	—	ns	15.19, 15.43, 15.55, 15.67, 15.70
$\overline{\text{WAIT}}$ hold time	t_{WTH}	15	—	ns	15.19, 15.43, 15.55, 15.67, 15.70
$\overline{\text{RAS}}$ delay time 1 (SDRAM)	t_{RASD1}	—	25	ns	15.38
$\overline{\text{RAS}}$ delay time 3 (DRAM)	t_{RASD3}	10	25	ns	15.47
$\overline{\text{CAS}}$ delay time 1 (SDRAM)	t_{CASD1}	—	25	ns	15.38
$\overline{\text{CAS}}$ delay time 3 (DRAM)	t_{CASD3}	10	25	ns	15.47
DQM delay time	t_{DQMD}	—	25	ns	15.38
CKE delay time	t_{CKED}	—	25	ns	15.37
$\overline{\text{CE}}$ delay time 2	t_{CED2}	10	25	ns	15.60
$\overline{\text{OE}}$ delay time 2	t_{OED2}	—	25	ns	15.60
$\overline{\text{IVECF}}$ delay time	t_{IVD}	—	25	ns	15.69
$\overline{\text{WE}}$ setup time	t_{WES1}	0	—	ns	15.16
Address setup time 1	t_{AS1}	0	—	ns	15.17
Address setup time 2	t_{AS2}	3	—	ns	15.60
Address hold time 2	t_{AH2}	0	—	ns	15.17
Row address setup time	t_{ASR}	3	—	ns	15.47
Column address setup time	t_{ASC}	3	—	ns	15.47
Write command setup time	t_{WCS}	3	—	ns	15.48
Write data setup time	t_{WDS}	3	—	ns	15.48
Address input setup time*	t_{ASIN}	15	—	ns	15.71
Address input hold time*	t_{AHIN}	10	—	ns	15.71
$\overline{\text{BS}}$ input setup time*	t_{BSS}	15	—	ns	15.71
$\overline{\text{BS}}$ input hold time*	t_{BSH}	10	—	ns	15.71
Read write input setup time*	t_{RWS}	15	—	ns	15.71
Read write input hold time*	t_{RWH}	10	—	ns	15.71
Data buffer on time	t_{DON}	—	25	ns	15.17, 15.39, 15.48, 15.61
Data buffer off time	t_{DOF}	—	25	ns	15.17, 15.39, 15.48, 15.61

Note: When the external addresses monitor function is used, the PLL must be on.

4496204 0054358 1T8

Table 15.9 Bus Timing With PLL Off (CKIO output) [mode 2] (Condition: V_{CC} = 5.0 V ±10%, Ta = –20 to +75°C)

Item	Symbol	Min	Max	Unit	Figures
Address delay time	t_{AD}	3	18	ns	15.16, 15.38, 15.47, 15.60, 15.67, 15.69
$\overline{BS}$ delay time	t_{BSD}	—	21	ns	15.16, 15.38, 15.47, 15.60, 15.67
$\overline{CS}$ delay time 1	t_{CSD1}	—	21	ns	15.16, 15.38, 15.47, 15.60, 15.67
$\overline{CS}$ delay time 3	t_{CSD3}	—	21	ns	15.16, 15.67
Read write delay time	t_{RWD}	3	18	ns	15.16, 15.38, 15.47, 15.60, 15.67
Read strobe delay time 2	t_{RSD2}	—	16	ns	15.16, 15.47, 15.60, 15.67, 15.69
Read data setup time 2	t_{RDS2}	12	—	ns	15.16, 15.38, 15.47, 15.60, 15.67, 15.69
Read data hold time 2	t_{RDH2}	0	—	ns	15.16, 15.67
Read data hold time 3 (SDRAM)	t_{RDH3}	1/2 tcyc	—	ns	15.38
Read data hold time 5 (DRAM)	t_{RDH5}	0	—	ns	15.47
Read data hold time 6 (PSRAM)	t_{RDH6}	0	—	ns	15.60
Read data hold time 7 (interrupt vector)	t_{RDH7}	0	—	ns	15.69
Write enable delay time 2	t_{WED2}	3	18	ns	15.17, 15.61
Write data delay time	t_{WDD}	3	18	ns	15.17, 15.39, 15.48, 15.61
Write data hold time 1	t_{WDH1}	3	—	ns	15.17, 15.39, 15.48, 15.61
Write data hold time 2	t_{WDH2}	5	—	ns	15.17
Write data hold time 3	t_{WDH3}	3	—	ns	15.61
DACK delay time 1	t_{DACD1}	—	18	ns	15.16, 15.38, 15.47, 15.60, 15.67
DACK delay time 3	t_{DACD3}	—	18	ns	15.16, 15.38, 15.47, 15.60, 15.67

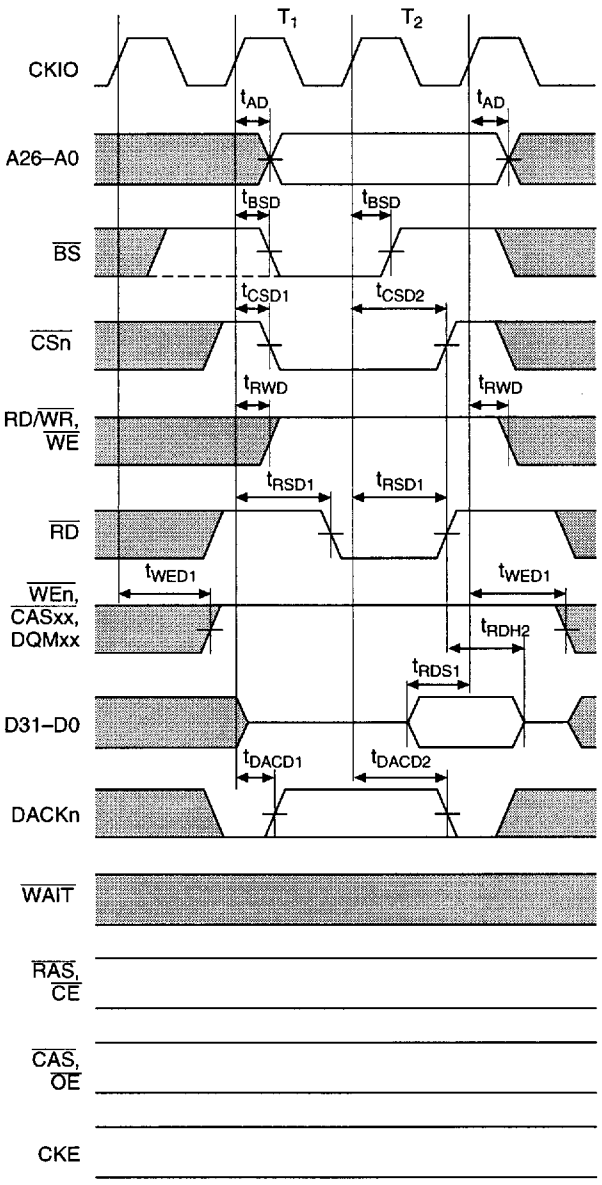
4496204 0054359 034

Table 15.9 Bus Timing With PLL Off (CKIO output) [mode 2] (Condition: V_{CC} = 5.0 V ±10%, Ta = –20 to +75°C) (cont)

Item	Symbol	Min	Max	Unit	Figures
$\overline{WAIT}$ setup time	t_{WTS}	22	—	ns	15.19, 15.43, 15.55, 15.67, 15.70
$\overline{WAIT}$ hold time	t_{WTH}	5	—	ns	15.19, 15.43, 15.55, 15.67, 15.70
$\overline{RAS}$ delay time 1 (SDRAM)	t_{RASD1}	—	18	ns	15.38
$\overline{RAS}$ delay time 3 (DRAM)	t_{RASD3}	3	18	ns	15.47
$\overline{CAS}$ delay time 1 (SDRAM)	t_{CASD1}	—	18	ns	15.38
$\overline{CAS}$ delay time 3 (DRAM)	t_{CASD3}	3	18	ns	15.47
DQM delay time	t_{DQMD}	—	18	ns	15.38
CKE delay time	t_{CKED}	—	21	ns	15.37
$\overline{CE}$ delay time 2	t_{CED2}	3	18	ns	15.60
$\overline{OE}$ delay time 2	t_{OED2}	—	18	ns	15.60
$\overline{IVECF}$ delay time	t_{IVD}	—	18	ns	15.69
Address input setup time*	t_{ASIN}	14	—	ns	15.71
Address input hold time*	t_{AHIN}	3	—	ns	15.71
$\overline{BS}$ input setup time*	t_{BSS}	15	—	ns	15.71
$\overline{BS}$ input hold time*	t_{BSH}	3	—	ns	15.71
Read write input setup time*	t_{RWS}	15	—	ns	15.71
Read write input hold time*	t_{RWH}	3	—	ns	15.71
Data buffer on time	t_{DON}	—	18	ns	15.17, 15.39, 15.48, 15.61
Data buffer off time	t_{DOF}	—	18	ns	15.17, 15.39, 15.48, 15.61
Address hold time 2	t_{AH2}	5	—	ns	15.17

Note: When the external addresses monitor function is used, the PLL must be on.

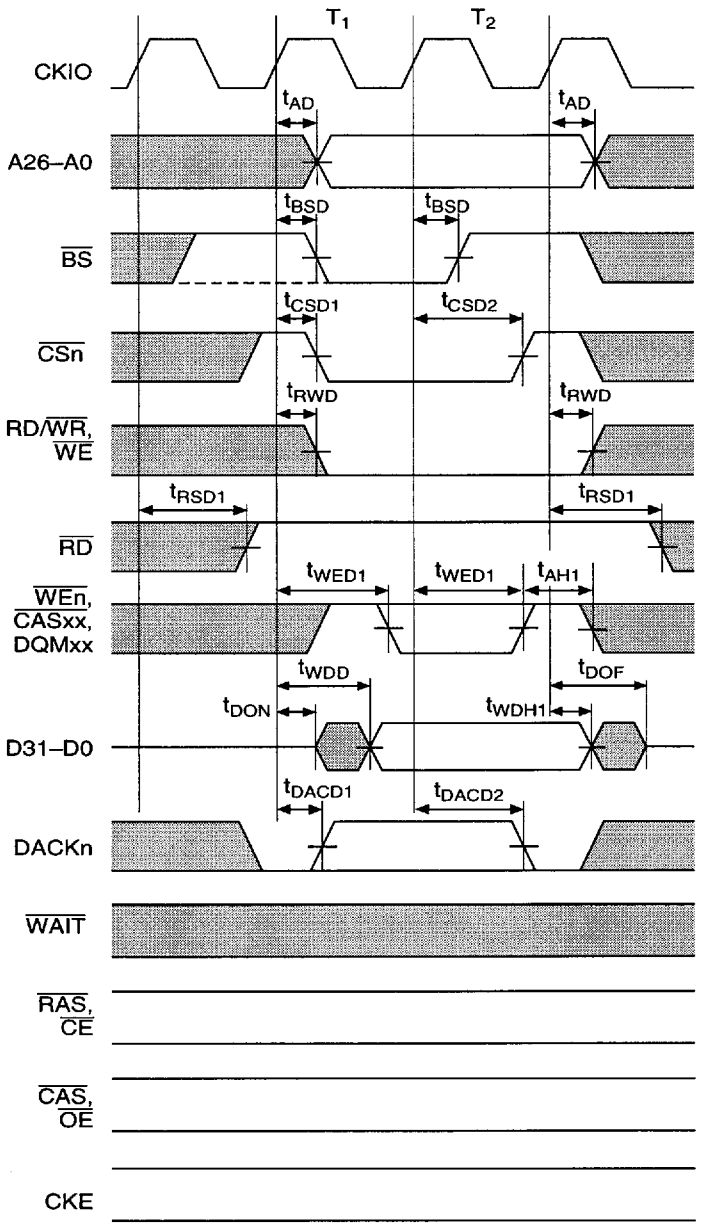
4496204 0054360 856



Notes: 1. Dotted lines indicate a synchronous DRAM is connected.
2. t_{RDH2} is defined by the faster of $\overline{CSn}$ and $\overline{RD}$.
3. The DACKn waveform shown is for the case where active high has been specified.

Figure 15.14 Basic Read Cycle (No Waits, PLL On)

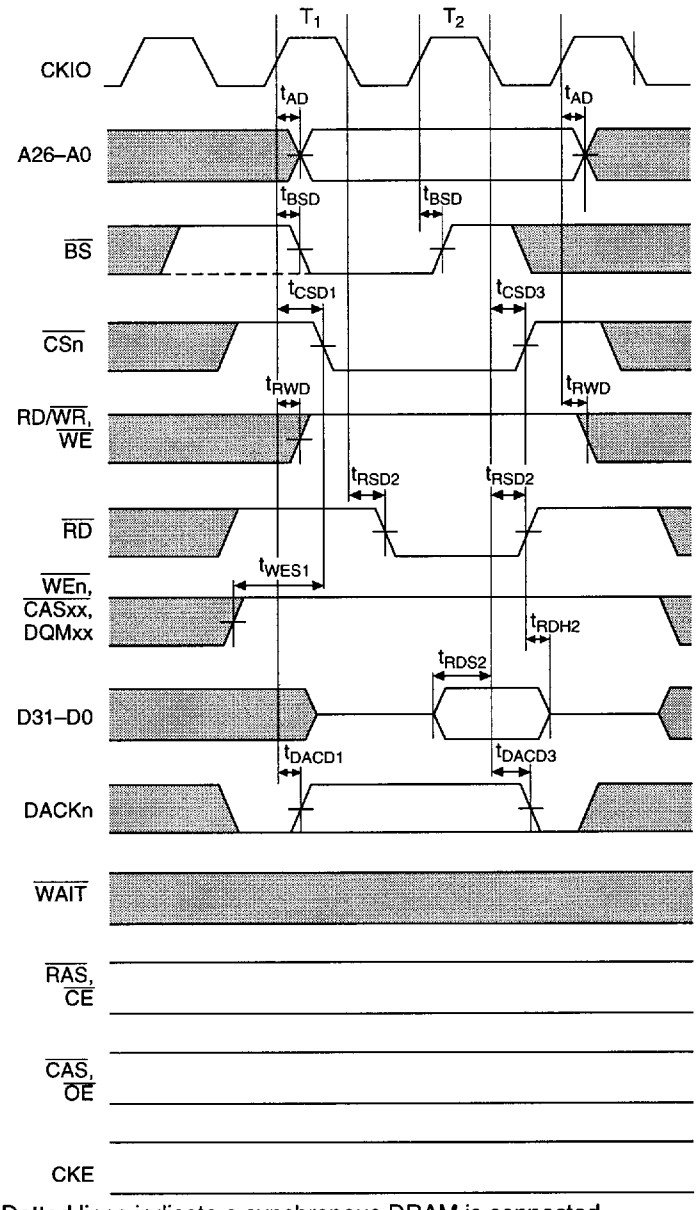
4496204 0054361 792



Notes: 1. Dotted lines indicate a synchronous DRAM is connected.
2. The DACKn waveform shown is for the case where active high has been specified.

Figure 15.15 Basic Write Cycle (No Waits, PLL On)

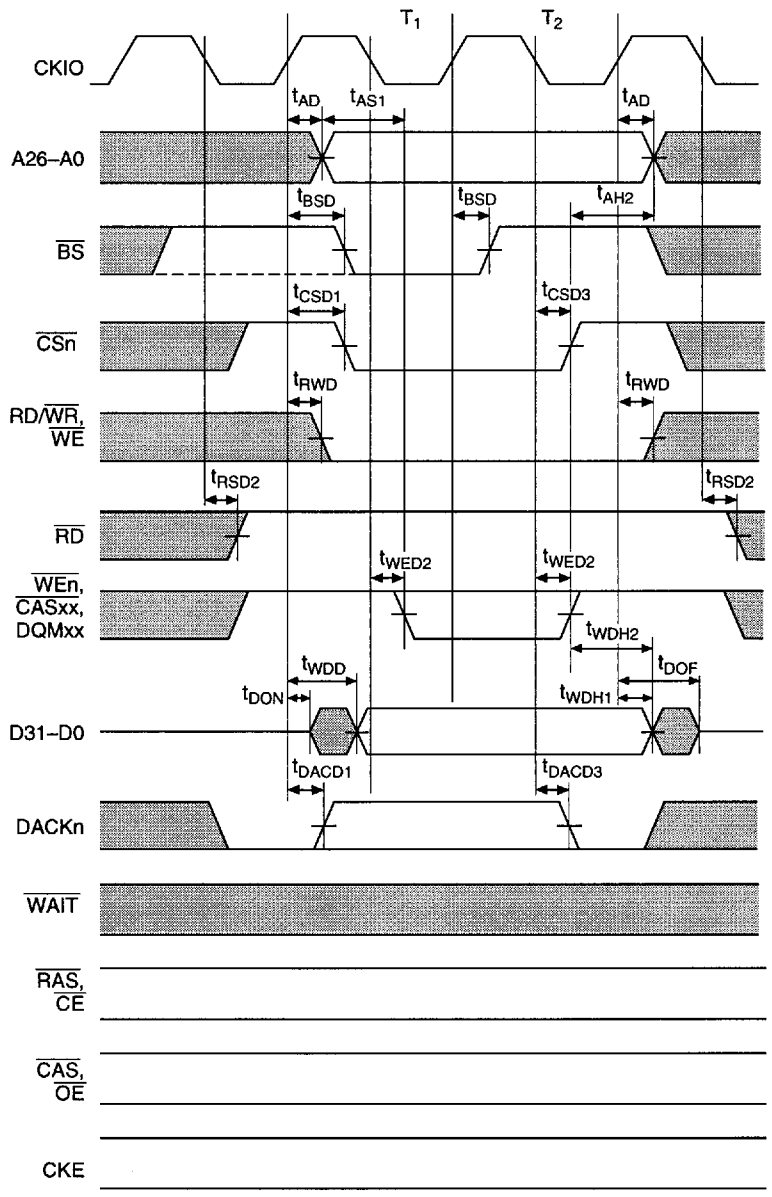
4496204 0054362 629



Notes: 1. Dotted lines indicate a synchronous DRAM is connected.
2. t_{RDH2} is defined by the faster of $\overline{CSn}$ and $\overline{RD}$.
3. The DACKn waveform shown is for the case where active high has been specified.

Figure 15.16 Basic Read Cycle (No Waits, PLL Off)

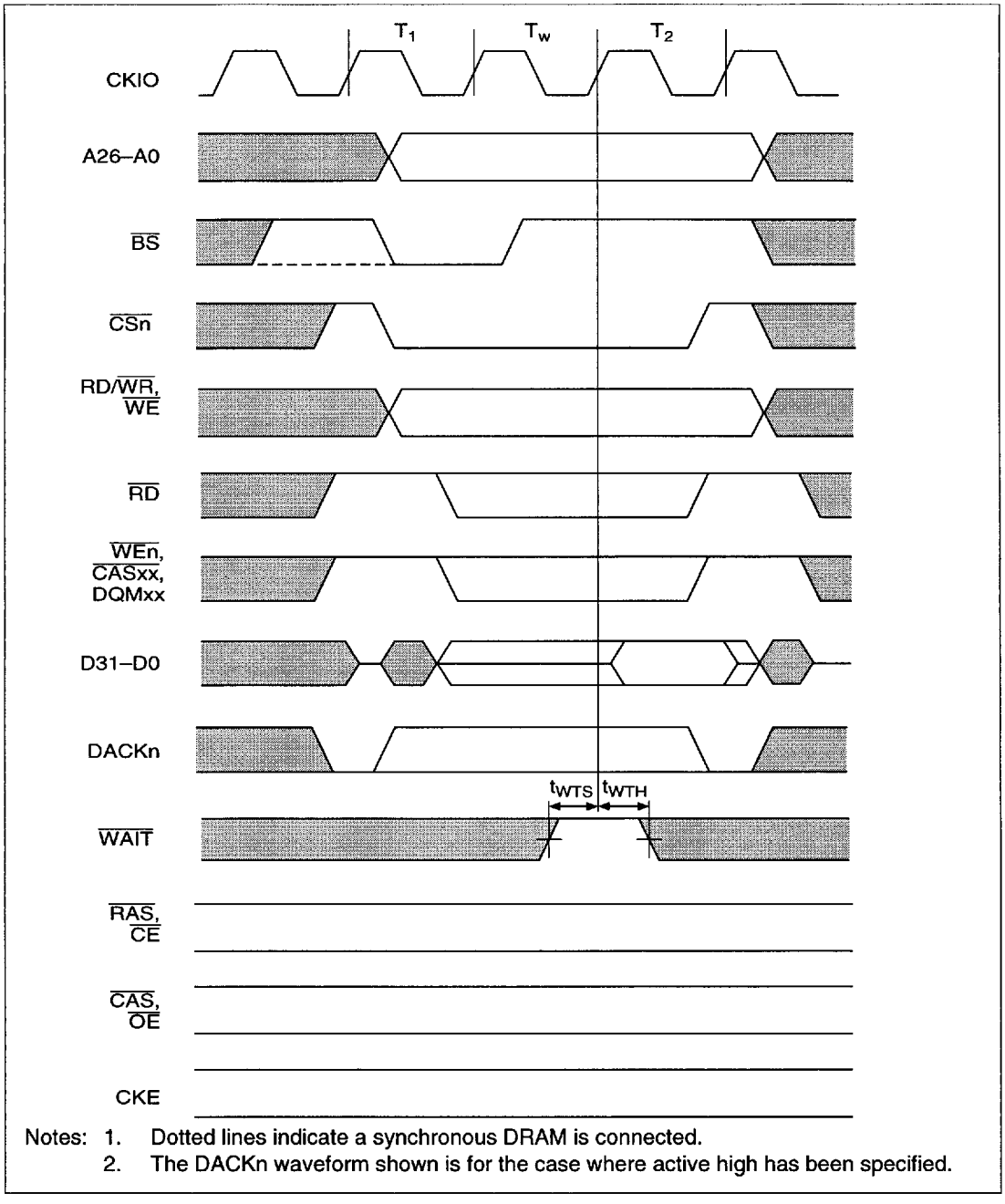
4496204 0054363 565



Notes: 1. Dotted lines indicate a synchronous DRAM is connected.
2. The DACKn waveform shown is for the case where active high has been specified.

Figure 15.17 Basic Write Cycle (No Waits, PLL Off)

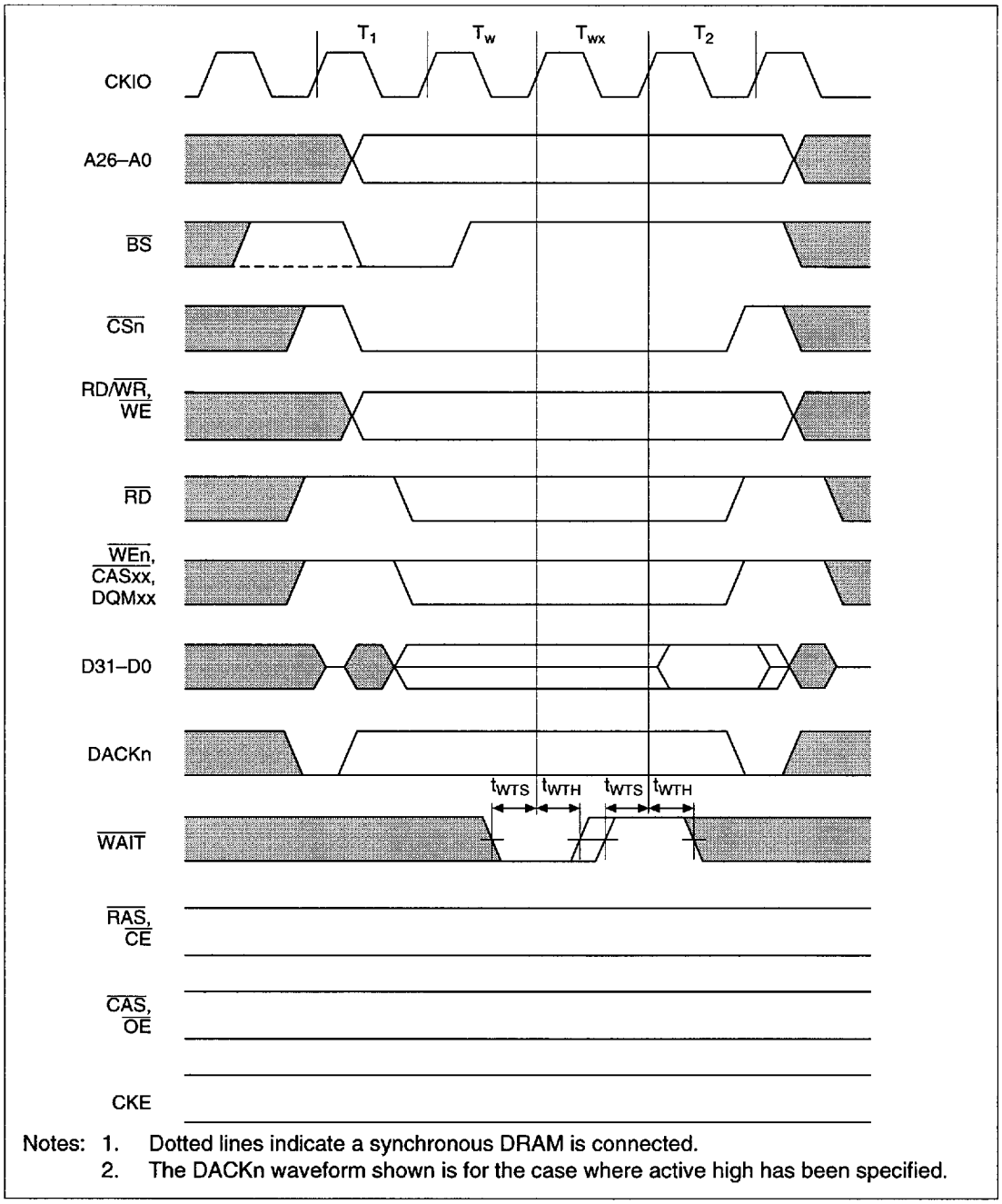
4496204 0054364 4T1



Notes: 1. Dotted lines indicate a synchronous DRAM is connected.
2. The DACKn waveform shown is for the case where active high has been specified.

Figure 15.18 Basic Bus Cycle (1 Wait Cycle)

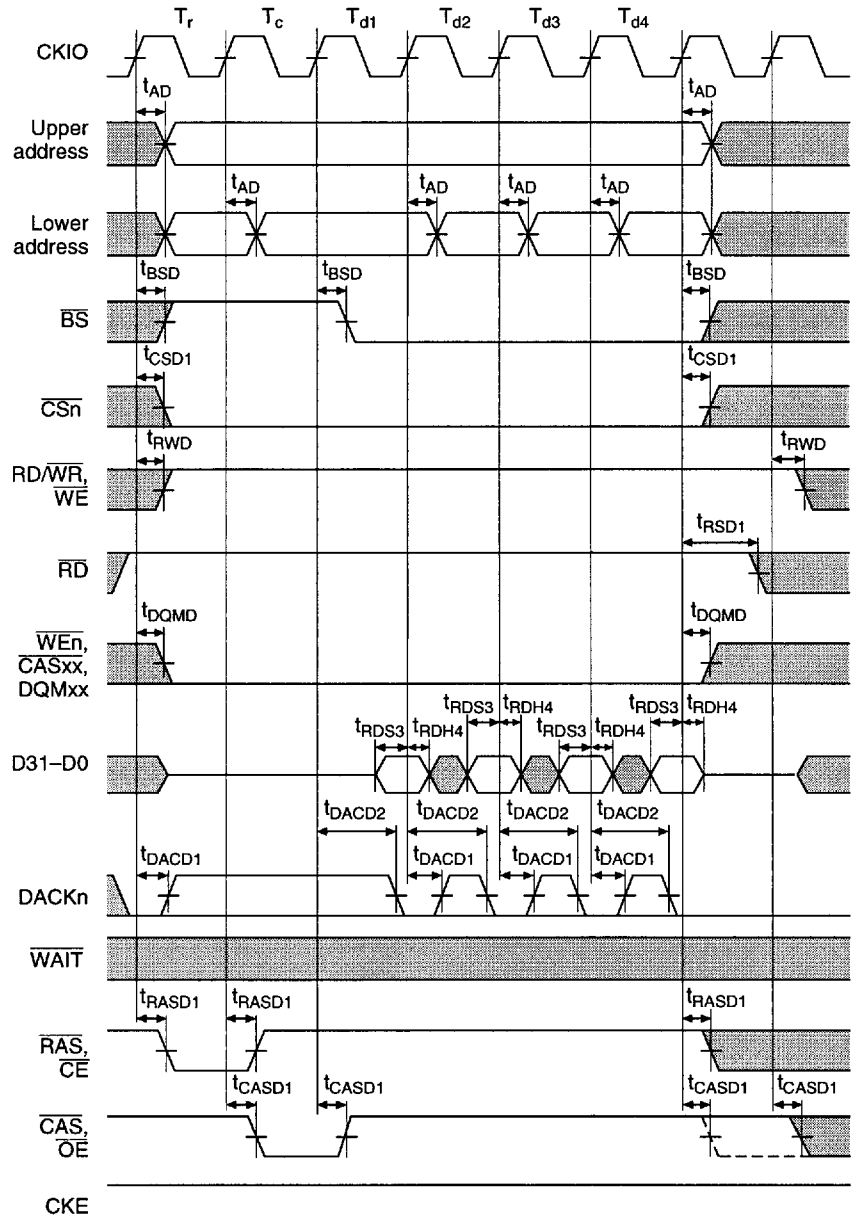
4496204 0054365 338



Notes: 1. Dotted lines indicate a synchronous DRAM is connected.
2. The DACKn waveform shown is for the case where active high has been specified.

Figure 15.19 Basic Bus Cycle (External Wait Input)

4496204 0054366 274



Notes: 1. Dotted lines indicate a synchronous DRAM in another CS space is connected.
2. The DACKn waveform shown is for the case where active high has been specified.

Figure 15.20 Synchronous DRAM Read Bus Cycle (RCD = 1 Cycle, CAS Latency = 1 Cycle, Bursts = 4, PLL On)

4496204 0054367 100

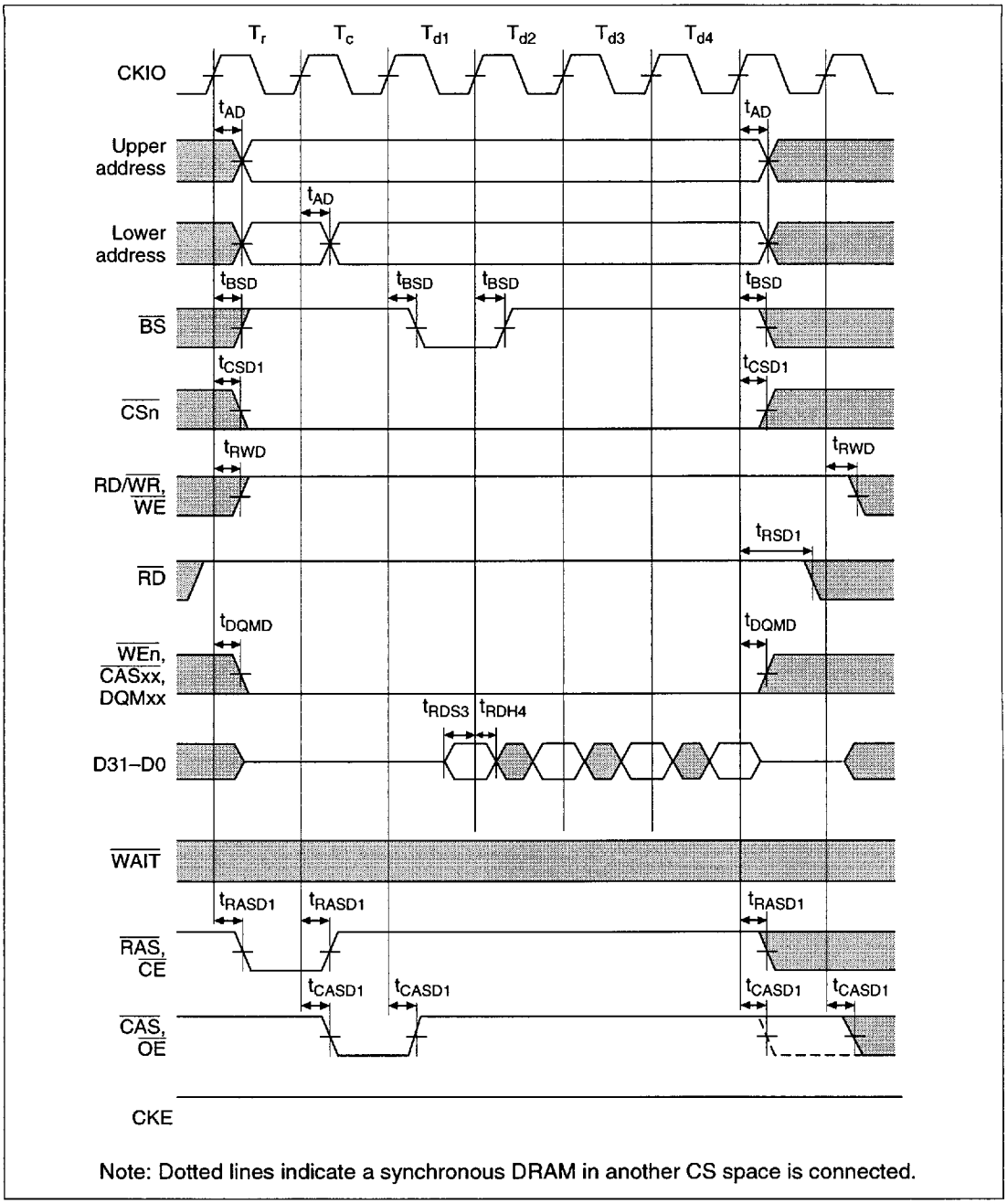
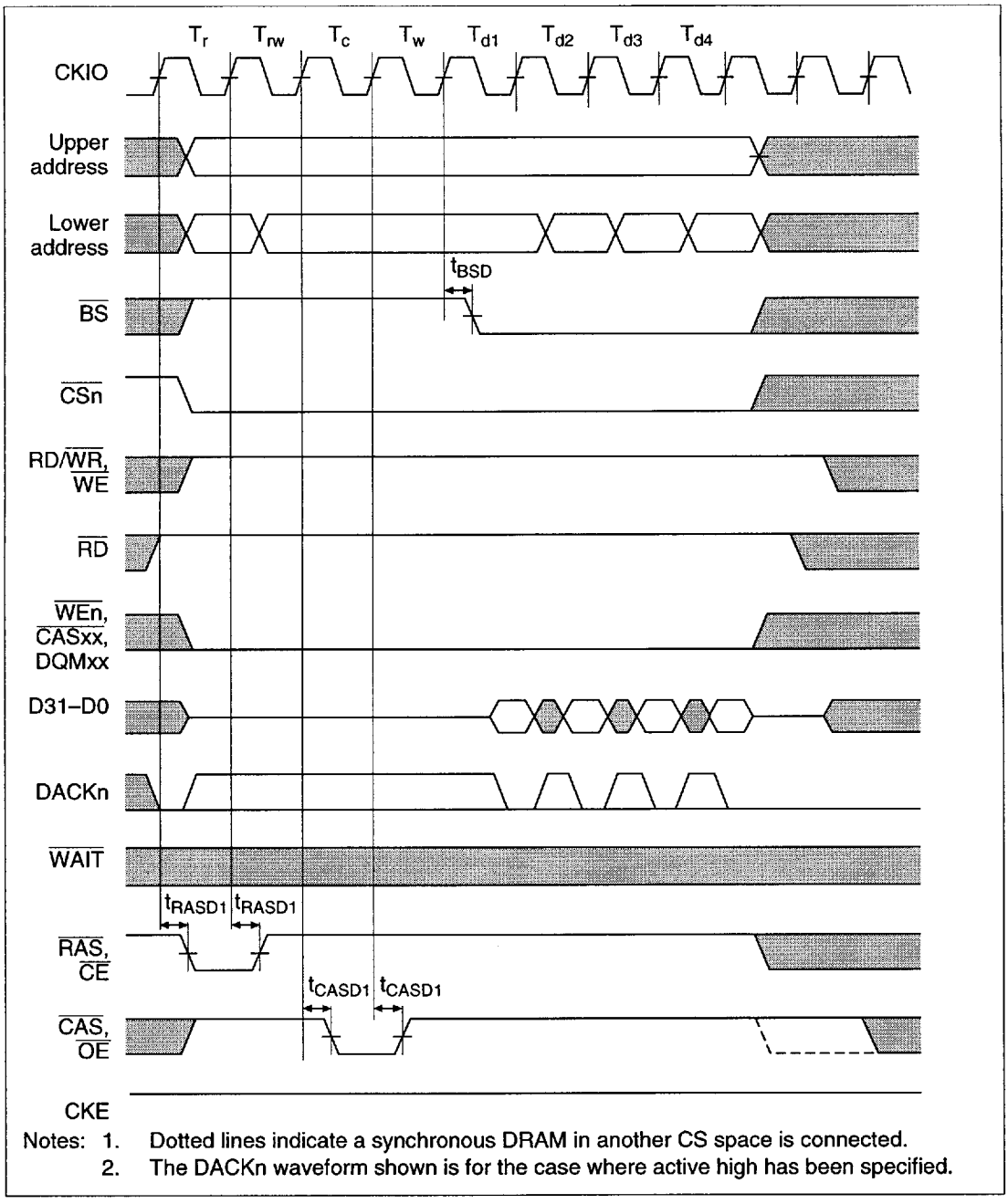


Figure 15.21 Synchronous DRAM Single Read Bus Cycle (RCD = 1 Cycle, CAS Latency = 1 Cycle, Bursts = 4, PLL On)

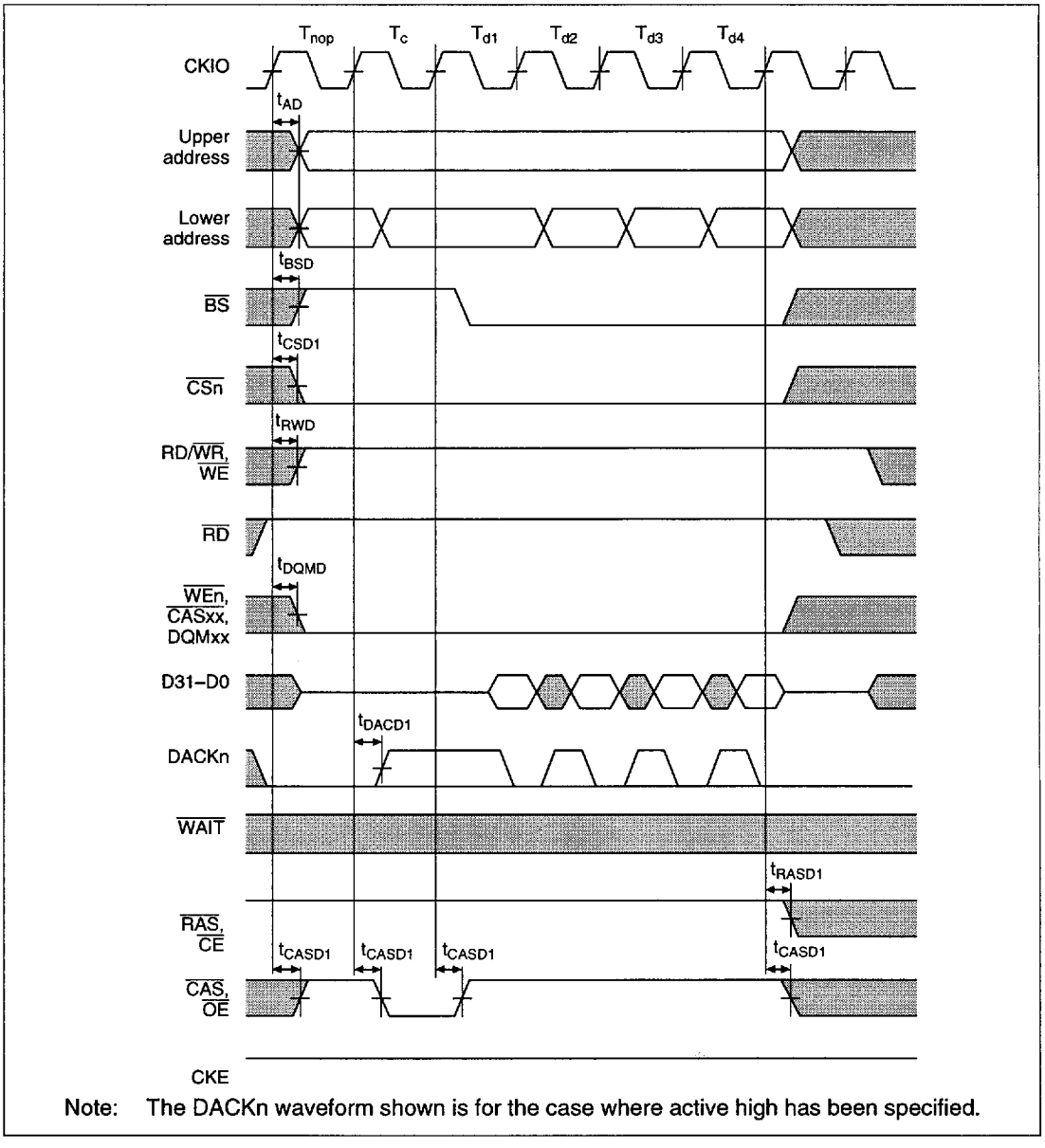
4496204 0054368 047



Notes: 1. Dotted lines indicate a synchronous DRAM in another CS space is connected.
2. The DACKn waveform shown is for the case where active high has been specified.

Figure 15.22 Synchronous DRAM Read Bus Cycle (RCD = 2 Cycle, CAS Latency = 2 Cycle, Bursts = 4)

4496204 0054369 T83



Note: The DACKn waveform shown is for the case where active high has been specified.

Figure 15.23 Synchronous DRAM Read Bus Cycle (Bank Active Same Row Access, CAS Latency = 1 Cycle)

4496204 0054370 7T5

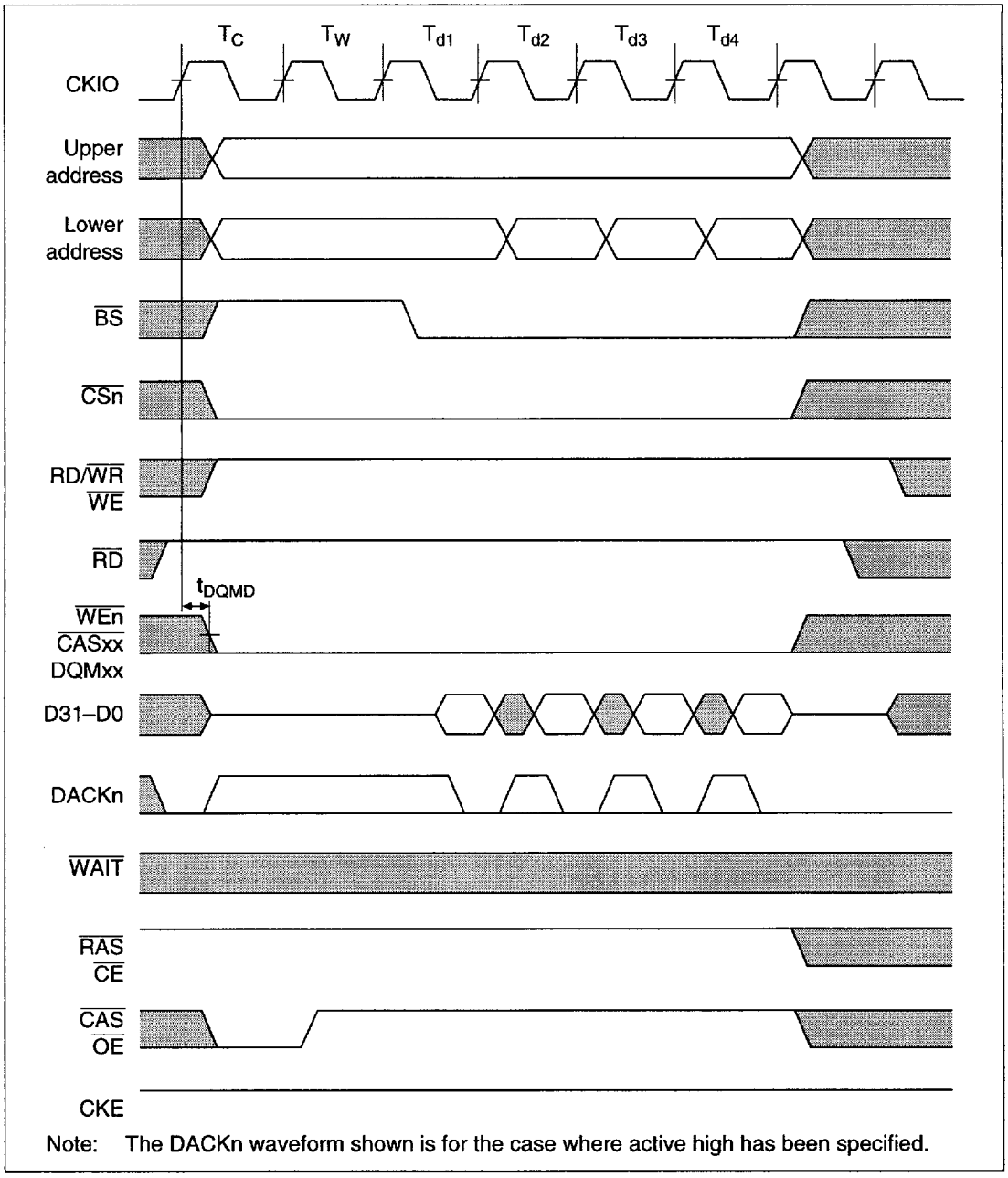
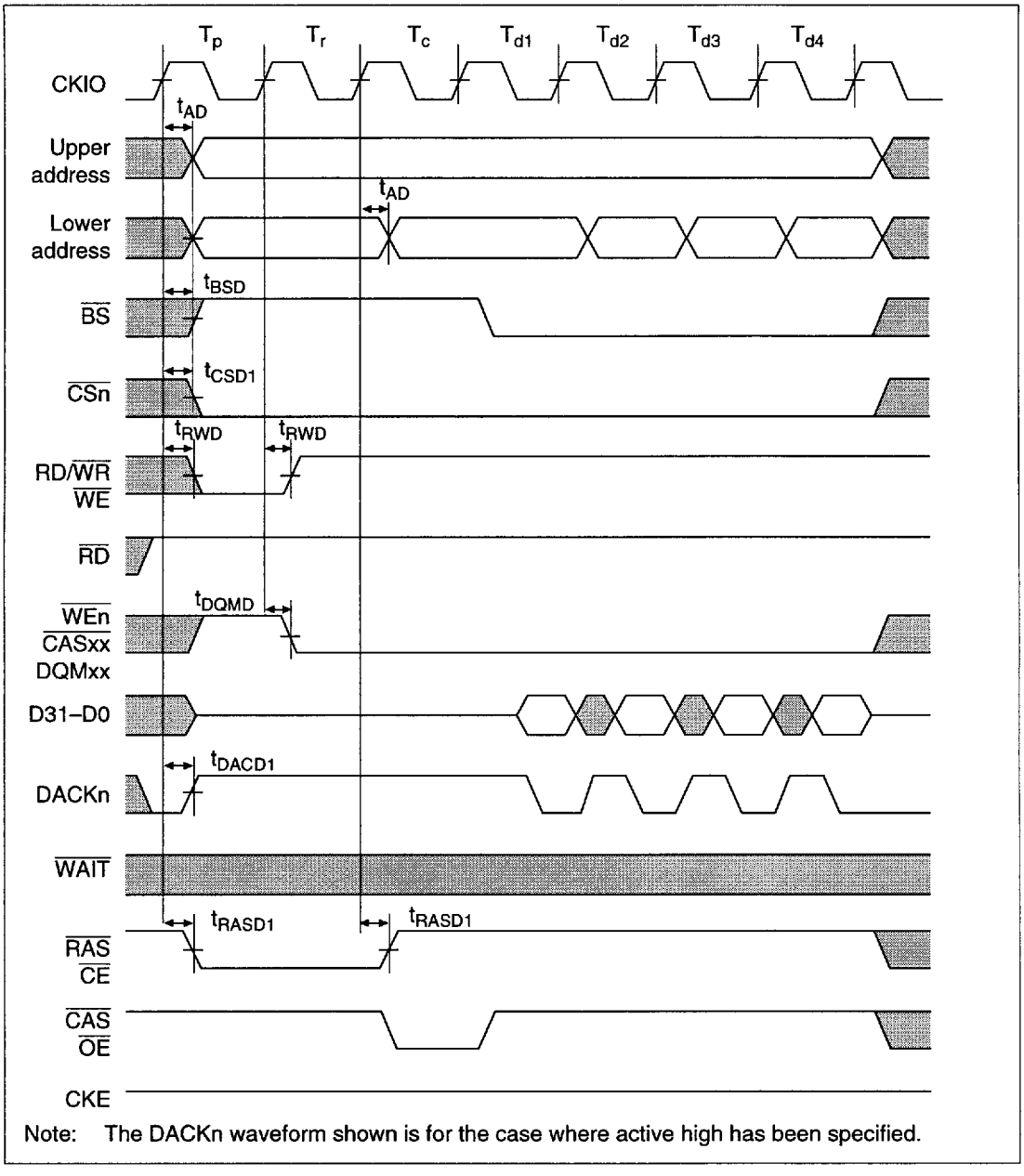


Figure 15.24 Synchronous DRAM Read Bus Cycle (Bank Active, Same Row Access, CAS Latency = 2 Cycle)

4496204 0054371 631



Note: The DACKn waveform shown is for the case where active high has been specified.

Figure 15.25 Synchronous DRAM Read Bus Cycle (Bank Active, Different Row Access TRP = 1 Cycle, RCD = 1 Cycle, CAS Latency = 1 Cycle)

4496204 0054372 578

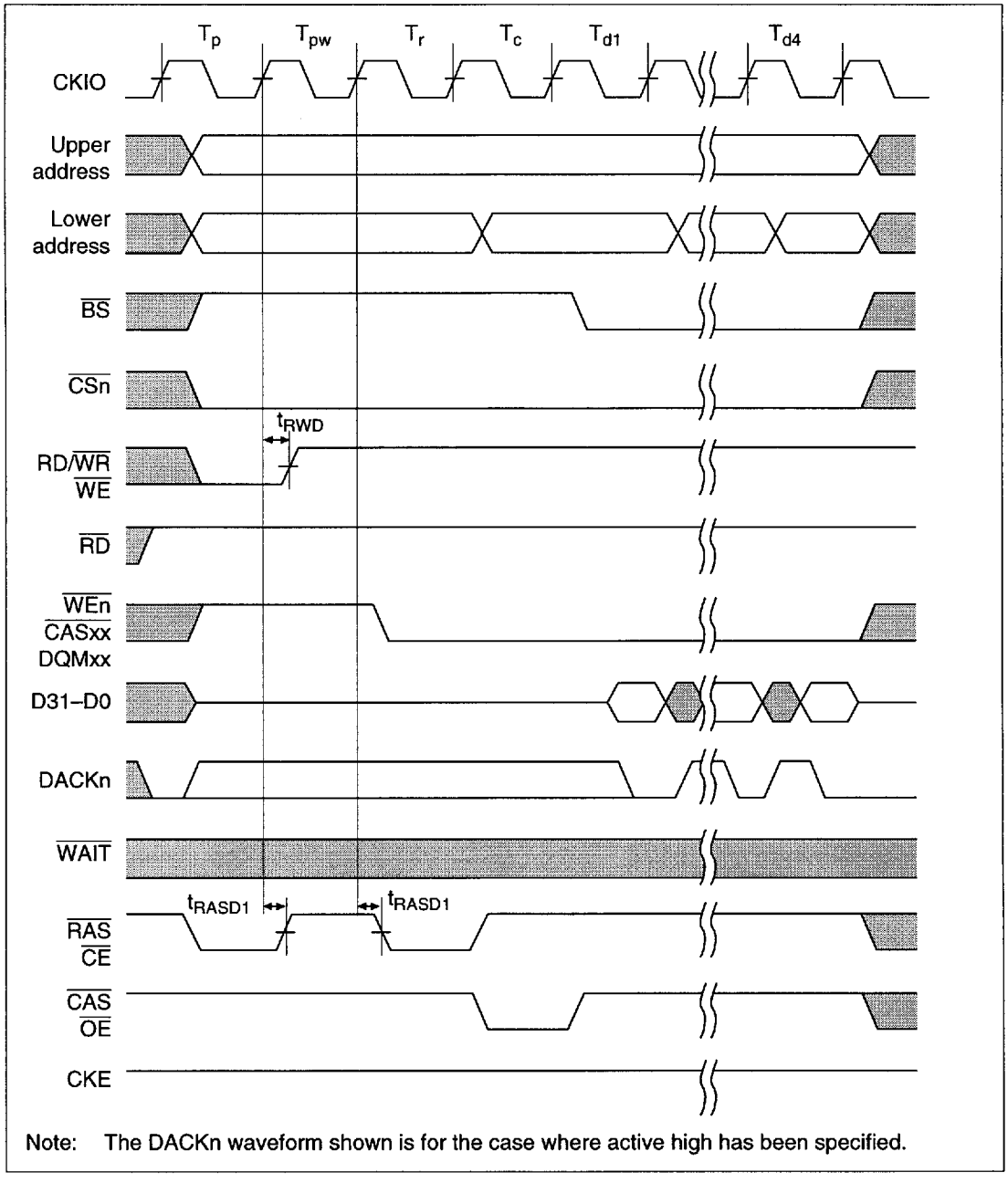
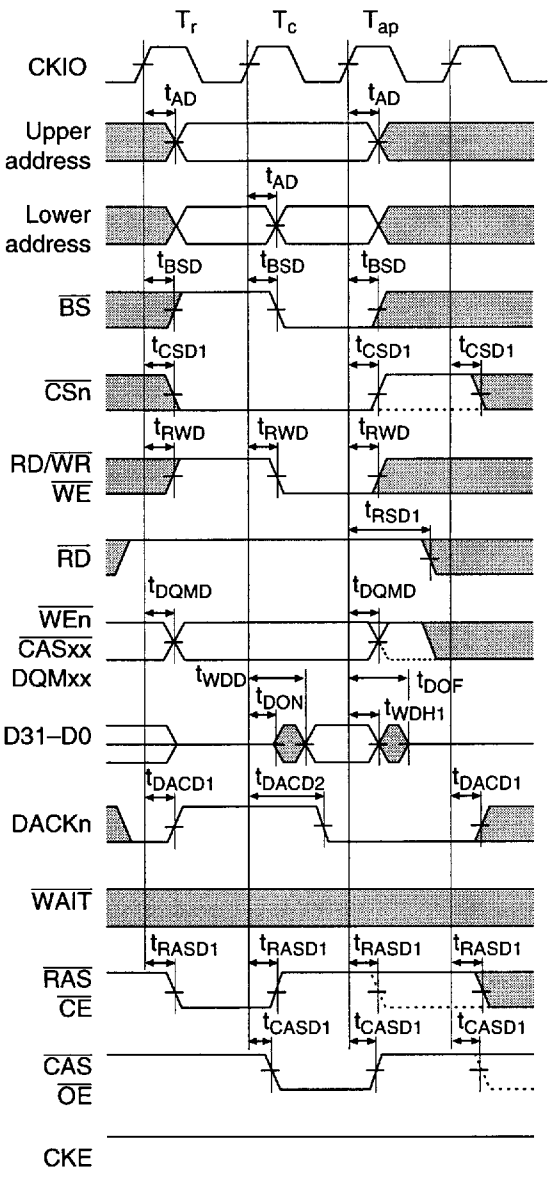


Figure 15.26 Synchronous DRAM Read Bus Cycle (Bank Active, Different Row Access TRP = 2 Cycles, RCD = 1 Cycle, CAS Latency = 1 Cycle)

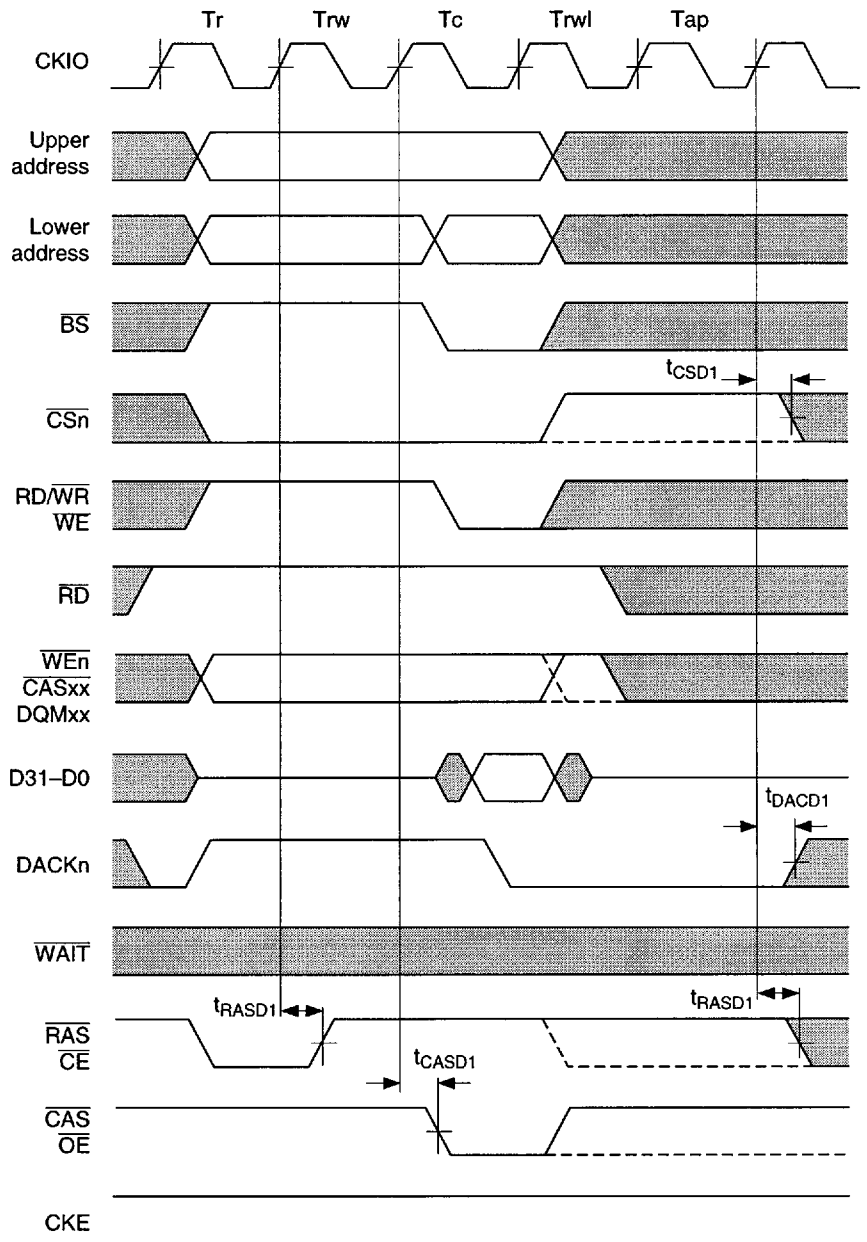
4496204 0054373 404



Notes: 1. Dotted lines indicate a synchronous DRAM in another CS space is accessed.
2. The DACKn waveform shown is for the case where active high has been specified.

Figure 15.27 Synchronous DRAM Write Bus Cycle (RCD = 1 Cycle, TRWL = 1 Cycle, PLL On)

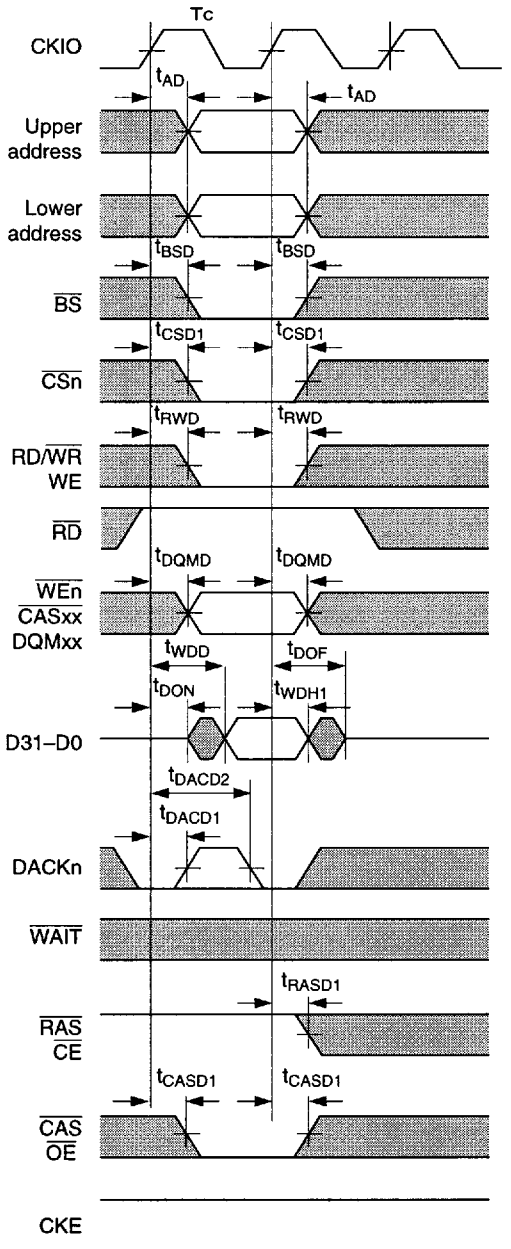
4496204 0054374 340



Notes: 1. Dotted lines indicate a synchronous DRAM in another CS space is accessed.
2. The DACKn waveform shown is for the case where active high has been specified.

Figure 15.28 Synchronous DRAM Write Bus Cycle (RCD = 2 Cycles, TRWL = 2 Cycles)

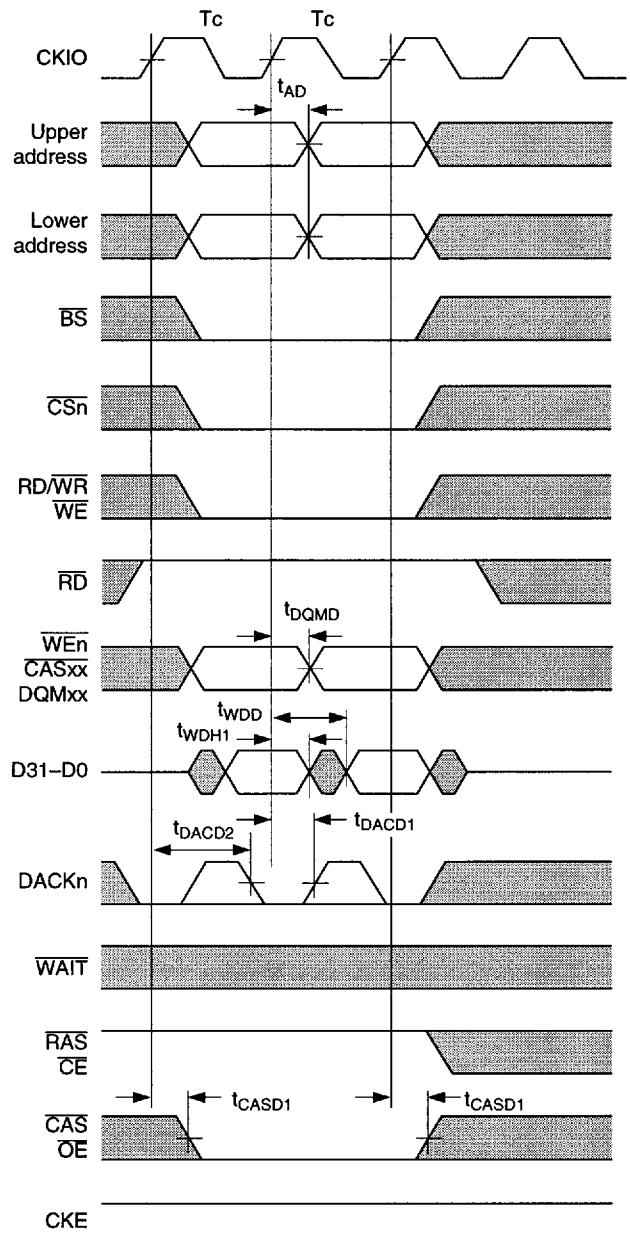
4496204 0054375 287



Note: The DACKn waveform shown is for the case where active high has been specified.

Figure 15.29 Synchronous DRAM Write Bus Cycle (Bank Active, Same Row Access)

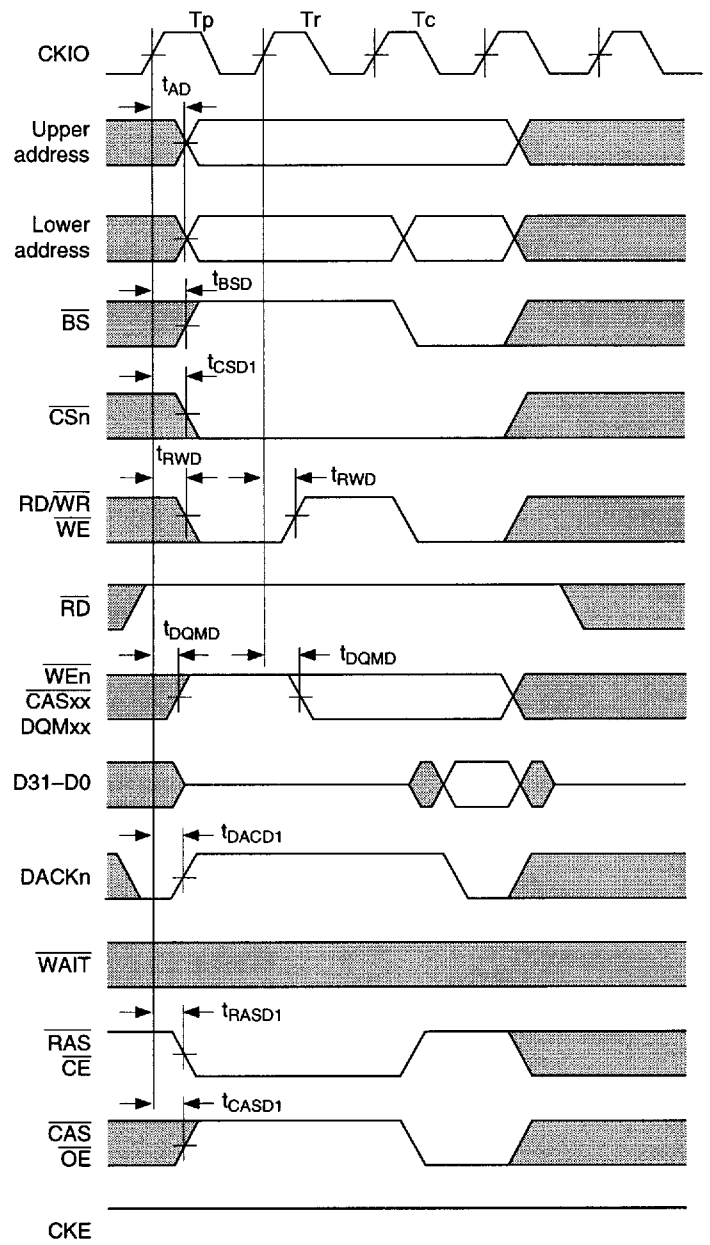
4496204 0054376 113



Note: The DACKn waveform shown is for the case where active high has been specified.

Figure 15.30 Synchronous DRAM Consecutive Write Cycle (Bank Active, Same Row Access)

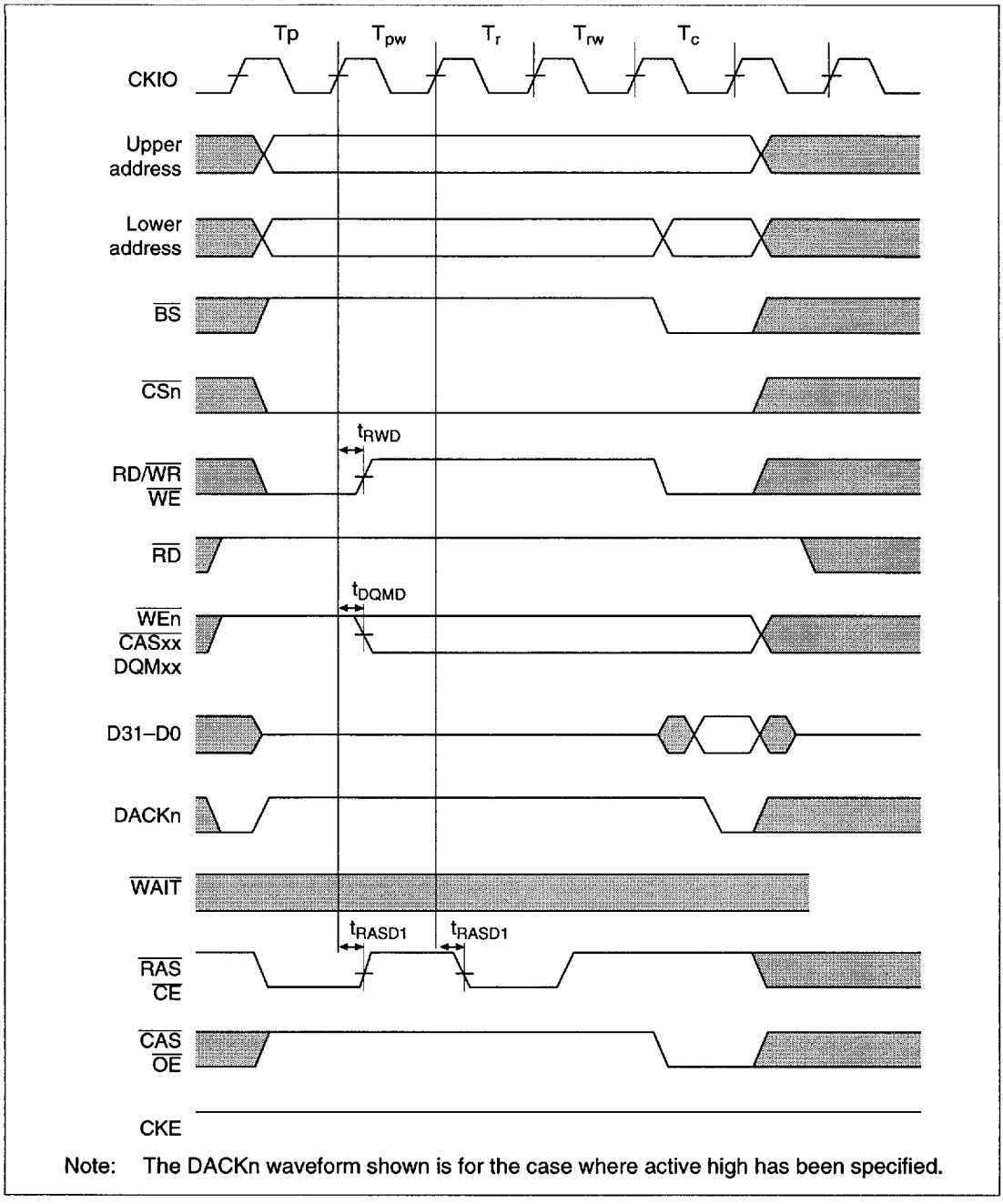
4496204 0054377 05T



Note: The DACKn waveform shown is for the case where active high has been specified.

Figure 15.31 Synchronous DRAM Write Bus Cycle (Bank Active, Different Row Access, TRP = 1 Cycle, RCD = 1 Cycle)

4496204 0054378 T96



Note: The DACKn waveform shown is for the case where active high has been specified.

Figure 15.32 Synchronous DRAM Write Bus Cycle (Bank Active, Different Row Access, TRP = 2 Cycles, RCD = 2 Cycles)

4496204 0054379 922

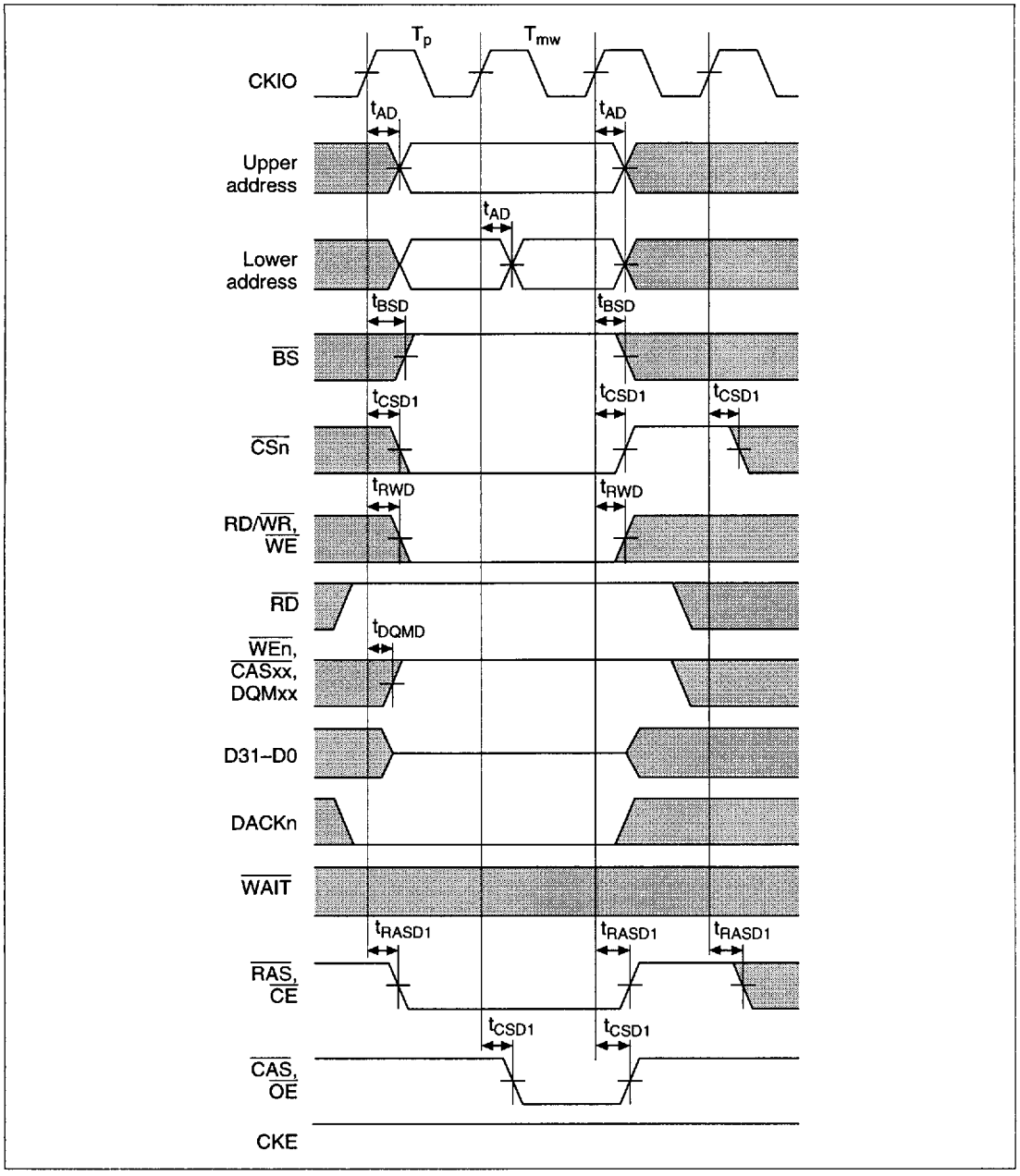


Figure 15.33 Synchronous DRAM Mode Register Write Cycle (TRP = 1 Cycle)

4496204 0054380 644

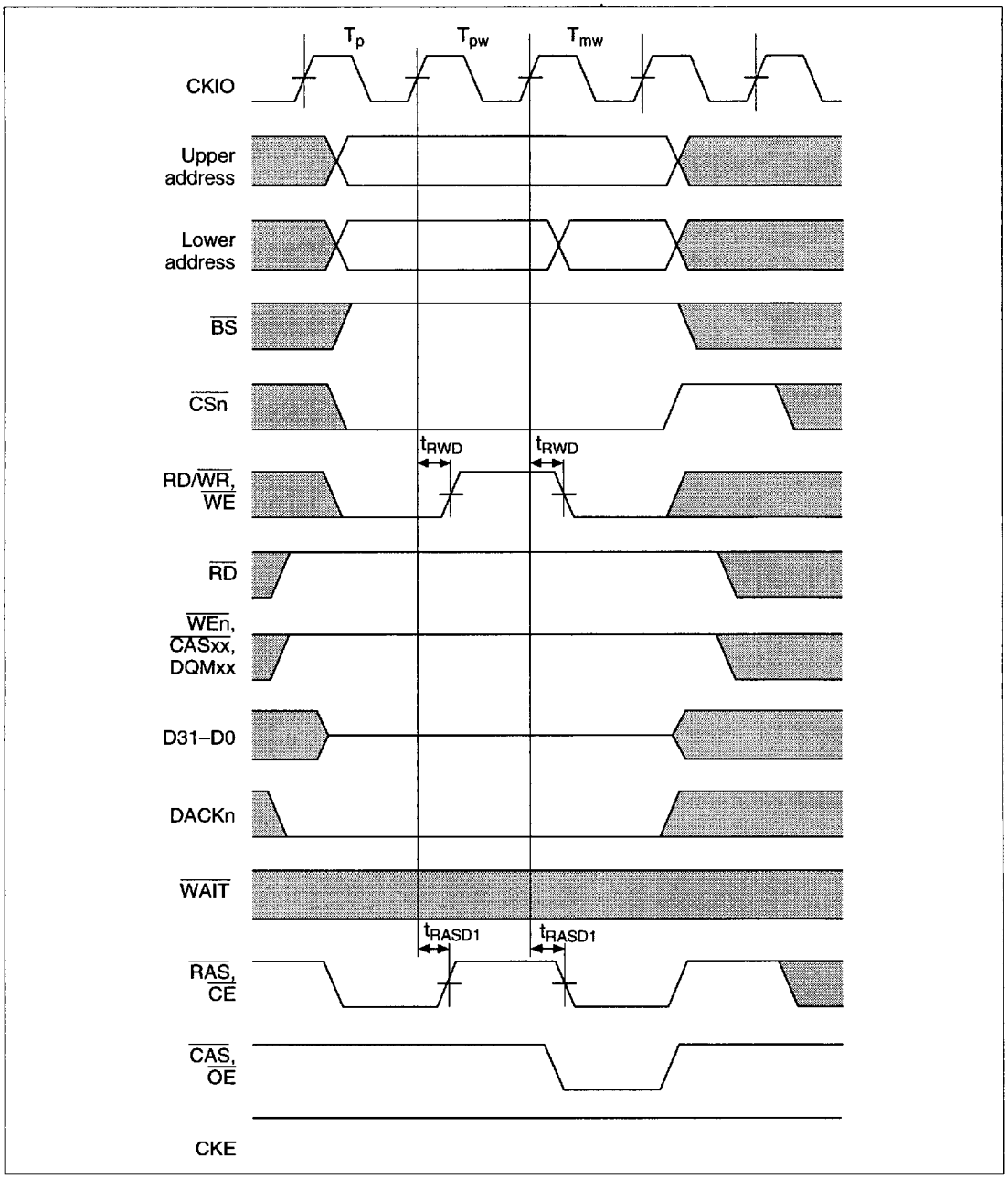
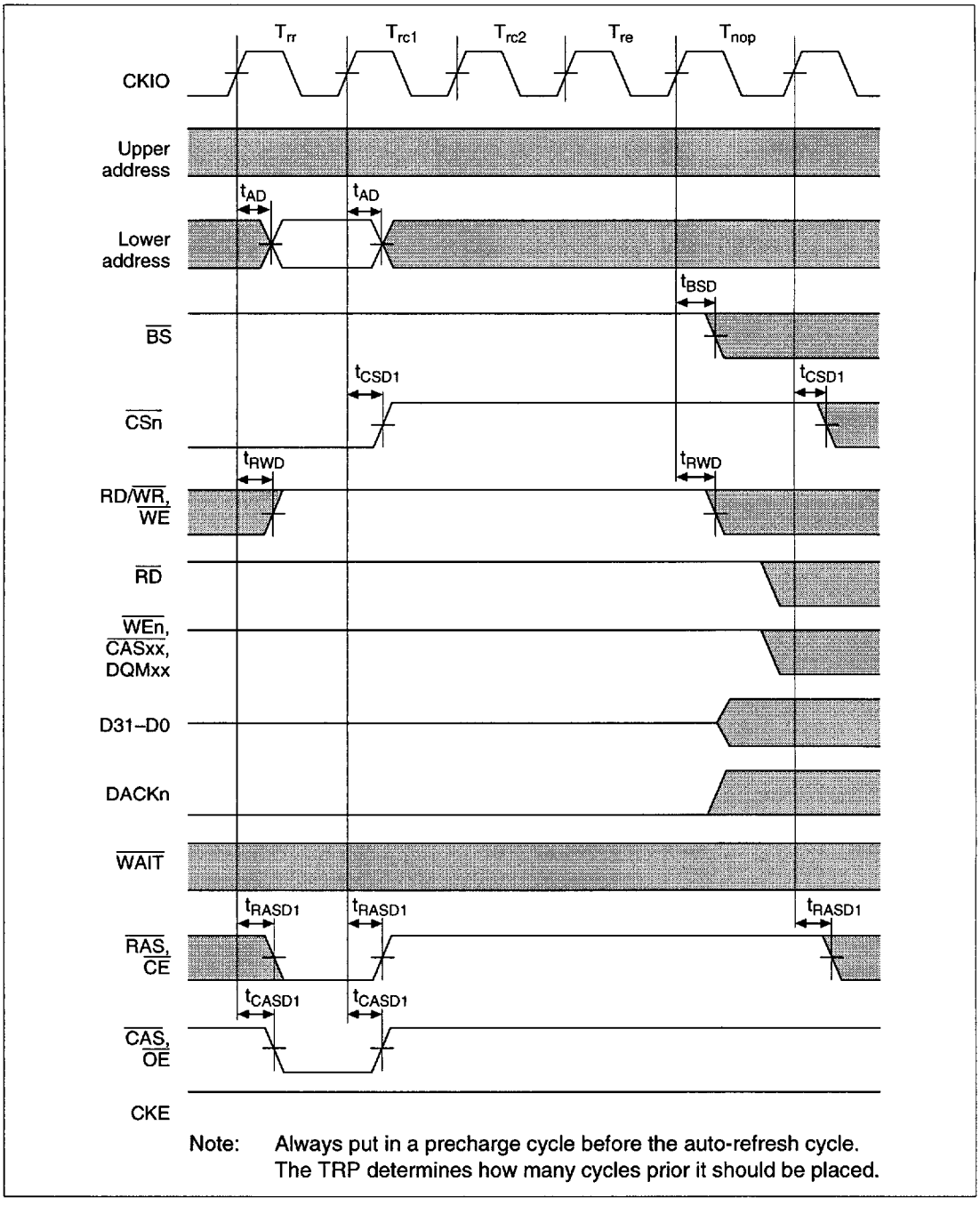


Figure 15.34 Synchronous DRAM Mode Register Write Cycle (TRP = 2 Cycles)

4496204 0054381 580



Note: Always put in a precharge cycle before the auto-refresh cycle. The TRP determines how many cycles prior it should be placed.

Figure 15.35 Synchronous DRAM Auto Refresh Cycle (TRAS = 2 Cycles)

4496204 0054382 417

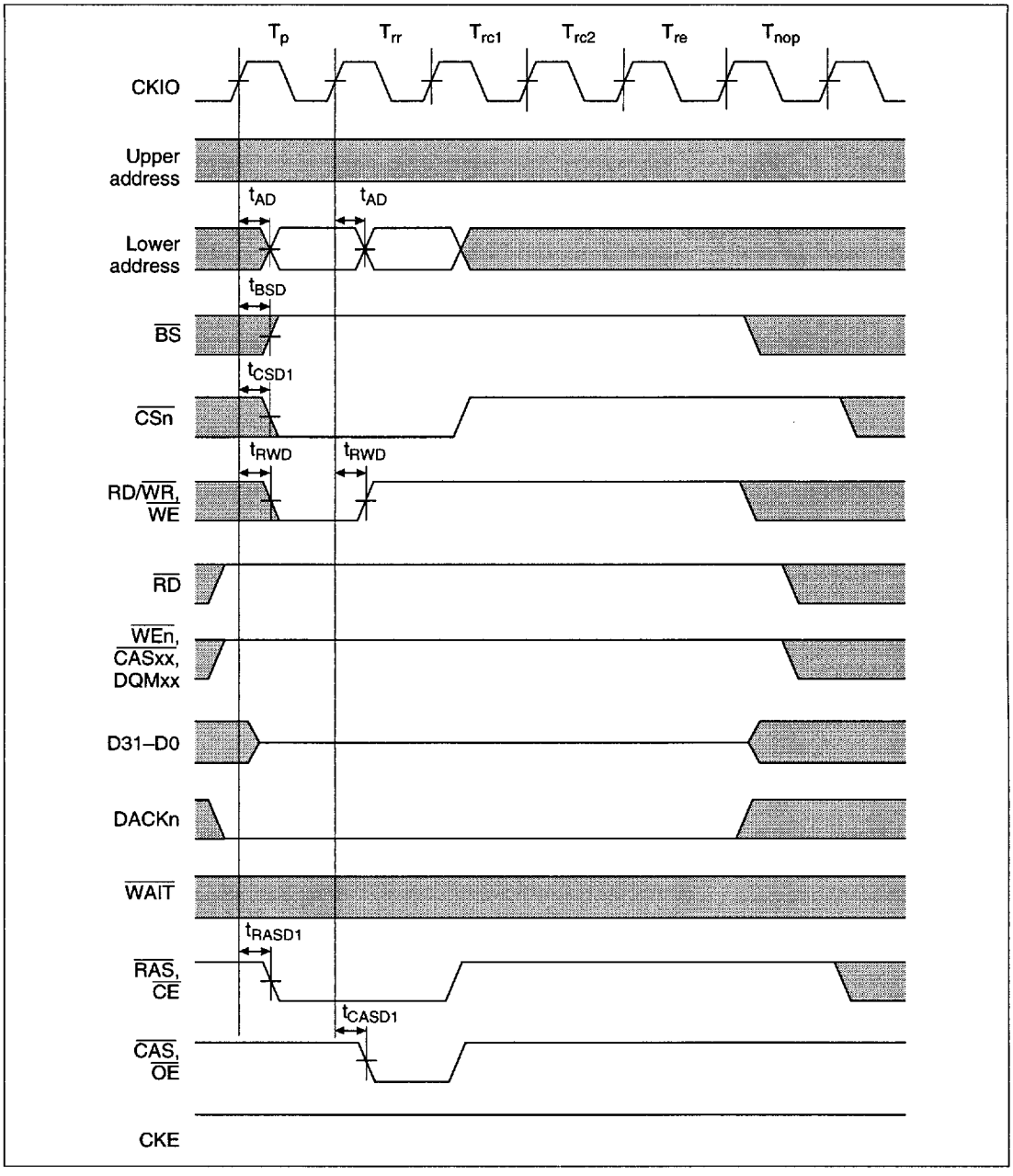
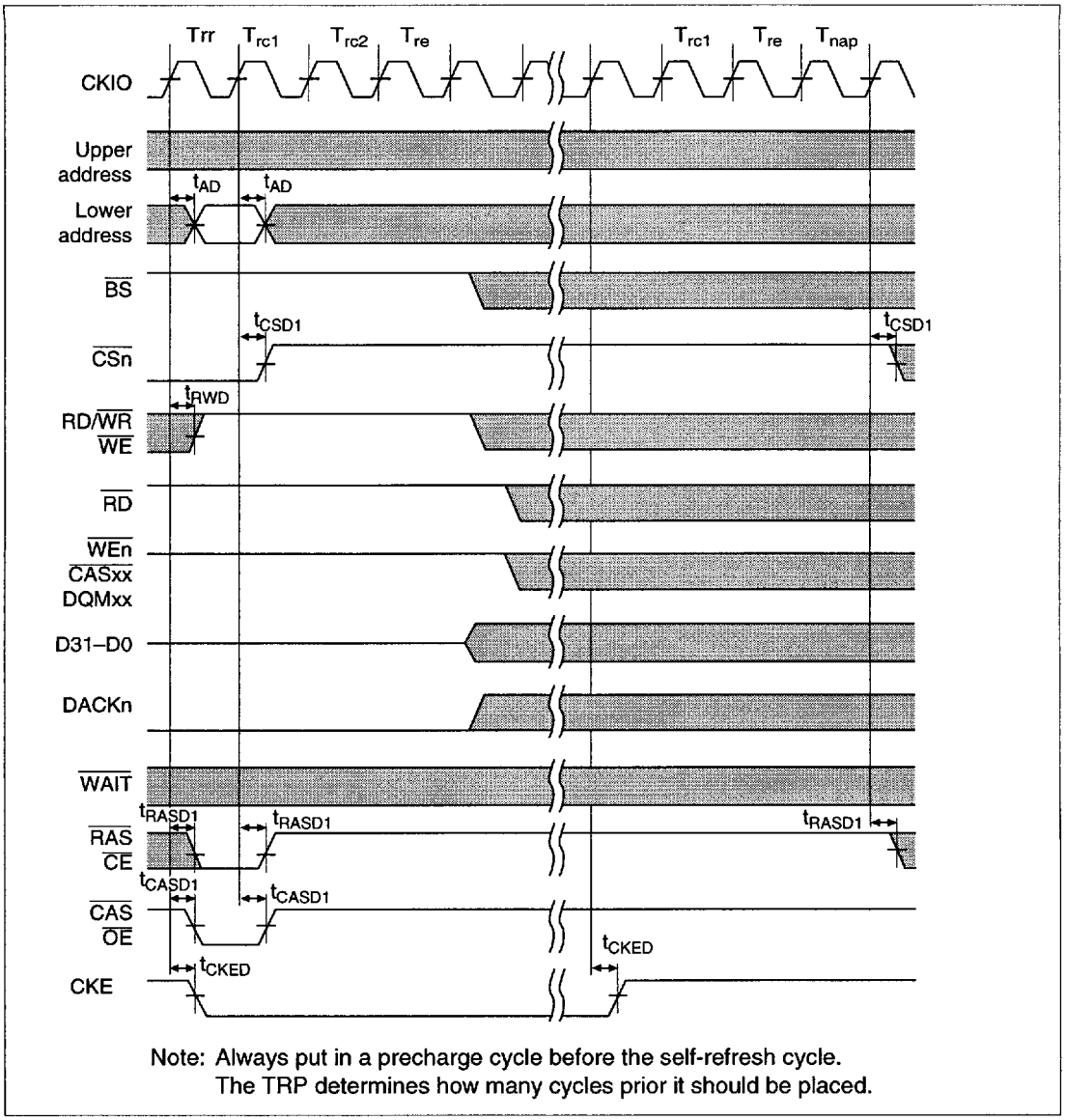


Figure 15.36 Synchronous DRAM Auto-Refresh Cycle (Shown From Precharge Cycle, TRP = 1 Cycle, TRAS = 2 Cycles)

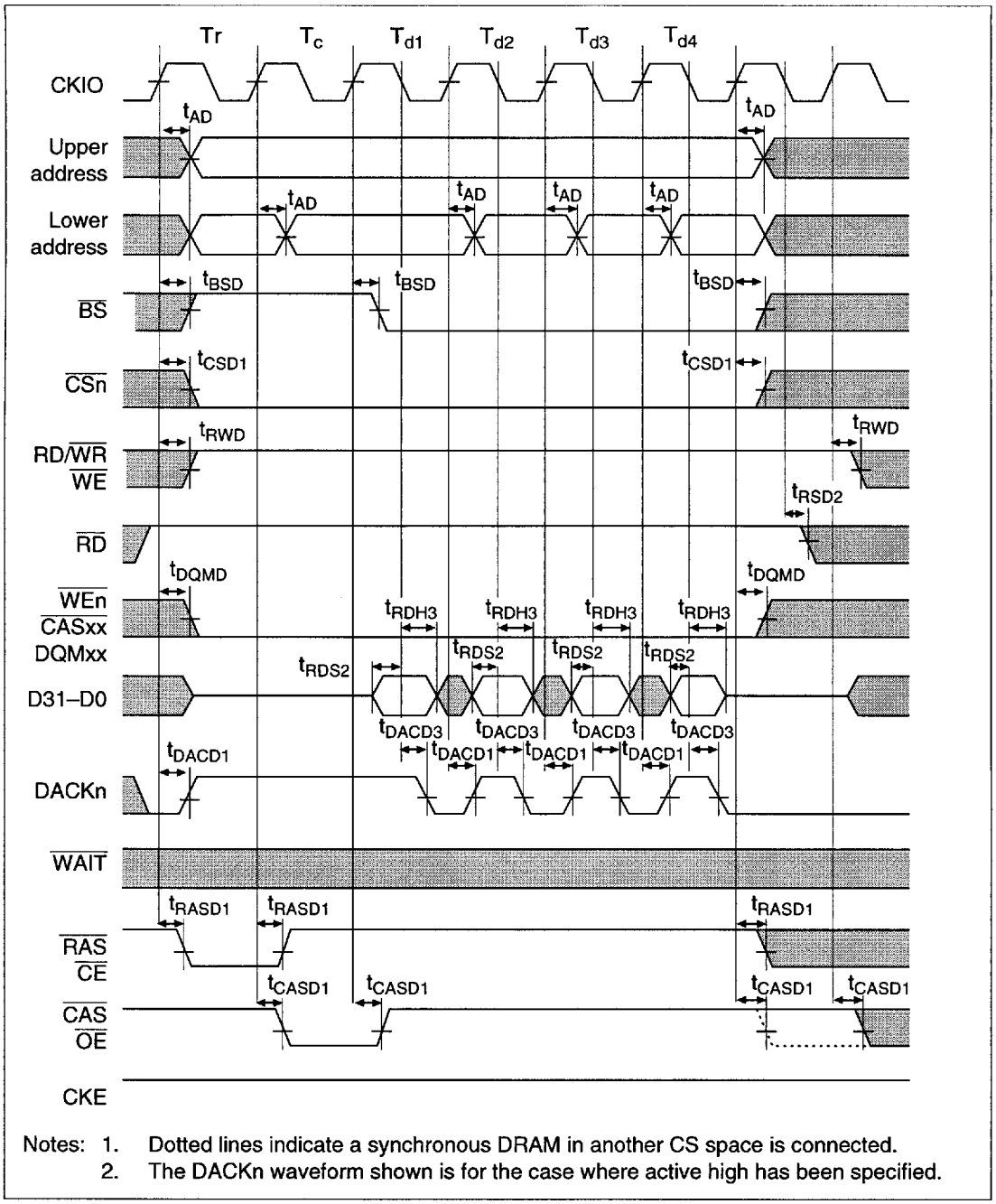
4496204 0054383 353



Note: Always put in a precharge cycle before the self-refresh cycle.
The TRP determines how many cycles prior it should be placed.

Figure 15.37 Synchronous DRAM Self-Refresh Cycle (TRAS = 2)

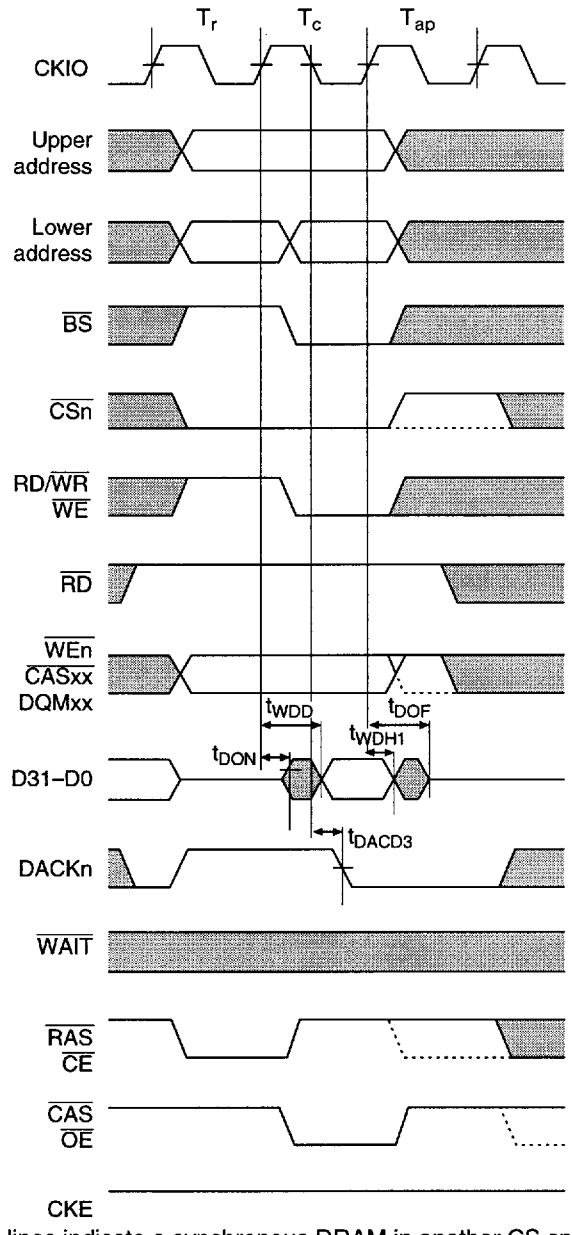
4496204 0054384 29T



Notes: 1. Dotted lines indicate a synchronous DRAM in another CS space is connected.
2. The DACKn waveform shown is for the case where active high has been specified.

Figure 15.38 Synchronous DRAM Read Bus Cycle (RCD = 1 Cycle, CAS Latency = 1 Cycle, TRP = 1 Cycle, Bursts = 4, PLL = Off)

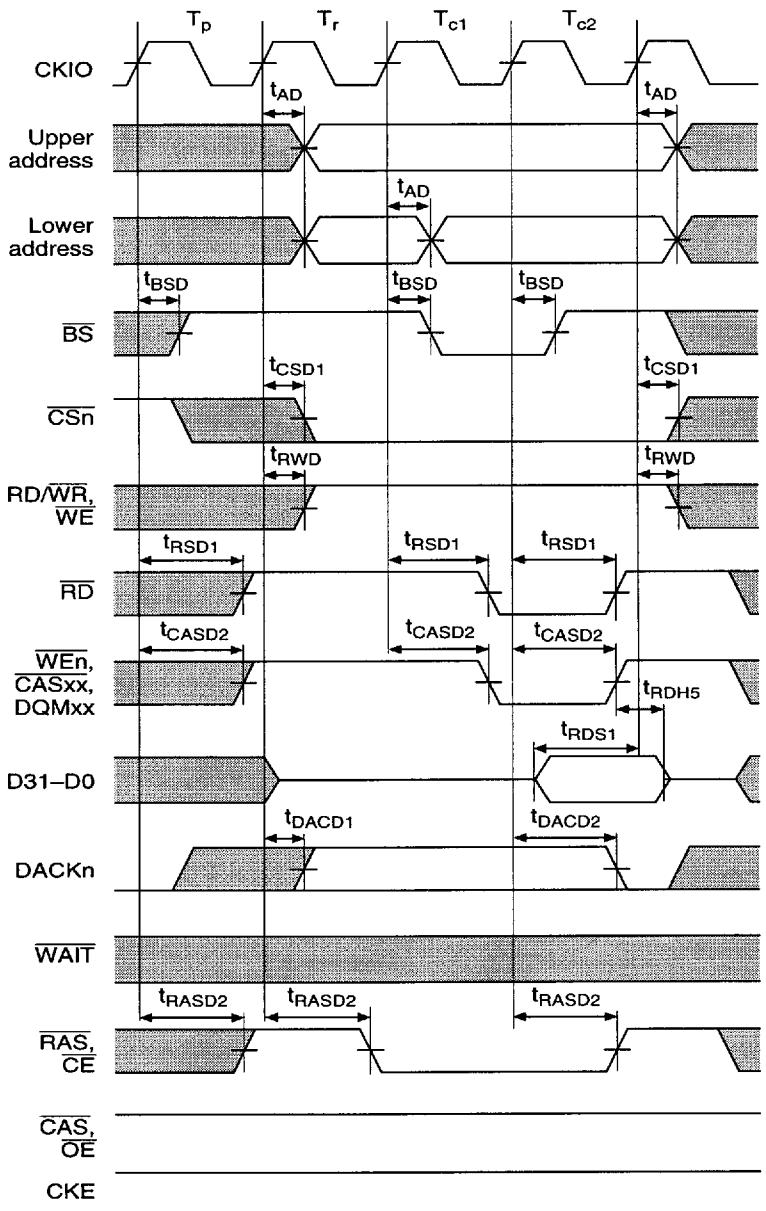
4496204 0054385 126



Notes: 1. Dotted lines indicate a synchronous DRAM in another CS space is connected.
2. The DACKn waveform shown is for the case where active high has been specified.

Figure 15.39 Synchronous DRAM Write Bus Cycle (RCD = 1 Cycle, TRWL = 1 Cycle, PLL = Off)

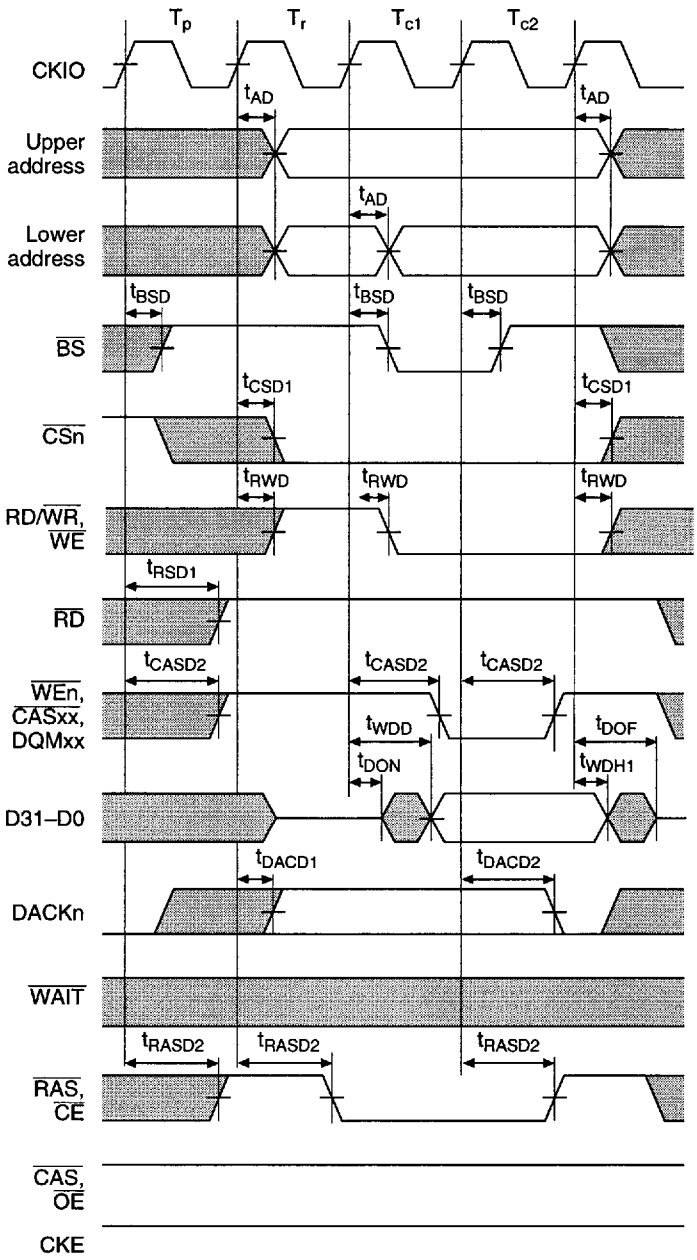
4496204 0054386 062



Notes: 1. t_{RDH5} is defined by the faster of $\overline{RD}$ and $\overline{CASxx}$ rise.
2. The DACKn waveform shown is for the case where active high has been specified.

Figure 15.40 DRAM Read Cycle (TRP = 1 Cycle, RCD = 1 Cycle, No Waits, PLL = On)

4496204 0054387 TT9



Note: The DACKn waveform shown is for the case where active high has been specified.

Figure 15.41 DRAM Write Cycle (TRP = 1 Cycle, RCD = 1 Cycle, No Waits, PLL = On)

4496204 0054388 935

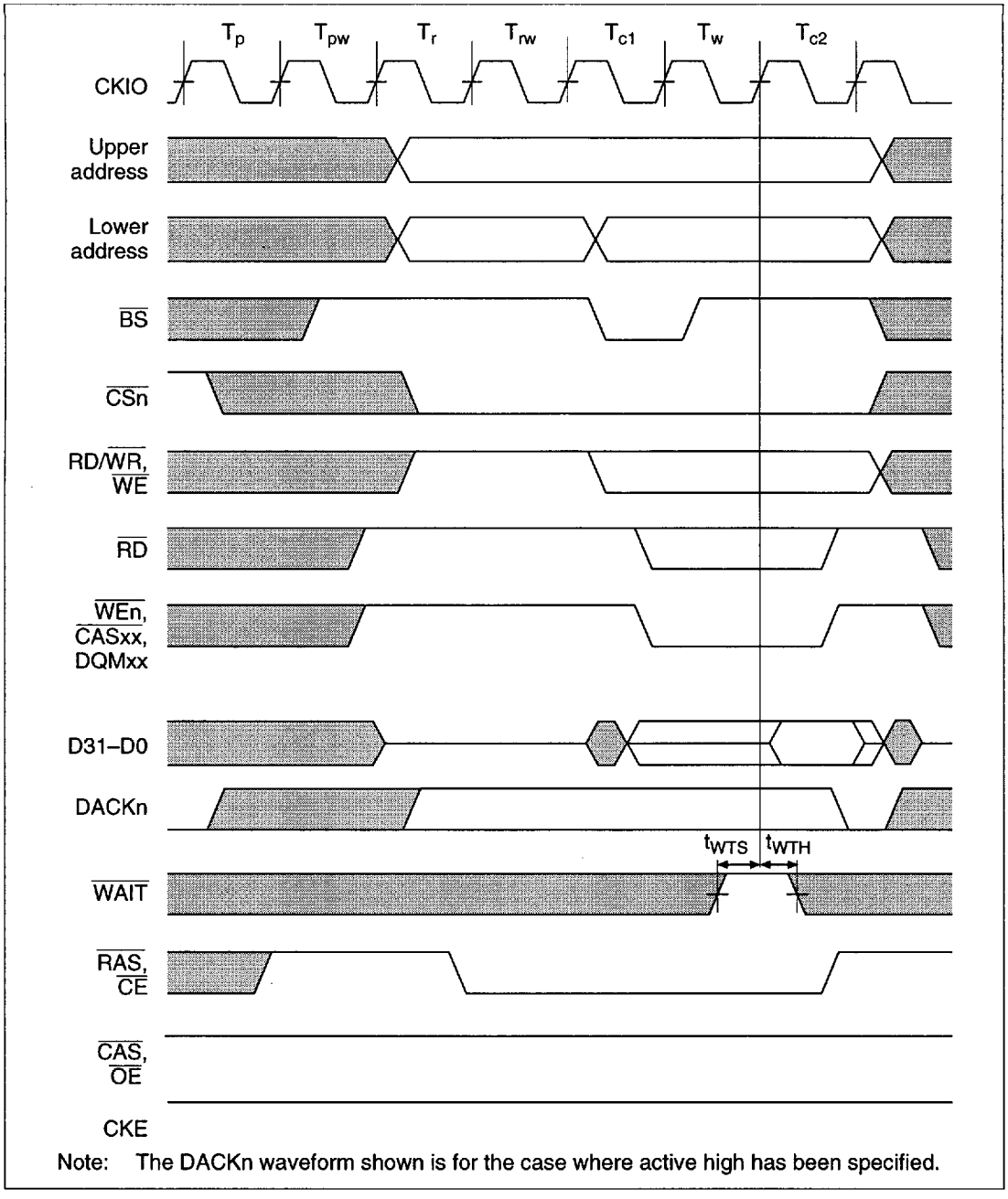
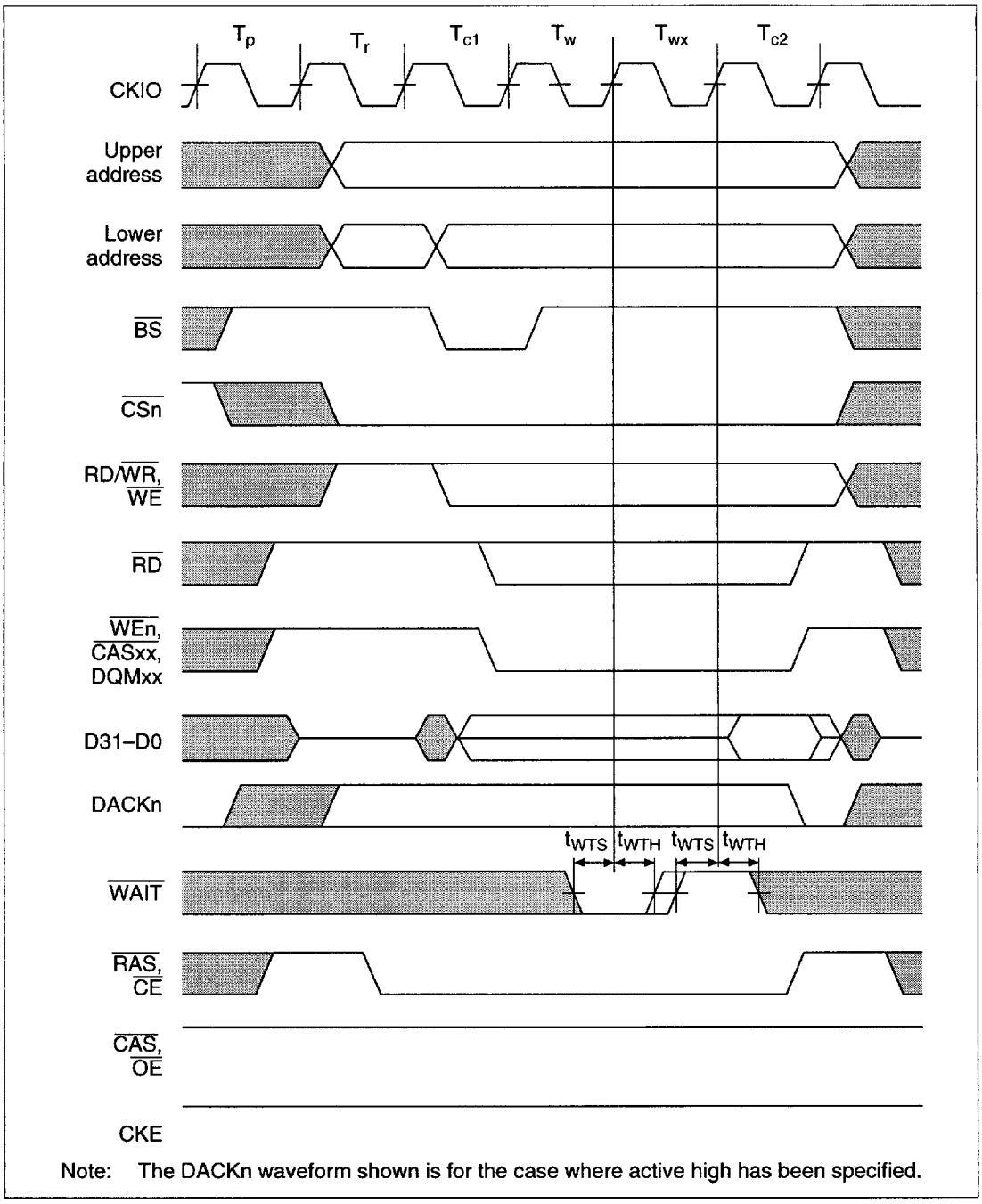


Figure 15.42 DRAM Bus Cycle (TRP = 2 Cycles, RCD = 2 Cycles, 1 Wait)

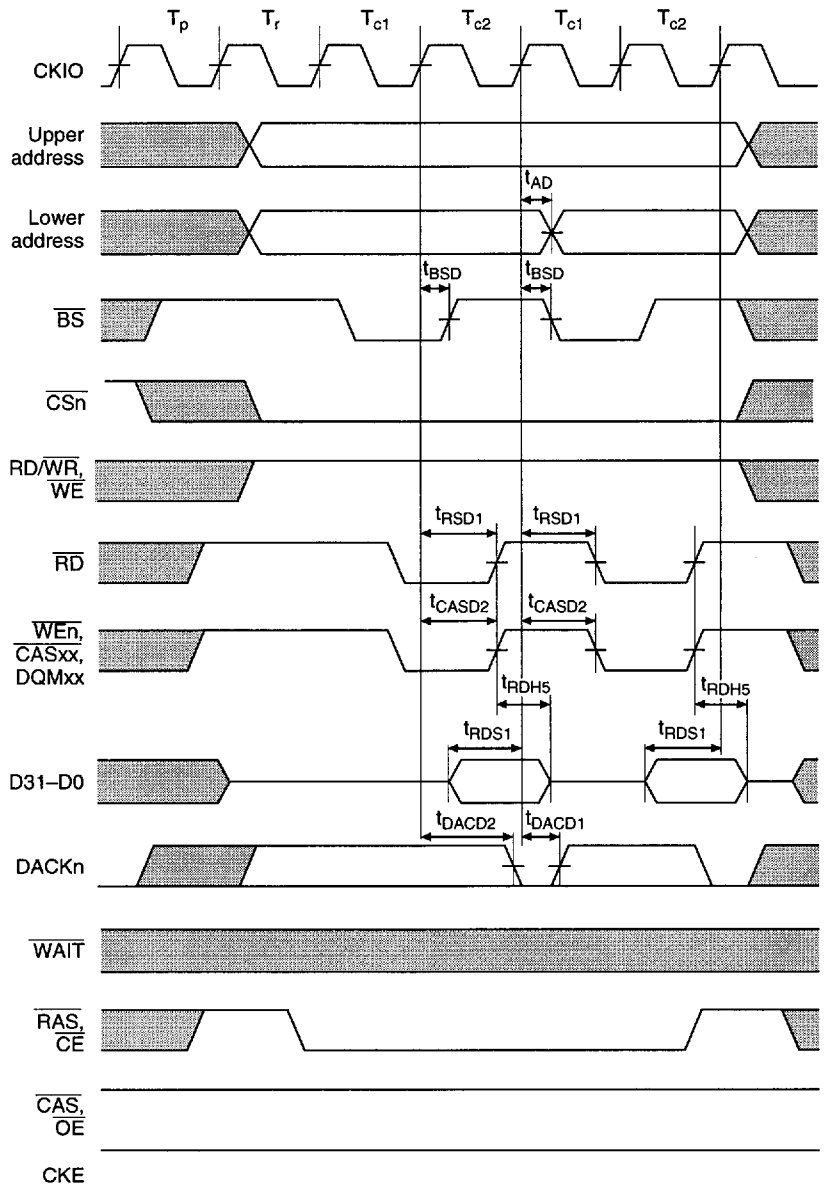
4496204 0054389 871



Note: The DACKn waveform shown is for the case where active high has been specified.

Figure 15.43 DRAM Bus Cycle (TRP = 1 Cycle, RCD = 1 Cycle, External Wait Input)

4496204 0054390 593



Notes: 1. t_{RDH5} is defined by the faster of $\overline{RD}$ and $\overline{CASxx}$ rise.
2. The DACKn waveform shown is for the case where active high has been specified.

Figure 15.44 DRAM Burst Read Cycle (TRP = 1 Cycle, RCD = 1 Cycle, No Waits, PLL On)

4496204 0054391 42T

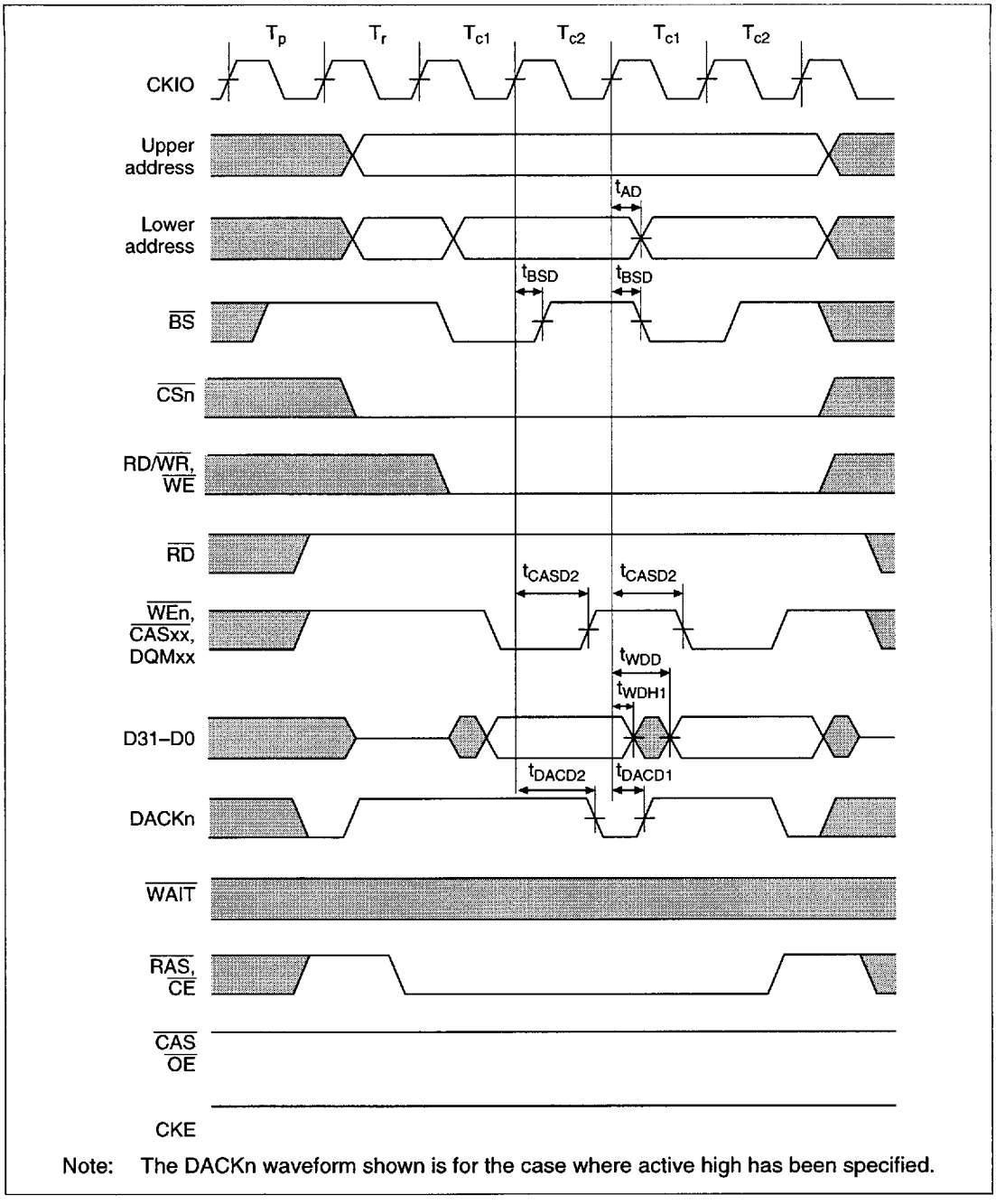


Figure 15.45 DRAM Burst Write Cycle (TRP = 1 Cycle, RCD = 1 Cycle, No Waits, PLL On)

4496204 0054392 366

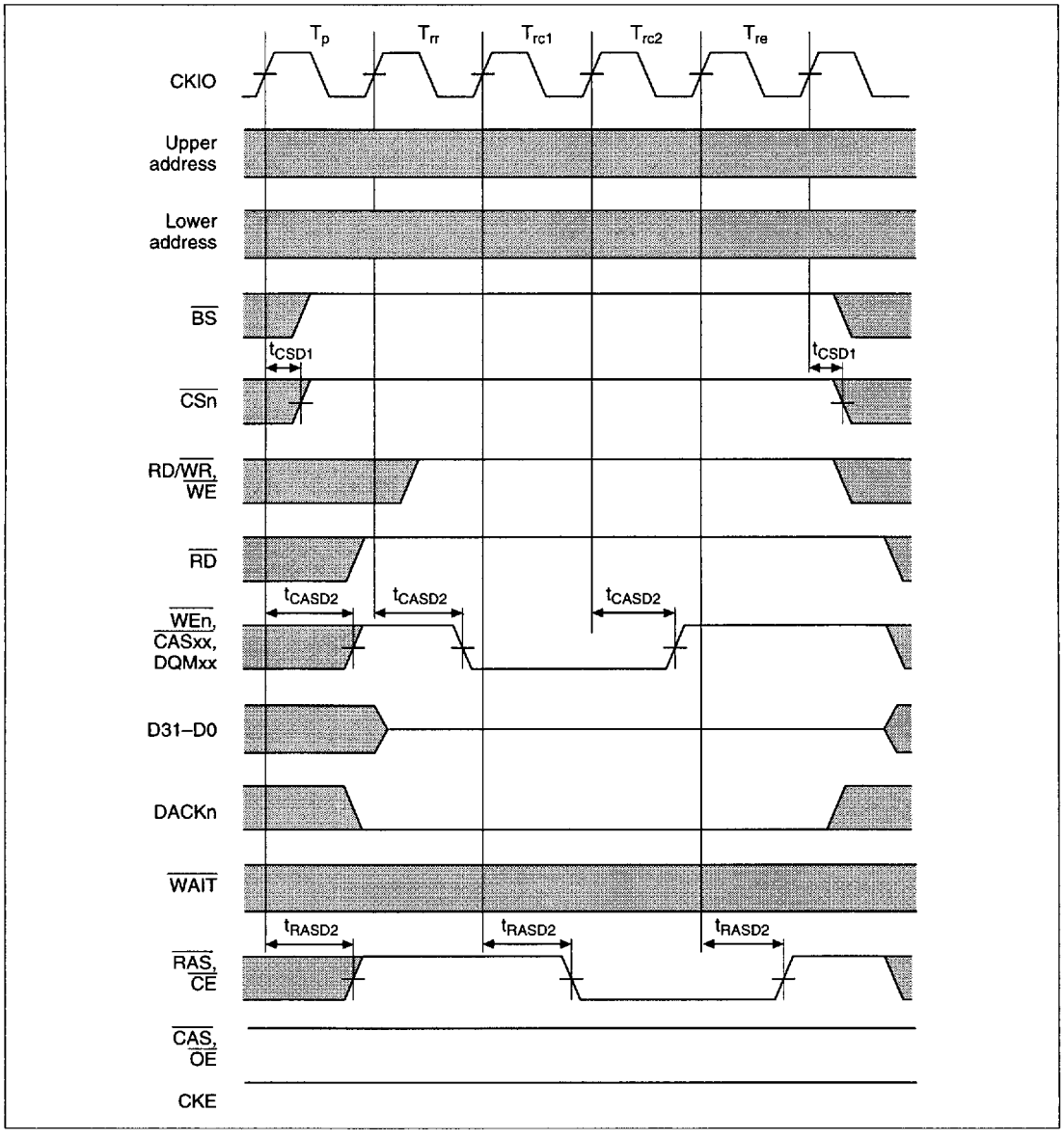
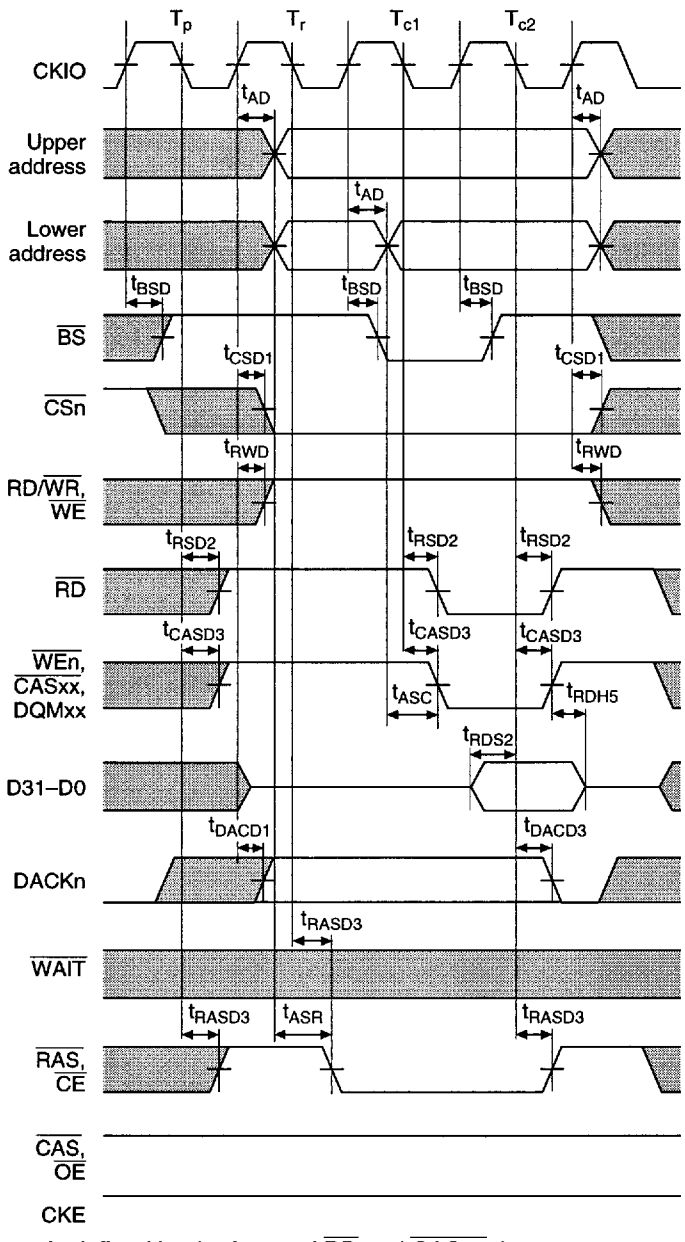


Figure 15.46 DRAM CAS-Before-RAS Refresh Cycle (TRP = 1 Cycle, TRAS = 2 Cycles, PLL On)

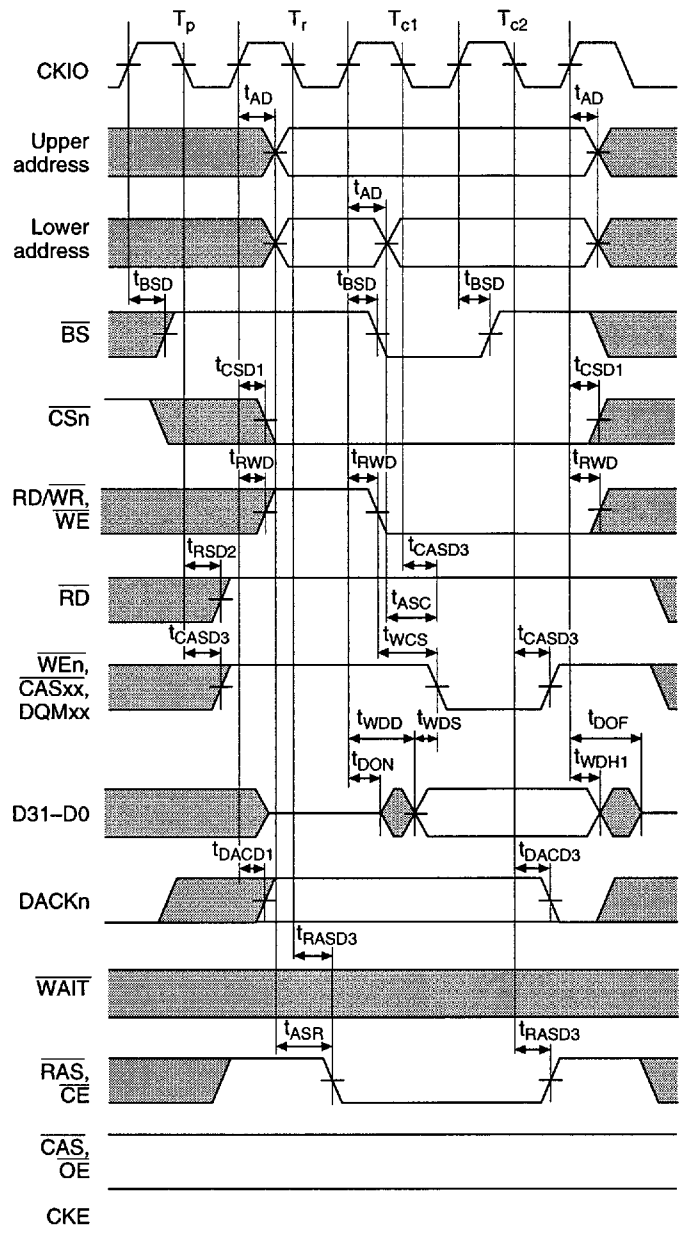
4496204 0054393 2T2



Notes: 1. t_{RDH5} is defined by the faster of $\overline{RD}$ and $\overline{CASxx}$ rise.
2. The DACKn waveform shown is for the case where active high has been specified.

Figure 15.47 DRAM Bus Cycle (TRP = 1 Cycle, RCD = 1 Cycle, No Waits, PLL Off)

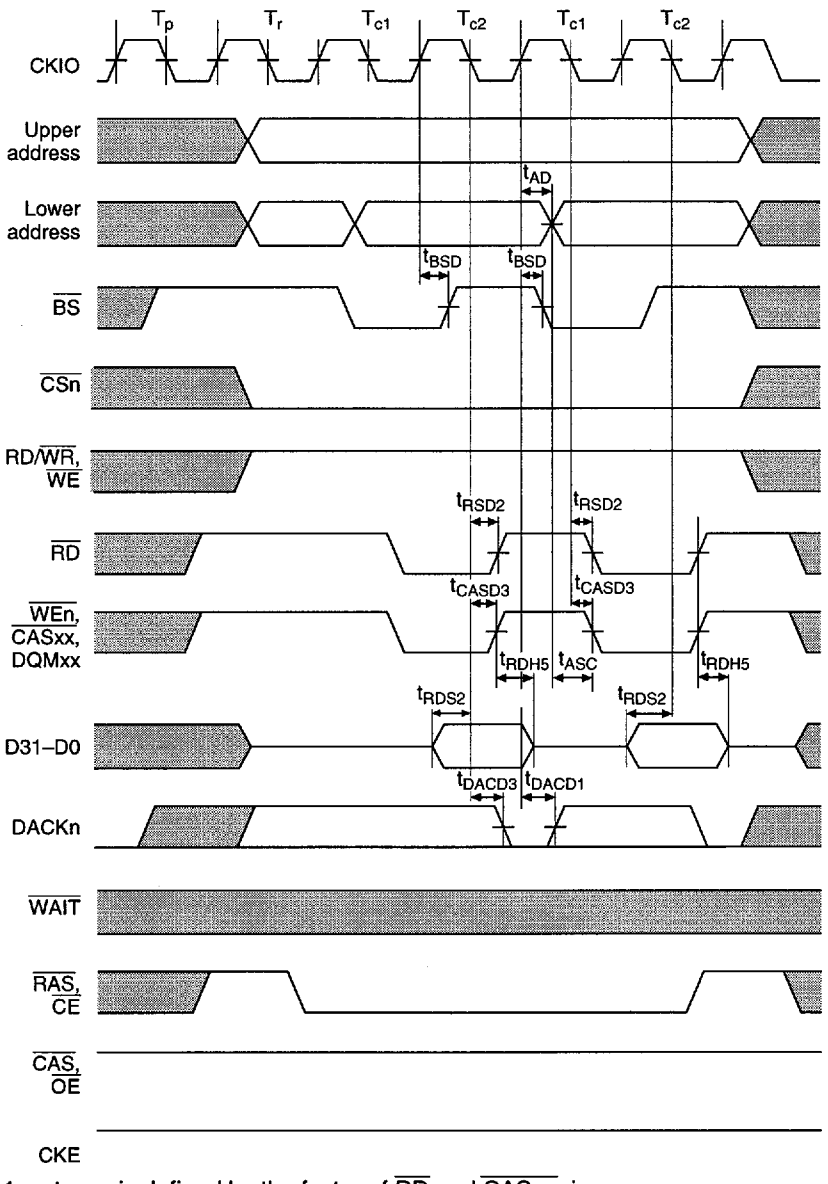
4496204 0054394 139



Note: The DACKn waveform shown is for the case where active high has been specified.

Figure 15.48 DRAM Write Cycle (TRP = 1 Cycle, RCD = 1 Cycle, No Waits, PLL Off)

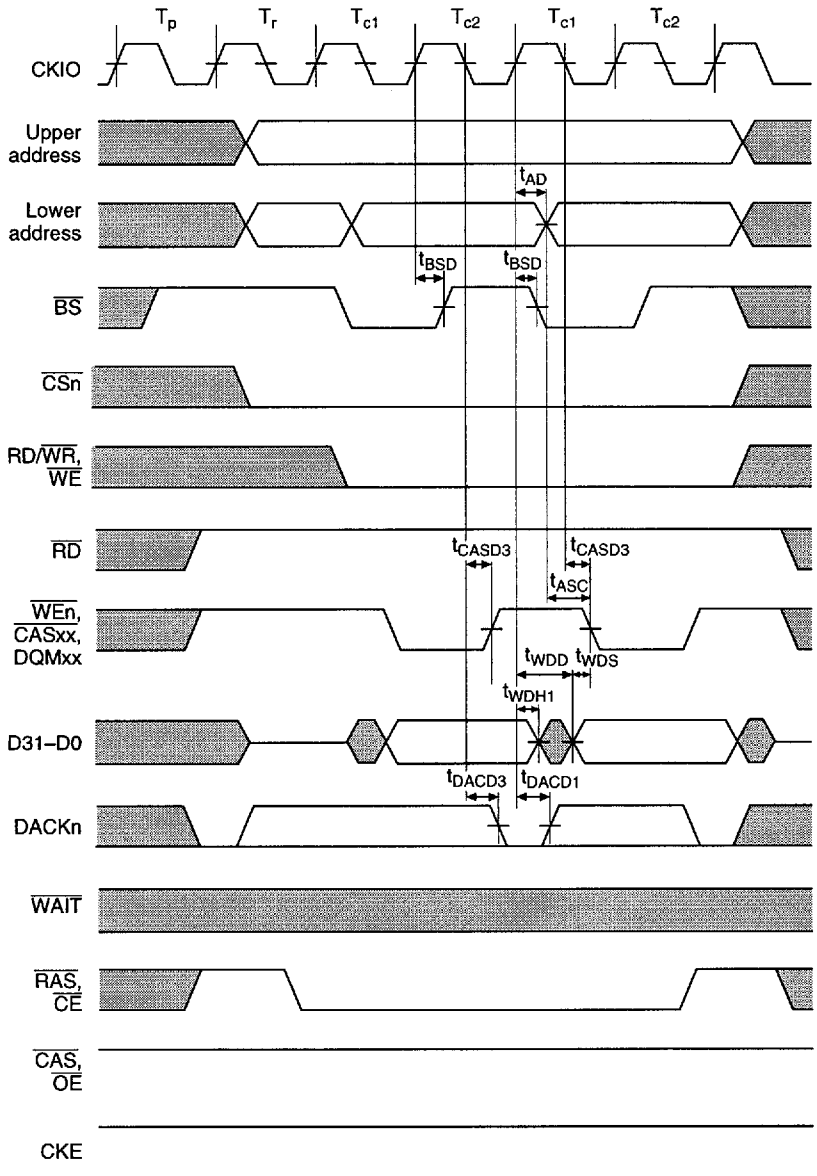
4496204 0054395 075



Notes: 1. t_{RDH5} is defined by the faster of $\overline{RD}$ and $\overline{CASxx}$ rise.
2. The DACKn waveform shown is for the case where active high has been specified.

Figure 15.49 DRAM Burst Read Cycle (TRP = 1 Cycle, RCD = 1 Cycle, No Waits, PLL Off)

4496204 0054396 T01



Note: The DACKn waveform shown is for the case where active high has been specified.

Figure 15.50 DRAM Burst Write Cycle (TRP = 1 Cycle, RCD = 1 Cycle, No Waits, PLL Off)

4496204 0054397 948

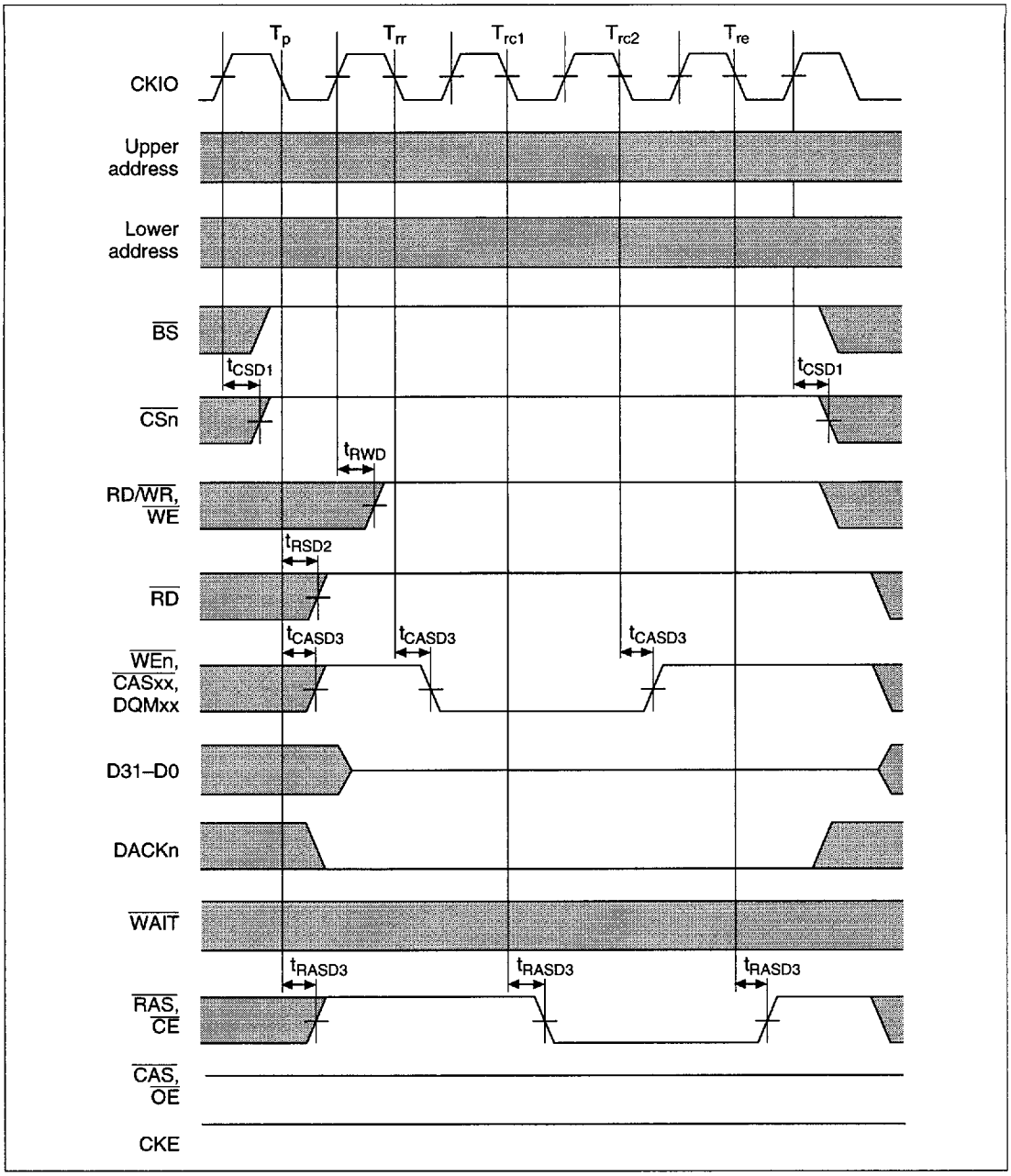
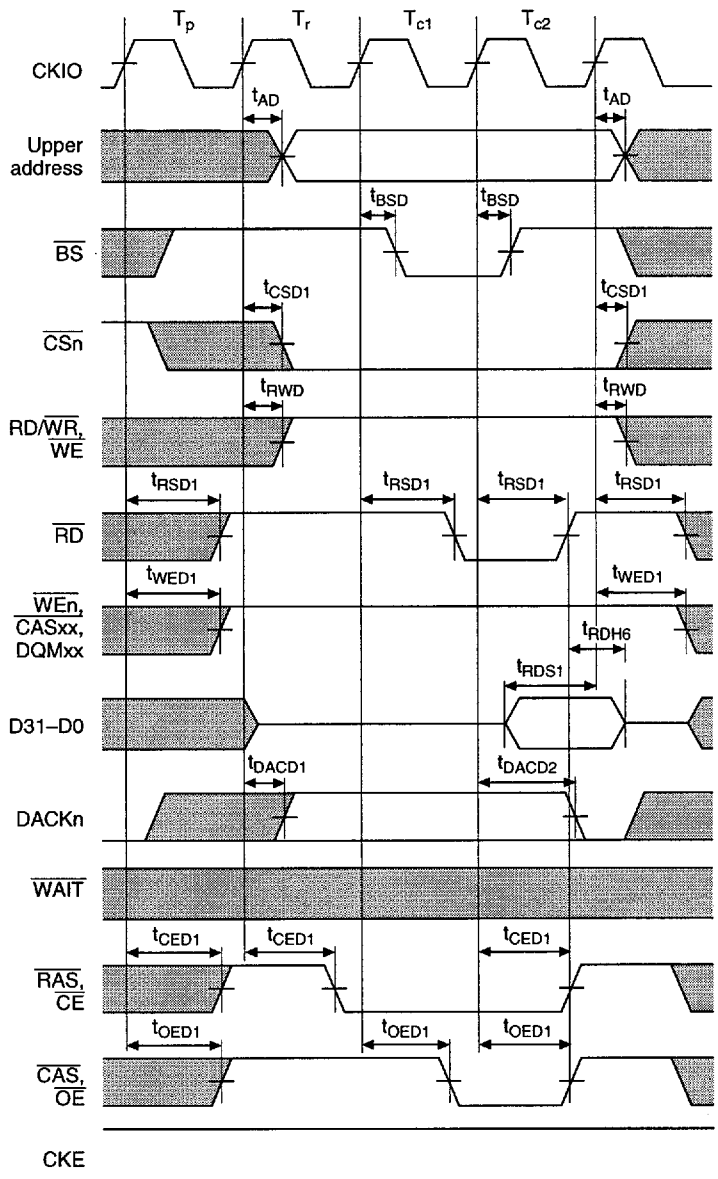


Figure 15.51 DRAM CAS-Before-RAS Refresh Cycle (TRP = 1 Cycle, TRAS = 2 Cycles, PLL Off)

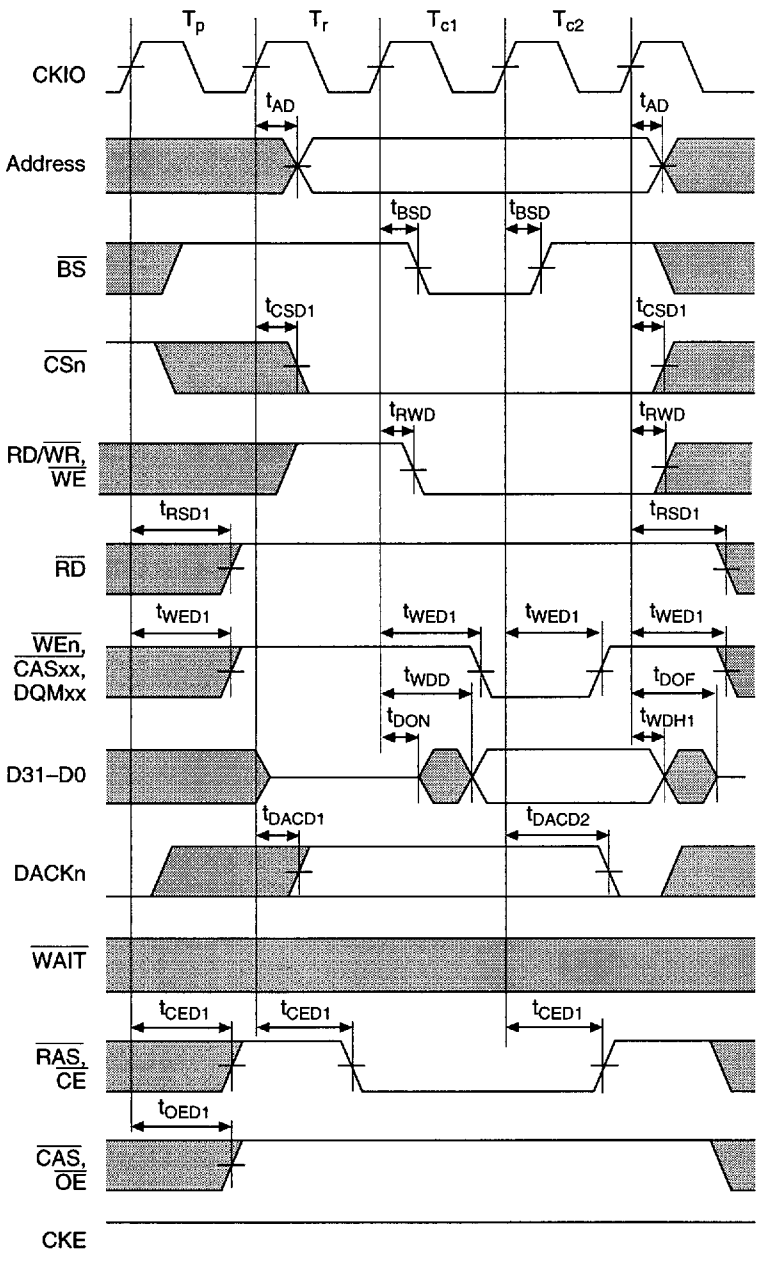
4496204 0054398 884



Note: The DACKn waveform shown is for the case where active high has been specified.

Figure 15.52 Pseudo- SRAM Read Cycle (PLL On, TRP = 1 Cycles, RCD = 1 Cycle, No Waits)

4496204 0054399 710



Note: The DACKn waveform shown is for the case where active high has been specified.

Figure 15.53 Pseudo-SRAM Write Cycle (PLL On, TRP = 1 Cycle, RCD = 1 Cycle, No Waits)

4496204 0054400 262

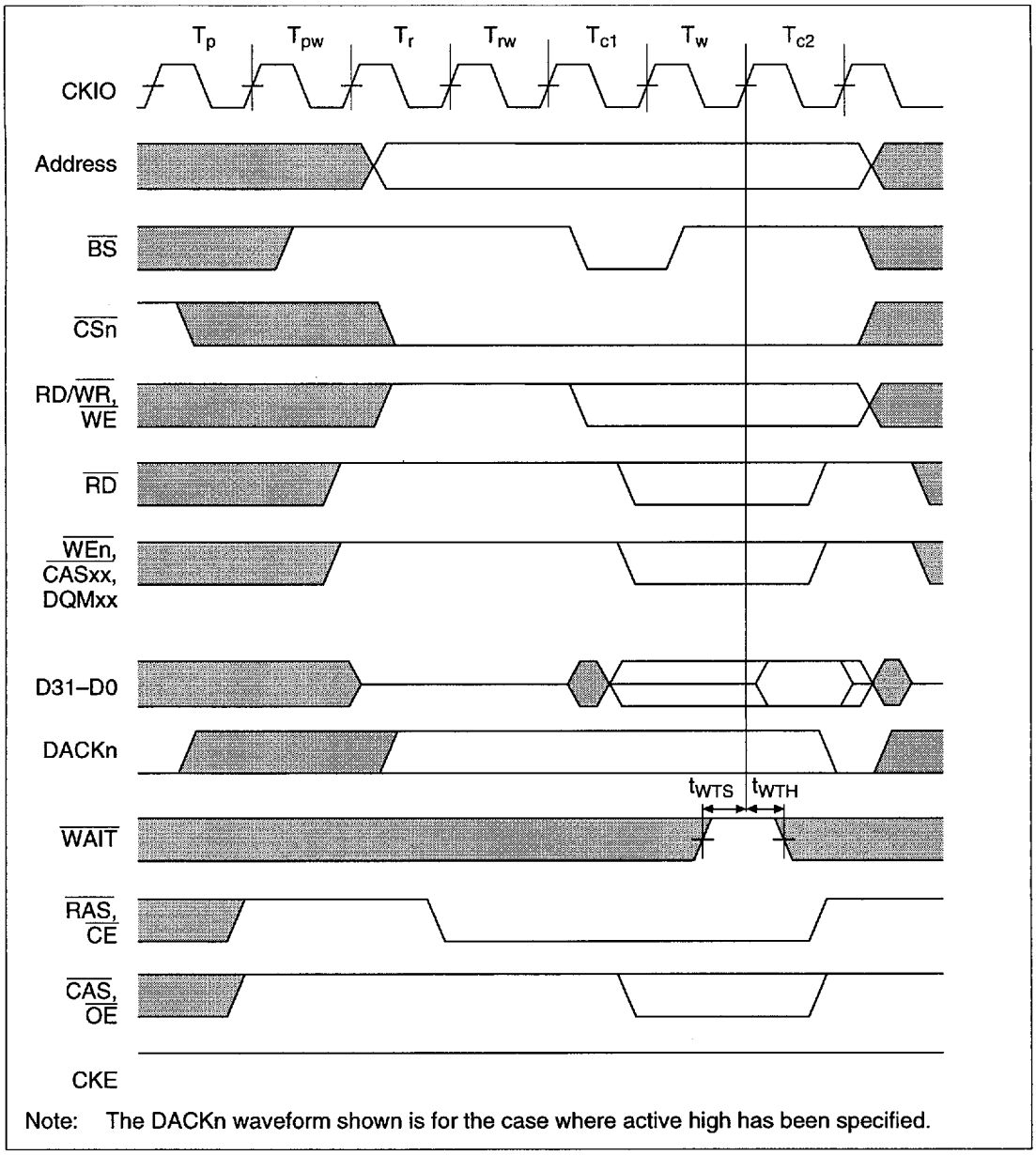
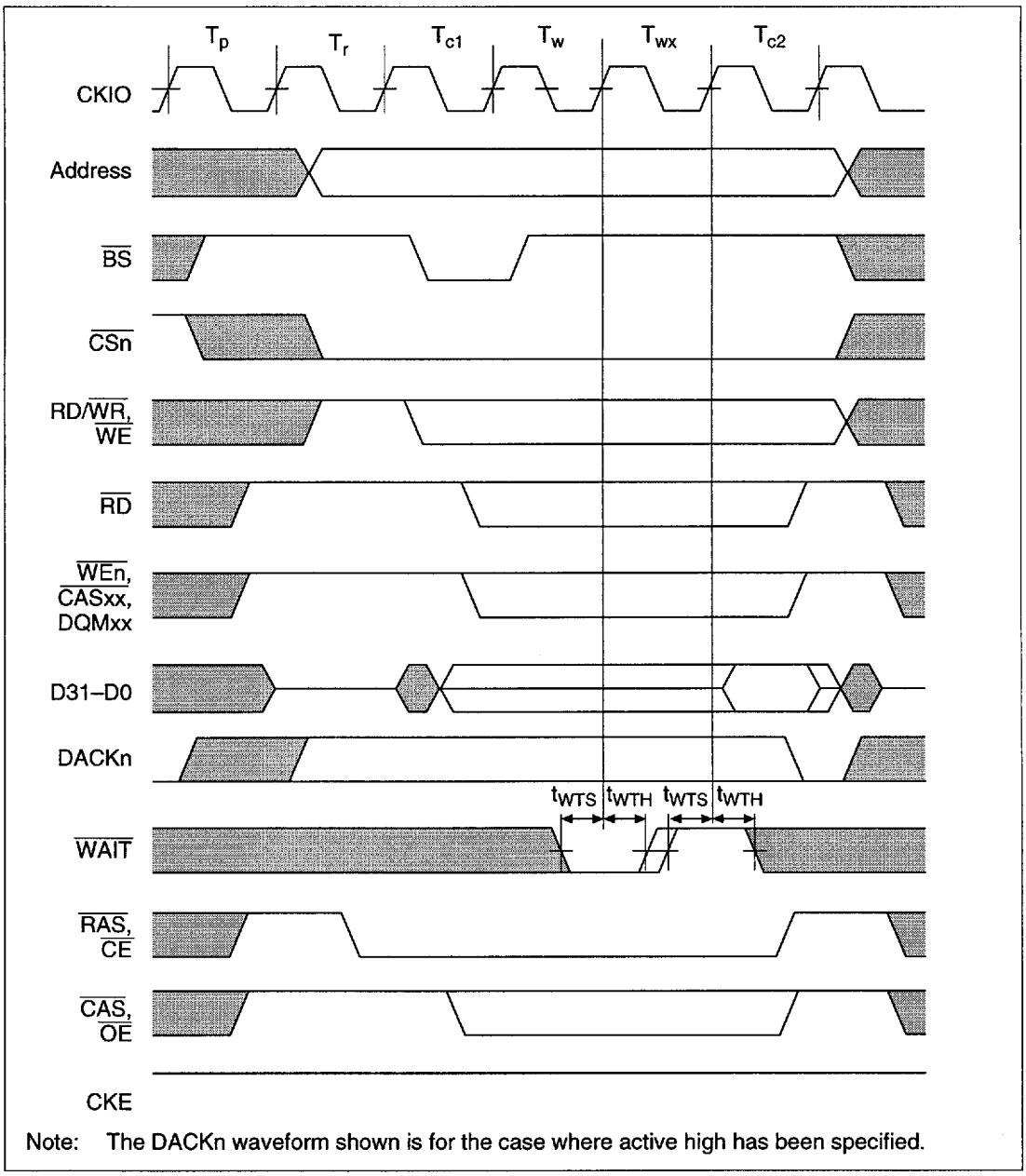


Figure 15.54 Pseudo-SRAM Bus Cycle (TRP = 2 Cycles, RCD = 2 Cycles, 1 Wait)

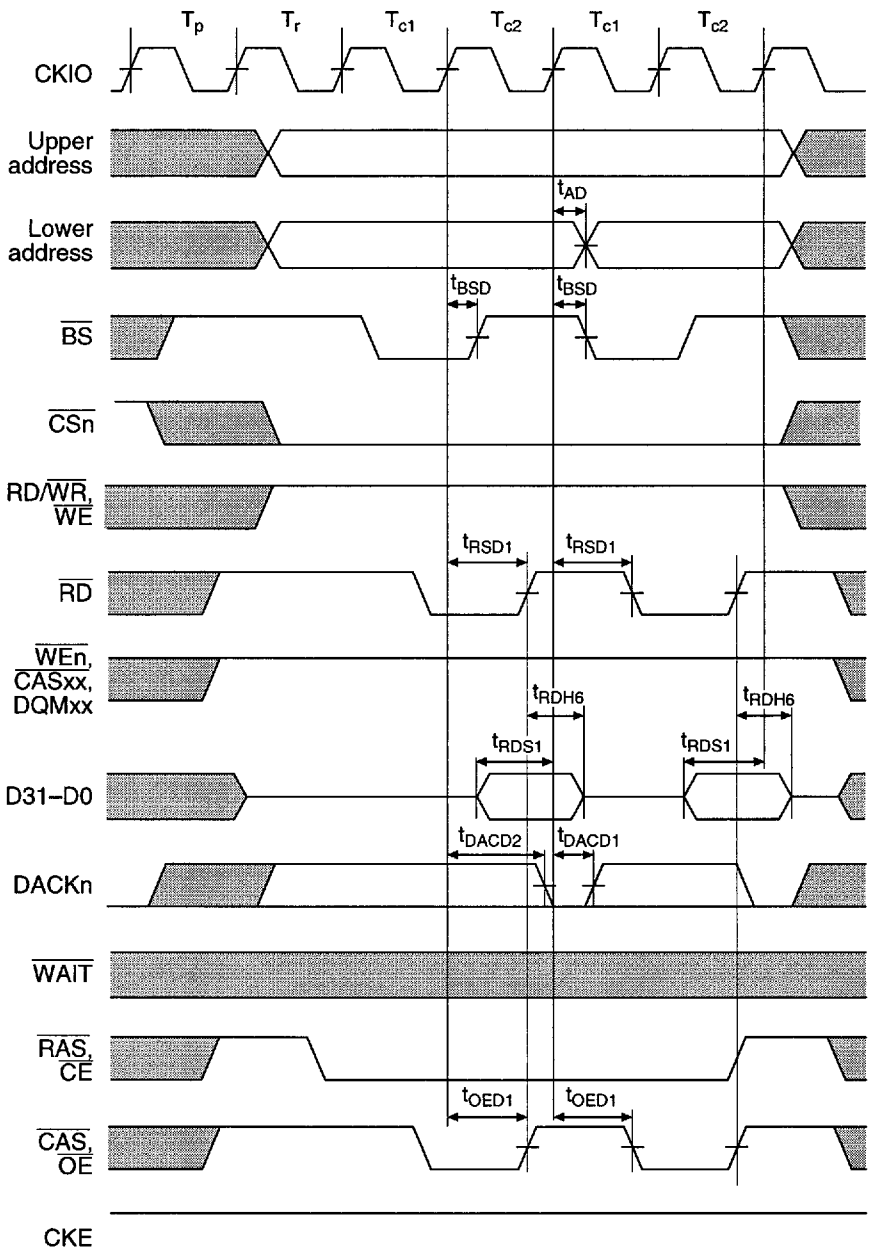
4496204 0054401 1T9



Note: The DACKn waveform shown is for the case where active high has been specified.

Figure 15.55 Pseudo-SRAM Bus Cycle (TRP = 1 Cycle, RCD = 1 Cycle, External Wait Input)

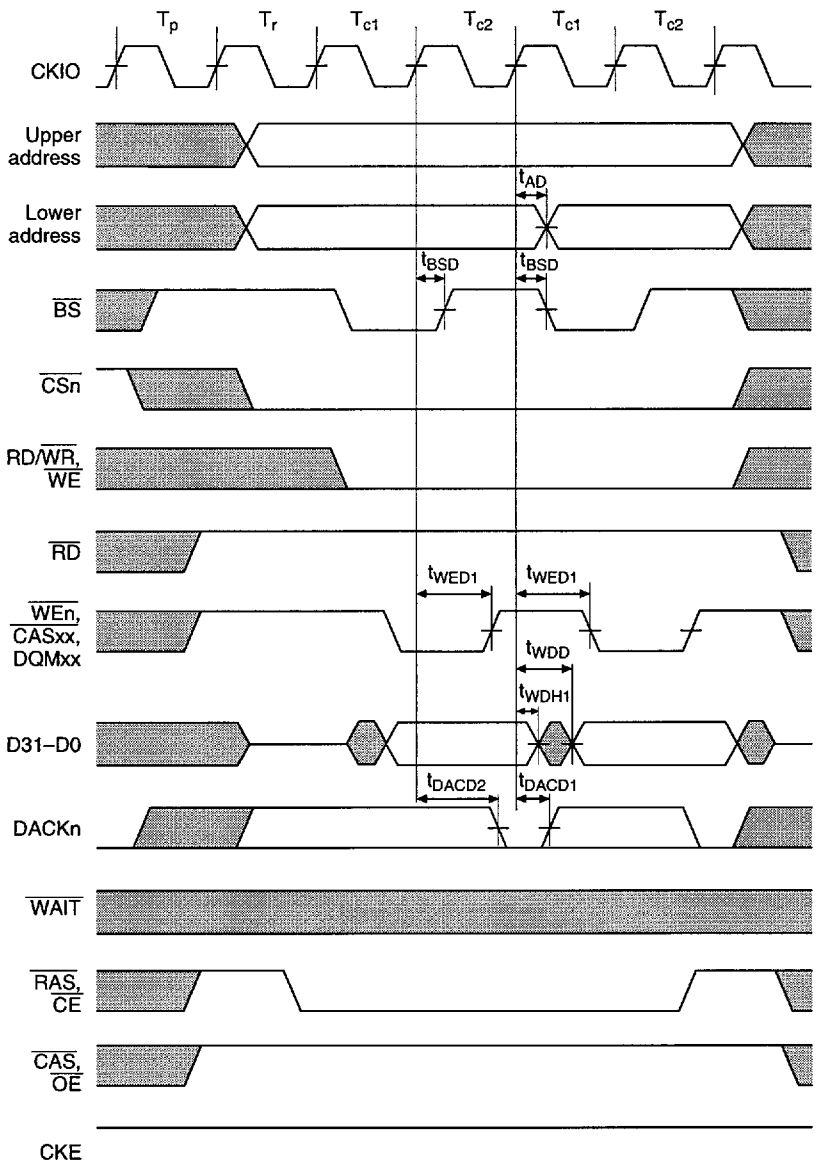
4496204 0054402 035



Note: The DACKn waveform shown is for the case where active high has been specified.

Figure 15.56 Pseudo-SRAM Read Cycle (Static Column Mode, PLL On, TRP = 1 Cycle, No Waits)

4496204 0054403 T71



Note: The DACKn waveform shown is for the case where active high has been specified.

Figure 15.57 Pseudo-SRAM Write Cycle (Static Column Mode, PLL On, TRP = 1 Cycle, RCD = 1 Cycle, No Waits)

4496204 0054404 908

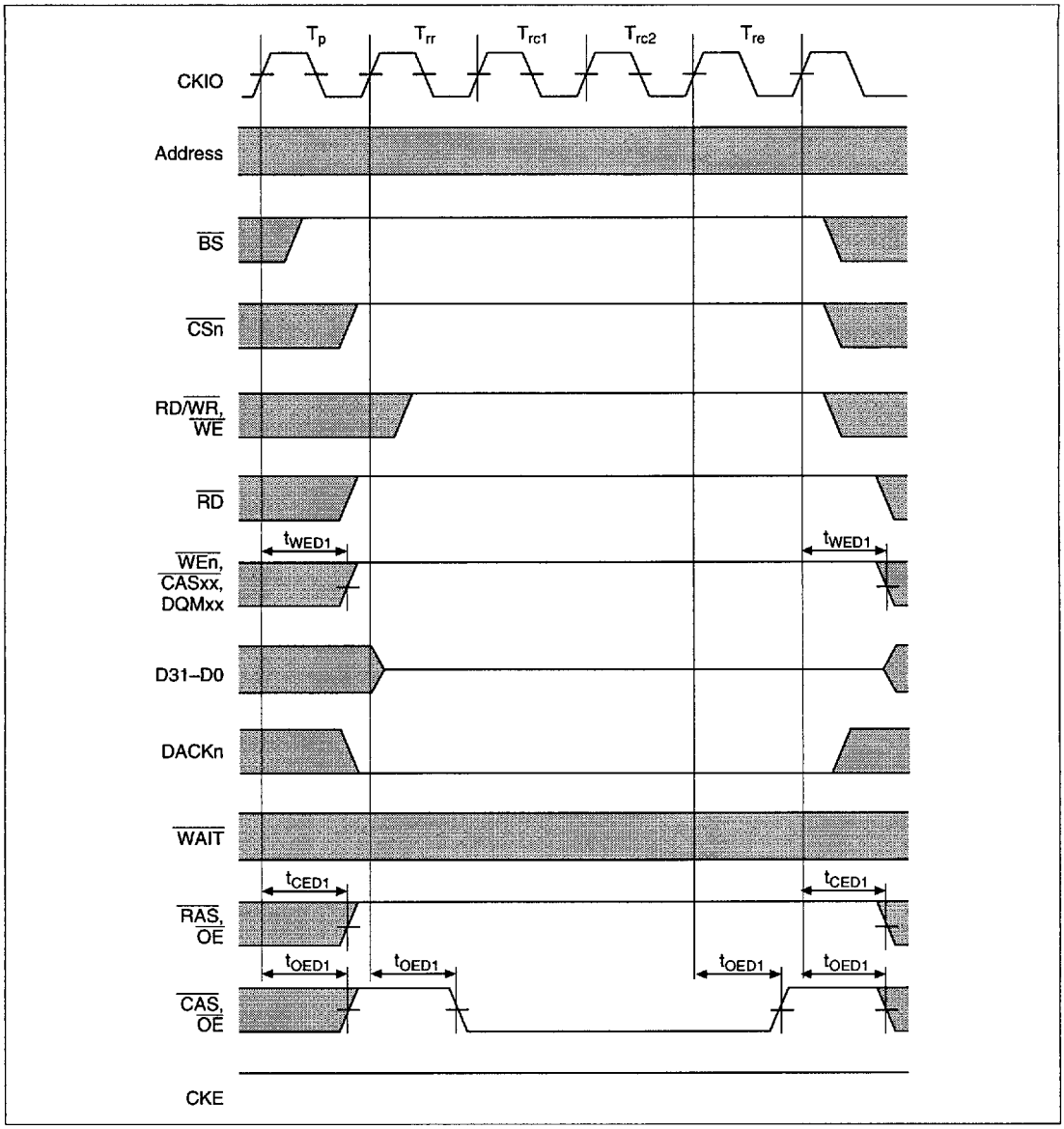


Figure 15.58 Pseudo-SRAM Auto-Refresh Cycle (PLL On, TRP = 1 Cycle, TRAS = 2 Cycles)

4496204 0054405 844

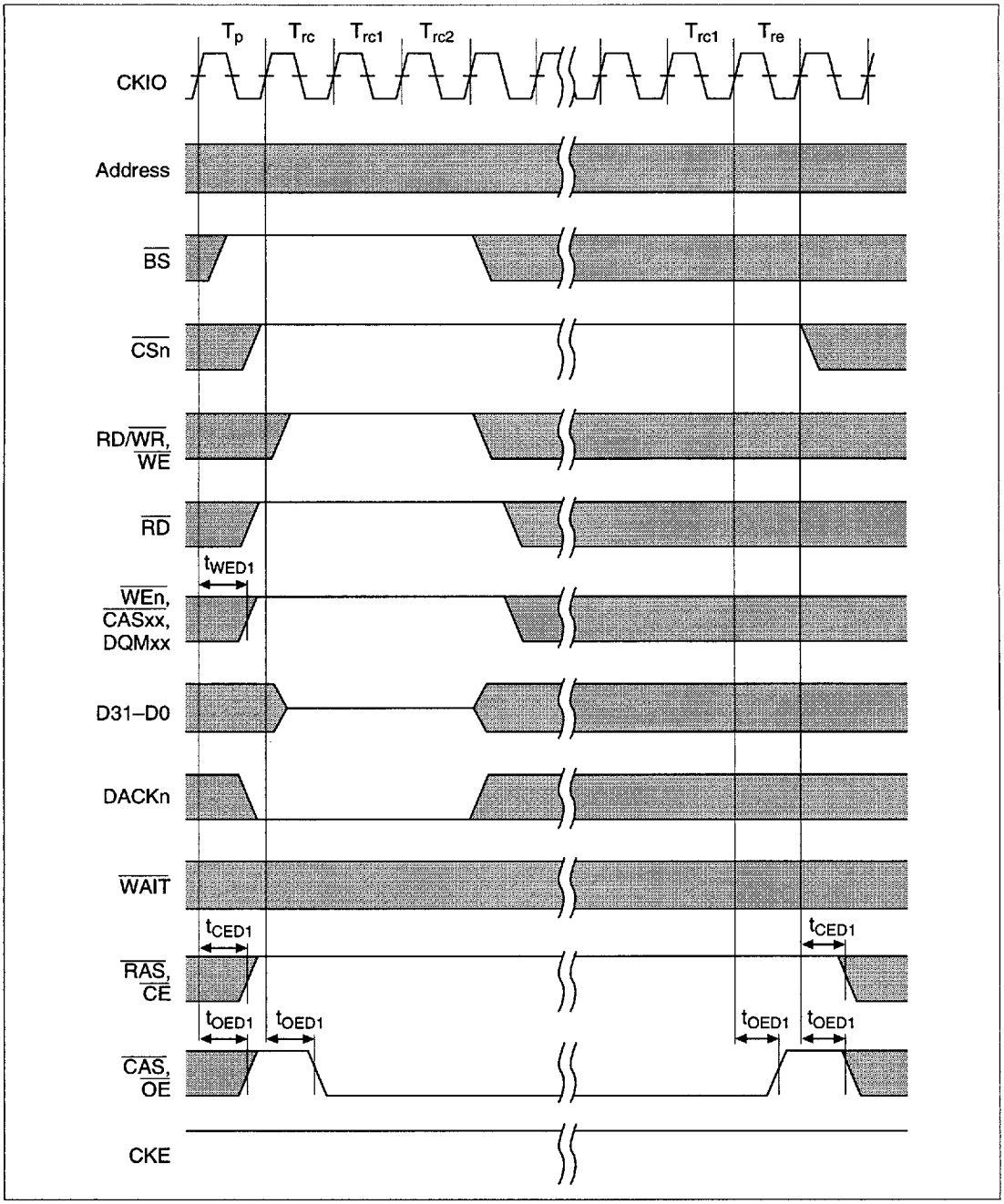
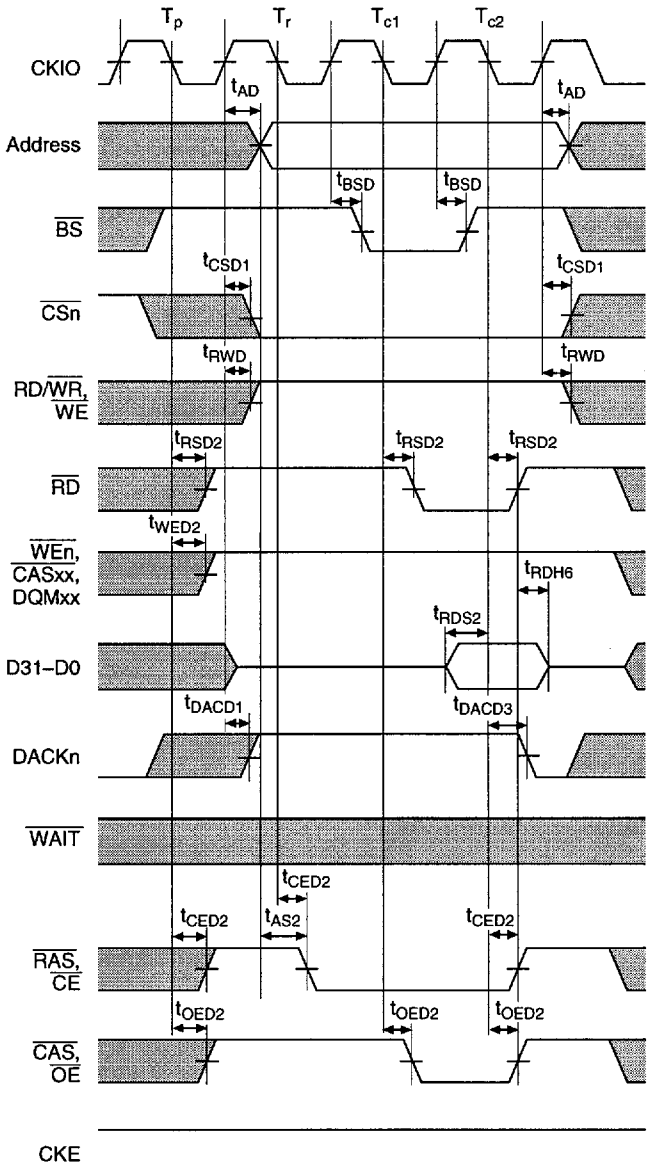


Figure 15.59 Pseudo-SRAM Self-Refresh Cycle (PLL On, TRP = 1 Cycle, TRAS = 2 Cycles)

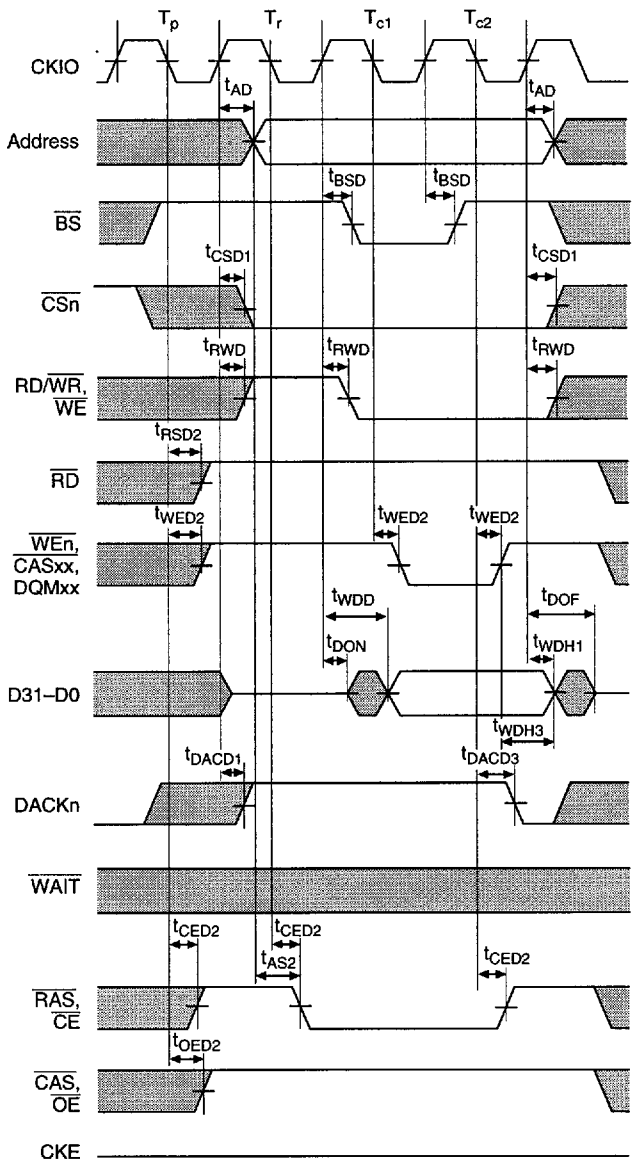
4496204 0054406 780



Note: The DACKn waveform shown is for the case where active high has been specified.

Figure 15.60 Pseudo-SRAM Read Cycle (PLL Off, TRP = 1 Cycle, RCD = 1 Cycle, No Waits)

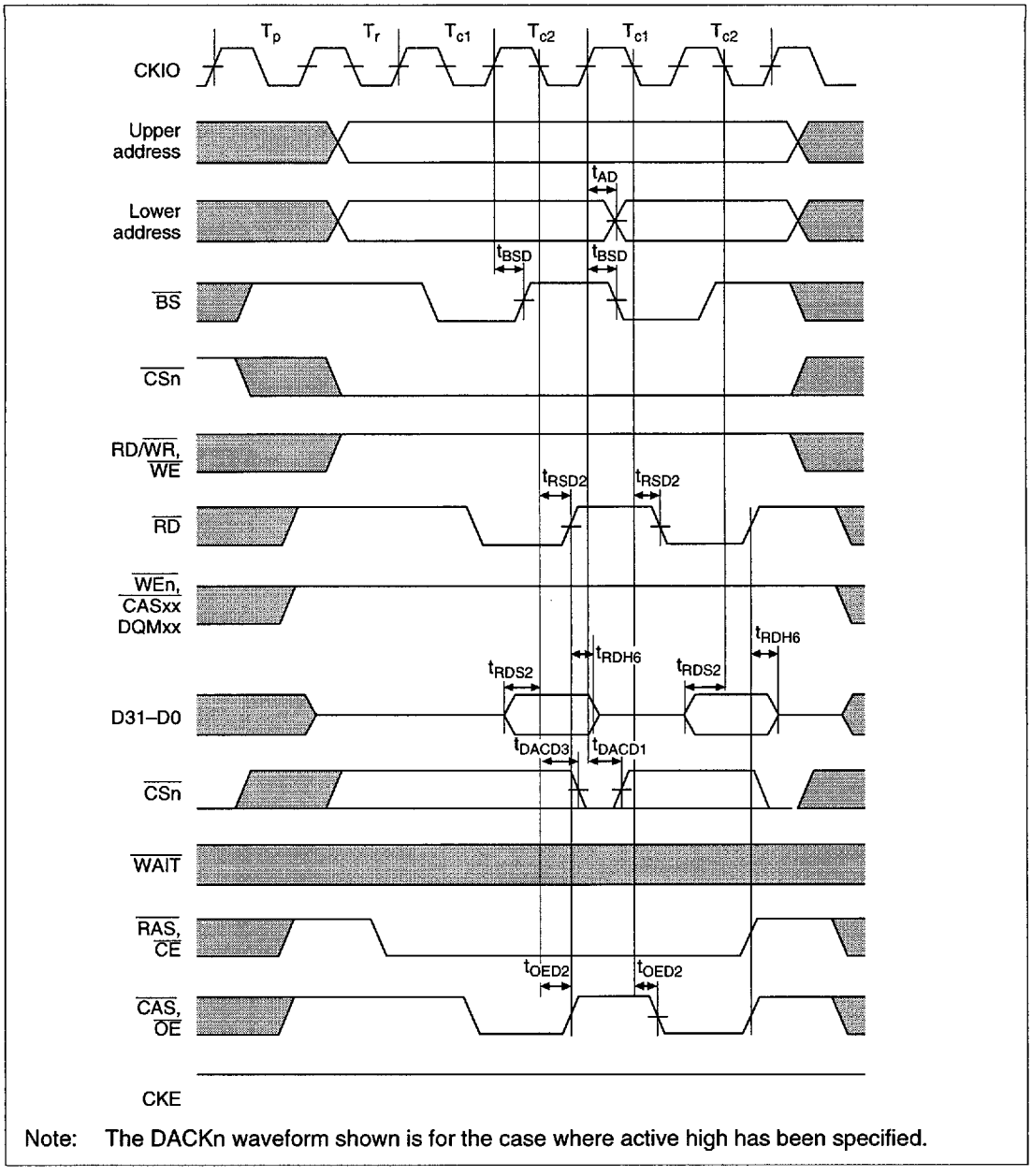
4496204 0054407 617



Note: The DACKn waveform shown is for the case where active high has been specified.

Figure 15.61 Pseudo-SRAM Write Cycle (PLL Off, TRP = 1 Cycle, RCD = 1 Cycle, No Waits)

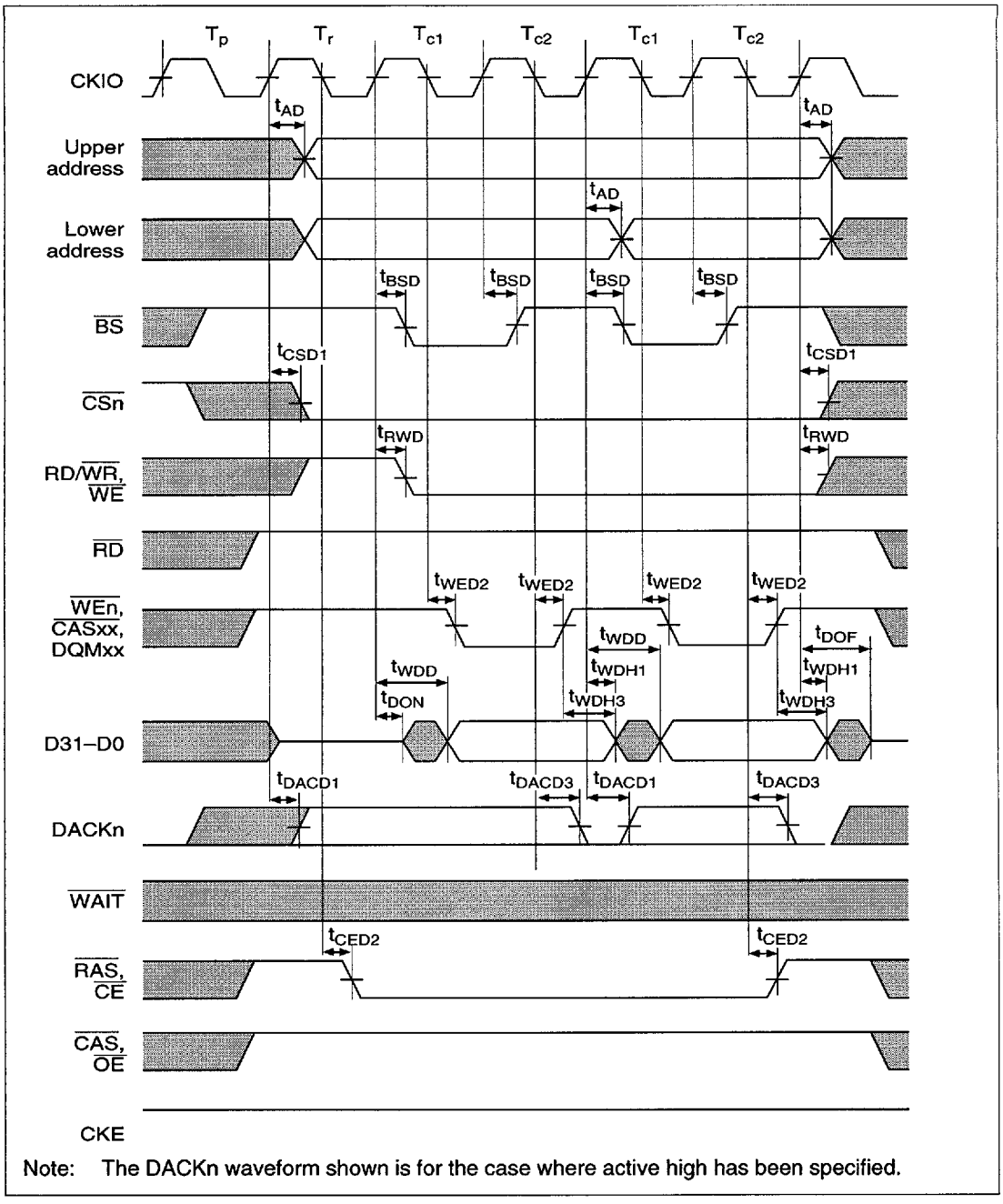
4496204 0054408 553



Note: The DACKn waveform shown is for the case where active high has been specified.

Figure 15.62 Pseudo-SRAM Read Cycle (Static Column Mode, PLL Off, TRP = 1 Cycle, RCD = 1 Cycle, No Waits)

4496204 0054409 49T



Note: The DACKn waveform shown is for the case where active high has been specified.

Figure 15.63 Pseudo-SRAM Write Cycle (Static Column Mode, PLL Off, TRP = 1 Cycle, RCD = 1 Cycle, No Waits)

4496204 0054410 101

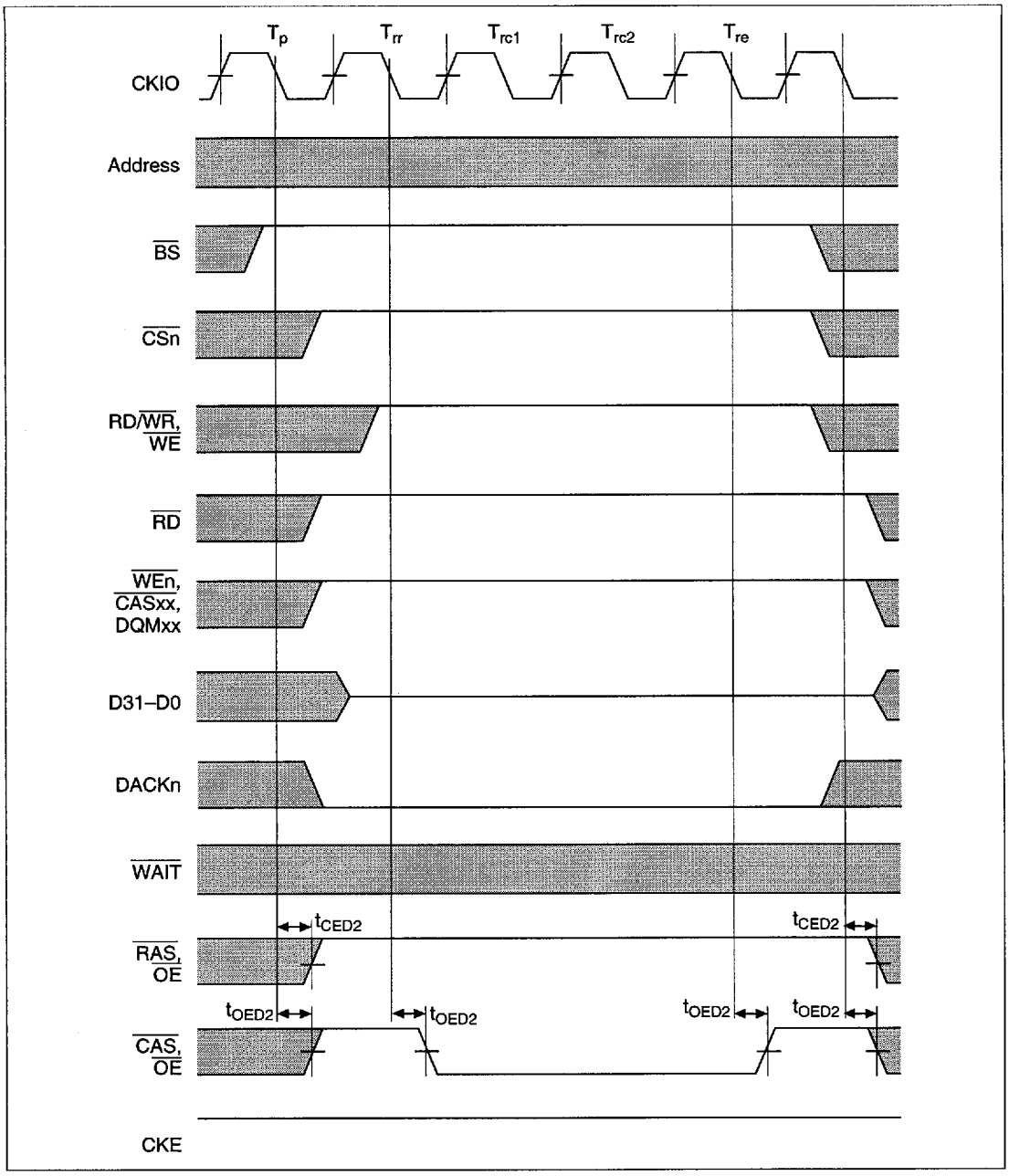


Figure 15.64 Pseudo-SRAM Auto-Refresh Cycle (PLL Off, TRP = 1 Cycle, TRAS = 2 Cycles)

4496204 0054411 048

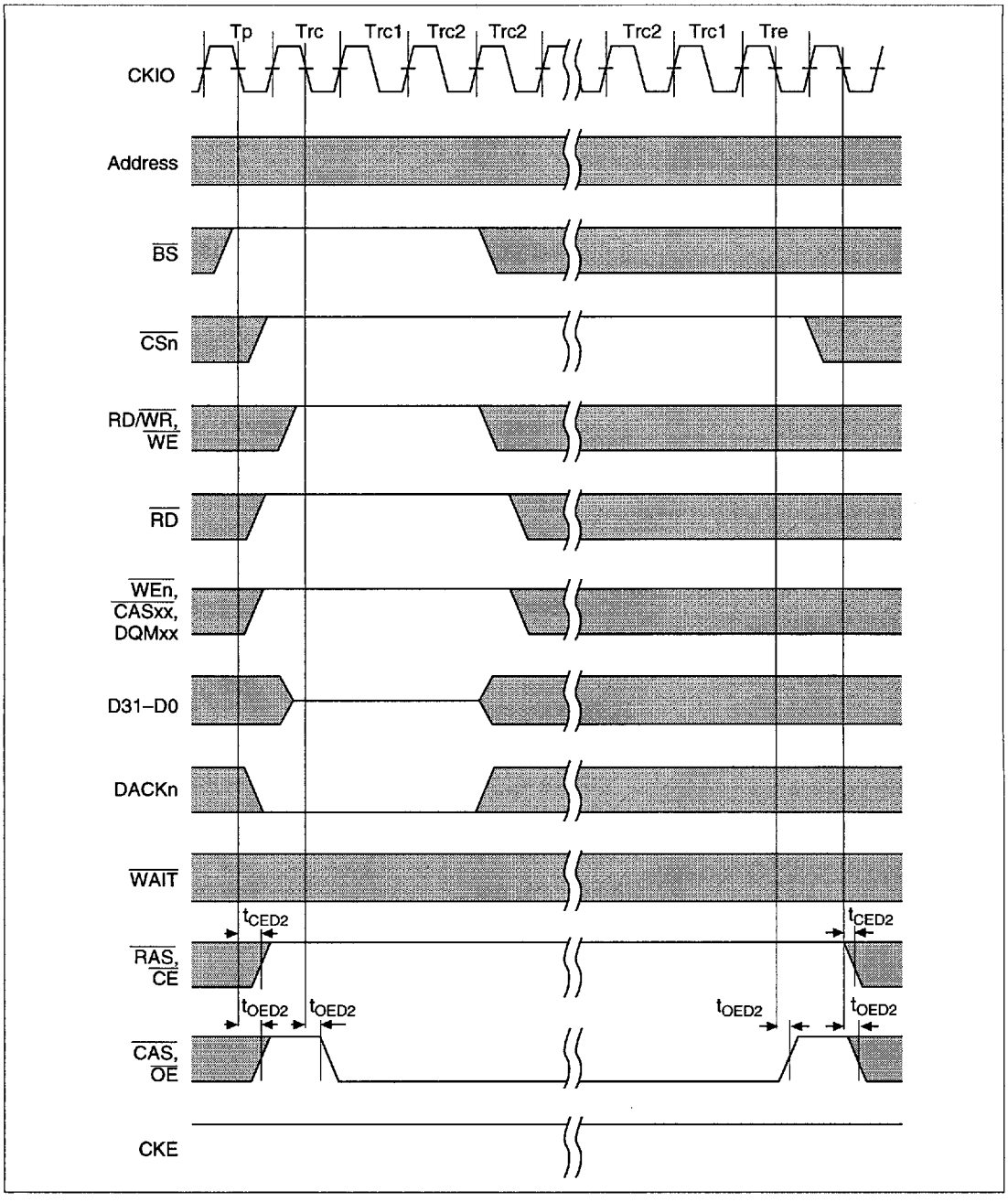
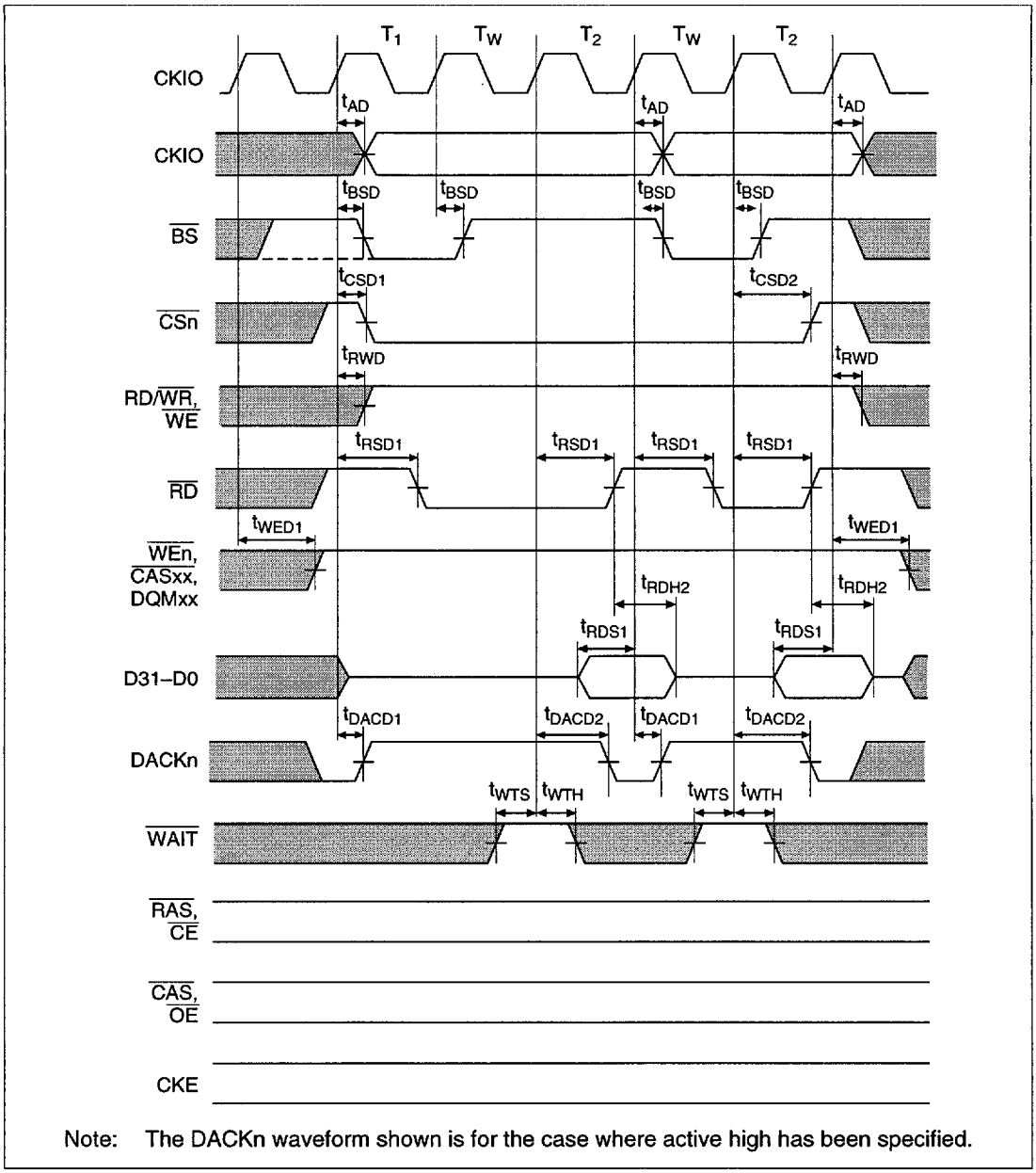


Figure 15.65 Pseudo-SRAM Self-Refresh Cycle (PLL Off, TRP = 1 Cycle, TRAS = 2 Cycles)

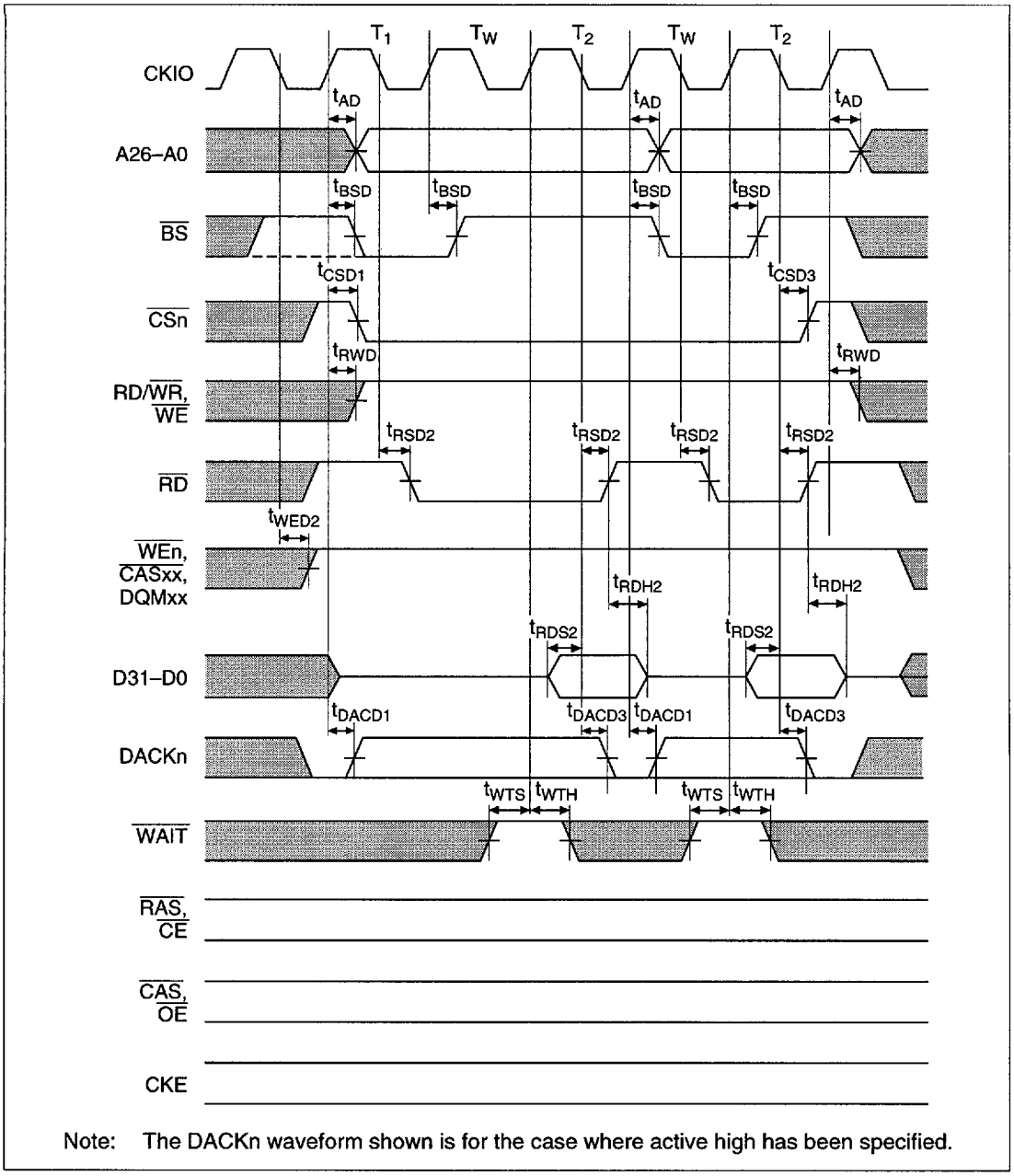
4496204 0054412 T84



Note: The DACKn waveform shown is for the case where active high has been specified.

Figure 15.66 Burst ROM Read Cycle (PLL On, 1 Wait)

4496204 0054413 910



Note: The DACKn waveform shown is for the case where active high has been specified.

Figure 15.67 Burst ROM Read Cycle (PLL Off, 1 Wait)

4496204 0054414 857

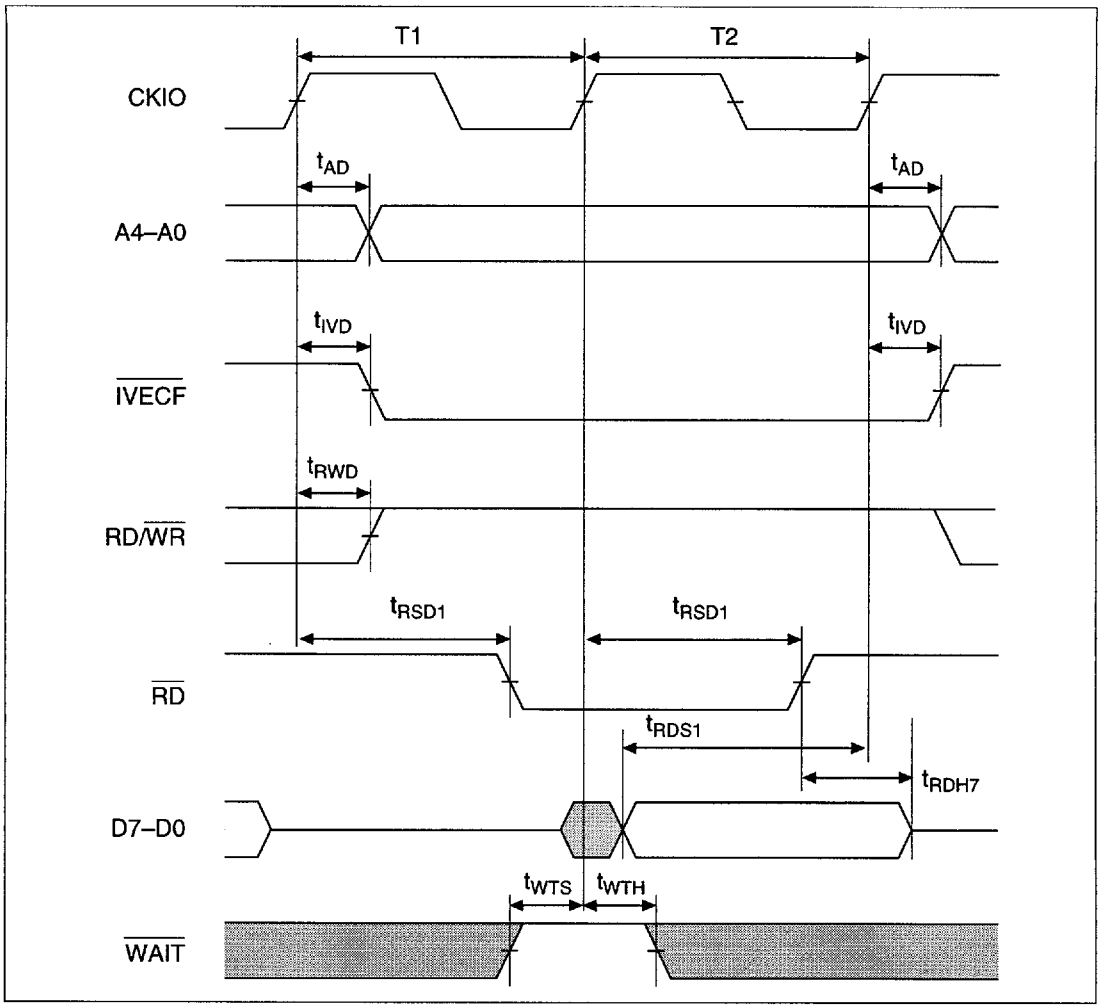


Figure 15.68 Interrupt Vector Fetch Cycle (PLL On, No Waits)

4496204 0054415 793

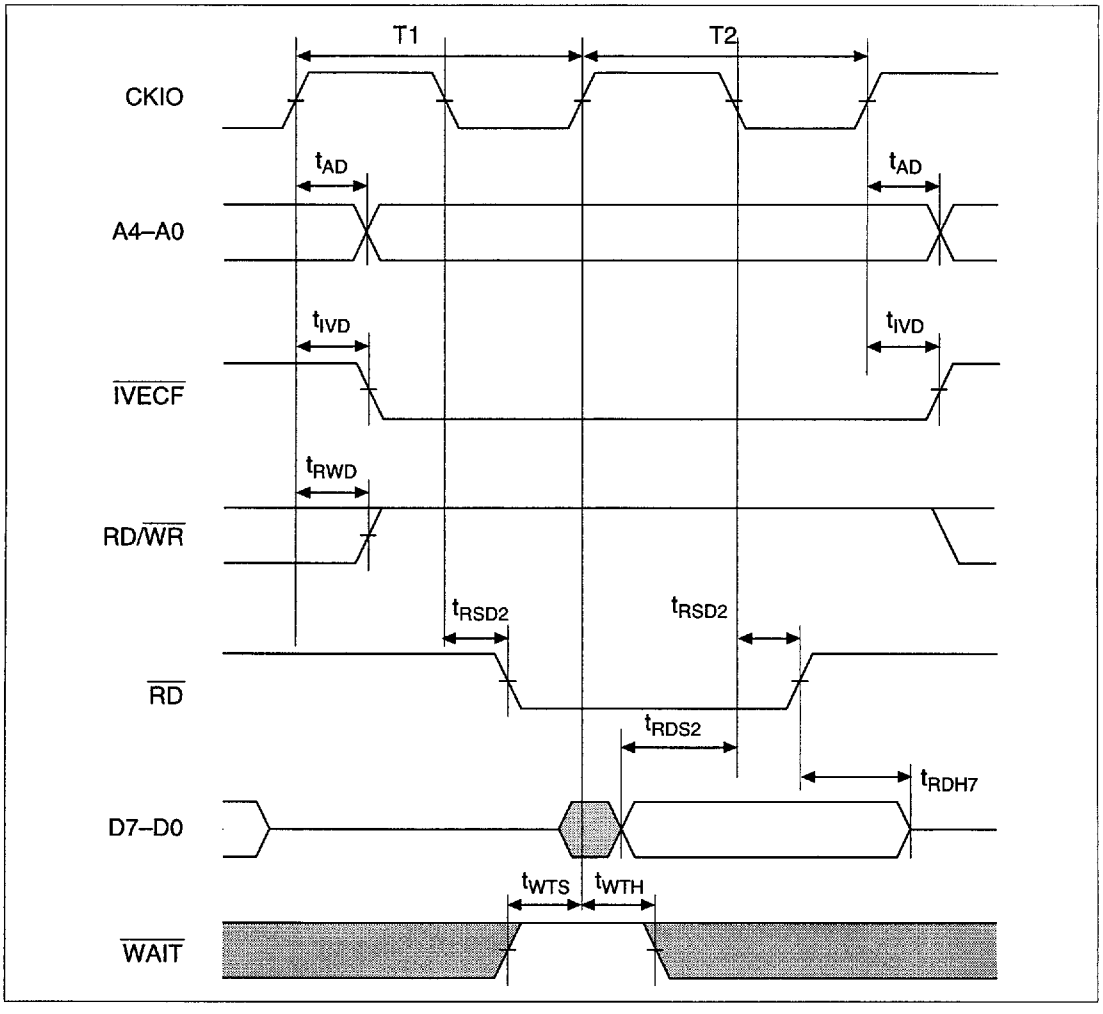


Figure 15.69 Interrupt Vector Fetch Cycle (PLL Off, No Waits)

4496204 0054416 62T

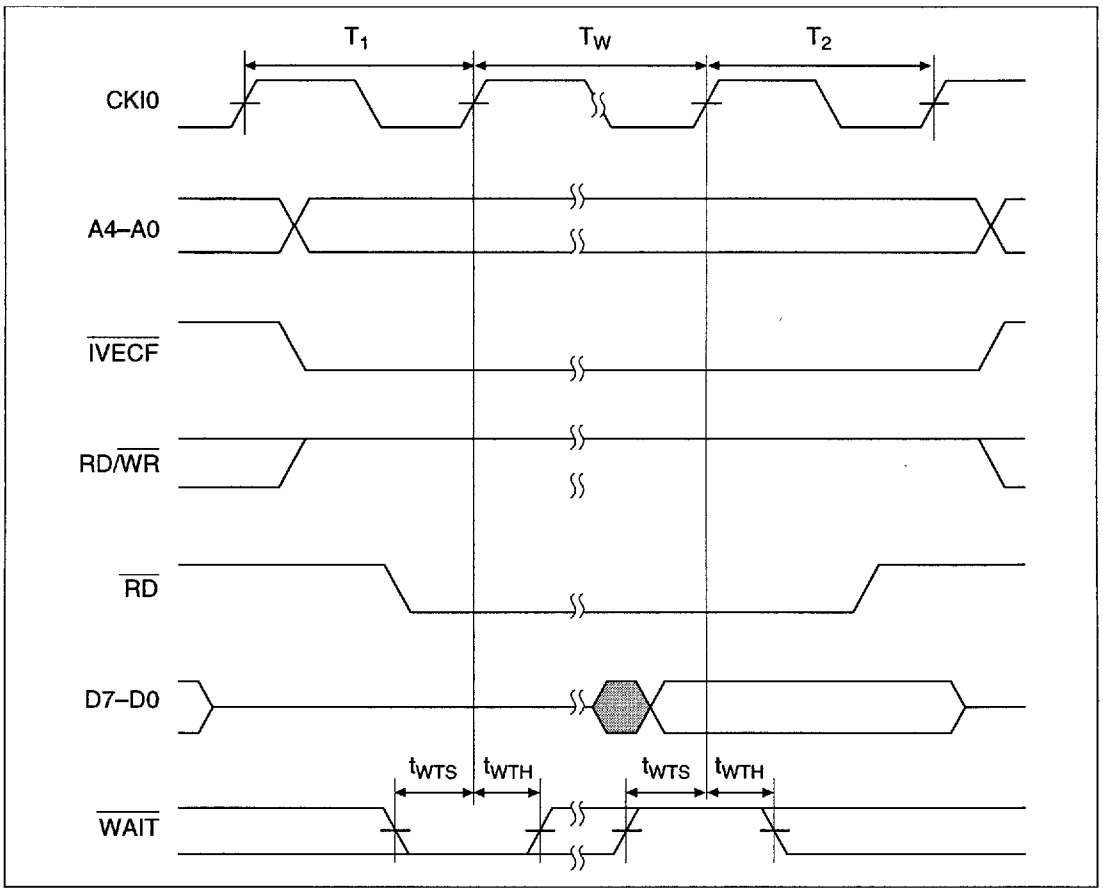


Figure 15.70 Interrupt Vector Fetch Cycle (1 External Wait Cycle)

4496204 0054417 566

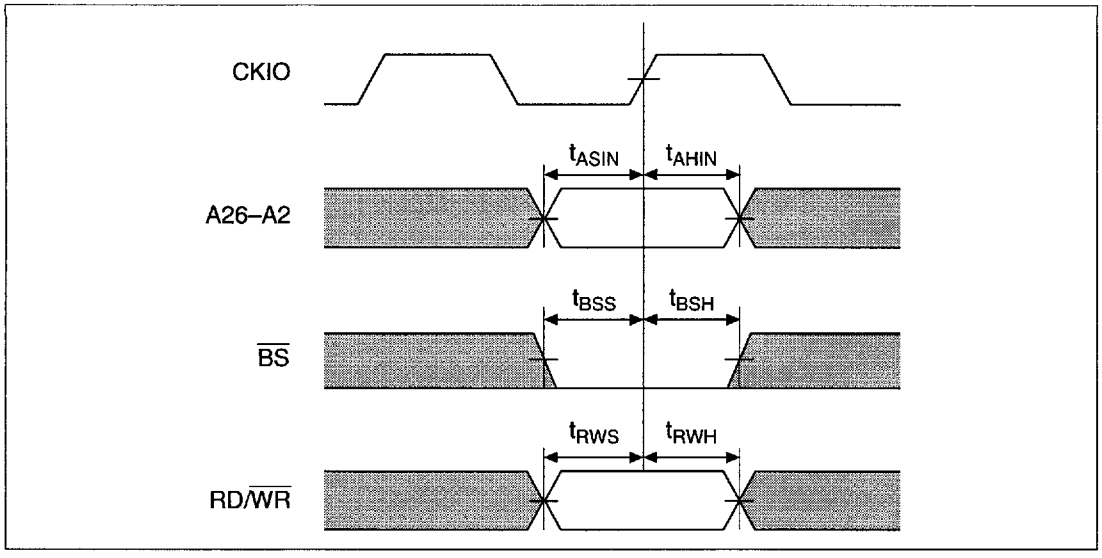


Figure 15.71 Address Monitor Cycle

15.3.4 DMAC Timing

Table 15.10 DMAC Timing (V_{CC} = 5.0 V ±10%, Ta = –20 to +75°C)

Item	Symbol	Min	Max	Unit	Figure
DREQ0, DREQ1 setup time (PLL Off, On)	t_{DRQS}	30	—	ns	15.72
DREQ0, DREQ1 setup time (PLL On, 1/4 cycle delay)	t_{DRQS}	30 – 1/4 tcyc	—	ns	
DREQ0, DREQ1 hold time (PLL Off, On)	t_{DRQH}	15	—	ns	
DREQ0, DREQ1 hold time (PLL On, 1/4 cycle delay)	t_{DRQH}	1/4 tcyc + 15	—	ns	
DREQ0, DREQ1 low level width	t_{DRQW}	1.5	—	t_{cyc}	

4496204 0054418 4T2

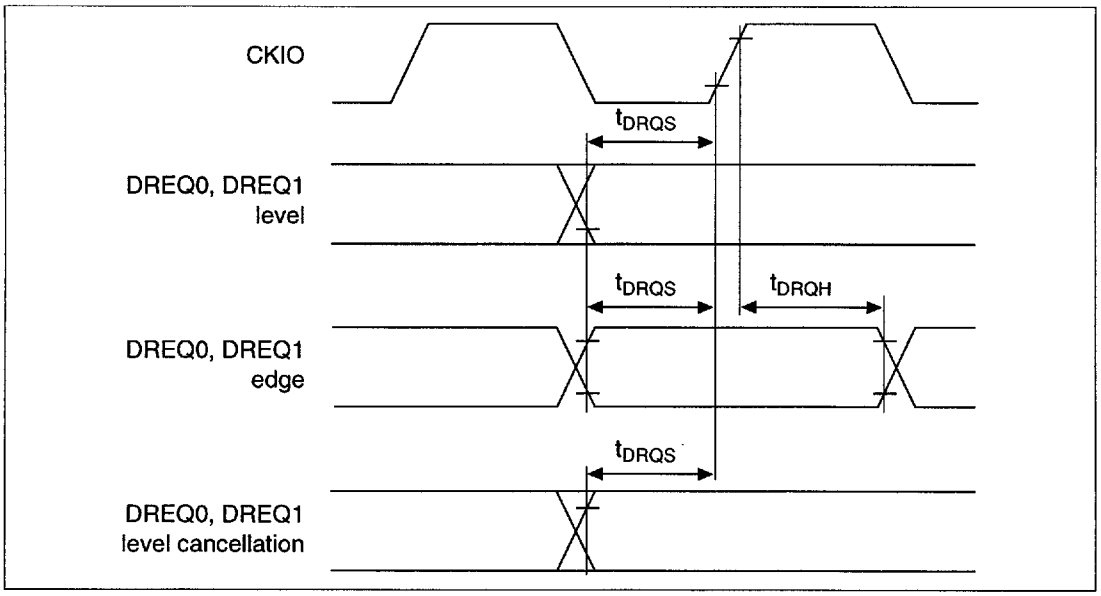


Figure 15.72 DREQ0, DREQ1 Input Timing

15.3.5 Free-Running Timer Timing

Table 15.11 Free-Running Timer Timing (V_{CC} = 5.0 V ±10%, Ta = –20 to +75°C)

Item	Symbol	Min	Max	Unit	Figure
Output compare delay time (PLL Off, On)	t_{TOCD}	—	160	ns	15.73
Output compare delay time (PLL On, 1/4 cycle delay)	t_{TOCD}	—	1/4 tcyc + 160	ns	
Input capture setup time (PLL Off, On)	t_{TICS}	80	—	ns	
Input capture setup time (PLL On, 1/4 cycle delay)	t_{TICS}	80 – 1/4 tcyc	—	ns	
Timer clock input setup time (PLL Off, On)	t_{TCKS}	80	—	ns	15.74
Timer clock input setup time (PLL On, 1/4 cycle delay)	t_{TCKS}	80 –1/4 tcyc	—	ns	
Timer clock pulse width (single edge)	t_{TCKWH}	4.5	—	t_{cyc}	
Timer clock pulse width (both edges)	t_{TCKWL}	8.5	—	t_{cyc}	

4496204 0054419 339

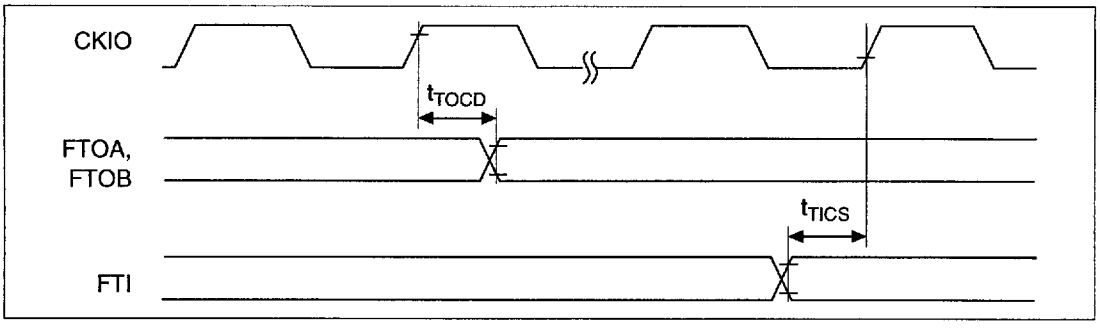


Figure 15.73 FRT Input/Output Timing

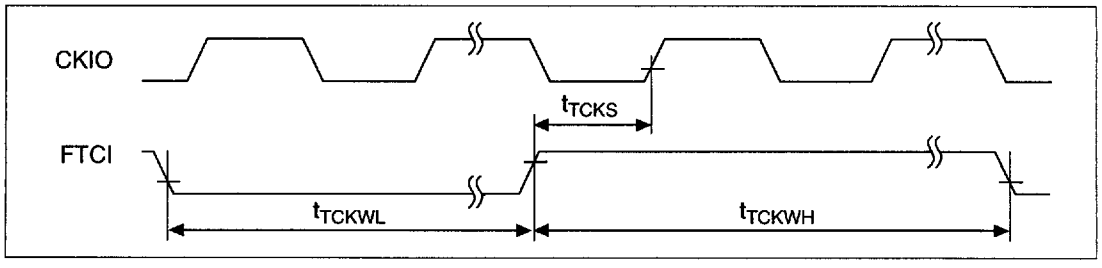


Figure 15.74 FRT Clock Input Timing

15.3.6 Watchdog Timer Timing

Table 15.12 Watchdog Timer Timing (V_{CC} = 5.0 V ±10%, Ta = –20 to +75°C)

Item	Symbol	Min	Max	Unit	Figure
$\overline{\text{WDTOVF}}$ delay time (PLL Off, On)	t_{WOVD}	—	70	ns	15.75
$\overline{\text{WDTOVF}}$ delay time (PLL On, 1/4 cycle delay)	t_{WOVD}	—	1/4 tcyc +ns 70		

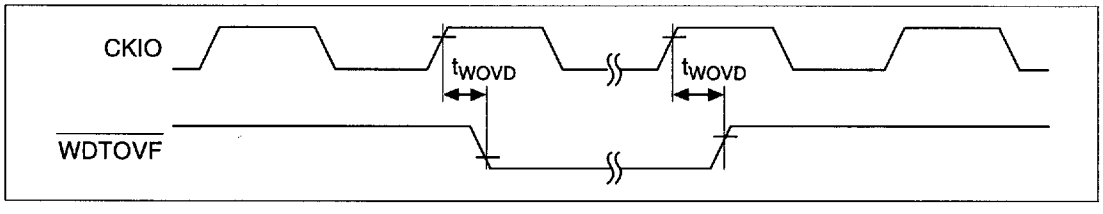


Figure 15.75 Watchdog Timer Output Timing

4496204 0054420 050

15.3.7 Serial Communications Interface Timing

Table 15.13 Serial Communications Interface Timing (V_{CC} = 5.0 V ±10%, Ta = –20 to +75°C)

Item	Symbol	Min	Max	Unit	Figure
Input clock cycle	t_{scyc}	16	—	t_{cyc}	15.76
Input clock cycle (clocked synchronization)	t_{scyc}	24	—	t_{cyc}	
Input clock pulse width	t_{sckw}	0.4	0.6	t_{scyc}	
Transmission data delay time (clocked synchronization)	t_{TXD}	—	70	ns	15.77
Receive data setup time (clocked synchronization)	t_{RXS}	70	—	ns	
Receive data hold time (clocked synchronization)	t_{RXH}	70	—	ns	

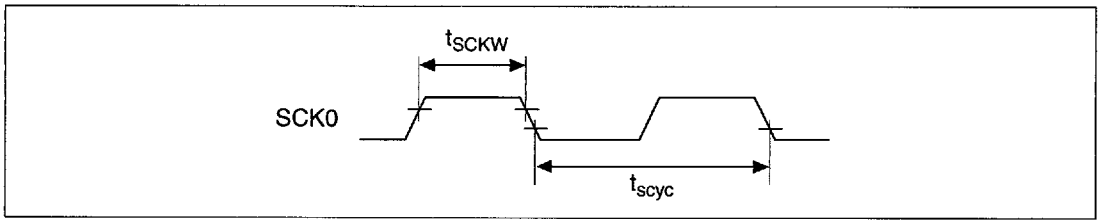


Figure 15.76 Input Clock I/O Timing

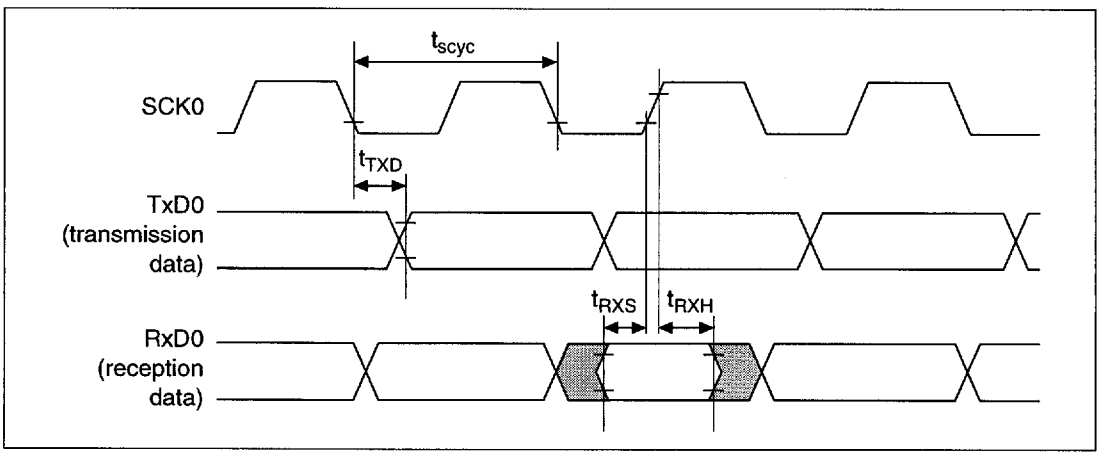
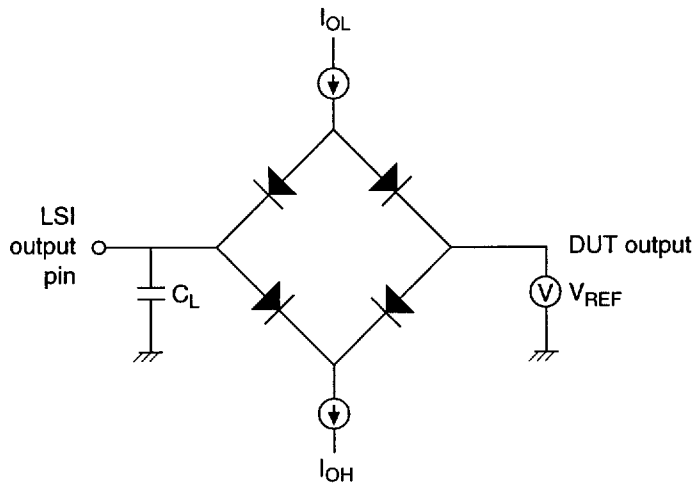


Figure 15.77 SCI I/O Timing (Clocked Synchronization Mode)

4496204 0054421 T97

15.3.8 AC Characteristics Measurement Conditions

- I/O signal reference level: 1.5 V
- Input pulse level: V_{SS} – 3.0 V (where RES, NMI, CKIO and MD5-MD0 are within V_{SS} – V_{CC})
- Input rise and fall times: 1 ns



Notes: 1. C_L is a total value that includes capacitance of measurement instruments and the like and is set as follows for each pin.
2. 30 pF: CKIO, $\overline{RAS}$, $\overline{CAS}$, CKE, $\overline{CS0}$–$\overline{CS3}$, $\overline{BREQ}$, $\overline{BACK}$, DACK0, DACK1, $\overline{IVECF}$, $\overline{CKPACK}$.
3. 50 pF: All output pins other than the above.
4. I_{OL} and I_{OH} values are as shown in section 15.2, DC Characteristics, and table 15.3, Permitted Output Current Values.

Figure 15.78 Output Load Circuit

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