IC WORKS

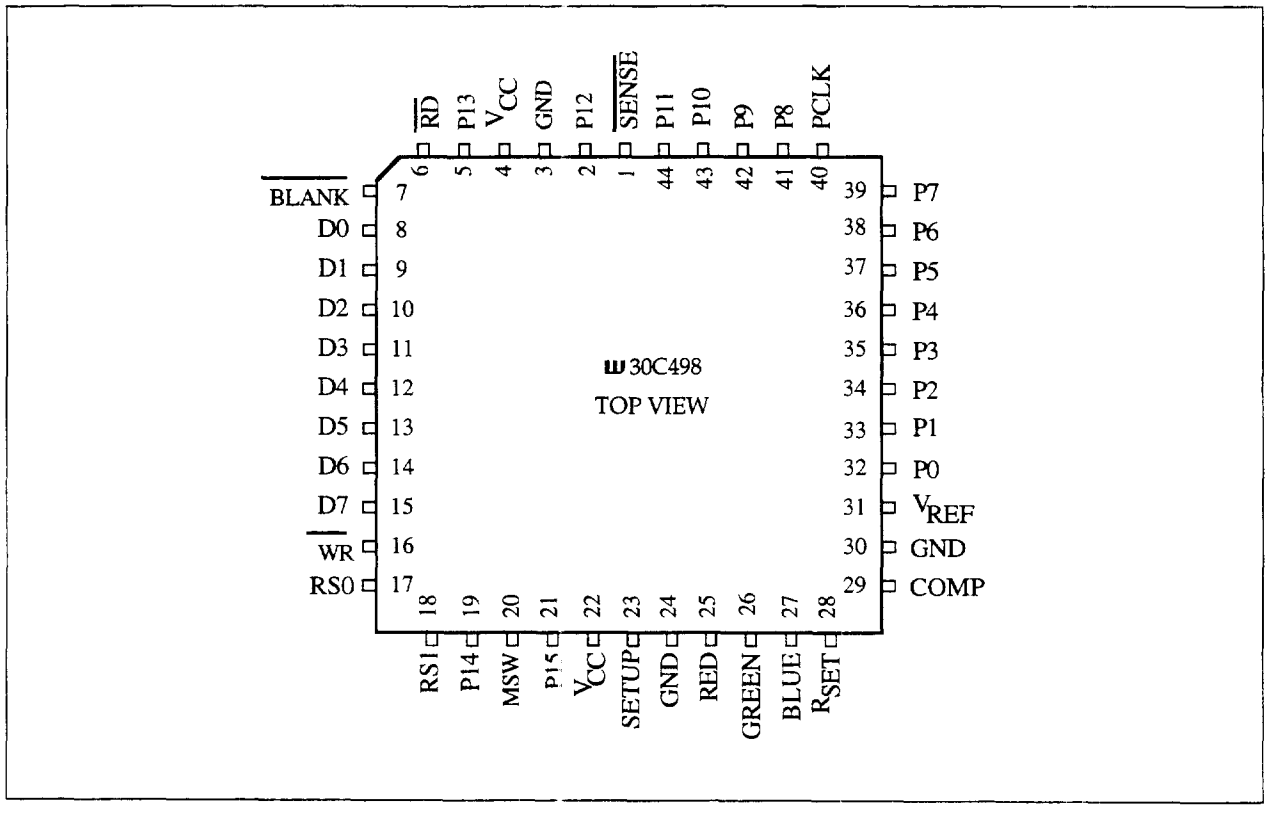
W30C498
True-Color RAMDAC

ADVANCE INFORMATION, AUGUST 1994

FEATURES

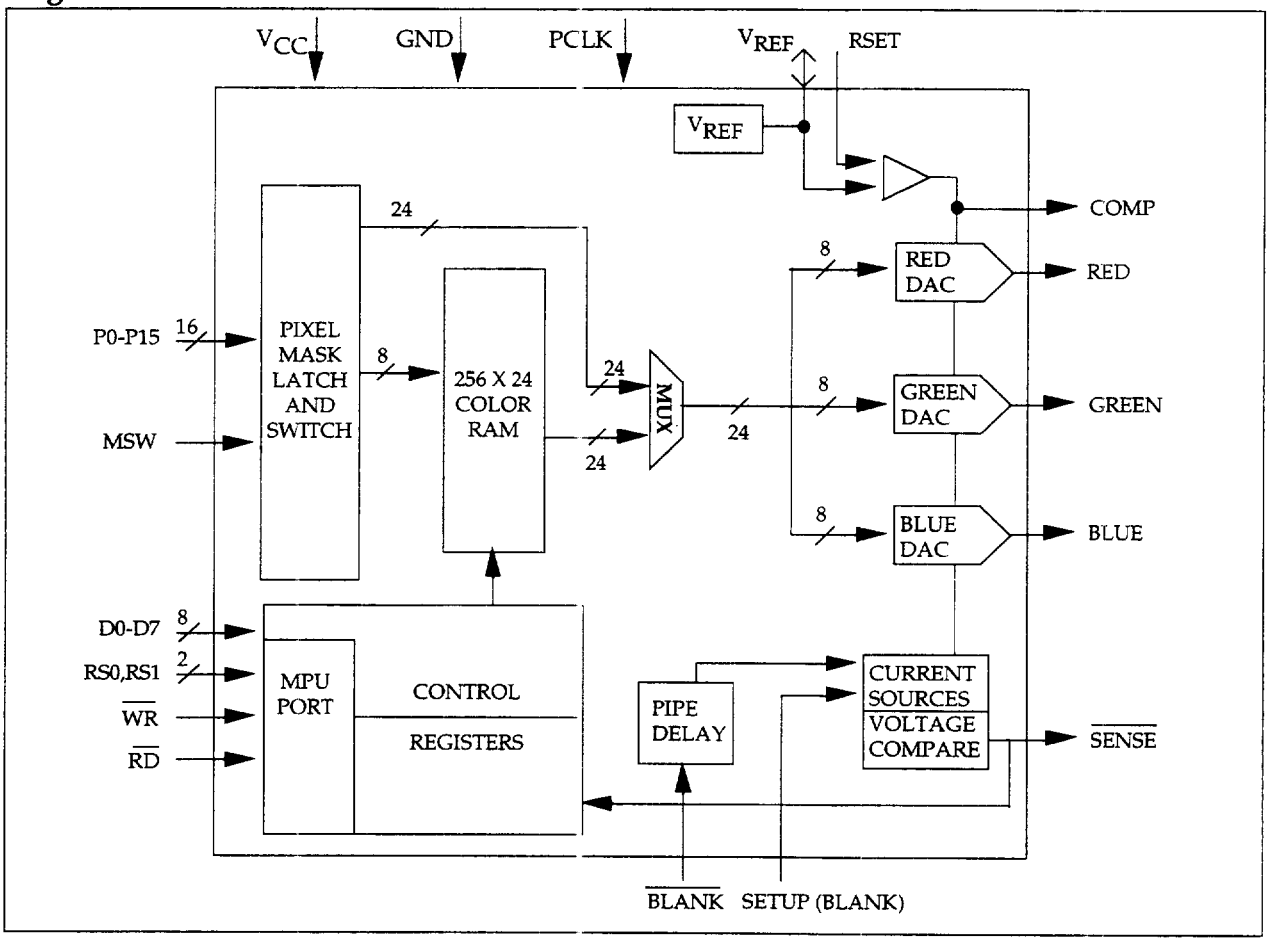
- **170, 135 and 110 MHz Versions**
- **16-bit Pixel Port**
- **8, 15, 16 or 24 bit-per-pixel modes**
  - **XGA™, HiColor™, TARGA™**
  - **Pixel-by-Pixel mode switching**
- **On-Chip Voltage Reference**
- **Software-readable output sense**
- **Device and manufacturer ID**
- **Anti-Sparkle circuitry**
- **Low power 5 volt CMOS**
- **Power-Down for Battery and Green PCs**
- **44-pin PLCC**

Figure 1: Pin Diagram: W30C498



XGA is a trademark of International Business Machines Corp.
TARGA is a trademark of Truevision Corp.
HiColor is a trademark of Sierra Semiconductor Corp.

Figure 2: FUNCTIONAL BLOCK DIAGRAM: W30C498



APPLICATIONS

- **True-Color Super-VGA**
- **Add-in card or motherboard**
- **Desktop, Notebook and Green PCs**
- **Screen resolutions up to:**
  - **1280 x 1024, 16-bit per pixel, 76Hz**
  - **1280 x 1024, 8-bit per pixel, 76Hz**
  - **1024 x 768, 16-bit per pixel, 127Hz**
  - **1024 x 768, 24-bit per pixel, 139Hz**

DESCRIPTION

The W30C498 is an advanced, high-performance super-VGA RAM/DAC specially enabled for both pseudo-color and true-color at higher resolution.

A 16-bit pixel interface allows higher data throughput for more colors at higher screen resolutions. In 8-bit pixel modes, an on-chip 2-1 data mulitplexer and on-chip clock doubler reduces external clock frequencies for easier FCC certification.

With 8, 15, 16 and 24 bit-per-pixel modes, the W30C498 supports all the major image formats, including XGA™, HiColor™ and TARGA™ Formats. In addition to VGA compatible 18-bit colors, a full 24-bit color look-up-table allows 8-bit modes to select 256 colors from the expanded 16 million color palette. Pixel-by-pixel mode switching allows mixing different image pixel formats on a single screen.

Software readable unique manufacturer and IC IDs allow for intillegent BIOS and plug-and-play board implementations.

Software controlled power-down modes are included for battery or green-PC applications.

Microsoft Windows is a registered trademark of Microsoft Corp.

Table 1: Pin description

Pin Name	I/O	Pin #	Name/Function
GND	-	3, 24	Ground: Connect these pins to circuit ground.
V_{CC}	--	4, 22	Power: Connect these pins to +5.0V.
P0-P15	I	2, 5, 19, 21 41-44 32-39	Pixel Inputs: TTL compatible. These pins are latched on the rising edge of PCLK. Unused inputs should be connected to GND.
RSET	I	28	Reference: An external resistor (RSET) is connected between the RSET pin and GND to control the magnitude of the full-scale current.
COMP	I	29	Compensation Pin: Bypass this pin with an external 0.1µF capacitor to V_{CC}.
V_{REF}	--	31	Voltage Reference: Bypass this pin with an external 0.1µF capacitor to GND.
$\overline{SENSE}$	O	1	$\overline{SENSE}$ (Active-Low): TTL compatible. This pin functions as the monitor detect signal $\overline{SENSE}$ is a logic 0 if one or more of the red, green, or blue outputs has exceeded the internal voltage reference level of 340mV.
PCLK	I	40	Pixel Clock: TTL compatible. The rising edge of the pixel clock latches the pixels, $\overline{BLANK}$ inputs.
$\overline{BLANK}$	I	7	Blank (Active-Low): TTL compatible $\overline{BLANK}$ is latched on the rising edge of PCLK. When $\overline{BLANK}$ is low, the 1.44mA current source on the analog outputs will be turned off and the DACs ignore digital input.

Table 1: Pin description (con't)

Pin Name	I/O	Pin #	Name/Function
D0-D7	I/O	15-8	Data Bus: TTL compatible. Data is transferred between the data bus and the internal registers under control of the $\overline{RD}$ and $\overline{WR}$ signals. In an MPU write operation, D0-D7 is latched on the rising edge of $\overline{WR}$. To read data D0-D7 from the device $\overline{RD}$ must be in an active low state. The rising edge of the $\overline{RD}$ signal indicates the end of a read cycle. Following the read cycle, the data bus will go to a high-impedance state. Note: for 6-bit operation, color data is

REGISTER DESCRIPTIONS

Table 2: Original VGA Register addressing.

Register Name	RS1	RS0	DAC Address	PC / VGA I/O Address (Hex)	LUT Function
Address_Mask	1	0	2	3C6	Address Mask
Read_Address	1	1	3	3C7	Address for Data Read
Store_Address	0	0	0	3C8	Address for Data Write
Data	0	1	1	3C9	Color Data

INTERNAL REGISTERS

The registers are read and written by the MPU (microprocessor). Bit 0 is the least significant bit and corresponds to pin D0 of the MPU port.

To maintain compatibility, the Extension Registers are addressed indirectly. Normally hidden, they become "visible" when a reserved sequence of operations is used. This operation is explained in the section Accessing the Extension Registers.

ORIGINAL REGISTERS

The Original Registers are accessed directly, selected by the RS0 and RS1 signals — just like the original VGA RAMDAC. The Original Registers are only used in 8-bit palette-color (Look-Up Table) modes. The addressing of the registers is shown in Table 2.

Store_Address

This register holds an 8-bit address used when storing data into the look-up-table. Write to this register before writing data to the Data Register. Writing the Store_Address sets the location and resets the data port color pointer to 'Red' for the next access. Each of the LUT locations are 24-bits wide (8 bits red, 8 bits green and 8 bits blue). To write all 24-bits of a LUT location, 3 successive writes are made to the Data Register. After the sequence of 3 writes is completed, the 24-bit value is transferred to the LUT RAM and the Store_Address Register will automatically increment by one. After writing LUT entry 255, the Address wraps back to address 0.

Read_Address

This register holds the 8-bit LUT address used for reading the LUT contents (via the Data Register). When the Read_Address Register is written, the LUT is accessed and the values are ready to be read via the Data Register. Writing the Read_Address sets the location and resets the data port color pointer to 'Red' for the next access. When the three reads from the LUT Data Register are complete, the Read_Address is incremented and new data is made ready for Data Register access.

LUT Data

This is the data port through which color data reads and writes are made to the LUT. This register is an 8-bit port into a 24-bit location. Three accesses are needed to read or write the LUT data register, first Red, then Green and finally Blue. Data is kept in a temporary holding area and transferred to the LUT when the third value (blue) is written to the Data Register.

The LUT Store_Address or LUT Read_Address register is used to specify which LUT location is to be accessed. One of these should be written with the desired LUT address before accessing the LUT Data Register for the first time. Once the address is written, the Data Register may be accessed an unlimited number of times. The address will auto-increment through the entire LUT and wrap back to address '0' after '255' is accessed.

Address_Mask

The contents of the Address_Mask Register is not initialized on power up. Address_Mask bits are logically ANDed with the 8-bit pixels before the pixel is used as the LUT address during display. A '1' stored in a bit of the Address_Mask leaves the corresponding bit in the pixel unchanged. A '0' in the Address_Mask sets the matching pixel bit to zero. The least significant bit of the Address_Mask Register corresponds to Look-Up Table address bit L0 (8-bit pixel bit 0).

Table 3: Extension Registers

Control Register 0 (CR0)		
CR0[0] Reserved, write zero for compatibility		
CR0[1] 8-bit or 6-bit Color Data		
CR0[2] Pixel-by -Pixel Color Format Change Enable		
CR0[3] Power Down		
CR0[7..4] Color Format		
Manufacturer Identification	(Read Only)	# Hex 84
Device Identification	(Read Only)	# Hex 98

EXTENSION REGISTERS

The functions beyond the original VGA functions are enabled and controlled by the Extension Registers. These registers, listed in Table 3, are not accessed directly by the RS1 and RS0 pins, but for compatibility, indirectly via software. The sequence which unlocks the Extension registers is the repeated reading of address 2 (RS1=1, RS0=0; VGA I/O 3C6 (hex)). Details are given in the section, "Accessing the Extension Registers".

Control Register 0 (CR0)

Table 3 lists the functions assigned the bits of the control register. The Power-up condition is zero for all bits.

CR0[7..4] The 4 most significant bits of Control Register 0 determine the way input pixel data is interpreted. Different combinations of color depths and clock combinations are available, as detailed in Table 5 and described in the section, Color Modes.

CR0[3] Setting bit 3 to a ' 1' puts the RAMDAC in power down mode. In the power down state, the device retains the information in the color look-up table. Microprocessor access to the color look-up table and internal registers are enabled during power down mode.

CR0[2] When bit 2 is set to a '1', the mode switching (via the MSW pin or data bit 15) is disabled and pixels are interpreted according to the mode in Table 5. When Pixel-by-pixel switching is enabled (CR0[2]=0), the alternate formats of Tables 6 and 7 are available.

CR0[1] Bit 1 of Control Register '0' determines whether 8- or 6-bits of color information is being passed over the D0-D7 port for LUT data. The 6-bit LUT mode is provided for VGA backward compatibility. In 6-bit mode write cycles, the RAMDAC only inputs D0..D5 and converts these 0 - 63 values into 0-255 values before writing the LUT. On read cycles, the 0-255 LUT values are converted back to the 0..63 range before passing data back to the MPU (D6 and D7 are set to 0).

CR0[0] Reserved. Write 0 for compatibility.

Manufacturer Identification (MID) (Read Only)
This is a read-only location which returns the IC Works ID of 84 (hex).

Device Identification (DID) (Read Only)
This is a read-only location which returns the W30C498 ID of 98 (hex).

ACCESSING THE EXTENSION REGISTERS

Access to the indirect registers is made by repeated access to address 2 (RS1-RS0 =10); (VGA address 3C6 (hex)). This address, normally accesses the Original register, Address_Mask as shown in Table 4.

Table 4: Extended Register Access States

State	Action	Result	Next State
0	Read address 0,1,3	Read from Original Register	0
	Write address 0,1,2,3	Write to Original Register	0
	Read address 2	Read from Address_Mask Register	1
1	Read address 0,1,3	Read from Original Register	0
	Write address 0,1,2,3	Write to Original Register	0
	Read address 2	Read from Address_Mask Register	2
2	Read address 0,1,3	Read from Original Register	0
	Write address 0,1,2,3	Write to Original Register	0
	Read address 2	Read from Address_Mask Register	3
3	Read address 0,1,3	Read from Original Register	0
	Write address 0,1,2,3	Write to Original Register	0
	Read address 2	Read from Address_Mask Register	4
4	Access address 0,1,3	Access Original Register	0
	Write address 2	Write to Control Register 0	0
	Read address 2	Read from Control Register 0	5
5	Access address 0,1,3	Access Original Register	0
	Write address 2	No Operation	0
	Read address 2	Read Manufacturer ID (84 hex)	6
6	Access address 0,1,3	Access Original Register	0
	Write address 2	No Operation	0
	Read address 2	Read Device ID (98 hex)	0

Table 5: Color Modes and Data Formats

Mode	Description	Destination of Input Pin Data															
CR0[7..4]		P15	P14	P13	P12	P11	P10	P9	P8	P7	P6	P5	P4	P3	P2	P1	P0
0	8-bit Palette 1 clock = 1 pixel									L7	L6	L5	L4	L3	L2	L1	L0
1	15-bit Hi-Color 1 clock = 1 pixel	-	R7	R6	R5	R4	R3	G7	G6	G5	G4	G3	B7	B6	B5	B4	B3
2	8-bit Palette 1 clock = 2 pixels	$L_2$7	$L_2$6	$L_2$5	$L_2$4	$L_2$3	$L_2$2	$L_2$1	$L_2$0	$L_1$7	$L_1$6	$L_1$5	$L_1$4	$L_1$3	$L_1$2	$L_1$1	$L_1$0
3	16-bit XGA Color 1 clock = 1 pixel	R7	R6	R5	R4	R3	G7	G6	G5	G4	G3	G2	B7	B6	B5	B4	B3
4	8-bit Palette 2 clocks = 1 pixel Nibble Wide	Clk-1 Clk-2												L3 L7	L2 L6	L1 L5	L0 L4
5	24-bit True-Color 2 clocks = 1 pixel Unpacked, Skip a Byte	G7	G6	G5	G4	G3	G2	G1	G0	B7 R7	B6 R6	B5 R5	B4 R4	B3 R3	B2 R2	B1 R1	B0 R0
6	16-bit XGA-Color 2 clocks = 1 pixel Byte Wide	Clk-1 Clk-2								G4 R7	G3 R6	G2 R5	B7 R4	B6 R3	B5 G7	B4 G6	B3 G5
7	24-bit True-Color 3 clocks = 1 pixel	Clk-1 Clk-2								B7 G7	B6 G6	B5 G5	B4 G4	B3 G3	B2 G2	B1 G1	B0 G0

COLOR MODES

The w30C498 provides thirteen color modes selected by control register bits CR0[7..4]. Modes 13, 14 and 15 are reserved. The w30C498 supports 24-bit and 16-bit true-color bypass along with 8-bit palette-color. A 16-bit pixel bus interface allows higher color resolution at higher screen resolution than ever available in a 44 pin RAMDAC.

Table 5 lists the modes along with the format of pixel data read from the input pins (P15..P0).

Some of the modes use more than one clock for each pixel. The $\overline{\text{BLANK}}$ signal resets the internal pixel clock so that the first rising edge of PCLK after $\overline{\text{BLANK}}$ is inactive will input the first part of the first pixel of a scan line (i.e. the LSB).

In 15-bit or 16-bit data modes (Hi-Color 5-5-5 or XGA-Color 5-6-5), the 5 or 6 bits of color data is sent to the most significant bits of the DACs and the least significant 2 or 3 bits of the DAC inputs are set to zero.

In addition to the primary data format listed in Table 5, most modes (0, 3, 4, 5, 6, 8, 9, 10 and 12) have a secondary data format switchable on a pixel-by-pixel basis by the input pin, MSW. This ability to switch on the fly allows a mixed mode screen where part of the screen is drawn with one data format, and another is drawn with another format. The most common use is to use 8-bit palette data with a high-color window for an image or video (Mode 0 switching to Mode 3 data). Some example mode switches are shown graphically in Figures 4, 5, 6, and 7.

When the MSW is 0, the RAMDAC interprets the incoming pixel data to be the primary mode format. When the MSW pin is 1, the RAMDAC interprets the incoming pixel data to be the secondary or alternate format as shown in Table 6, Mode Switching using the MSW Pin. This table shows the two data formats available in each of the modes. On the right, is a column which lists the mode which has the same data format as the alternate format. To see bit packing of the alternate format, look up the equivalent mode data in Table 5.

In addition to the modes which change formats using the MSW pin, one mode (#1) changes format without any signal on the MSW pin. This mode uses the most significant pixel bit (P15) to switch between 15-bit Hi-Color (the primary mode) and 8-bit palette color. This is shown in Table 7, Mode Switching Using Data Bit 15.

Pixel-by-Pixel format switching (either MSW or P15 pins) must be enabled by setting CR0[2] to a'0'. If this bit is a '1', no Pixel-by-Pixel format switching will occur in any mode. At power-up, CR0 is reset to all zeros. This means the chip powers up in the standard VGA backward compatibility configuration of Mode 0 with Pixel-by-Pixel switching enabled.

Mode 0 8-bit palette-color; 1 clock per pixel

This is the power-up default mode. Standard VGA compatible, each PCLK brings in an 8-bit pixel on pins P0..P7. The pixel accesses the color LUT and the resulting 24-bit color drives the DACs.
Secondary data format is 16-bit XGA color.

Mode 1 15-bit Hi-Color; 1 clock per pixel

This mode displays data formatted for 15-bit per pixel Hi-color (5-5-5) on pins P0..P14.
This mode is unique in that the mode switch is determined by the most significant pixel bit (P15) and not by the MSW pin. The MSW input has no effect on mode 1 and may be either high or low. When P15 = 0 the pixel data is interpreted as 15-bit true-color. When P15 = 1, the pixel data on pins P0..P7 is interpreted as 8-bit palette-color and pins P8..P14 are ignored.

Mode 2 8-bit Palette Color; 16-bit wide; 1 clock, 2 pixels

Mode 2 uses 16-bit pixel data to input two 8-bit palette-color pixels at a time. The w30C516 uses a built-in 2:1 data multiplexer and an internal PCLK clock doubler to convert the double-wide input stream into a double-speed analog output stream. This reduced external PCLK helps to reduce EMI problems at higher screen resolutions.

There is no secondary data format for mode 2. When mode 2 is selected, bit CR0[0] should be set to "0" if PCLK is less than 45 MHz or "1" otherwise.

Mode 3 16-bit XGA-color (5-6-5); 1 clock per pixel
Mode 3 uses the full 16-bits for each pixel. Green has 6 bits of accuracy while Red and Blue have 5 bits each.

The secondary data format is 8-bit palette color.

Mode 4 8-bit palette-color; 2 clocks per pixel
This mode accepts data formatted as 8-bit palette-color latched by two pixel clocks as 4-bit nibbles. Latching two nibbles allows mode switching to 24-bit true-color (mode 5 format) without changing pixel clock frequencies. See Figure 6.

Mode 5
24-bit true-color (8-8-8); 2 clocks per pixel
Two 16-bit words are used for each 24-bit pixel. The MSb of the second 16-bit word is not used.

The secondary data format is 16-bit XGA color.

Mode 6
16-bit XGA-color (5-6-5); 2 clocks per pixel
The 16-bit pixel is latched in two bytes with two PCLKs. The LSBs are latched first followed by the MSBs. Latching one byte per clock allows mode switching to 24-bit true-color (mode 5 format) without changing pixel clock frequencies. See Figure 7.

Color data is 5 bits Red, 6 bits Green and 5 bits Blue.

Mode 7
24-bit true color (8-8-8), three clocks per pixel
The 24-bit pixel is latched in three bytes with three PCLKs. The pixel information is collected over three rising edges of the pixel clock. $\overline{\text{BLANK}}$ going high will signal the first pixel information of a scanline is available on P0-P7. The Blue data is latched first followed by Green then Red.

Mode 7 has no secondary data format.

Mode 8 8-bit palette color; two clocks per pixel
This mode accepts data formatted as 8-bit palette color latched by two pixel clocks in 4-bit nibbles. Latching two nibbles allows mode switching to 16-bit true color (mode 6 format) without changing pixel clock frequencies.

Mode 9 8-bit palette-color; two clocks per pixel
Eight bits are taken from P0-P7 on the first cycle. The second cycle is a dummy cycle with no input allowing format switching to 24-bit true color (mode 5 format) without changing clock frequency.

Mode 11 24-bit True-Color; 3 clocks per 2 pixels
This mode uses all 16 data inputs to allow two 24-bit pixels in 3 clocks. The first clock reads in the Green and Blue bits of the first pixel. The second clock reads in the Blue bits of the second pixel and the Red bits of the first pixel. The third clock reads in the Red and Green bits of the second pixel. See Table 5 for a bit packing diagram.

Mode 11 has no secondary data format.

Mode 12 8-bit palette-color; 1 clock per pixel
Standard VGA compatible data, each PCLK brings in an 8-bit pixel on pins P0..P7. The pixel accesses the color LUT and the resulting 24-bit color drives the DACs.

Secondary data format is 15-bit Hi-Color (5-5-5).

Modes 10 and 13 through 15: Reserved.

Figure 4: On the fly mode switch from 8bpp to 16bpp (mode 0 changing to mode 3)

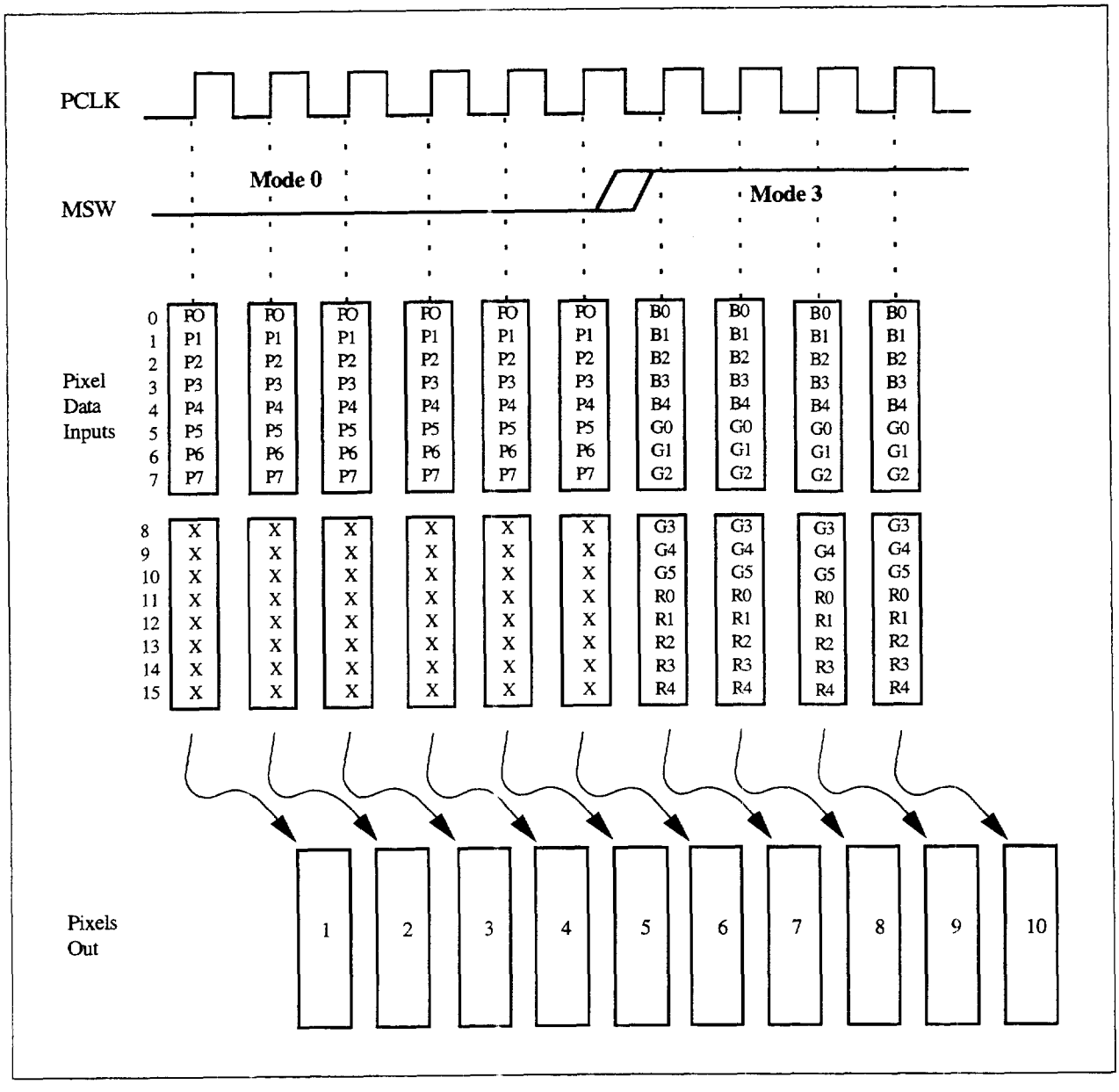


Figure 5: On the fly mode switch from 8bpp to 15bpp
(Setup in mode 1, P15=1 Mode 12 format data changing to mode 1 format P15=0)

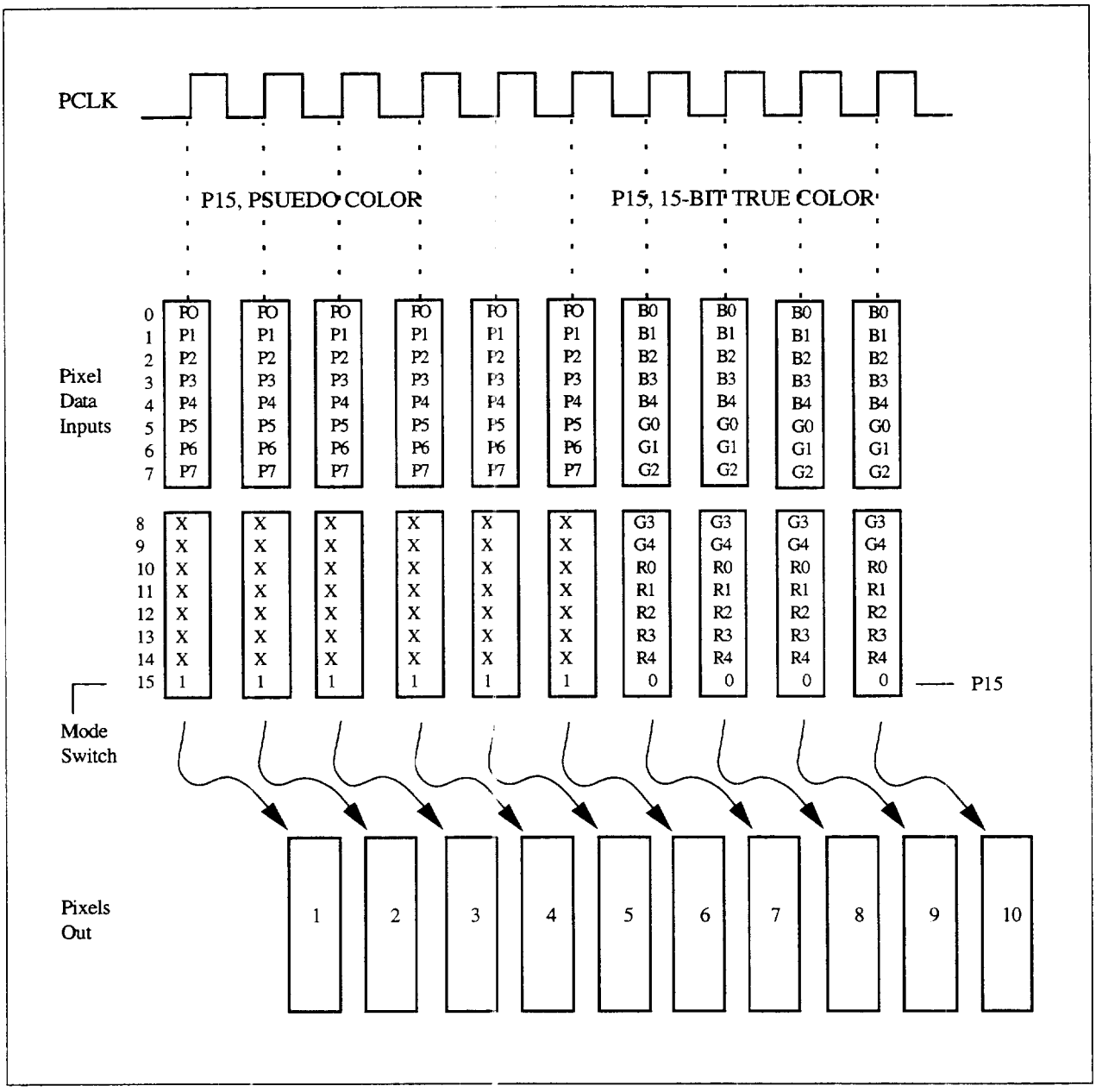


Figure 6: On the fly mode switch from 8bpp to 24bpp (mode 4 changing to mode 5)

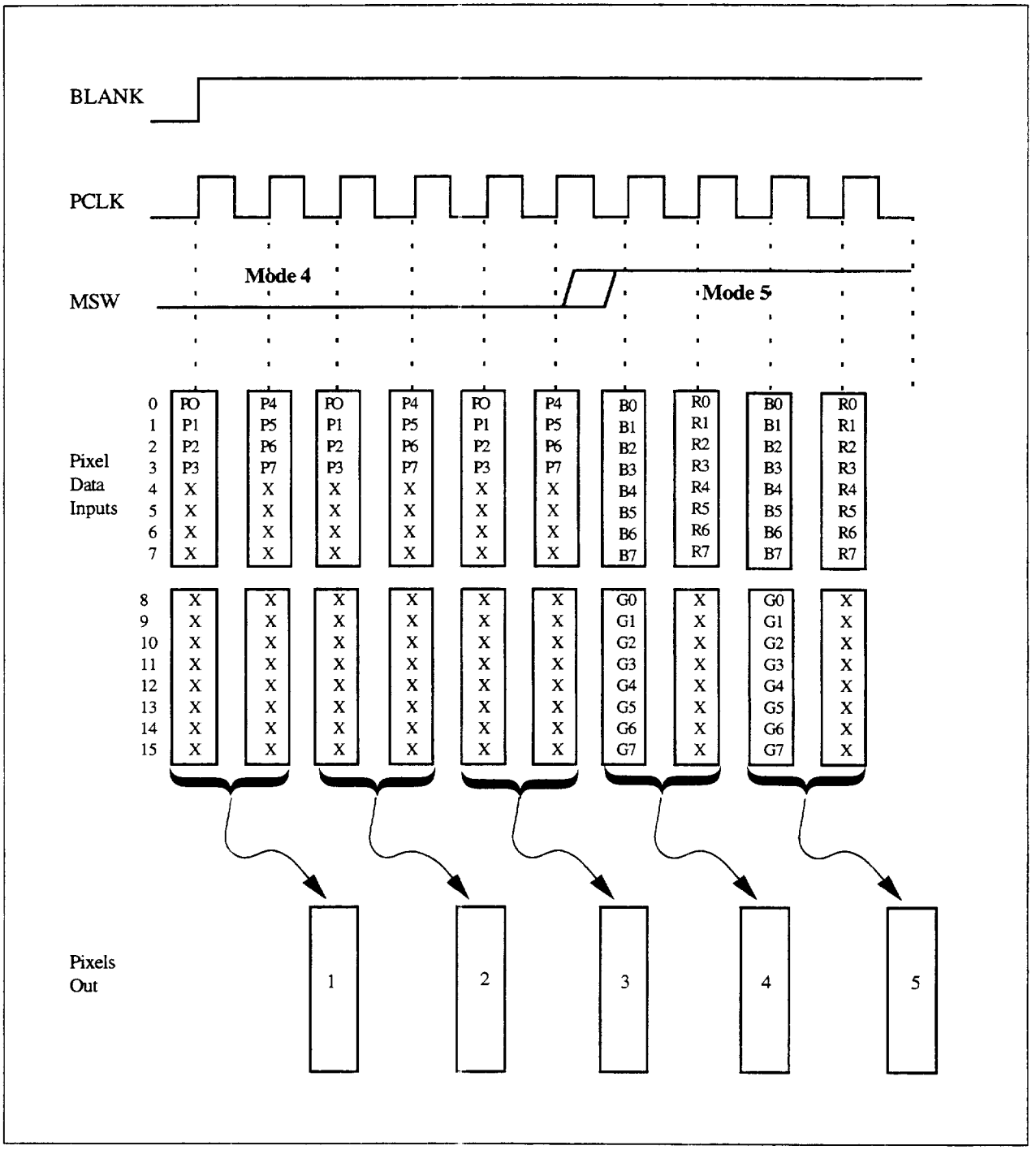


Figure 7: On the fly mode switch from 16bpp to 24bpp (mode 6 changing to mode 5)

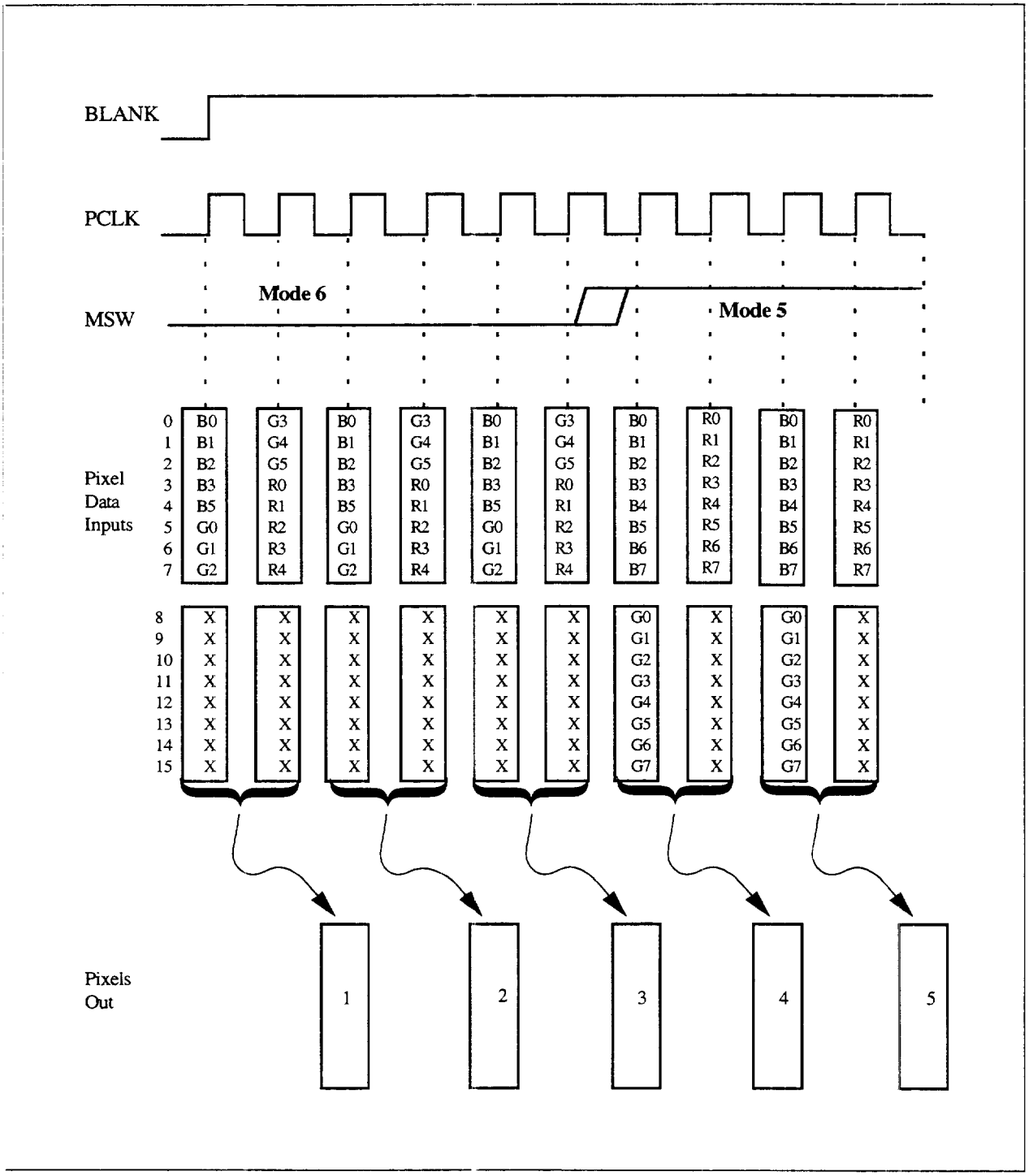


Table 6: Mode Switching using MSW Pin (CR0[2]=0)

Selected Mode	MSW = 0	MSW = 1	Mode With Equivalent Format
0	8-bit Palette 1 clock = 1 pixel -------- XXXXXXXX	16-bit XGA Color 1 clock = 1 pixel XXXXXXXX XXXXXXX	3
3	16-bit XGA Color 1 clock = 1 pixel XXXXXXXX XXXXXXXX	8-bit Palette 1 clock = 1 pixel -------- XXXXXXXX	0
4	8-bit Palette 2 clocks = 1 pixel Nibble Wide -------- ----XXXX -------- ----XXXX	24-bit True-Color 2 clocks = 1 pixel Unpacked, Skip a Byte XXXXXXXX XXXXXXXX -------- XXXXXXXX	5
5	24-bit True-Color 2 clocks = 1 pixel Unpacked, Skip a Byte XXXXXXXX XXXXXXXX -------- XXXXXXXX	16-bit XGA-Color 2 clocks = 1 pixel Byte Wide -------- XXXXXXXX -------- XXXXXXXX	6
6	16-bit XGA-Color 2 clocks = 1 pixel Byte Wide Unpacked, Skip a Byte -------- XXXXXXXX -------- XXXXXXXX	24-bit True-Color 2 clocks = 1 pixel XXXXXXXX XXXXXXXX -------- XXXXXXXX	5
8	8-bit Palette 2 clocks = 1 pixel Nibble Wide -------- ----XXXX -------- ----XXXX	16-bit XGA-Color 2 clocks = 1 pixel Byte Wide -------- XXXXXXXX -------- XXXXXXXX	6
9	8-bit Palette 2 clocks = 1 pixel Skip Bytes Unpacked, Skip a Byte -------- XXXXXXXX -------- --------	24-bit True-Color 2 clocks = 1 pixel XXXXXXXX XXXXXXXX -------- XXXXXXXX	5
12	8-bit Palette 1 clock = 1 pixel -------- XXXXXXXX	15-bit Hi-Color 1 clock = 1 pixel -XXXXXXX XXXXXXXX	1

Table 7: Mode Switching using Data Bit P15 (CR0[2]=0)

Selected Mode	P15 = 0	P15 = 1	Mode With Equivalent Format
1	15-bit Hi-Color 1 clock = 1 pixel 0XXXXXXX XXXXXXXX	8-bit Palette 1 clock = 1 pixel 1 - - - - - - - XXXXXXX	12

MPU Interface

The W30C498 supports a standard MPU interface, allowing the MPU direct access to the Store_Address Register, RAMDAC color RAM, Address_Mask Register or Read_Address Register. As outlined in Table 2, the RS0-RS1 select inputs indicate whether the MPU is accessing the address register Store_Address Register, RAMDAC color RAM, Address_Mask Register or Read_Address Register. To eliminate the requirement for external address multiplexers, the 8-bit address register is used to address the RAMDAC RAM. Store_Address Register[O] and Read_Address Register[O] corresponds to DO and is the least significant bit.

Writing the RAMDAC

The MPU writes the address register (Store_Address Register) with the address of the RAMDAC color RAM location to be modified. Using RS0-RS1 to select the RAMDAC color RAM (LUT), the MPU completes three continuous write cycles (6- or 8-bits each of red, green, and blue). Following the blue write cycle, the 3 bytes of color information are concatenated into an 18- or 24-bit word and written to the location specified by the address register. The address register advances to the next location which the MPU can modify by simply writing another sequence of red, green, and blue data. A block of color values in successive locations can be written to by writing the start address and performing continuous red, green and blue write cycles until the entire block has been written.

Reading the RAMDAC

The MPU loads the address register (Read_Address Register) with the address of the RAMDAC color RAM location to be read. The contents of the RAMDAC color RAM at the specified address are copied into the RGB register, and the address register advances to the next RAM location. Using RS0-RS1 to select the RAMDAC color RAM (LUT), the MPU completes three continuous read cycles (6- or 8-bits each of red, green, and blue). After the blue read cycle, the contents of the RAMDAC color RAM at the address specified by the address register are copied into the RGB registers, and the address register advances to the next address. A block of color values in successive locations can be read by writing the start address and performing continuous red, green and blue read cycles until the entire block has been read.

ADDITIONAL INFORMATION

Following a blue read or write cycle to color RAM location $FF, the address register resets to $00.

Operation of the MPU interface occurs asynchronously to the pixel clock. Internal logic synchronizes data transfers between the RAMDAC color RAM, and the red, green, and blue color subregister. The transfers occur between MPU accesses. As a result, the $\overline{WR}$ and $\overline{RD}$ signals must maintain a logic high for several clock cycles. See the ac timing characteristics under $\overline{RD}$ and $\overline{WR}$ high time for further information. To eliminate sparkling on the CRT screen during MPU access to the RAMDAC RAMs, internal logic maintains the previous output color data on the analog outputs while the transfer between look-up table RAMs and the RGB registers occurs.

The Store_Address Register and Read_Address Register address registers increment following a blue read or write cycle, and are accessible to the MPU and are used to address RAMDAC RAM locations (LUT). The MPU can read the address register at any time without modifying its contents or the existing read/write mode. Note that the pixel clock must be active for MPU accesses to the RAMDAC RAM (LUT).

8-/ 6-bit Color Resolution

The 8-/6-bit in the control register (CR01) determines whether the MPU port reads and writes 8-or 6-bits of color data to the color look-up table RAM. In 6-bit mode, color data is on the lower 6-bits of the data bus, with D0 being the LSB and D5, the MSB of color data. When writing color data, D6 and D7 are ignored. During color read cycles, D6 and D7 will be logic 0.

Software Identification

The w30C498 may be differentiated from other RAMDACs by reading the Manufacturer's ID (MIR) and Device ID DIR registers. The Manufacturer's ID is 84 (hex). The Device ID is 98 (hex).

Powerdown

CRO bit 3 controls the powerdown. The device operates normally while the bit is a logic 0. A logic 1 in the bit will turn off power to the computation logic and DACs. The RAM and internal registers still retain data and can be read and written by the CPU while the chip is powered down.

$\overline{\text{SENSE}}$ Output

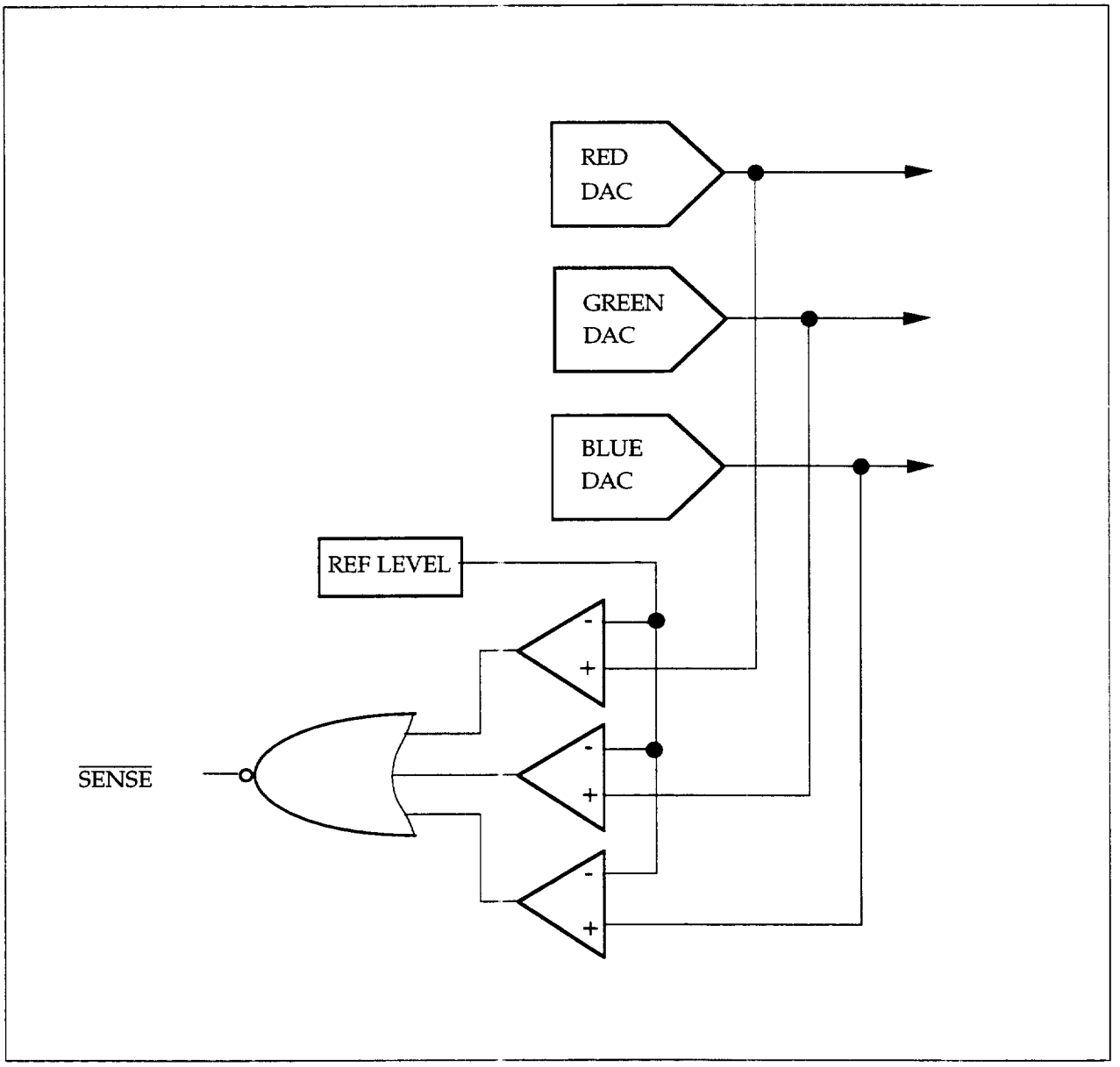
$\overline{\text{SENSE}}$ is a logic 0 if one or more of the red, green, or blue outputs have exceeded the internal voltage reference level (340mV +/- 70mV) shown schematically in Figure 8. By setting the DAC input to values near the threshold and reading $\overline{\text{SENSE}}$, diagnostic software can determine if the output line is loaded or unloaded. This enables the software to detect the presence of a CRT monitor and also whether the connected monitor is monochrome or color.

Note the $\overline{\text{SENSE}}$ logic is slower than the video speeds. After setting the DAC ouputs, diagnostic software should wait an appropriate time before reading the $\overline{\text{SENSE}}$ result — see Table 19 for $\overline{\text{SENSE}}$ delay times.

DAC Gain

The device gain is a function of the Voltage Reference (Vref) and the bias current resistor (Rset). With the internal Vref, the recommended RSET for RS-343A compatibility applications (doubly terminated 75Ω) is 147Ω. The recommended RSET for PS/2 applications (50Ω) is 182Ω's.

Figure 8: Output Comparison Circuitry for Detecting the Presence of a Monitor



APPLICATION INFORMATION

Board Layout

Careful configuration and placement of supply planes, components and signal traces ensures a low noise board. This helps ensure proper functionality and low signal emissions in restricted frequency bands as required by regulatory agencies.

A four layer PC board with segmented power planes (analog and digital) and a single ground plane will likely result in a board with quieter signals and supplies.

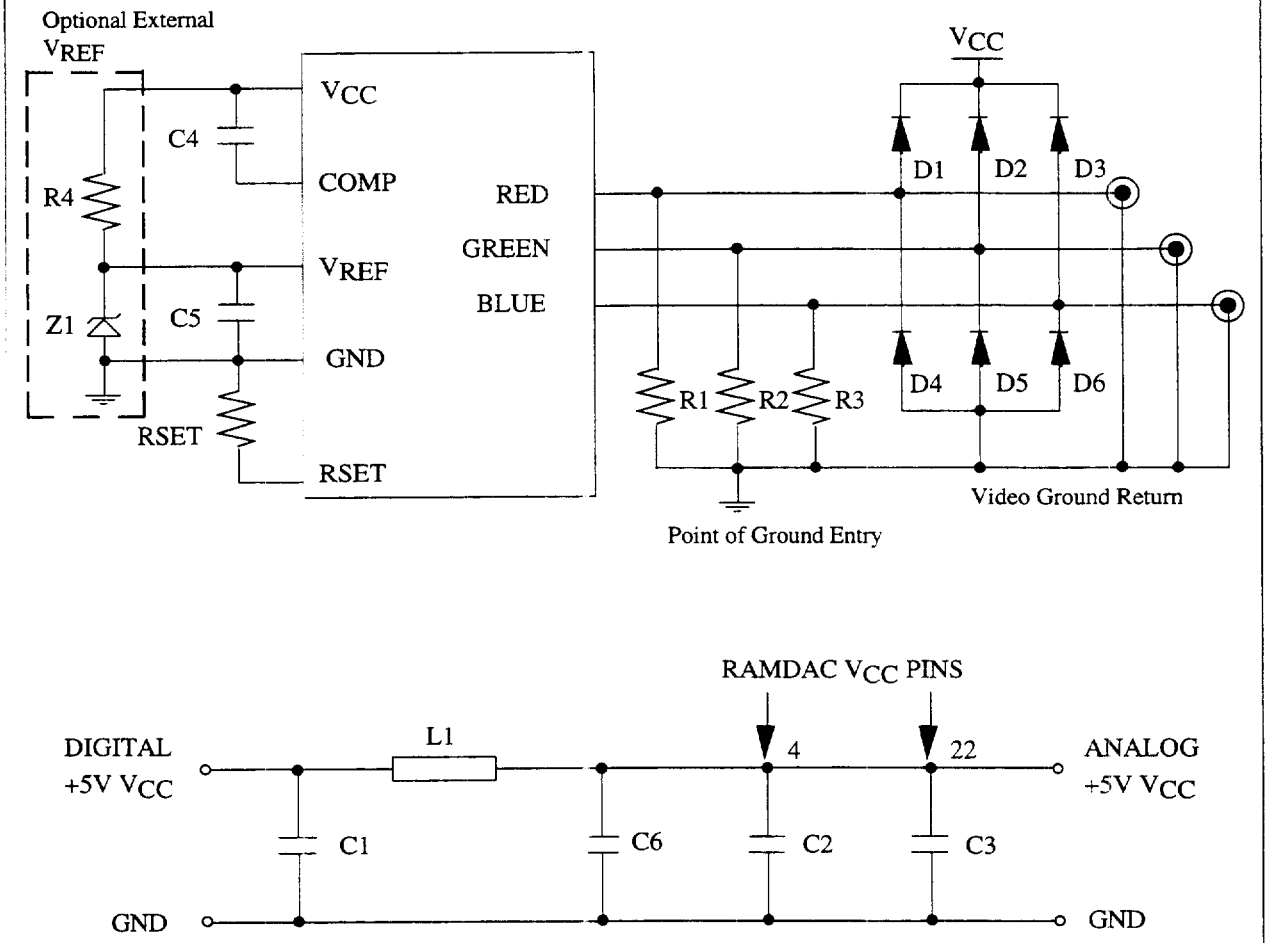
The W30C498 should be placed close to the video output connector and between the video output connector and the edge card connector. This will keep the high speed DAC output traces short and minimize the amount of circuitry between the RAMDAC and the supply pins on the edge card connector.

DAC Output Protection

The W30C498 analog outputs should be protected against high-energy discharges, such as those from monitor arc-over or from hot-switching AC coupled monitors.

The diode protection circuit shown in Figure 9 can protect against these situations. The 1N4148/9 are low-capacitance, fast-switching diodes chosen to avoid affecting the DAC output signals.

Figure 9: Typical Connection Diagram Using an Internal or External Voltage Reference



Location	Description	Vendor Part Number
C1-C5	0.1µF ceramic Capacitor	Erie RPE112Z5U104M50V
C6	10µF Capacitor	Mallory CSR13G106KM
L1	Ferrite bead	Fair-Rite 2743001111
R1-R3	75Ω 1% Metal Film Resistor	Dale CMF-55C
RSET	147Ω 1% Metal Film resistor	Dale CMF-55C
D1-D6	Fast-switching Diodes	National 1N4148/49

Note: The above vendor numbers are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of RAMDAC.

Table 8: Absolute Maximum Ratings

Absolute Maximum Ratings and recommended operating conditions. Stresses in excess of the Absolute Maximum Ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to Absolute Maximum Ratings for extended periods can adversely affect device reliability.

Parameter	Symbol	Min	Typ	Max	Unit
V_{CC} (measured to GND)	–	–		7.0	V
Voltage on any Digital Pin	–	GND 0.5		V_{CC} + 0.5	V
Case Operating Temperature	T_C			85	°C
Storage Temperature	T_{STG}	-55		125	°C
Junction Temperature	T_J	-65		150	°C
Vapor Phase Soldering (60s)	TV_{SOL}	–		150	°C
		–		220	°C

Table 9: Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply	V_{CC}	4.75	5.00	5.25	V
Ambient Operating Temperature	T_A	0	–	70	°C
Output Load	R_L	–	37.5	–	Ω
Reference Voltage	V_{REF}	1.2	1.235	1.27	V

Table 10: DC Characteristics

Test conditions generate RS-343A video signals unless otherwise specified. The recommended operation condition for generating test signals is RSET = 147Ω, V_{REF} = 1.235V. The parameters below are applicable over full voltage and temperature ranges as shown in the Recommended Operating Conditions Table.

Parameter	Symbol	Min	Typ	Max	Unit
Digital Inputs:					
Input Voltage:					
Low	V_{IL}	GND- 0.5	–	0.8	V
High	V_{IH}	2.0	–	V_{CC} +0.5	V
Input Current					
Low (V_{IN} = 0.4V)	I_{IL}	–		-1	μA
High (V_{IN} = 2.4V)	I_{IH}	–	–	1	μA
Capacitance	C_{IN}	–	–	7	pF
(f = 1MHz, V_{IN} = 2.4V)			–		
Digital Outputs					
Output Voltage					
Low (I_{OL} = 3.2mA	VOL	–	–	0.4	V
High (I_{OH} = -400μA)	VOH	2.4	–	–	V
Three-state Current	IOZ	–	–	50	μA
Capacitance	C_{OUT}	–	–	7	pF

Table 11: DC Characteristics

Test conditions generate RS-343A video signals unless otherwise specified. The recommended operation condition for generating test signals is RSET = 147Ω, V_{REF} = 1.235V. The parameters below are applicable over full voltage and temperature ranges as shown in the Recommended Operating Conditions Table.

Parameter	Symbol	Min	Typ	Max	Unit
Resolution (each DAC)	–	8	8	8	Bits
Accuracy					
Integral Linearity Error	I_L	–	–		
(each DAC, 6-bit mode)		–	–	± 1/2	LSB
(each DAC, 8-bit mode)		–	–	± 1	
Differential Linerity Error	D_L				
(each DAC, 6-bit mode)				± 1/2	LSB
(each DAC, 8-bit mode)				±1	
Gain Error	–			± 7	%
Monotonicity	–	–	guaranteed	–	Scale
Coding	–	–	–	–	Binary
Analog Outputs					
Gray Scale Current Rangs	I_{GRAY}	–	–	20	mA
Output Current					
White Level Relative to Black	I_{WB}	16.39	17.62	18.85	mA
Black Level Relative to Blank	I_{BB}	–	–	–	
Blank Pedestal		0.95	1.44	1.90	mA
No Blank Pedestal		0	5	50	µA
Blank Level	I_{BLANK}	0	5	50	µA
LSB Size	I_{ISB}	–	–	–	
6-bit		–	279.68	–	µA
8-bit		--	69.1	–	µA
DAC to DAC Matching	–	--	2	5	%
Output Compliance	V_{OC}	-0.5	–	1.5	V
Output Impedance	R_A	–	10	–	KΩ
Output Capacitance	CA_{OUT}	–	–	30	pF
(f = 1MHz, I_{OUT} = 0 mA)					
Internal Reference Output	V_{REF}	1.2	1.235	1.27	V
$\overline{SENSE}$ Trip Level	V_{SEN}	270	340	410	mV
Power Supply Rejection Ratio	PSRR	–	–	0.5	%%V_{CC}
(COMP = 0.1F, f = 1KHz)		–	–	-6	dB

Table 12: AC Characteristics

The recommended operation condition for generating test signals is RSET = 147Ω V_{REF} = 1.235V. TTL level input values are 0V to 3V, with input rise/fall times ≤ 3ns, measured from 10% to 90k% points. Timing reference points are 50% for both inputs and outputs. Analog output load ≤ 10pF, $\overline{SENSE}$, D0-D7 output load ≤ 50pF. The parameters below are applicable over full voltage and temperature ranges as shown in the Recommended Operating Conditions Table.

Max. PCLK and Pixel Output Rates

Modes	110 MHz Part PCLK	Pixel Rate	135 MHz Part PCLK	Pixel Rate	170 MHz Part PCLK	Pixel Rate
0,1,3,12	110	110	135	135	135	135
2	55	110	67.5	135	85	170*
4,5,6,8,9	110	55	135	67.5	135	67.5
7	110	36.7	135	45	135	45
11	110	73.3	135	90	135	90

* Max with filter function enabled is 135 MHz Pixel Rate

Table 13: AC Characteristics

The recommended operation condition for generating test signals is RSET = 147Ω V_{REF} = 1.235V. TTL level input values are 0V to 3V, with input rise/fall times ≤ 3ns, measured from 10% to 90k% points. Timing reference points are 50% for both inputs and outputs. Analog output load ≤ 10pF, $\overline{SENSE}$, D0-D7 output load ≤ 50pF. The parameters below are applicable over full voltage and temperature ranges as shown in the Recommended Operating Conditions Table.

Parameter	Sym	170MHz Devices			135MHz Devices			110MHz Devices			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
DAC Performance											
AnalogOutput Delay	3	--	--	30	--	--	30	--	--	30	ns
Analog Output Rise/Fall Time	4	--	3	--	--	3	--	--	3	--	ns
Analog Output Settling Time	--	--	13	--	--	13	--	--	13	--	ns
Clock and Data Feedthrough*	--	--	-30	--	--	-30	--	--	-30	--	dB
Glitch Energy	--	--	75	--	--	75	--	--	75	--	pV-s
$\overline{SENSE}$ Output Delay	--	--	1	--	--	1	--	--	1	--	µs
PCLK Duty Cycle	--	45	-	55	45	-	55	45	--	55	%
DAC to DAC Crosstalk	--	--	-23	--	--	-23	--	--	-23	--	dB
Analog Output Skew	--	--	--	2	--	--	2	--	--	2	ns
Supply Current											
V_{CC} Supply Current**	ICC	--	TBD	TBD	--	TBD	TBD	--	TBD	TBD	mA
Sleep Current***	ISLP	--	TBD	TBD	--	TBD	TBD	--	TBD	TBD	mA

*Clock and data feed through are functions of the edge rates, overshoot, and undershoot on the digital inputs. For this test, the digital inputs have a 1KΩ resistor to ground and are driven by 74 HC logic. Settling time does not include clock and data feedthrough. Glitch impulse includes clock and data feedthrough. -3dB test bandwidth = 2XCLK rate.

**At fmax, ICC (typ) at VCC =5V ICC (max) at VCC (max)

***External voltage reference automatically disabled during powerdown. Test conditions: 25 °C to 70 °C. Pixel and data ports at 0.4V

Table 14: AC Characteristics

The recommended operation condition for generating test signals is RSET = 147Ω V_{REF} = 1.235V. TTL level input values are 0V to 3V, with input rise/fall times ≤ 3ns, measured from 10% to 90k% points. Timing reference points are 50% for both inputs and outputs. Analog output load ≤ 10pF, $\overline{SENSE}$, D0-D7 output load ≤ 50pF. The parameters below are applicable over full voltage and temperature ranges as shown in the Recommended Operating Conditions Table.

Parameter		170MHz Devices			135MHz Devices			110MHz Devices			
	Sym	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
Pixel and Control Timing											
P0-P15, MSW , $\overline{BLANK}$ Setup	5	2	--	--	2	--	--	3	--	--	ns
P0-P15, MSW, $\overline{BLANK}$ Hold	6	2	--	--	2	--	--	3	--	--	ns
Microprocessor Port											
RS0-RS1 Set-up Time	7	5	--	--	5	--	--	5	--	--	ns
RS0-RS1 Hold Time	8	5	--	--	5	--	--	5	--	--	ns
$\overline{RD}$ Asserted to D0-D7 Driven	9	2	--	--	2	--	--	2	--	--	ns
$\overline{RD}$ Asserted to D0-D7 Valid	10	--	--	30	--	--	30	--	--	30	ns
$\overline{RD}$ Negated to D0-D7 Three-stated	12	--	--	10	--	--	10	--	--	10	ns
Read D0-D7 Hold Time	11	2	--	--	2	--	--	2	--	--	ns
Write D0-D7 Setup Time	13	5	--	--	5	--	--	5	--	--	ns
Write D0-D7 Hold Time	14	5	--	--	5	--	--	5	--	--	ns
$\overline{RD}$, $\overline{WR}$ Pulse Width Low	15	50	--	--	50	--	--	50	--	--	ns
$\overline{RD}$, $\overline{WR}$ Pulse Width High	16	6	--	--	6	--	--	6	--	--	PCLK

Table 15: Pipeline Delay

Mode	Delay	Unit
0,1,2,3	6	PCLK
4,5,6	9	PCLK
7	8	PCLK
8,9	9	PCLK
11	6	PCLK
12	6	PCLK

TIMING CHARACTERISTICS

Figure 10: Basic Read Cycle

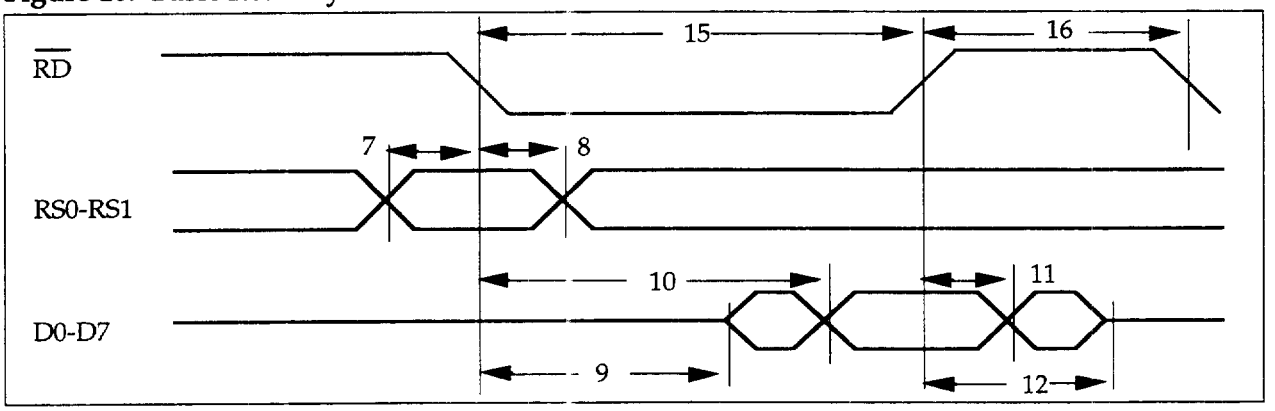


Figure 11: Basic Write Cycle

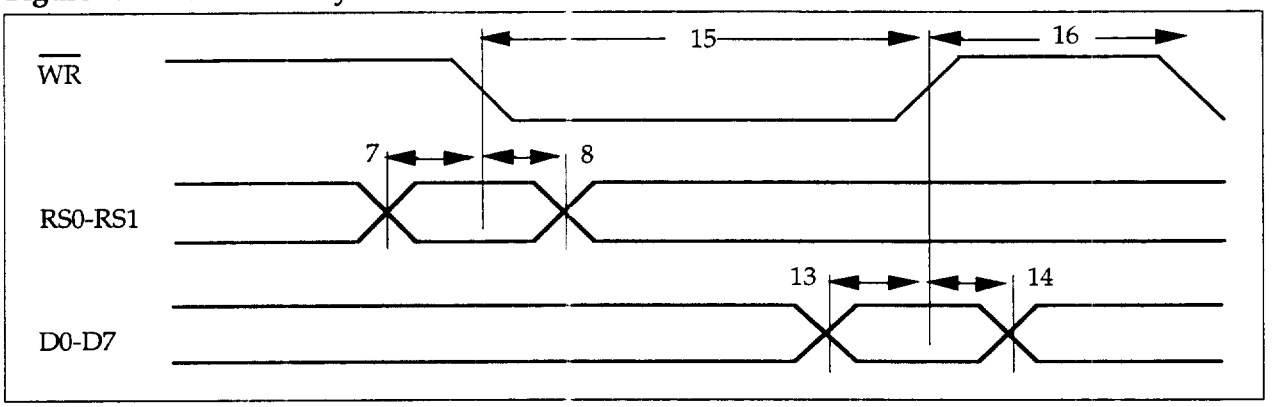


Figure 12: Pixel Input Timing

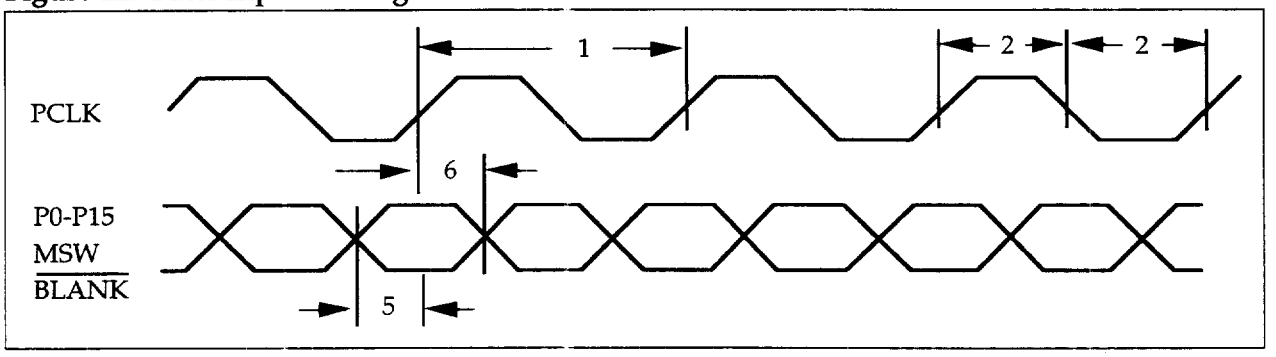
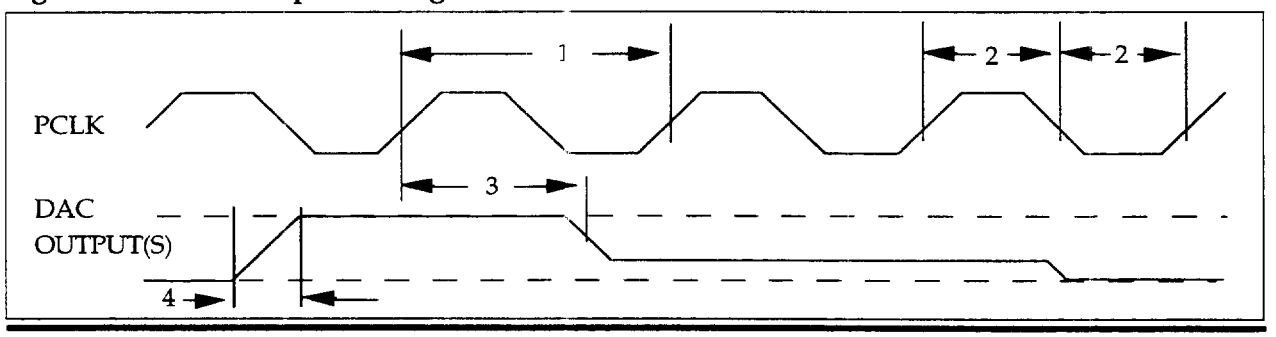
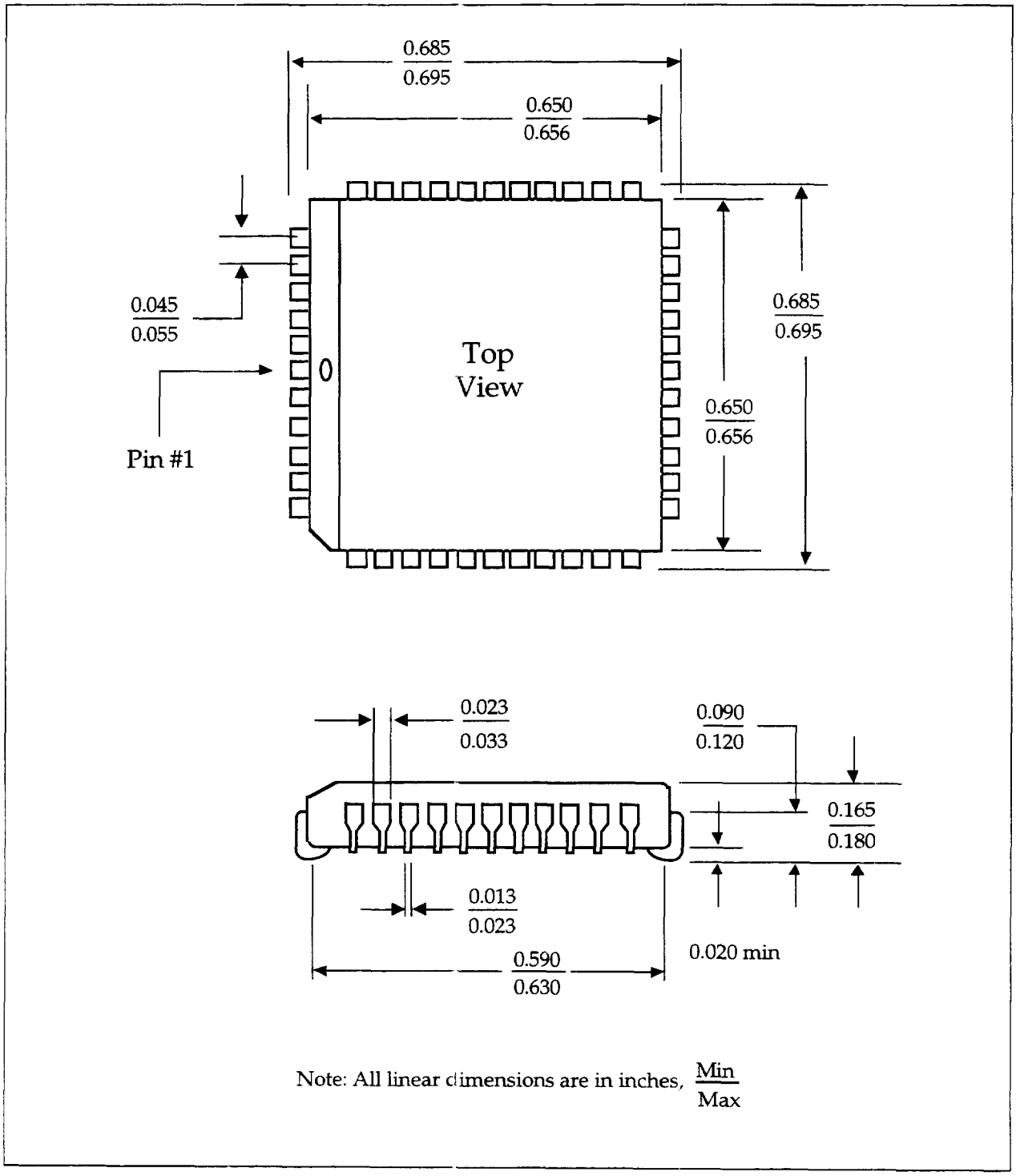


Figure 13: Video Output Timing

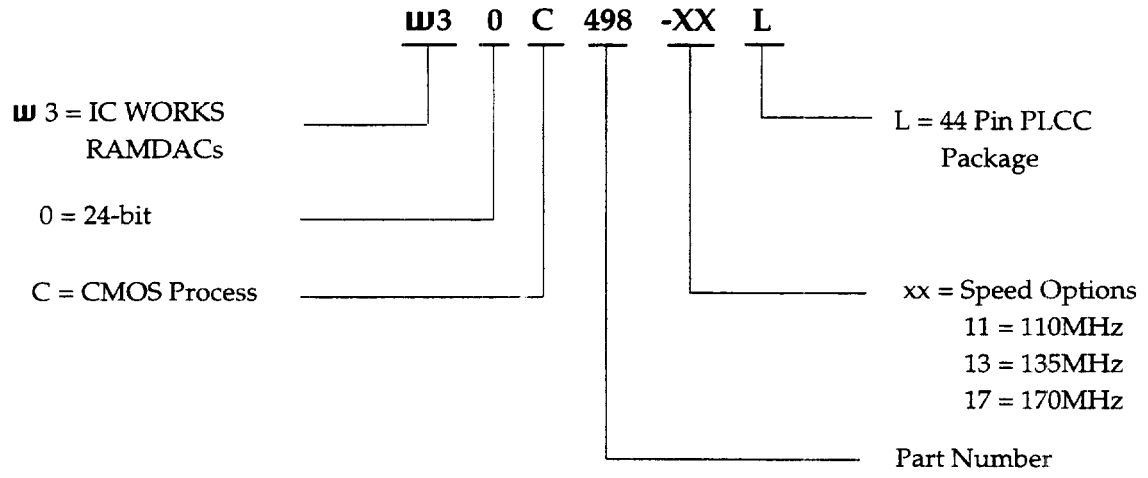


PACKAGE INFORMATION

Figure 14: 44 Pin PLCC Package



ORDERING INFORMATION



VALID PART NUMBERS

ω30C498-11L ω30C498-13L

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