HM67A4101 Series — Under development

1048576-words × 4-bits I/O Separate Clocked Random Access Memory

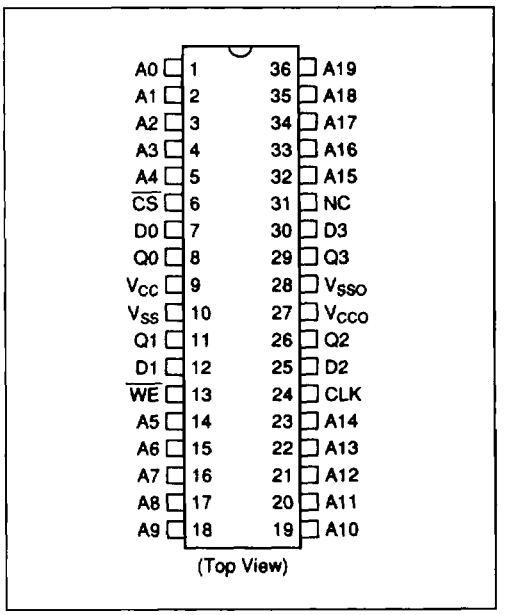
Features

- 1048576-words × 4-bits organization
- Directly TTL compatible input and output
- Choice of 5.0 V or 3.3 V power supplies for output buffers
- Completely static memory
- Access time from clock: 8 ns (max)
- Cycle time: 15 ns/18 ns (min)
- Inputs registered on chip
- Outputs registered on chip
- Revolutional pin arrangement
- 400 mil 36 pin Plastic SOJ or TSOP (II)

Ordering Informations

Type No.	Cycle time	Package
HM67A4101JP-15	15 ns	400 mil 36-pin SOJ (CP-36DB)
HM67A4101JP-18	18 ns	
HM67A4101TT-15	15 ns	400 mil 36-pin TSOP (II) (TTP-36DA)
HM67A4101TT-18	18 ns	

Pin Arrangement



(Top View)

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Note: This document contains information on a product under development.
Hitachi reserves the right to change or discontinue the product without notice.

Pin Description

Pin name	Function
A0–A19	Address input
D0–D3	Data input
Q0–Q3	Data output
$\overline{WE}$	Write enable
$\overline{CS}$	Chip select
NC	No connection
CLK	Clock input
V_{CC}	+5 V power supply
V_{CCO}	Output buffer power supply
V_{SSO}	Output buffer ground
V_{SS}	Ground