256K x 1 SRAM

SRAM MEMORY ARRAY

AVAILABLE AS MILITARY SPECIFICATIONS

- SMD 5962-88725
- SMD 5962-88544
- MIL-STD-883

FEATURES

- High Speed: 35, 45, 55, and 70
- Battery Backup: 2V data retention
- Low power standby
- High-performance, low-power, CMOS double-metal process
- Single +5V (±10%) Power Supply
- Easy memory expansion with CE\
- All inputs and outputs are TTL compatible

OPTIONS MARKING

- **Timing**

35ns access	-35
45ns access	-45
55ns access	-55*
70ns access	-70*

- **Package(s)**

Ceramic DIP (300 mil)	C	No. 106
Ceramic LCC	EC	No. 204

- **Operating Temperature Ranges**

Industrial (-40°C to +85°C)	IT
Military (-55°C to +125°C)	XT

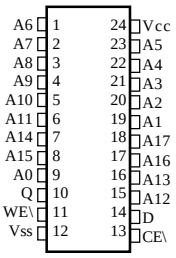
- 2V data retention/low power L

*Electrical characteristics identical to those provided for the 45ns access devices.

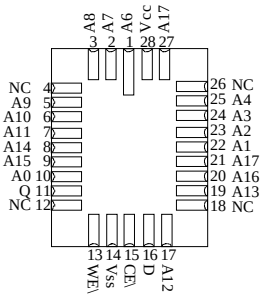
For more products and information please visit our web site at
www.austinsemiconductor.com

PIN ASSIGNMENT
(Top View)

24-Pin DIP (C)
(300 MIL)



28-Pin LCC (EC)



GENERAL DESCRIPTION

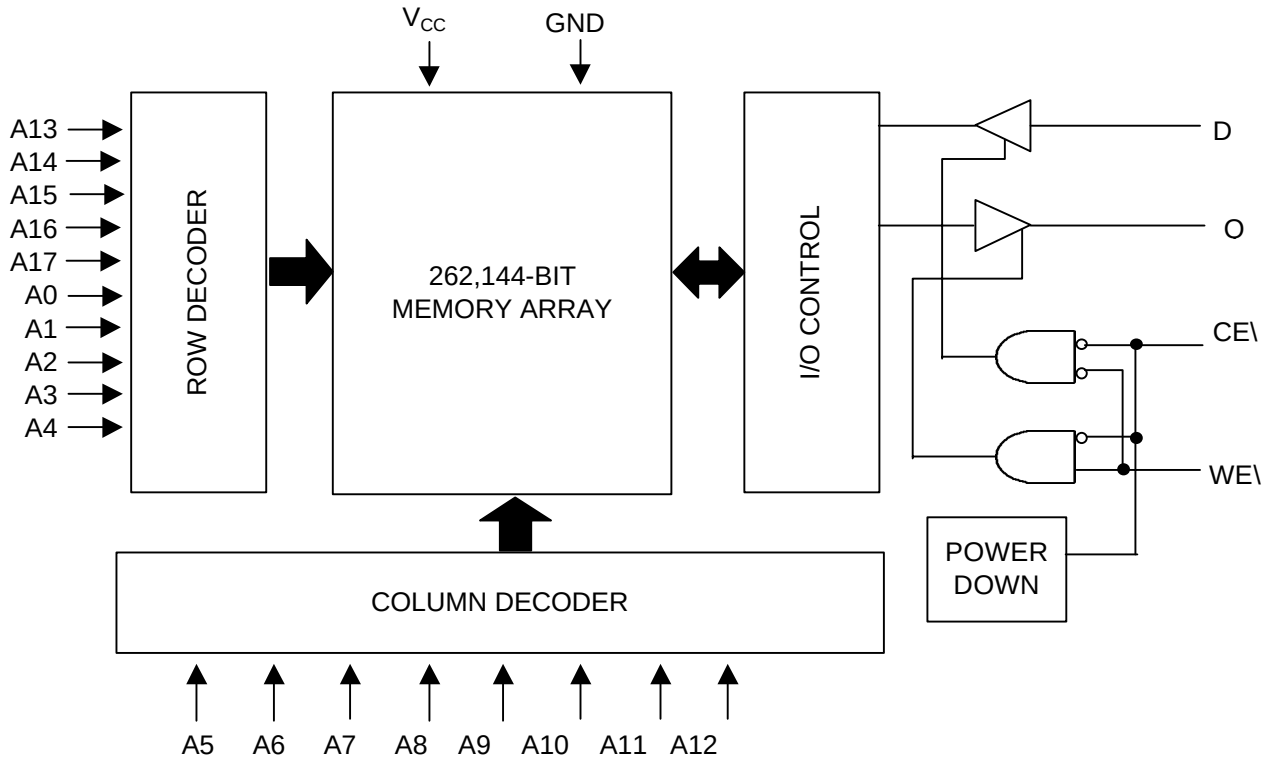
The Austin Semiconductor SRAM family employs high-speed, low-power CMOS and are fabricated using double-layer metal, double-layer polysilicon technology.

For flexibility in high-speed memory applications, Austin Semiconductor offers chip enable (CE\) on all organizations. This enhancement can place the outputs in High-Z for additional flexibility in system design. The x1 configuration features separate data input and output.

Writing to these devices is accomplished when write enable (WE\) and CE\ inputs are both LOW. Reading is accomplished when WE\ remains HIGH and CE\ goes LOW. The device offers a reduced power standby mode when disabled. This allows system designs to achieve low standby power requirements.

These devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	CE\	WE\	DQ	POWER
STANDBY	H	X	HIGH-Z	STANDBY
READ	L	H	Q	ACTIVE
WRITE	L	L	HIGH-Z	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Vss.....-0.5V to +7V
Voltage on Vcc Supply Relative to Vss.....-0.5V to +7V
Voltage Applied to Q.....-0.5V to +6V
Storage Temperature.....-65°C to +150°C
Power Dissipation.....1W
Short Circuit Output Current.....50mA
Lead Temperature (soldering 10 seconds).....+260°C
Junction Temperature.....+175°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($-55^oC \leq T_C \leq 125^oC$; $V_{CC} = 5V \pm 10\%$)

DESCRIPTION	CONDITIONS	SYM	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC}+0.5	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \leq V_{IN} \leq V_{CC}$	IL_I	-10	10	µA	
Output Leakage Current	Output(s) disabled $0V \leq V_{OUT} \leq V_{CC}$	IL_O	-10	10	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1

PARAMETER	CONDITIONS	SYM	MAX -35	MAX -45	UNITS	NOTES
Power Supply Current: Operating	$CE\backslash \leq V_{IL}$; V_{CC} = MAX, f = MAX = $1/t_{RC}$ (MIN), Output Open	I_{CCSP}	120	120	mA	3
		I_{CCLP}	100	100	mA	3
Power Supply Current: Standby	$CE\backslash \geq V_{IH}$; All Other Inputs $\leq V_{IL}$ or $\geq V_{IH}$, V_{CC} = MAX, f = 0 Hz	I_{SBT1}	25	25	mA	
	$CE\backslash \geq V_{CC}$ -0.2V; V_{CC} = MAX, $V_{IL} \leq V_{SS}$ +0.2V, $V_{IH} \geq V_{CC}$ -0.2V; f = 0 Hz	I_{SBCSP}	20	20	mA	
	"L" Version Only	I_{SBCLP}	3	3	mA	

CAPACITANCE

PARAMETER	CONDITIONS	SYM	MAX	UNITS	NOTES
Input Capacitance	$T_A = 25^oC$, f = 1MHz, Vcc = 5V	C_I	10	pF	4
Output Capacitance		C_O	12	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) ($-55^{o}C \leq T_C \leq 125^{o}C$; $V_{CC} = 5V \pm 10\%$)

DESCRIPTION	SYMBOL	-35		-45		UNITS	NOTES
		MIN	MAX	MIN	MAX		
READ CYCLE							
READ cycle time	t_{RC}	35		45		ns	
Address access time	t_{AA}		35		45	ns	
Chip Enable access time	t_{ACE}		35		45	ns	
Output hold from address change	t_{OH}	3		3		ns	
Chip Enable to output in Low-Z	t_{LZCE}	3		3		ns	7
Chip disable to output in High-Z	t_{HZCE}		20		20	ns	6, 7
Chip Enable to power-up time	t_{PU}	0		0		ns	4
Chip disable to power-down time	t_{PD}		35		45	ns	4
WRITE CYCLE							
WRITE cycle time	t_{WC}	35		45		ns	
Chip Enable to end of write	t_{CW}	30		40		ns	
Address valid to end of write	t_{AW}	30		40		ns	
Address setup time	t_{AS}	0		0		ns	
Address hold from end of write	t_{AH}	5		5		ns	
WRITE pulse width	t_{WP}	30		40		ns	
Data setup time	t_{DS}	20		20		ns	
Data hold time	t_{DH}	0		0		ns	
Write disable to output in Low-Z	t_{LZWE}	0		0		ns	7
Write Enable to output in High-Z	t_{HZWE}	0	15	0	20	ns	6, 7

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

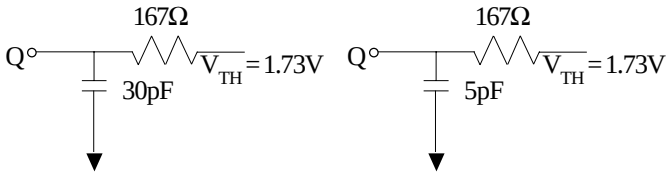


Fig. 1 Output Load Equivalent

Fig. 2 Output Load Equivalent

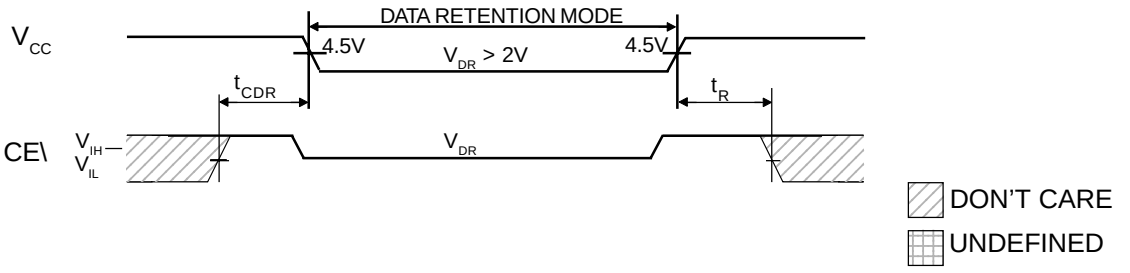
NOTES

1. All voltages referenced to V_{SS} (GND).
2. -3V for pulse width < 20ns
3. I_{CC} is dependent on output loading and cycle rates. The specified value applies with the outputs unloaded, and f = $\frac{1}{t_{RC}\ (MIN)}$ Hz.
4. This parameter is guaranteed but not tested.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. t_{LZCE}, t_{LZWE}, t_{LZOE}, t_{HZCE}, t_{HZOE} and t_{HZWE} are specified with CL = 5pF as in Fig. 2. Transition is measured ±200mV typical from steady state voltage, allowing for actual tester RC time constant.
7. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, and t_{HZWE} is less than t_{LZWE} and t_{HZOE} is less than t_{LZOE}.
8. WE\ is HIGH for READ cycle.
9. Device is continuously selected. Chip enable is held in its active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. t_{RC} = Read Cycle Time.
12. Chip enable (CE\) and write enable (WE\) can initiate and terminate a WRITE cycle.

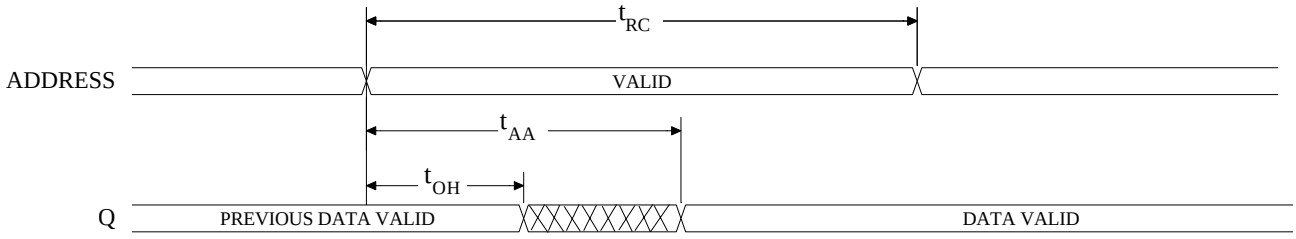
DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

DESCRIPTION	CONDITIONS		SYM	MIN	MAX	UNITS	NOTES
VCC for Retention Data			V_{DR}	2	---	V	
Data Retention Current	CE\ ≥ (V_{CC} - 0.2V) V_{IN} ≥ (V_{CC} - 0.2V) or ≤ 0.2V	V_{CC} = 2V	I_{CCDR}		900	µA	
Chip Deselect to Data Retention Time			t_{CDR}	0	---	ns	4
Operation Recovery Time			t_R	t_{RC}		ns	4, 11

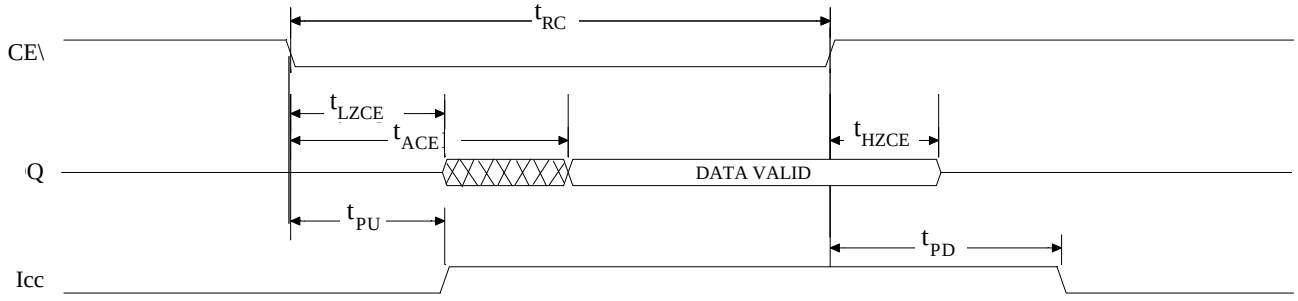
LOW Vcc DATA RETENTION WAVEFORM



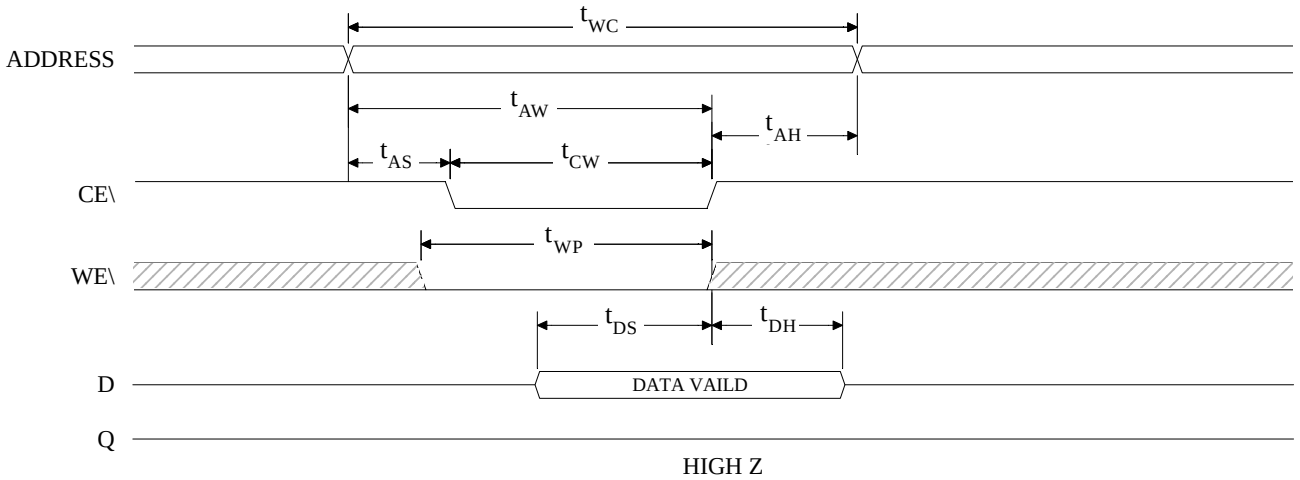
READ CYCLE NO. 1 [8, 9]



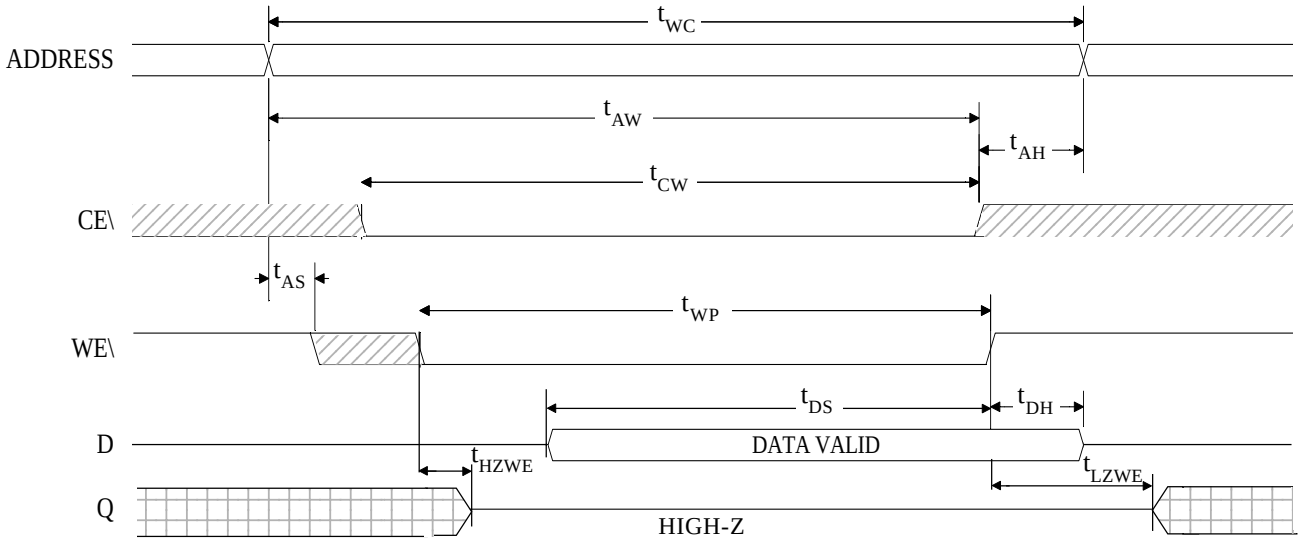
READ CYCLE NO. 2 [7, 8, 10]



WRITE CYCLE NO. 1 [12]
(Chip Enabled Controlled)



WRITE CYCLE NO. 2 [7, 12]
(Write Enabled Controlled)



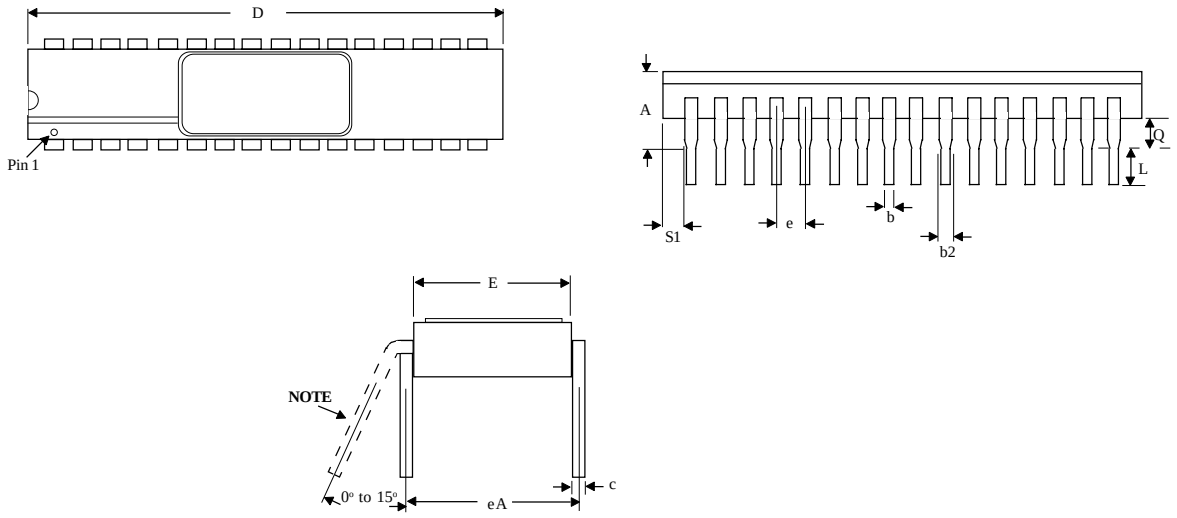
DON'T CARE

UNDEFINED

NOTE: Output enable (OE\) is inactive (HIGH).

MECHANICAL DEFINITIONS*

ASI Case #106 (Package Designator C)
SMD #5962-88544 & #5962-88725, Case Outline L



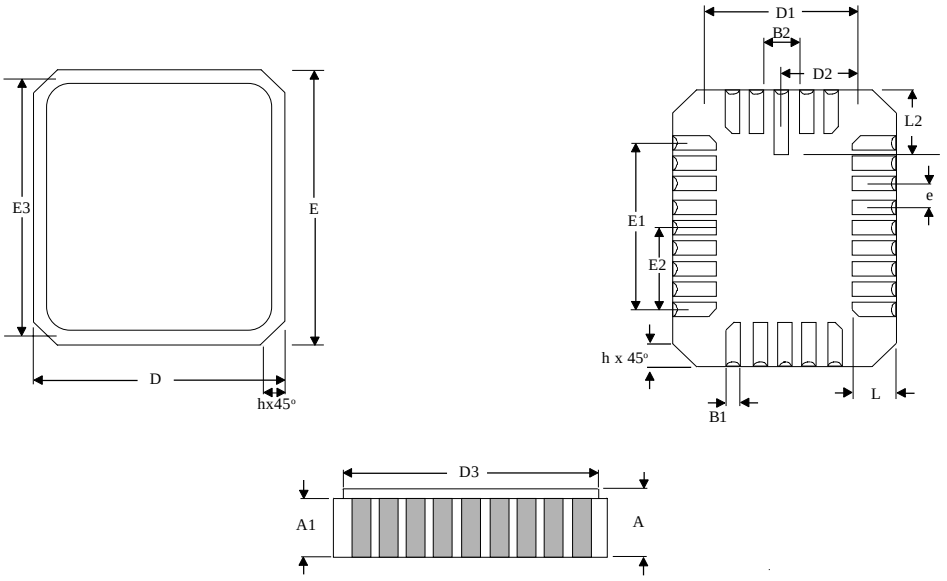
SYMBOL	SMD SPECIFICATIONS	
	MIN	MAX
A	---	0.200
b	0.014	0.026
b2	0.045	0.065
c	0.008	0.018
D	---	1.280
E	0.220	0.310
eA	0.300 BSC	
e	0.100 BSC	
L	0.125	0.200
Q	0.015	0.060
S1	0.005	---

NOTE: *These dimensions are per the SMD. ASI's package dimensional limits may differ, but they will be within the SMD limits.*

All measurements are in inches.

MECHANICAL DEFINITIONS*

ASI Case #204 (Package Designator EC)
SMD# 5962-88544, Case Outline X



SYMBOL	SMD SPECIFICATIONS	
	MIN	MAX
A	0.060	0.120
A1	0.050	0.088
B1	0.022	0.028
B2	0.072 REF	
D	0.342	0.358
D1	0.200 BSC	
D2	0.100 BSC	
D3	---	0.358
E	0.540	0.560
E1	0.400 BSC	
E2	0.200 BSC	
E3	---	0.558
e	0.050 BSC	
h	0.040 REF	
L	0.045	0.055
L2	0.075	0.095

NOTE: *These dimensions are per the SMD. ASI's package dimensional limits may differ, but they will be within the SMD limits.*

All measurements are in inches.

ORDERING INFORMATION

EXAMPLE: MT5C2561C-45L/IT

Device Number	Package Type	Speed ns	Options**	Process
MT5C2561	C	-35	L	/*
MT5C2561	C	-45	L	/*
MT5C2561	C	-55	L	/*
MT5C2561	C	-70	L	/*

EXAMPLE: MT5C2561EC-70/XT

Device Number	Package Type	Speed ns	Options**	Process
MT5C2561	EC	-35	L	/*
MT5C2561	EC	-45	L	/*
MT5C2561	EC	-55	L	/*
MT5C2561	EC	-70	L	/*

***AVAILABLE PROCESSES**

IT = Industrial Temperature Range -40°C to +85°C
XT = Extended Temperature Range -55°C to +125°C
883C = Full Military Processing -55°C to +125°C

**** OPTIONS**

L = 2V Data Retention/Low Power

ASI TO DSCC PART NUMBER CROSS REFERENCE*

ASI Package Designator C

ASI Part #	SMD Part #
MT5C2561C-35/883C	5962-8872501LX
MT5C2561C-45/883C	5962-8872502LX
MT5C2561C-55/883C	5962-8872503LX
MT5C2561C-70/883C	5962-8872504LX
MT5C2561C-35L883C	5962-8854401LX
MT5C2561C-45L883C	5962-8854402LX
MT5C2561C-55L883C	5962-8854403LX
MT5C2561C-70L883C	5962-8854404LX

ASI Package Designator EC

ASI Part #	SMD Part #
MT5C2561EC-35/883C	5962-8872501XX
MT5C2561EC-45/883C	5962-8872502XX
MT5C2561EC-55/883C	5962-8872503XX
MT5C2561EC-70/883C	5962-8872504XX
MT5C2561EC-35L883C	5962-8854401XX
MT5C2561EC-45L883C	5962-8854402XX
MT5C2561EC-55L883C	5962-8854403XX
MT5C2561EC-70L883C	5962-8854404XX

** ASI part number is for reference only. Orders received referencing the SMD part number will be processed per the SMD.*