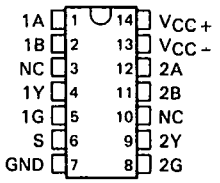
SN75207, SN75207B, SN75208, SN75208B DUAL SENSE AMPLIFIERS FOR MOS MEMORIES OR DUAL HIGH-SENSITIVITY LINE RECEIVERS

D1314, JULY 1973—REVISED SEPTEMBER 1986

T-73-51

- Plug-In Replacement for SN75107A, SN75107B, SN75108A, SN75108B with Improved Characteristics
- ±10 mV Guaranteed Input Sensitivity
- TTL Compatible
- Standard Supply Voltages . . . ±5 V
- Differential Input Common-Mode Voltage Range of ±3 V
- Strobe Inputs for Channel Selection
- '207 and '207B Have Totem-Pole Outputs
- '208 and '208B Have Open-Collector Outputs
- "B" Versions Have Diode-Protected Input Stage for Power-Off Condition
- Sense Amplifier for MOS Memories
- Dual Comparator
- High-Sensitivity Line Receiver

D, J, OR N PACKAGE
(TOP VIEW)



NC—No internal connection

FUNCTION TABLE

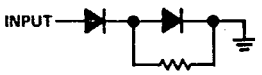
DIFFERENTIAL INPUTS A-B	STROBES G	STROBES S	OUTPUT Y
$V_{ID} \geq 10$ mV	X	X	H
-10 mV $< V_{ID} <$ 10 mV	X	L	H
	L	X	H
	H	H	Indeterminate
$V_{ID} \leq -10$ mV	X	L	H
	L	X	H
	H	H	L

H = high level, L = low level, X = irrelevant

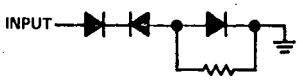
description

The SN75207, SN75207B, SN75208, and SN75208B are pin-for-pin replacements for the SN75107A, SN75107B, SN75108A, and SN75108B, respectively. The improved input sensitivity makes them more suitable for MOS memory sense amplifiers and can result in faster memory cycles. Improved sensitivity also makes them more useful in line receiver applications by allowing use of longer transmission line lengths. The '207 and '207B each features a TTL-compatible active-pull-up output. The '208 and '208B each features an open-collector output that permits wired-AND logic connections with similar output configurations.

The essential difference between the unsuffixed and "B" versions can be seen in the schematics. Input-protection diodes are in series with the collectors of the differential-input transistors of the "B" versions. These diodes are useful in certain "party-line" systems that may have multiple V_{CC+} power supplies and may be operated with some of the V_{CC+} supplies turned off. In such a system, if a supply is turned off and allowed to go to ground, the equivalent input circuit connected to that supply would be as follows:



UNSUFFIXED VERSION



"B" VERSION

This would be a problem in specific systems that might possibly have the transmission lines biased to some potential greater than 1.4 volts.

These devices are characterized for operation from 0°C to 70°C and are available in ceramic dual-in-line (J) package, plastic small outline (D) package, or plastic dual-in-line (N) package.

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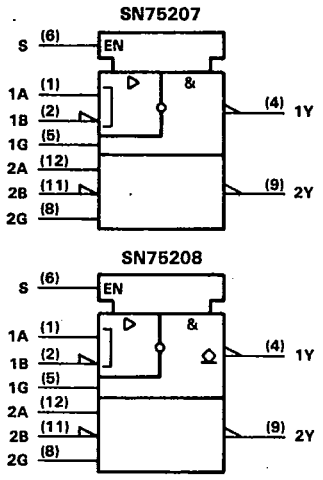
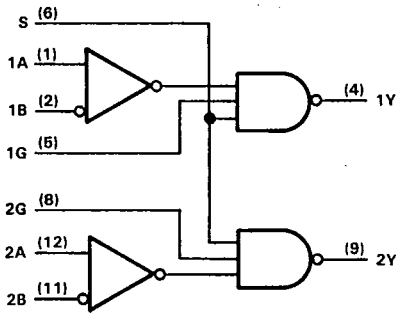
logic symbols†

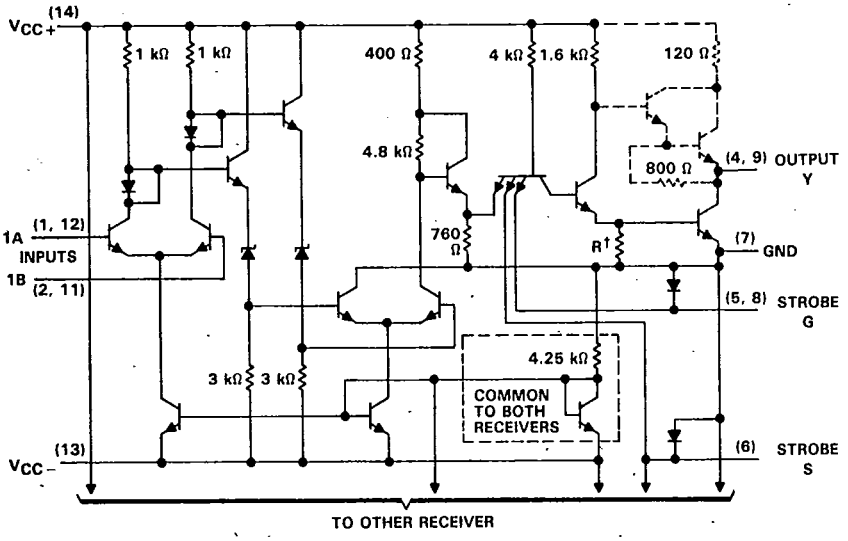


† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematic (each receiver)



† R = 1 kΩ for '207 and '207B, 750 Ω for '208 and '208B.

NOTES: A. Resistor values shown are nominal.

B. Components shown with dashed lines in the output circuitry are applicable to the '207 and '207B only. Diodes in series with the collectors of the differential input transistors are short-circuited on '207 and '208.

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design characteristics

The '207, '207B, '208, and '208B line receivers/sense amplifiers are TTL-compatible dual circuits intended for use in high-speed data-transmission systems or MOS memory systems. They are designed to detect low-level differential signals in the presence of common-mode noise and variations of temperature and supplies. Dc specifications reflect worst-case conditions of temperature, supply voltages, and input voltages.

The input common-mode voltage range is ±3 volts. This is adequate for application in most systems. In systems with requirements for greater common-mode voltage range, input attenuators may be used to decrease the noise to an acceptable level at the receiver-input terminals.

The circuits feature individual strobe inputs for each channel and a strobe input common to both channels for logic versatility. The strobe inputs are tested to guarantee 400 millivolts of dc noise margin when interfaced with Series 54/74 TTL.

The circuits feature high input impedance and low input currents, which induce very little loading on the transmission line. This makes these devices especially useful in party-line systems. The excellent input sensitivity (3 millivolts typical) is particularly important when data is to be detected at the end of a long transmission line and the amplitude of the data has deteriorated due to cable losses. The circuits are designed to detect input signals of 10 millivolts (or greater) amplitude and convert the polarity of the signal into appropriate TTL-compatible output logic levels.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1)	7 V
Supply voltage, V_{CC-}	−7 V
Differential input voltage (see Note 2)	±6 V
Common-mode input voltage (see Note 3)	±5 V
Strobe input voltage	5.5 V
Continuous total dissipation at (or below) 25°C free-air temperature: (see Note 4)	
D package	950 mW
J package	1025 mW
N package	1150 mW
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds:	
J package	300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds:	
D or N package	260°C

NOTES: 1. All voltage values, except differential voltages, are with respect to ground terminal.
2. Differential input voltage values are at the noninverting (A) terminal with respect to the inverting (B) terminal.
3. Common-mode input voltage is the average of the voltages at the A and B inputs.
4. For operation above 25°C free-air temperature, derate linearly to 608 mW at 70°C at the rate of 7.6 mW/°C for the D package, 656 mW at 70°C at the rate of 8.2 mW/°C for the J package, and 736 mW at 70°C at the rate of 9.2 mW/°C for the N package.

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recommended operating conditions (see Note 5)

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC+}	4.75	5	5.25	V
Supply voltage, V_{CC-}	−4.75	−5	−5.25	V
High-level differential input voltage V_{IDH} (see Note 6)	0.01		5	V
Low-level differential input voltage, V_{IDL}	−5†		−0.01	V
Common-mode input voltage, V_{IC} (see Notes 6 and 7)	−3†		3	V
Input voltage, any differential input to ground (see Note 6)	−5†		3	V
High-level input voltage at strobe inputs, $V_{IH(S)}$	2		5.5	V
Low-level input voltage at strobe inputs, $V_{IL(S)}$	0		0.8	V
Low-level output current, I_{OL}			−16	mA
Operating free-air temperature, T_A	0		70	°C

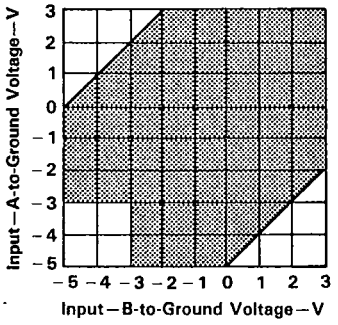
† The algebraic convention, in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

NOTES: 5. When using only one channel of the line receiver, the strobe G of the unused channel should be grounded and at least one of the differential inputs of the unused receiver should be terminated at some voltage between −3 V and 3 V.

6. The recommended combinations of input voltages fall within the shaded area of the figure shown.

7. The common-mode voltage may be as low as −4 V provided that the more positive of the two inputs is not more negative than −3 V.

RECOMMENDED COMBINATIONS OF INPUT VOLTAGES



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electrical characteristics over recommended free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		'207, '207B MIN	'207, '207B TYP†	'207, '207B MAX	'208, '208B MIN	'208, '208B TYP†	'208, '208B MAX	UNIT
I_{IH}	High-level input current	A	$V_{CC\pm}$ = ±5.25 V	V_{ID} = 5 V		30	75		30	75	µA
		B		V_{ID} = −5 V		30	75		30	75	
I_{IL}	Low-level input current	A	$V_{CC\pm}$ = ±5.25 V	V_{ID} = −5 V			−10			−10	µA
		B		V_{ID} = 5 V			−10			−10	
I_{IH}	High-level input current into 1G or 2G		$V_{CC\pm}$ = ±5.25 V, $V_{IH(S)}$ = 2.4 V				40			40	µA
			$V_{CC\pm}$ = ±5.25 V, $V_{IH(S)}$ = ±5.25 V				1			1	mA
I_{IL}	Low-level input current into 1G or 2G		$V_{CC\pm}$ = ±5.25 V, $V_{IL(S)}$ = 0.4 V				−1.6			−1.6	mA
I_{IH}	High-level input current into S		$V_{CC\pm}$ = ±5.25 V, $V_{IH(S)}$ = 2.4 V				80			80	µA
			$V_{CC\pm}$ = ±5.25 V, $V_{IH(S)}$ = ±5.25 V				2			2	mA
I_{IL}	Low-level input current into S		$V_{CC\pm}$ = ±5.25 V, $V_{IL(S)}$ = 0.4 V				−3.2			−3.2	mA
V_{OH}	High-level output voltage		$V_{CC\pm}$ = ±4.75 V, $V_{IL(S)}$ = 0.8 V, V_{IDH} = 10 mV, I_{OH} = −400 µA, V_{IC} = −3 V to 3 V		2.4						V
V_{OL}	Low-level output voltage		$V_{CC\pm}$ = ±4.75 V, $V_{IH(S)}$ = 2 V, V_{IDL} = −10 mV, I_{OL} = 16 mA, V_{IC} = −3 V to 3 V				0.4			0.4	V
I_{OH}	High-level output current		$V_{CC\pm}$ = ±4.75 V, V_{OH} = 5.25 V							250	µA
I_{OS}	Short-circuit output current‡		$V_{CC\pm}$ = ±5.25 V		−18		−70				mA
I_{CCH+}	Supply current from V_{CC+}, outputs high		$V_{CC\pm}$ = ±5.25 V, T_A = 25°C			18	30		18	30	mA
I_{CCH-}	Supply current from V_{CC-}, outputs high		$V_{CC\pm}$ = ±5.25 V, T_A = 25°C			−8.4	−15		−8.4	15	mA

† All typical values are at V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C.
‡ Not more than one output should be shorted at a time.

switching characteristics, V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	'207, '207B MIN	'207, '207B MAX	'208, '208B MIN	'208, '208B MAX	UNIT
$t_{PLH(D)}$	Propagation delay time, low-to-high-level output, from differential inputs A and B	R_L = 470 Ω, C_L = 15 pF, See Figure 1		35		35	ns
$t_{PHL(D)}$	Propagation delay time, high-to-low-level output, from differential inputs A and B			20		20	ns
$t_{PLH(S)}$	Propagation delay time, low-to-high-level output, from strobe input G or S			17		17	ns
$t_{PHL(S)}$	Propagation delay time, high-to-low-level output, from strobe input G or S			17		17	ns

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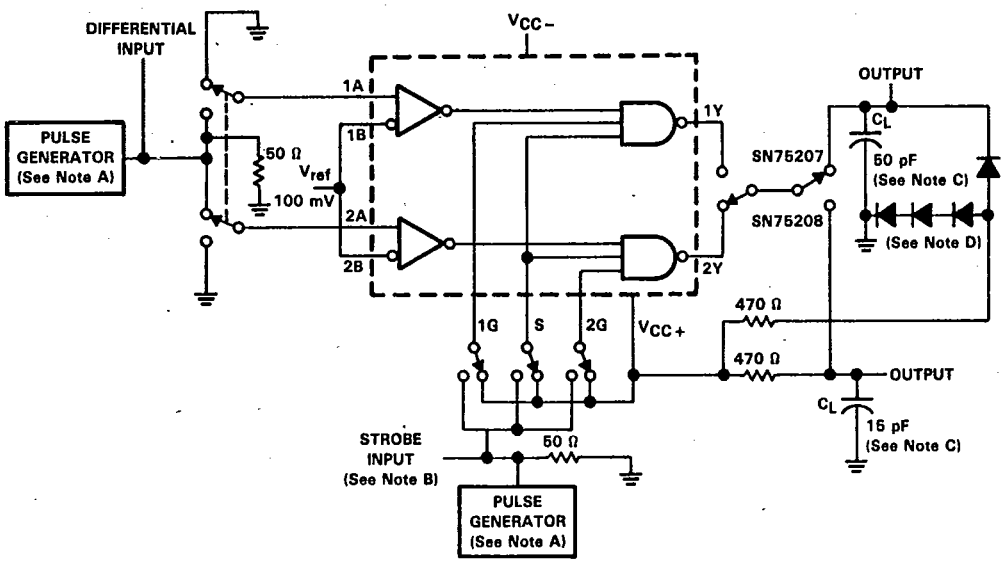
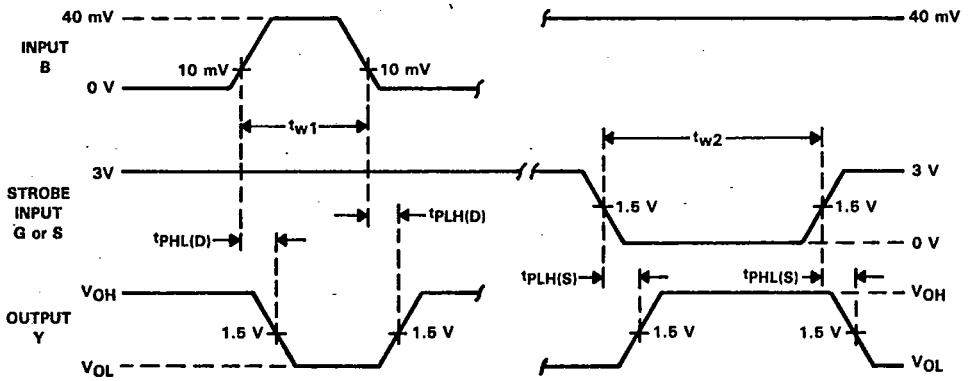
PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generators have the following characteristics: Z_{out} = 50 Ω, $t_r \leq 5$ ns, $t_f \leq 5$ ns, t_{w1} = 500 ns with PRR ≤ 1 MHz, t_{w2} = 1 μs with PRR ≤ 500 kHz.

B. Strobe input pulse is applied to Strobe 1G when inputs 1A-1B are being tested, to Strobe S when inputs 1A-1B or 2A-2B are being tested, and to Strobe 2G when inputs 2A-2B are being tested.

C. C_L includes probe and jig capacitance.

D. All diodes are 1N916.

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TYPICAL APPLICATION DATA

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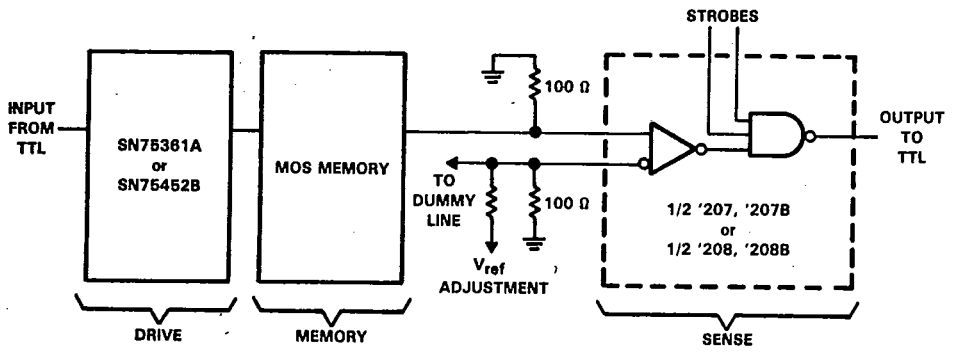
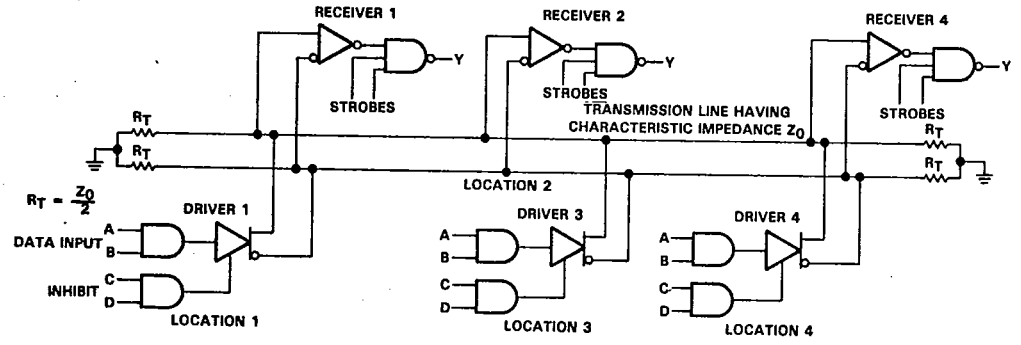


FIGURE 2. MOS MEMORY SENSE AMPLIFIER



Receivers are '207, '207B, or 208', or '208B; drivers are SN55109A, SN75109A, SN55110A, SN75110A, or SN75112.

FIGURE 3. DATA-BUS OR PARTY-LINE SYSTEM

PRECAUTIONS: When only one receiver in a package is being used, at least one of the differential inputs of the unused receiver should be terminated at some voltage between −3 volts and 3 volts, preferably at ground. Failure to do so will cause improper operation of the unit being used because of common bias circuitry for the current sources of the two receivers. Strobe G of the unused channel should be grounded.