SERIES 55460/75460 DUAL PERIPHERAL DRIVERS

BULLETIN NO. DL-S 12425, DECEMBER 1976—REVISED AUGUST 1977

PERIPHERAL DRIVERS FOR HIGH-VOLTAGE, HIGH-CURRENT DRIVER APPLICATIONS

performance

- Characterized for Use to 300 mA
- High-Voltage Outputs
- No Output Latch-Up at 30 V (After Conducting 300 mA)
- Medium-Speed Switching

ease-of-design

- Circuit Flexibility for Varied Applications and Choice of Logic Function
- TTL- or DTL-Compatible Diode-Clamped Inputs
- Standard Supply Voltages
- Available in Plastic and Ceramic Packages

SUMMARY OF SERIES 55460/75460

DEVICE	LOGIC OF COMPLETE CIRCUIT	PACKAGES
SN55460	AND†	J
SN55461	AND	JG
SN55462	NAND	JG
SN55463	OR	JG
SN55464	NOR	JG
SN75460	AND†	J, N
SN75461	AND	JG, P
SN75462	NAND	JG, P
SN75463	OR	JG, P
SN75464	NOR	JG, P

†With output transistor base connected externally to output of gate.

description

Series 55460/75460 dual peripheral drivers are functionally interchangeable with Series 55450B/75450B and Series 55460/75460 peripheral drivers, but are designed for use in systems that require higher breakdown voltages than either of those series can provide at the expense of slightly slower switching speeds. Typical applications include logic buffers, power drivers, relay drivers, lamp drivers, MOS drivers, line drivers, and memory drivers. Series 55460 drivers are characterized for operation over the full military temperature range of −55°C to 125°C; Series 75460 drivers are characterized for operation from 0°C to 70°C.

The SN55460 and SN75460 are unique general-purpose devices each featuring two standard Series 54/74 TTL gates and two uncommitted, high-current, high-voltage, n-p-n transistors. These devices offer the system designer the flexibility of tailoring the circuit to the application.

The SN55461/SN75461, SN55462/SN75462, SN55463/SN75463, and SN55464/SN75464 are dual peripheral AND, NAND, OR, and NOR drivers, respectively, (assuming positive logic) with the output of the gates internally connected to the bases of the n-p-n output transistors.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		SN55460	SN55461 SN55462 SN55463 SN55464	SN75460	SN75461 SN75462 SN75463 SN75464	UNIT
Supply voltage, V_{CC} (see Note 1)		7	7	7	7	V
Input voltage		5.5	5.5	5.5	5.5	V
Interemitter voltage (see Note 2)		5.5	5.5	5.5	5.5	V
V_{CC}-to-substrate voltage		40		40		V
Collector-to-substrate voltage		40		40		V
Collector-base voltage		40		40		V
Collector-emitter voltage (see Note 3)		40		40		V
Collector-emitter voltage (see Note 4)		25		25		V
Emitter-base voltage		5		5		V
Off-state output voltage			35		35	V
Continuous collector or output current (see Note 5)		400	400	400	400	mA
Peak collector or output current ($t_w \leq 10$ ms, duty cycle $\leq 50\%$, see Note 5)		500	500	500	500	mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 6)	J package	1375		1025		mW
	JG package		1050		825	
	N package			1150		
	P package				1000	
Operating free-air temperature range		−55 to 125	−55 to 125	0 to 70	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	−65 to 150	−65 to 150	°C
Lead temperature 1/16 inch from case for 60 seconds	J or JG package	300	300	300	300	°C
Lead temperature 1/16 inch from case for 10 seconds	N or P package	260	260	260	260	°C

NOTES: 1. Voltage values are with respect to network ground terminal unless otherwise specified.
2. This is the voltage between two emitters of a multiple emitter transistor.
3. This value applies when the base-emitter resistance (R_{BE}) is equal to or less than 500 Ω.
4. This value applies between 0 and 10 mA collector current when the base-emitter diode is open-circuited.
5. Both halves of these dual circuits may conduct rated current simultaneously; however, power dissipation averaged over a short time interval must fall within the continuous dissipation rating.
6. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in the Thermal Information Section, which starts on page 11. In the J and JG packages, SN55460 through SN55464 chips are alloy-mounted; SN75460 through SN75464 chips are glass-mounted.

recommended operating conditions (see Note 7)

	SERIES 55460			SERIES 75460			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Operating free-air temperature, T_A	−55		125	0		70	°C

NOTE 7: For SN55460 and SN75460 only, the substrate (pin 8) must always be at the most-negative device voltage for proper operation.

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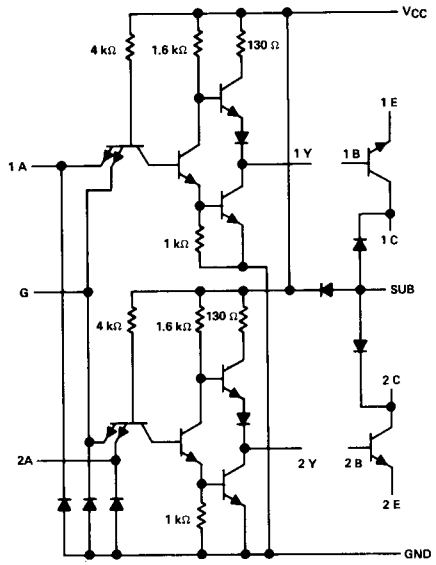
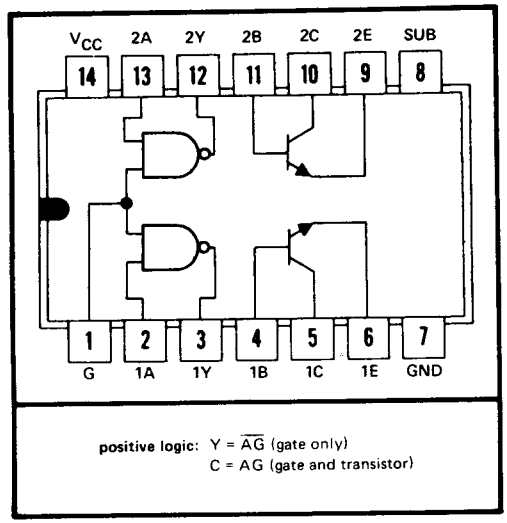
schematic



Resistor values shown are nominal.

SN55460 . . . J
SN75460 . . . J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $Y = \overline{AG}$ (gate only)
$C = AG$ (gate and transistor)

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

TTL gates

PARAMETER			TEST CONDITIONS†	SN55460 MIN	SN55460 TYP‡	SN55460 MAX	SN75460 MIN	SN75460 TYP‡	SN75460 MAX	UNIT
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = −12 mA		−1.2	−1.5		−1.2	−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = 0.8 V, I_{OH} = −400 μA	2.4	3.3		2.4	3.3		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = 16 mA		0.25	0.5		0.25	0.4	V
I_I	Input current at maximum input voltage	input A	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
		input G				2			2	
I_{IH}	High-level input current	input A	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
		input G				80			80	
I_{IL}	Low-level input current	input A	V_{CC} = MAX, V_I = 0.4 V			−1.6			−1.6	mA
		input G				−3.2			−3.2	
I_{OS}	Short-circuit output current§		V_{CC} = MAX	−18	−35	−55	−18	−35	−55	mA
I_{CCH}	Supply current, outputs high		V_{CC} = MAX, V_I = 0		2.8	4		2.8	4	mA
I_{CCL}	Supply current, outputs low		V_{CC} = MAX, V_I = 5 V		7	11		7	11	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

output transistors

PARAMETER		TEST CONDITIONS†		SN55460 MIN	SN55460 TYP‡	SN55460 MAX	SN75460 MIN	SN75460 TYP‡	SN75460 MAX	UNIT
$V_{(BR)CBO}$	Collector-Base Breakdown Voltage	I_C = 100 μA, I_E = 0		40			40			V
$V_{(BR)CEO}$	Collector-Emitter Breakdown Voltage	I_C = 10 mA, I_B = 0, See Note 8		25			25			V
$V_{(BR)CER}$	Collector-Emitter Breakdown Voltage	I_C = 100 μA, R_{BE} = 500 Ω		40			40			V
$V_{(BR)EBO}$	Emitter-Base Breakdown Voltage	I_E = 100 μA, I_C = 0		5			5			V
h_{FE}	Static Forward Current Transfer Ratio	V_{CE} = 3 V, I_C = 100 mA, T_A = 25°C	See Note 8	25			25			
		V_{CE} = 3 V, I_C = 300 mA, T_A = 25°C		30			30			
		V_{CE} = 3 V, I_C = 100 mA, T_A = MIN		10			20			
		V_{CE} = 3 V, I_C = 300 mA, T_A = MIN		15			25			
V_{BE}	Base-Emitter Voltage	I_B = 10 mA, I_C = 100 mA	See Note 8		0.85	1.2		0.85	1	V
		I_B = 30 mA, I_C = 300 mA			1	1.4		1	1.2	
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	I_B = 10 mA, I_C = 100 mA	See Note 8		0.25	0.5		0.25	0.4	V
		I_B = 30 mA, I_C = 300 mA			0.45	0.8		0.45	0.7	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 8: These parameters must be measured using pulse techniques. t_w = 300 μs, duty cycle ≤ 2%.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

TTL gates

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15 pF, R_L = 400 Ω, See Figure 1		22		ns
t_{PHL}	Propagation delay time, high-to-low-level output			8		ns

output transistors

PARAMETER		TEST CONDITIONS‡	MIN	TYP	MAX	UNIT
t_d	Delay time	I_C = 200 mA, $I_{B(1)}$ = 20 mA, $I_{B(2)}$ = −40 mA, $V_{BE(off)}$ = −1 V, C_L = 15 pF, R_L = 50 Ω, See Figure 2		10		ns
t_r	Rise time			16		ns
t_s	Storage time			23		ns
t_f	Fall time			14		ns

‡Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

gates and transistors combined

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	I_C ≈ 200 mA, C_L = 15 pF, R_L = 50 Ω, See Figure 3		45	65	ns
t_{PHL}	Propagation delay time, high-to-low-level output			35	50	ns
t_{TLH}	Transition time, low-to-high-level output			10	20	ns
t_{THL}	Transition time, high-to-low-level output			10	20	ns
V_{OH}	High-level output voltage after switching	V_S = 30 V, I_C ≈ 300 mA, R_{BE} = 500 Ω, See Figure 4	V_S−10			mV

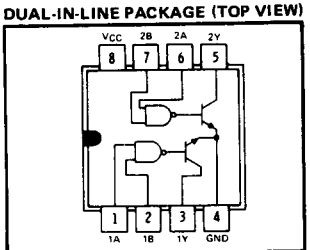
logic

FUNCTION TABLE
(EACH DRIVER)

A	B	Y
L	L	L (on state)
L	H	L (on state)
H	L	L (on state)
H	H	H (off state)

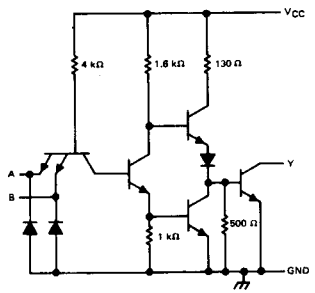
H = high level, L = low level

SN55461 . . . JG
SN75461 . . . JG OR P
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: Y = AB

schematic (each driver)



Resistor values shown are nominal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN55461 MIN	SN55461 TYP‡	SN55461 MAX	SN75461 MIN	SN75461 TYP‡	SN75461 MAX	UNIT
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA		−1.2	−1.5		−1.2	−1.5	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IH} = 2 V, V_{OH} = 35 V			300			100	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V, I_{OL} = 100 mA		0.25	0.5		0.25	0.4	V
		V_{CC} = MIN, V_{IL} = 0.8 V, I_{OL} = 300 mA		0.5	0.8		0.5	0.7	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V		−1	−1.6		−1	−1.6	mA
I_{CCH}	Supply current, outputs high	V_{CC} = MAX, V_I = 5 V		8	11		8	11	mA
I_{CCL}	Supply current, outputs low	V_{CC} = MAX, V_I = 0		56	76		56	76	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	$I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50 Ω, See Figure 3		30	55	ns
t_{PHL}	Propagation delay time, high-to-low-level output			25	40	ns
t_{TLH}	Transition time, low-to-high-level output			8	20	ns
t_{THL}	Transition time, high-to-low-level output			10	20	ns
V_{OH}	High-level output voltage after switching	V_S = 30 V, $I_O \approx$ 300 mA, See Figure 4	V_S−10			mV

TYPES SN55462, SN75462
DUAL PERIPHERAL POSITIVE-NAND DRIVERS

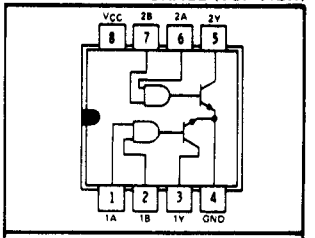
logic

FUNCTION TABLE
(EACH DRIVER)

A	B	Y
L	L	H (off state)
L	H	H (off state)
H	L	H (off state)
H	H	L (on state)

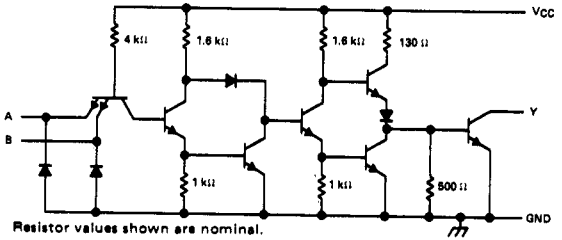
H = high level, L = low level

SN55462 . . . JG
SN75462 . . . JG OR P
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $Y = \overline{AB}$

schematic (each driver)



Resistor values shown are nominal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SN55462			SN75462			UNIT
			MIN	TYP†	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA		−1.2	−1.5		−1.2	−1.5	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IL} = 0.8 V, V_{OH} = 35 V			300			100	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = 100 mA		0.25	0.5		0.25	0.4	V
		V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = 300 mA		0.5	0.8		0.5	0.7	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V		−1.1	−1.6		−1.1	−1.6	mA
I_{CCH}	Supply current, outputs high	V_{CC} = MAX, V_I = 0 V		13	17		13	17	mA
I_{CCL}	Supply current, outputs low	V_{CC} = MAX, V_I = 5V		61	76		61	76	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	$I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50 Ω, See Figure 3		45	65	ns
t_{PHL}	Propagation delay time, high-to-low-level output			30	50	ns
t_{TLH}	Transition time, low-to-high-level output			13	25	ns
t_{THL}	Transition time, high-to-low-level output			10	20	ns
V_{OH}	High-level output voltage after switching	V_S = 30 V, $I_O \approx$ 300 mA, See Figure 4	V_S−10			mV

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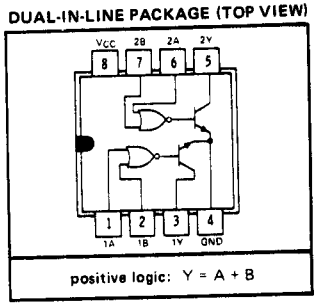
SN55463 . . . JG
SN75463 . . . JG OR P
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: Y = A + B

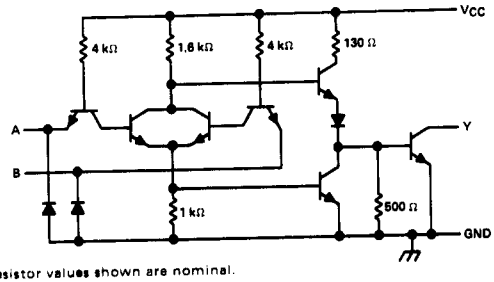
logic

FUNCTION TABLE
(EACH DRIVER)

A	B	Y
L	L	L (on state)
L	H	H (off state)
H	L	H (off state)
H	H	H (off state)

H = high level, L = low level

schematic (each driver)



Resistor values shown are nominal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN55463			SN75463			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA		−1.2	−1.5		−1.2	−1.5	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IH} = 2 V, V_{OH} = 35 V			300			100	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V, I_{OL} = 100 mA		0.25	0.5		0.25	0.4	V
		V_{CC} = MIN, V_{IL} = 0.8 V, I_{OL} = 300 mA		0.5	0.8		0.5	0.7	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V		−1	−1.6		−1	−1.6	mA
I_{CCH}	Supply current, outputs high	V_{CC} = MAX, V_I = 5 V		8	11		8	11	mA
I_{CCL}	Supply current, outputs low	V_{CC} = MAX, V_I = 0		58	76		58	76	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	I_O ≈ 200 mA, C_L = 15 pF, R_L = 50 Ω, See Figure 3		30	55	ns
t_{PHL}	Propagation delay time, high-to-low-level output			25	40	ns
t_{TLH}	Transition time, low-to-high-level output			8	25	ns
t_{THL}	Transition time, high-to-low-level output			10	25	ns
V_{OH}	High-level output voltage after switching	V_S = 30 V, I_O ≈ 300 mA, See Figure 4	V_S−10			mV

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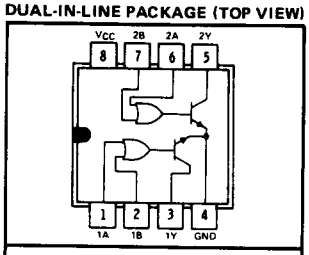
logic

FUNCTION TABLE
(EACH DRIVER)

A	B	Y
L	L	H (off state)
L	H	L (on state)
H	L	L (on state)
H	H	L (on state)

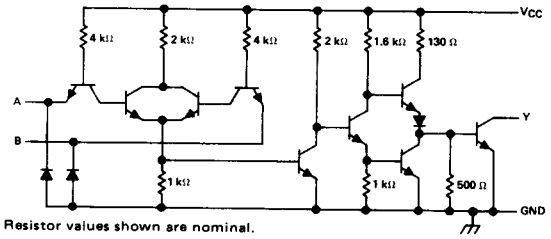
H = high level, L = low level

SN55464 . . . JG
SN75464 . . . JG OR P
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $Y = \overline{A + B}$

schematic (each driver)



Resistor values shown are nominal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN55464			SN75464			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA		−1.2	−1.5		−1.2	−1.5	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IL} = 0.8 V, V_{OH} = 25 V			300			100	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = 100 mA		0.25	0.5		0.25	0.4	V
		V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = 300 mA		0.5	0.8		0.5	0.7	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V		−1	−1.6		−1	−1.6	mA
I_{CCH}	Supply current, outputs high	V_{CC} = MAX, V_I = 0 V		14	19		14	19	mA
I_{CCL}	Supply current, outputs low	V_{CC} = MAX, V_I = 5 V		67	85		67	85	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	$I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50 Ω, See Figure 3		40	65	ns
t_{PHL}	Propagation delay time, high-to-low-level output			30	50	ns
t_{TLH}	Transition time, low-to-high-level output			8	20	ns
t_{THL}	Transition time, high-to-low-level output			10	20	ns
V_{OH}	High-level output voltage after switching	V_S = 30 V, $I_O \approx$ 300 mA, See Figure 4	V_S−10			mV

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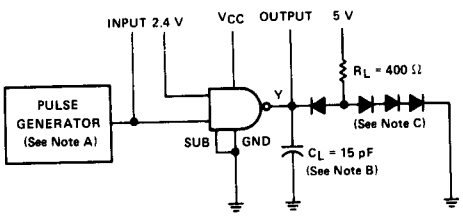
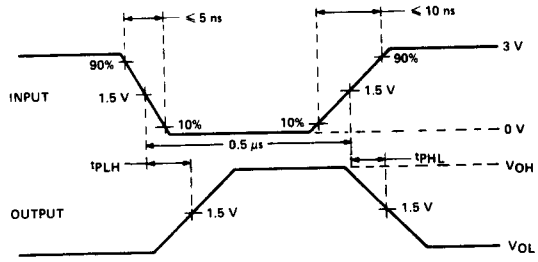
PARAMETER MEASUREMENT INFORMATION



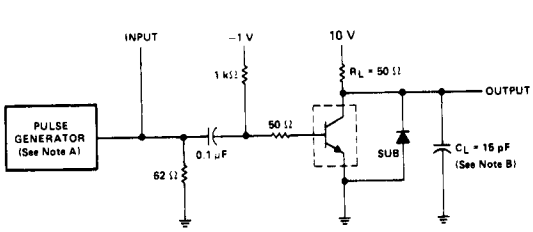
TEST CIRCUIT



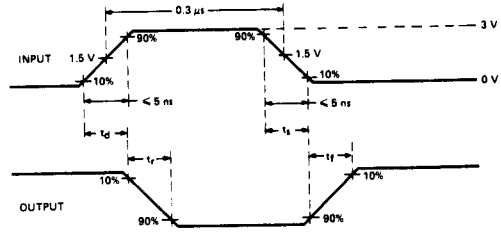
VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
B. C_L include probe and jig capacitance.
C. All diodes are 1N3064.

FIGURE 1–PROPAGATION DELAY TIMES, EACH GATE (SN55460 AND SN75460 ONLY)



TEST CIRCUIT

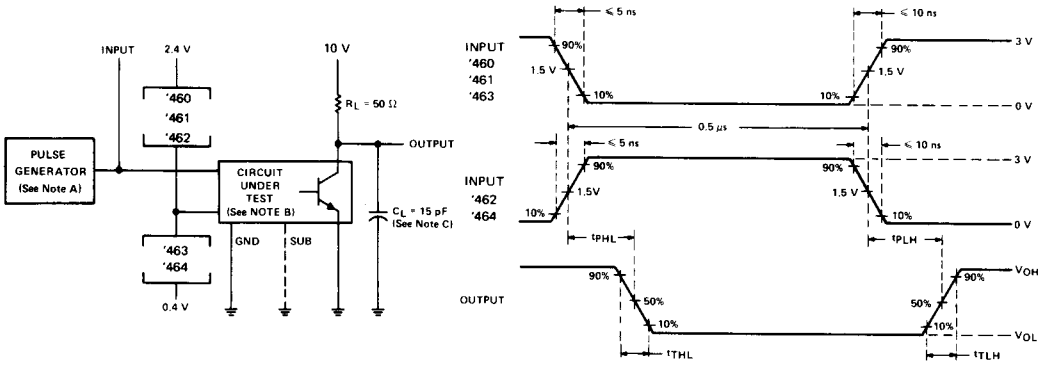


VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: duty cycle ≤ 1%, $Z_{out} \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.

FIGURE 2–SWITCHING TIMES, EACH TRANSISTOR (SN55460 AND SN75460 ONLY)

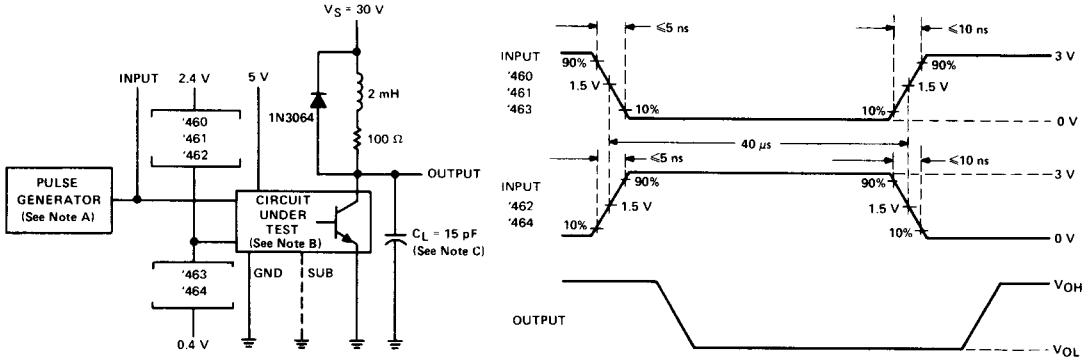
PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$
B. When testing SN55460 or SN75460, connect output Y to transistor base and ground the substrate terminal.
C. C_L includes probe and jig capacitance.

FIGURE 3–SWITCHING TIMES OF COMPLETE DRIVERS



TEST CIRCUIT VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 12.5 kHz, Z_{out} = 50 Ω.
B. When testing SN55460 or SN75460, connect output Y to transistor base with a 500-Ω resistor from there to ground, and ground the substrate terminal.
C. C_L includes probe and jig capacitance.

FIGURE 4–LATCH-UP TEST OF COMPLETE DRIVERS

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