

# MN74HC4024/MN74HC4024S

## 7-Stage Binary Counter

### ■ Outline

The MN74HC4024/MN74HC4024S is a 7-stage high speed ripple carry counter. This counter advances at the falling edge of the clock input. When the level is "H", the clear input clears the counter irrespectively of the clock input, and the levels of all the outputs (Q1~Q7) become "L".

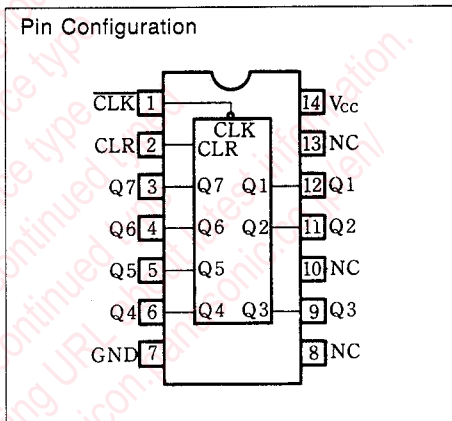
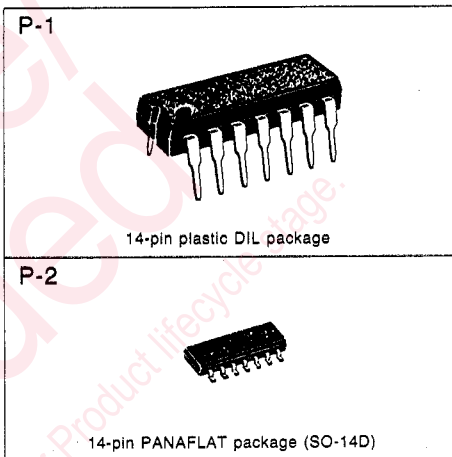
Owing to the silicon gate CMOS process, this counter has realized low power consumption and high noise immunity equivalent to those of a standard CMOS and the operation speed as high as of an LS TTL, and can directly drive ten LS TTL inputs.

To protect the input and output against electrostatic breakdown, a resistor and a diode are used for the V<sub>CC</sub> and the GND. The pin configuration and the function are the same as those of the standard CMOS logic 4000 family.

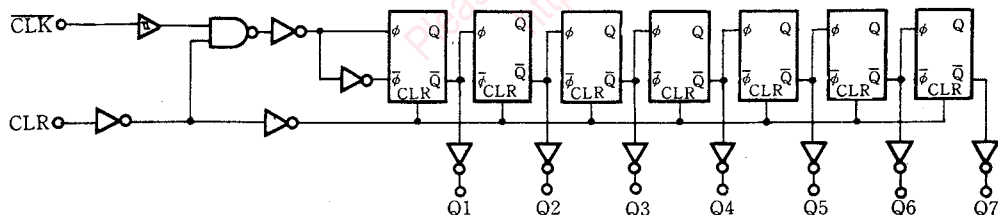
### ■ Truth Table

CLK	CLR	Mode
X	H	All Outputs are low
↔	L	No Change
↘	L	Counter Advances

Note) 1. X : "H" or "L" either will do  
 2. ↔ : Leading of clock from "L" to "H".  
 3. ↘ : Leading of clock from "H" to "L"



### ■ Logic Diagram



### ■ Absolute Maximum Ratings

Item		Symbol	Rating	Unit
Supply voltage		$V_{CC}$	-0.5~+7.0	V
Input output voltage		$V_I, V_O$	-0.5~ $V_{CC}+0.5$	V
Input protective diode current		$I_{IK}$	±20	mA
Output parasitic diode current		$I_{OK}$	±20	mA
Output current		$I_O$	±25	mA
Supply current		$I_{CC}, I_{GND}$	±50	mA
Storage temperature		$T_{stg}$	-65~+150	°C
Power dissipation	MN74HC4024	$T_a = -40 \sim +60^\circ\text{C}$	400	mW
		$T_a = +60 \sim +85^\circ\text{C}$		
	MN74HC4024S	$T_a = -40 \sim +60^\circ\text{C}$	275	
		$T_a = +60 \sim +85^\circ\text{C}$		

### ■ Recommended Operating Conditions

Item	Symbol	$V_{CC}(V)$	Rating	Unit
Operating power supply voltage	$V_{CC}$		1.4~6.0	V
Input output voltage	$V_I, V_O$		0~ $V_{CC}$	V
Operating temperature	$T_A$		-40~+85	°C
Input rise, fall time	$t_r, t_f$	2.0	0~1000	ns
		4.5	0~500	ns
		6.0	0~400	ns

### ■ DC Characteristics (GND=0V)

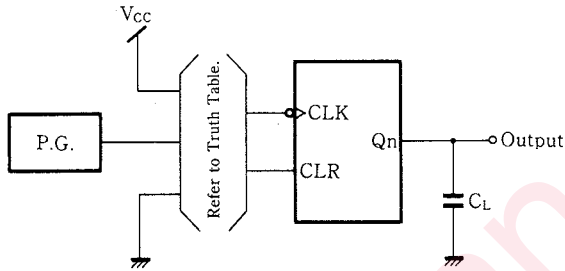
Item	Symbol	$V_{CC}$ (V)	Test Condition			Temperature				Unit	
			$V_I$	$V_O$	Unit	$T_a = 25^\circ\text{C}$			$T_a = -40 \sim +85^\circ\text{C}$		
						min.	typ.	max.	min.		max.
Input voltage high level	$V_{IH}$	2.0				1.5			1.5	V	
		4.5				3.15			3.15		
		6.0				4.2			4.2		
Input voltage low level	$V_{IL}$	2.0						0.3	0.3	V	
		4.5						0.9	0.9		
		6.0						1.2	1.2		
Output voltage high level	$V_{OH}$	2.0		-20.0	$\mu\text{A}$	1.9	2.0		1.9	V	
		4.5	$V_{IH}$	-20.0	$\mu\text{A}$	4.4	4.5		4.4		
		6.0	or	-20.0	$\mu\text{A}$	5.9	6.0		5.9		
		4.5	$V_{IL}$	-4.0	mA	3.92			3.84		
		6.0		-5.2	mA	5.48			5.34		
Output voltage low level	$V_{OL}$	2.0		20.0	$\mu\text{A}$		0.0	0.1	0.1	V	
		4.5	$V_{IH}$	20.0	$\mu\text{A}$		0.0	0.1	0.1		
		6.0	or	20.0	$\mu\text{A}$		0.0	0.1	0.1		
		4.5	$V_{IL}$	4.0	mA			0.26	0.33		
		6.0		5.2	mA			0.26	0.33		
Input leakage current	$I_I$	6.0	$V_I = V_{CC}$ or GND					±0.1	±1.0	$\mu\text{A}$	
Static supply current	$I_{CC}$	6.0	$V_I = V_{CC}$ or GND, $I_O = 0$					8.0	80.0	$\mu\text{A}$	

■ AC Characteristics (GND=0V, Input transition time $\leq$ 6ns, C<sub>L</sub>=50pF)

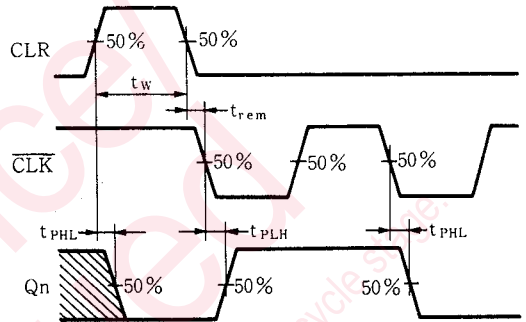
Item	Symbol	V <sub>CC</sub> (V)	Test Condition	Temperature					Unit
				Ta=25°C			Ta=-40~+85°C		
				min.	typ.	max.	min.	max.	
Output rise time	t <sub>TLH</sub>	2.0			26	75		95	ns
		4.5			8	15		19	
		6.0			7	13		16	
Output fall time	t <sub>THL</sub>	2.0			22	75		95	ns
		4.5			6	15		19	
		6.0			5	13		16	
Propagation time CLK→Q1 (L→H)	t <sub>PLH</sub>	2.0			42	150		190	ns
		4.5			16	30		38	
		6.0			13	26		33	
Propagation time CLK→Q1 (H→L)	t <sub>PHL</sub>	2.0			41	150		190	ns
		4.5			15	30		38	
		6.0			12	26		33	
Propagation time Q <sub>n</sub> →Q <sub>n+1</sub> (L→H)	t <sub>PLH</sub>	2.0			14	75		95	ns
		4.5			5	15		19	
		6.0			4	13		16	
Propagation time Q <sub>n</sub> →Q <sub>n+1</sub> (H→L)	t <sub>PHL</sub>	2.0			20	75		95	ns
		4.5			7	15		19	
		6.0			6	13		16	
Propagation time CLR→Q <sub>n</sub> (H→L)	t <sub>PHL</sub>	2.0			40	150		190	ns
		4.5			17	30		38	
		6.0			12	26		33	
Minimum pulse width CLR	t <sub>w</sub>	2.0			15	125		155	ns
		4.5			7	25		31	
		6.0			6	21		26	
Minimum recovery time	t <sub>rem</sub>	2.0			7	75		95	ns
		4.5			4	15		19	
		6.0			3	13		16	
Maximum clock frequency	f <sub>max</sub>	2.0			6	30	4		MHz
		4.5			30	70	24		
		6.0			35	80	28		

• Switching time measuring circuit and waveforms

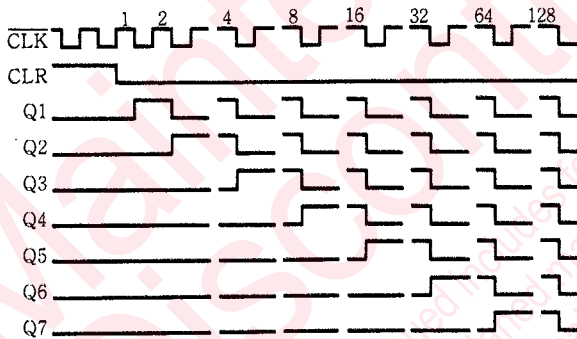
1. Measuring circuit



2. Switching waveforms



■ Typical Operating Condition



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