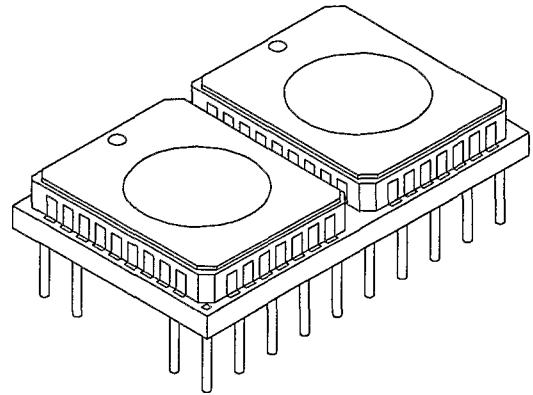


PRELIMINARY

DESCRIPTION:

The DPV32X16A is a 40-pin Pin Grid Array (PGA) consisting of two 32K X 8 UVEPROM devices in ceramic LCC packages surface mounted on a co-fired ceramic substrate with matched thermal coefficients. The LCCs are mounted in a pattern resulting in the smallest possible module outline.

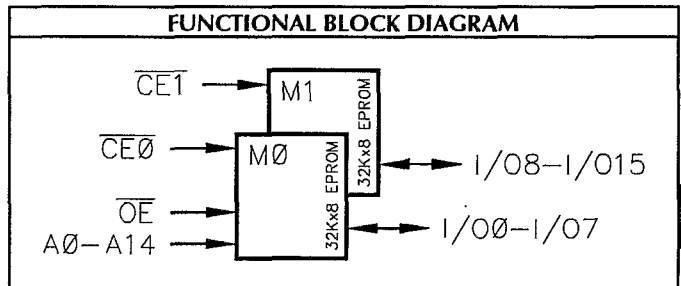
The pins have been arranged around a central 0.3" gap which can accommodate a heat rail, if desired. In this central gap is a cavity containing two 0.1µf decoupling capacitors.



FEATURES:

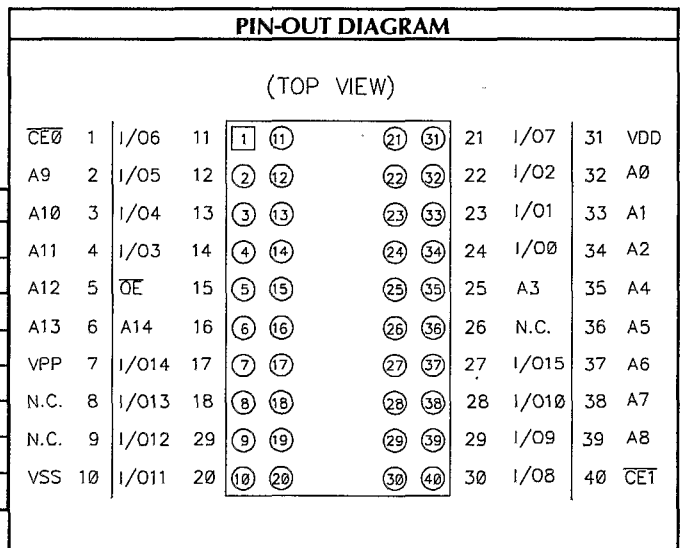
- Organizations Available:
64K X 8 or 32K X 16
- Access Times:
55*, 70, 90, 120, 150, 170, 200, 250ns
- Fully Static Operation - No clock or refresh required
- Programming Voltage 12.5 Vdc
- Simple Programming Requirements
- Three-State Outputs
- High Speed Programming Algorithm (1.0ms Pulses Typ.)
- Common Data Inputs and Outputs
- TTL-compatible Inputs and Outputs
- 40-Pin PGA (Pin Grid Array) Package

* Commercial only.



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PIN NAMES	
A0 - A14	Address Inputs
I/O0 - I/O15	Data In/Out
CE0, CE1	Chip Enables
OE	Output Enable
VDD	Power (+5V)
VSS	Ground
VPP	Programming Voltage
N.C.	No Connect



PRELIMINARY

ABSOLUTE MAXIMUM RATINGS ¹			
Symbol	Parameter	Value	Unit
T _{STG}	Storage Temperature	-65 to +125	°C
T _{BIAS}	Temperature Under Bias	-55 to +125	°C
V _{DD}	Supply Voltage ²	-0.5 to +7.0	V
V _{I/O}	Input/Output Voltage ²	-0.5 to +7.0	V
V _{PP}	Programming Voltage ²	-0.5 to +13.0	V

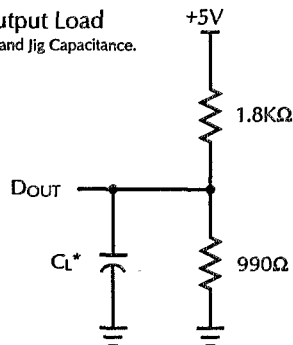
AC TEST CONDITIONS: Including Programming	
Input Pulse Levels	0V to 3.0V
Input Pulse Rise and Fall Time	≤ 20ns
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V

RECOMMENDED OPERATING RANGE ²					
Symbol	Characteristic	Min.	Typ.	Max.	Unit
V _{DD}	Supply Voltage ⁴	4.5	5.0	5.5	V
V _{IH}	Input HIGH Voltage	2.2		V _{DD} +1.0	V
V _{IL}	Input LOW Voltage	-0.2		0.8	V
V _{PP}	V _{PP} Supply Voltage ⁵	12.25	12.5	12.75	V

Output Load		
Float	C _L	Parameters Measured
1	100 pF	except t _{DF} and t _{DFP}
2	5 pF	t _{DF} and t _{DFP}

CAPACITANCE ³ : T _A = 25°C, F = 1.0MHz				
Symbol	Parameter	Max.	Unit	Condition
C _{CE}	Chip Enable	15	pF	V _{IN} = 0V
C _{ADR}	Address Input	35		
C _{OE}	Output Enable	35		
C _{I/O}	Data Input/Output	25		

Figure 1. Output Load
* Including Scope and Jig Capacitance.



DC OPERATING CHARACTERISTICS ⁶ : Over operating ranges							
Symbol	Characteristics	Test Conditions	X8		X16		Unit
			Min.	Max.	Min.	Max.	
I _{IN}	Input Leakage Current	V _{IN} = V _{DD}	-20	20	-20	20	μA
I _{OUT}	Output Leakage Current	C _E = V _{IH} , V _{IN} = V _{DD} or V _{SS}	-10	10	-20	20	μA
I _{CC}	V _{DD} Operating Current, Read	V _{IN} = V _{IH} or V _{IL} , I _{OUT} = 0mA Cycle = min. Duty = 100%	120-250ns	75	140		mA
			55-90ns	95	180		
I _{SB1}	V _{DD} Standby Current I _{OUT} = 0mA (TTL)	C _E = V _{IH} , V _{IN} = V _{IH} or V _{IL}	120-250ns	10	10		mA
			55-90ns	90	90		
I _{SB2}	V _{DD} Standby Current (CMOS)	C _E = V _{DD} ± 0.3V, I _{OUT} = 0mA V _{IN} ≥ V _{DD} - 3.0V or V _{IN} ≤ 0.3V	120-250ns	600	600		μA
			55-90ns	90	90		
I _{PP1}	V _{PP} Supply Current Programming	C _E , V _{IL} , C _{OE} = V _{IH}		30	60		mA
I _{PP3}	V _{PP} Supply Current Read ⁴	C _E , C _{OE} = V _{IL} , I _{OUT} > 0mA		400	400		μA
V _{OL}	Output LOW Voltage	I _{OUT} = 2.1mA		0.45	0.45		V
V _{OH1}	Output HIGH Voltage	I _{OUT} = -400μA	2.4		2.4		V
V _{IL}	Input LOW Level		-0.2	0.8	-0.2	0.8	V
V _{IH}	Input HIGH Level		2.2	V _{DD} +1	2.2	V _{DD} +1	V



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FUNCTIONS AND PIN CONNECTIONS						
Mode	Function	\overline{CE}	\overline{OE}	V _{PP}	V _{DD}	I/O0 - I/O15
Read Operations	Read	L	L	5V	5V	Data Out
	Output Deselect	L	H			High Impedance
	Standby	H	X			High Impedance
Program Operations (T _A = +25 ± 5°C)	Program	L	H	12.5V	6V	Data In
	Program Inhibit	H	H			High Impedance
	Program Verify	H	L			Data Out

L = LOW, H = HIGH and X = Don't Care

AC OPERATING CONDITIONS AND CHARACTERISTICS - READ: Over operating ranges											
No.	Symbol	Parameter	-55*		-70		-90		-12		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
1	t _{ACC}	Address Access Time ⁸		55		70		90		120	ns
2	t _{CE}	Chip Enable to Output Valid ⁷		55		70		90		120	ns
3	t _{OE}	Output Enable to Output Valid ^{7, 8}		30		30		35		35	ns
4	t _{DF}	\overline{OE} or \overline{CE} HIGH to Output Float ^{3, 9}	0	30	0	30	0	35	0	35	ns
5	t _{OH}	Output Hold from Address Change	0		0		0		0		ns

* Commercial only.

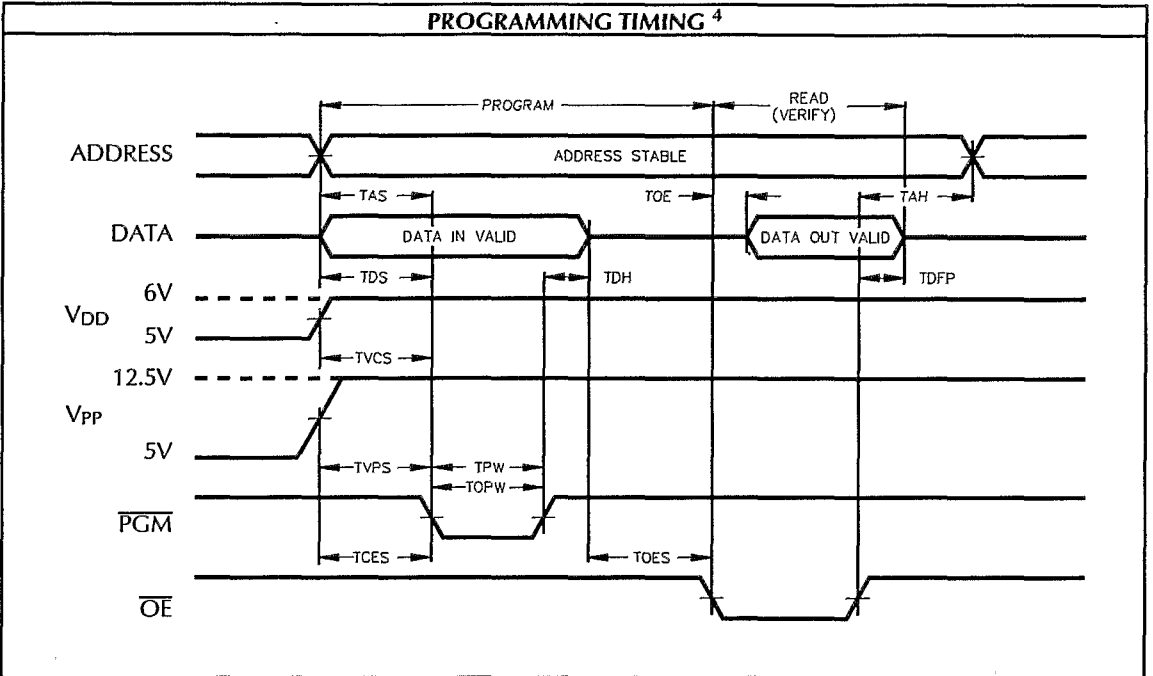
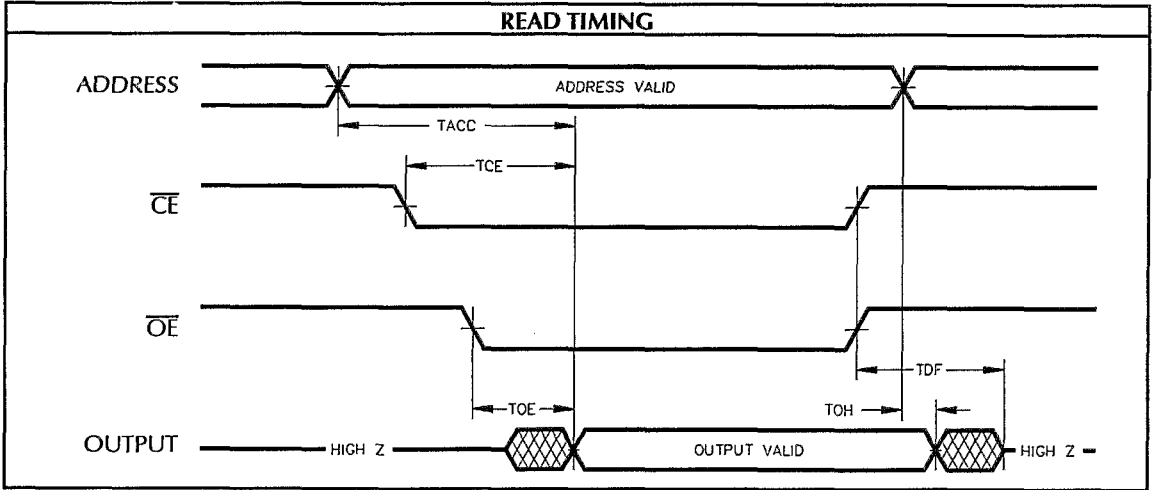
AC OPERATING CONDITIONS AND CHARACTERISTICS - READ: Over operating ranges											
No.	Symbol	Parameter	-15		-17		-20		-25		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
1	t _{ACC}	Address Access Time ⁸		150		170		200		250	ns
2	t _{CE}	Chip Enable to Output Valid ⁷		150		170		200		250	ns
3	t _{OE}	Output Enable to Output Valid ^{7, 8}		70		70		75		100	ns
4	t _{DF}	\overline{OE} or \overline{CE} HIGH to Output Float ^{3, 9}	0	50	0	50	0	55	0	60	ns
5	t _{OH}	Output Hold from Address Change	0		0		0		0		ns

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AC PROGRAMMING CONDITIONS AND CHARACTERISTICS: Over operating ranges					
No.	Symbol	Parameter	Min.	Max.	Unit
6	t _{AS}	Address Set-up Time	2		μs
7	t _{CES}	Chip Enable Set-up Time	2		μs
8	t _{OES}	Output Enable Set-up Time	2		μs
9	t _{DS}	Data Set-up Time	2		μs
10	t _{VCS}	V _{CC} Set-up Time ⁵	2		μs
11	t _{VPS}	V _{PP} Set-up Time ⁵	2		μs
12	t _{AH}	Address Hold Time	0		μs
13	t _{DH}	Data Hold Time	2		μs
14	t _{DFP}	Output Enable HIGH Output Float Delay ³	0	130	ns
15	t _{PW}	Programming Pulse Width ¹⁰	0.95	1.05	ms
16	t _{OPW}	Over Programming Pulse Width ¹¹	2.85	78.75	ms



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PROGRAMMING AND ERASING INFORMATION

Programming

Upon delivery from Dense-Pac, or after erasure (See *Erasure section*), the DPV32X16A contains "1's" in every location, and read data is in the high state. "0's" are written into the DPV32X16A through the procedure of programming. A 0.1 μ F capacitor between V_{PP} and V_{SS} is required to prevent excessive voltage transients during programming which could damage the device. Programming modes require +6.0V and +12.5V to be applied to V_{DD} and V_{PP} respectively.

Individual bytes or address locations can be selected and programmed by using the programming algorithm shown in Figure 2. In the programming mode, \overline{CE} is set at V_{IL} , \overline{OE} is set at V_{IH} , V_{DD} is set at +6.0V, and V_{PP} is set at +12.5V. After the applied address and input data signals are stable, programming is accomplished by a 1.0ms V_{IL} pulse on the \overline{CE} pin (refer to the *Programming Timing Diagram*).

The programmed byte is then verified. If the programming was successful, then a 3ms over program pulse is applied. If the programming was unsuccessful after the first 1ms pulse, then up to 25 1ms pulses are applied with a verification after each pulse. When the byte passes, an over program pulse of 3ms times the number of initial programming pulses (78.75ms max.) is applied.

If the device fails to program after 25 attempts, the programming is considered failed. After the first byte is programmed, continue the algorithm through all the required addresses. Then lower V_{DD} and V_{PP} to +5.0Vdc and compare the data programmed with the original data to determine if the device passes. A programming adapter for programming on standard EPROM programmers is available, contact Dense-Pac sales for more information.

Erasure

To clear all locations of their programmed contents it is necessary to expose the DPV32X16A to an ultraviolet light source. A dosage of 15W-seconds/cm² is required to completely erase a DPV32X16A. This dosage can be obtained by exposure to an ultraviolet lamp [wavelength of 2537 Angstroms (Å) with an intensity of 12,000 μ W/cm²] for 21 minutes.

The DPV32X16A and similar devices can be erased by light sources having wavelengths shorter than 4000Å. Although erasure time will be much longer than with UV sources at 2537Å, nevertheless the exposure to fluorescent light or sunlight will eventually erase the DPV32X16A. After programming, the package windows should be covered by an opaque label or substance, to prevent inadvertent erasure.

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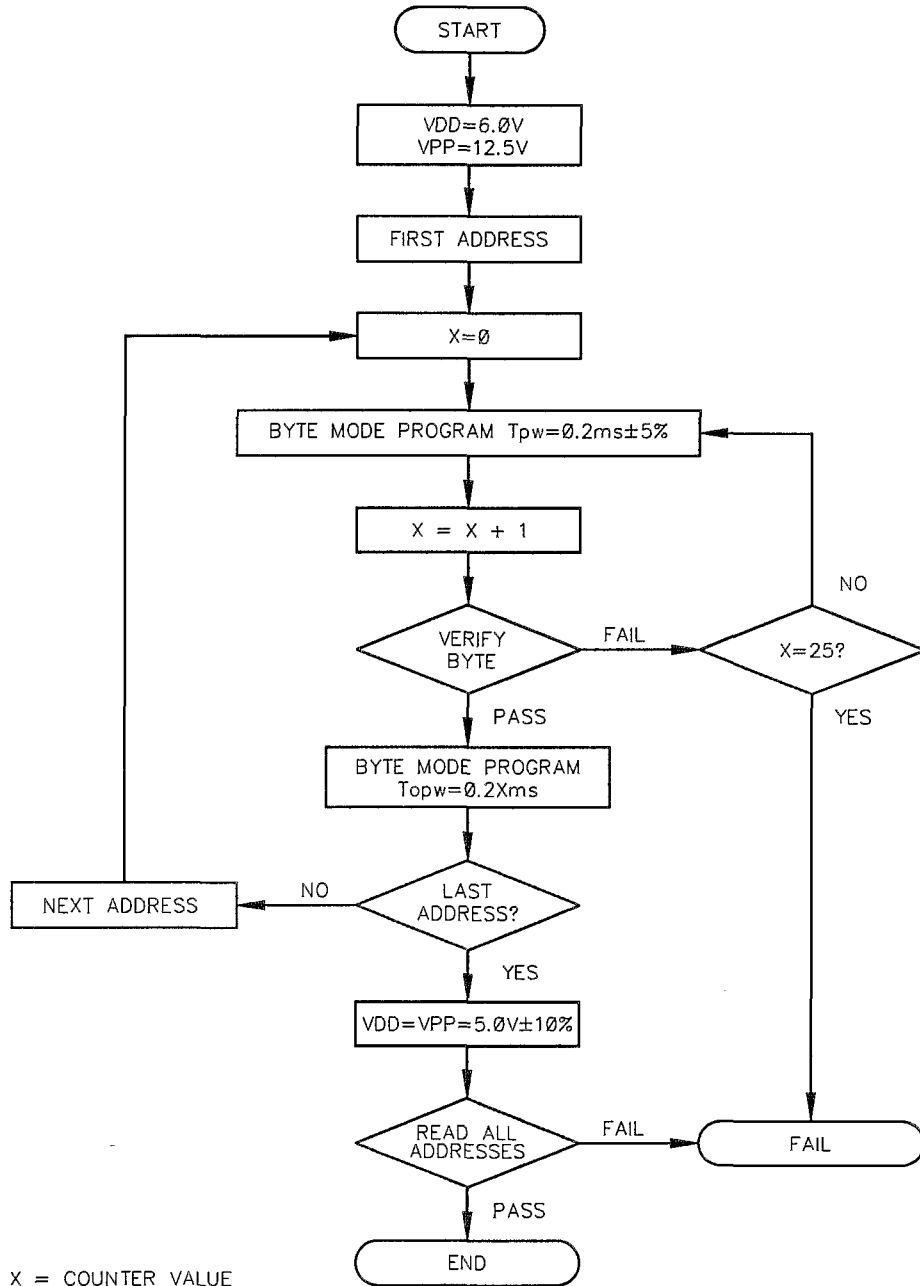
NOTES:

1. Stresses greater than those listed under **ABSOLUTE MAXIMUM RATINGS** may cause permanent damage to the device. This is stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. All voltages are with respect to V_{SS} .
3. This parameter is guaranteed and not 100% tested.
4. V_{DD} must be applied either coincident with or before V_{PP} and removed either coincident with or after V_{PP} .
5. V_{PP} must not be greater than 13.0V including overshoot. Permanent device damage may occur if the device is taken out or put into socket with $V_{PP} = 13.0V$. Also, during $\overline{CE} = V_{IL}$, V_{PP} must not be switched from 5.0V to 13.0V or vice-versa.
6. $t_A = -55^\circ C$ to $+125^\circ C$, $V_{DD} = 5.0V \pm 0.5V$, and $V_{PP} = V_{DD}$ reading. $t_A = +25^\circ C \pm 5^\circ C$, $V_{DD} = 6.0 \pm 0.25V$, $V_{PP} = 12.5V \pm 0.3V$ programming.
7. \overline{OE} may be delayed up to $t_{CE} - t_{OE}$ after the following edge of \overline{CE} without impact on t_{CE} .
8. \overline{OE} may be delayed up to $t_{ACC} - t_{OE}$ after the following Address is valid without impact on t_{ACC} .
9. T_{DF} is specified from \overline{OE} or \overline{CE} , whichever occurs first.
10. Initial Program Pulse Width Tolerance is 1ms \pm 5%.
11. The length of the overprogram pulse may vary from 2.85ms to 78.75ms as a function of the iteration counter value X.



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Figure 2. Programming Flow Chart



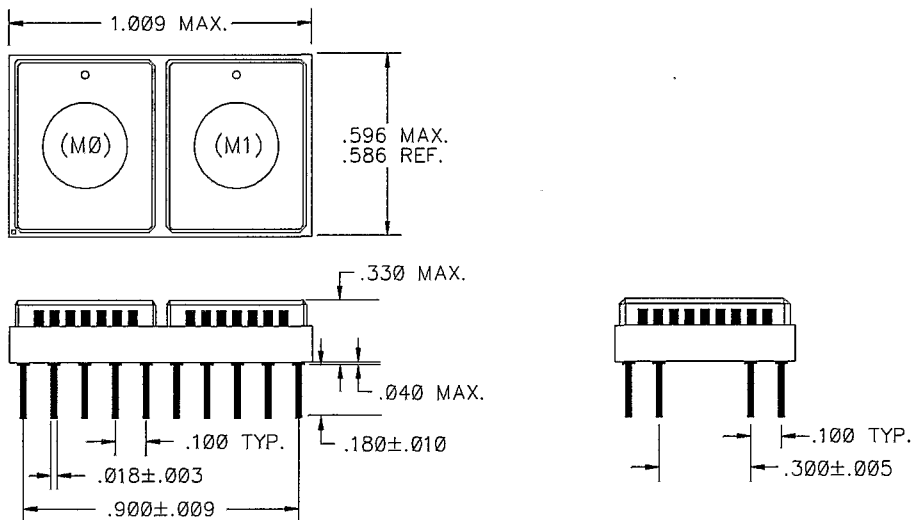
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ORDERING INFORMATION

DP	V32X16	A	-	XX	X	
PREFIX	DEVICE TYPE	PACKAGE		SPEED	GRADE	
						C COMMERCIAL 0°C to +70°C
						I INDUSTRIAL -40°C to +85°C
						M MILITARY -55°C to +125°C
						B* MIL-PROCESSED -55°C to +125°C
						55 55ns (COMMERCIAL ONLY)
						70 70ns
						90 90ns
						12 120ns
						15 150ns
						17 170ns
						20 200ns
						25 250ns
						A 40-PIN PGA MODULE
						UVEPROM 64KX8 OR 32KX16

* B grade modules are constructed with 883 devices.

MECHANICAL DIAGRAMS



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