MX·COM, INC. MiXed Signal ICs

DATA BULLETIN

MX802 DVSR CODEC

Features

- **DVSR (Data/Voice Storage and Retrieval) Codec**
- **CVSD Codec Encoder and Decoder**
- **Control and Timing Circuitry for 4Mbits of external DRAM**
- **Low Power Operation**
- **Member of DBS800 Family (C-BUS Compatible)**

Applications

- **Answering Machines where an incoming speech message is stored for later recall**
- **Busy Buffering, in which an outgoing speech message is stored temporarily**
- **Automatic transmission of pre-recorded alarm or status messages.**
- **Time Domain Scrambling of Speech messages**
- **VOX control of transmitter functions**
- **Temporary Data Storage, such as buffering of over-air data transmissions**
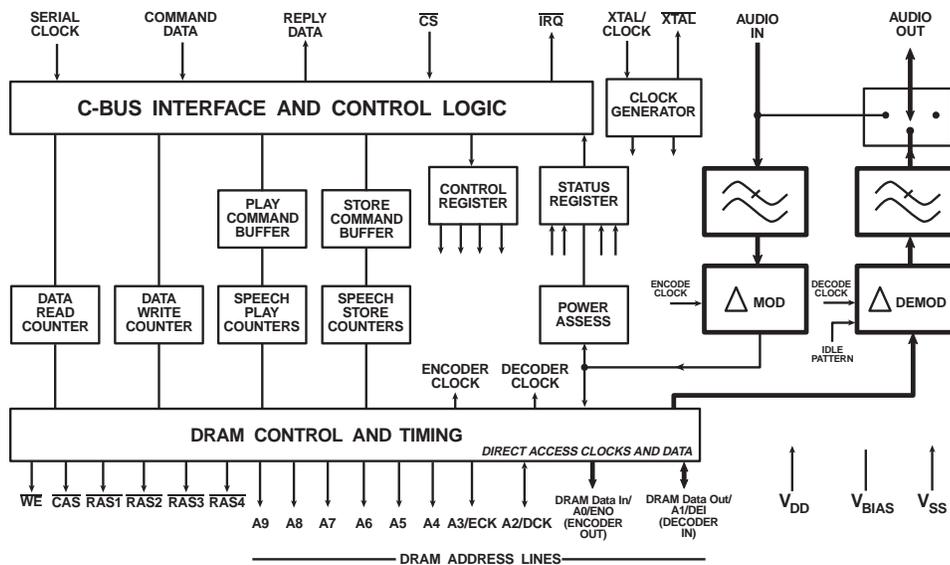
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When used with external DRAM, theMX802 had four primary functions: Speech Storage, Speech layback, Data Storage, and Data Retrieval. The Speech Storage and Playback may be performed concurrently with data storage or retrieval.

On-chip the Delta Codec is supported by input and output analog switched-capacitor filters and audio output switching circuitry. The DRAM control and timing circuitry provides all the necessary address, control, and refresh signals to interface to external DRAM.

The MX802 may also be used without DRAM (as a "stand alone" CVSD Codec), in which case direct access is provided to the CVSD Codec digital data and clock signals. All signals are controlled by "C-BUS" commands from the system microcontroller.

The MX802 may be used with a 5.0V power supply and is available in the following packages:
24-pin PLCC (MX802LH), 28-pin PLCC (MX802LH8), and 28-pin PDIP (MX802P).

Contents

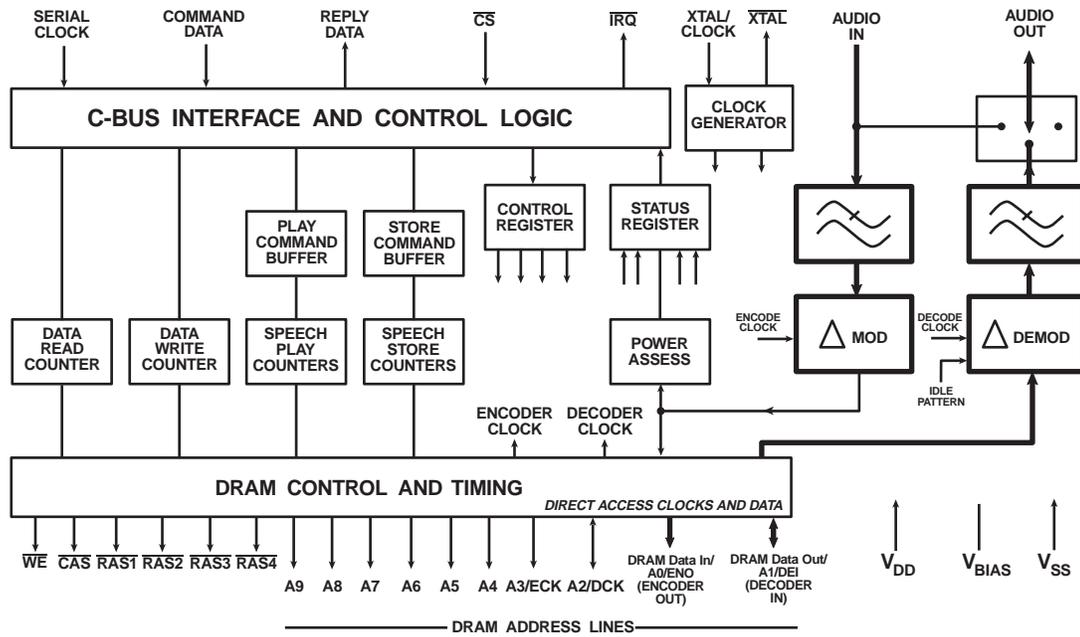MXCOM, Inc. reserves the right to change specifications at any time without notice.

1 Block Diagram

Figure 1: Block Diagram

2   Signal List

J/LH8	LH	Signal	Description
1		$\overline{RAS2}$	$\overline{Row\ Address\ Strobe\ 2}$ This pin should be connected to the Row Address Strobe input of the second 1Mbit DRAM chip (if used).
2	1	$\overline{RAS1}$	$\overline{Row\ Address\ Strobe\ 1}$ This pin should be connected to the Row Address Strobe input of the first DRAM chip.
3	2	$\overline{Write\ Enable}$	($\overline{WE}$) The DRAM of Read/Write control pin.
4		$\overline{Xtal}$	This is the output of the 4.0MHz on –chip clock oscillator. External components are required at the output when a Xtal is used. A Xtal cannot be used with the 24-pin version.
5	3	Xtal/Clock	This is the input to the on-chip clock oscillator inverter. A 4.0MHz Xtal or externally derived clock should be connected here. See Figure 2. This clock provides timing for on-chip elements, filters, etc. A Xtal cannot be used with the 24-pin version. Various Xtal frequencies can be used with this device. See Table 5 for Sampling Rate Variations.
6	4	$\overline{IRQ}$	$\overline{Interrupt\ Request}$ The output of this pin indicates an interrupt condition to the microcontroller by going to logic'0'. This 'wire-or able' output, enabling the connection of up to 8 peripherals to 1 interrupt port on the microcontroller. This pin is an open drain output. It therefore has a low impedance pulldown to logic '0' when active and a high impedance when inactive. Conditions indicated by this function are Power Reading Ready, Play Command Complete, and Store Command Complete.
7	5	Serial Clock	This is the C-BUS serial clock input. This clock, produced by the microcontroller, is used to transfer timing commands and data to and from the DVSR Codec. See timing diagrams. Clock requirements vary for different MX802 functions.
8	6	Command Data	This is the C-BUS serial data input from the microcontroller. Data is loaded to this device in 8-bit bytes, MSB (bit 7) first, and LSB (bit 0) last, synchronized to the Serial clock. See Timing diagrams.
9	7	$\overline{CS}$	$\overline{Chip\ Select}$: The C-BUS data transfer control function, this input is provided by the microcontroller. Command Data transfer sequences are initiated, completed, or aborted by the $\overline{CS}$ signal. See Timing Diagrams.
10	8	Reply Data	This is the C-BUS serial data output to the microcontroller. The transmission of Reply Data bytes is synchronized to the Serial Data Clock under the control of the Chip Select input. This 3-state output s held at high impedance when not sending data to the microcontroller. See Timing diagrams.
11	9	V_{BIAS}	This is the output of the on-chip analog circuitry bias system, held internally at $V_{DD}/2$. This pin should be decoupled to V_{SS} by capacitor C1. See Figure 2.
12	10	Audio Out	This is the Analog signal out.
13	11	Audio In	This is the audio (speech) input. The signal to this pin must be AC coupled by capacitor C4 and decoupled to V_{SS} by HF capacitor C6. For optimum noise performance this input should be driven from a source impedance of less than 100Ω.
14	12	V_{SS}	Negative Supply (GND)
15	13	Encoder Out (ENO)	DRAM Data In/A0/Direct Access -- This is connected to the DRAM data input and address line A0. With no DRAM used, this output is available in a Direct Access mode as the Delta Encoder digital data Output. Direct Access control is achieved by Control Register byte 1, bit 7.

J/LH8	LH	Signal	Description
16	14	Decoder In (DEI)	DRAM Data Out/A1/Direct Access --: This is connected to the DRAM data output and address line A1. With no DRAM used, this pin is available in a Direct Access mode as the Delta Decoder Clock input. Direct Access control is achieved by Control Register byte 1, bit 6.
17	15	Decoder Clock (DCK):	DRAM A2/Direct Access -- This is the DRAM address line A2. With no DRAM employed, this pin is available in a Direct Access mode as the Delta Decoder Clock Input. Direct Access control is achieved by Control Register byte 1, bit 6.
18	16	Encoder Clock (ECK)	DRAM A3/Direct Access: This is the DRAM address line A3. With no DRAM employed, this pin is available in a Direct Access mode as the Delta Encoder Clock Output. Direct Access control is achieved by Control Register byte1, bit 6.
19	17	DRAM A4	DRAM address line 4.
20	18	DRAM A5	DRAM address line 5.
21	19	DRAM A6	DRAM address line 6.
22	20	DRAM A7	DRAM address line 7.
23	21	DRAM A8	DRAM address line 8.
24		$\overline{RAS4}$	$\overline{\text{Row Address Strobe } 4}$: This pin should be connected to the Row Address Strobe input of the fourth 1Mbit DRAM chip (if used).
25		$\overline{RAS3}$	$\overline{\text{Row Address Strobe } 3}$: This pin should be connected to the Row Address Strobe input of the third 1Mbit DRAM chip (if used).
26	22	DRAM A9	This is DRAM address line A9. This pin is not connected when a 256kbit DRAM is used. Note: To simplify PCB layout, the DRAM address inputs A0-A8 may be connected in any physical order to the DVSR Codec output pins A0-A8.
27	23	$\overline{CAS}$	$\overline{\text{Column Address Strobe}}$: This is the DRAM Column Address Strobe pin. It should be connected to the $\overline{CAS}$ pins of all DRAM chips.
28	24	V_{DD}	Positive supply. A single, stable +5 volt supply is required. Levels and voltages within the DVSR Codec are dependent upon this supply.

Table 1: Signal List

3   External Components
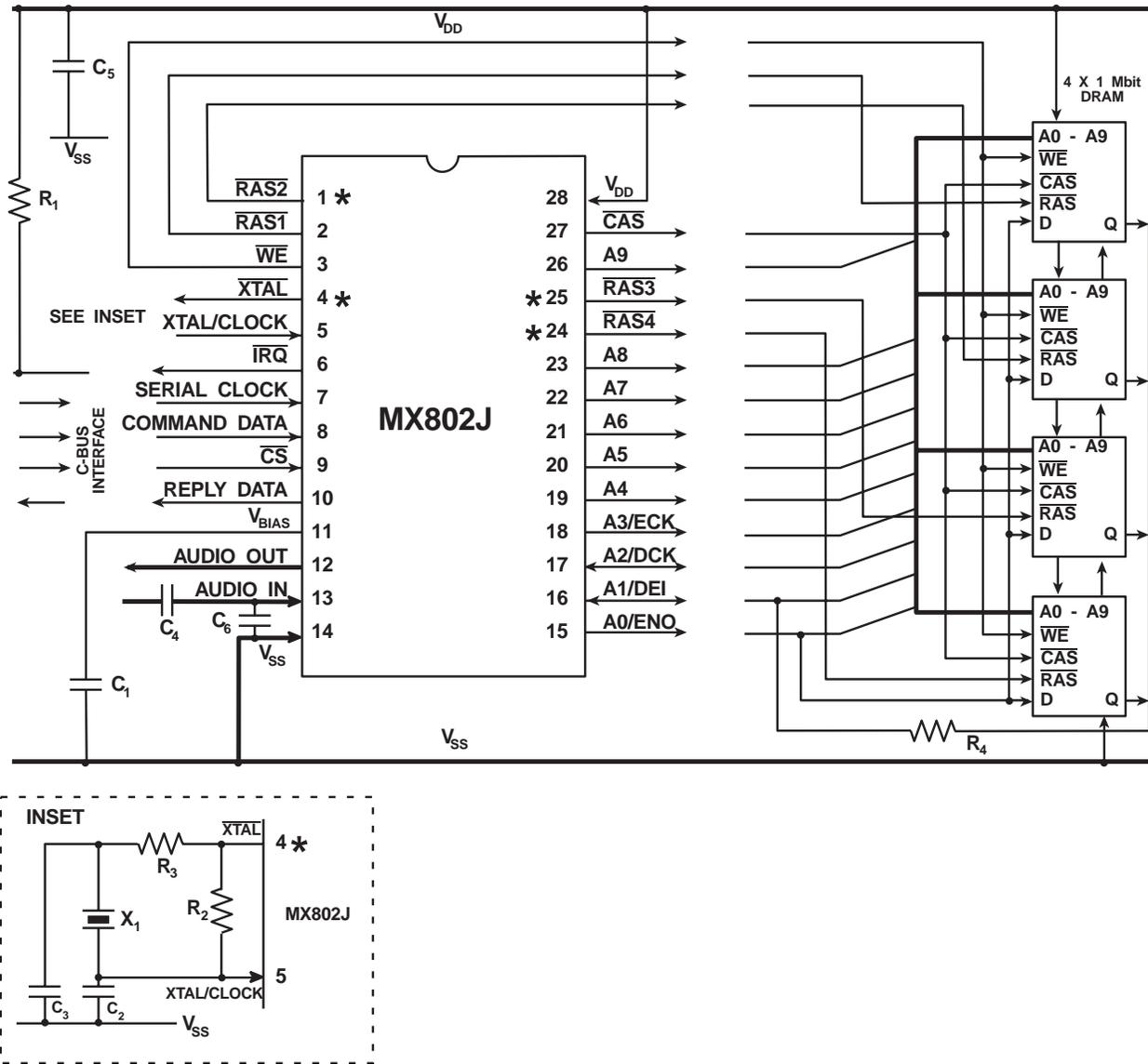
Figure 2:   Recommended External Components

Component	Notes	Value	Tolerance
R1		22.0kΩ	±5%
R2		1.0MΩ	±10%
R3	1		±10%
R4		1.0kΩ	±10%
C1		1.0μF	±10%
C2		33.0pF	±20%
C3		33.0pF	±20%

Component	Notes	Value	Tolerance
C4		1.0μF	±20%
C5		1.0μF	±20%
C6		.001μF	±20%
X1		4.00MHz	
X1		4.032MHz	
X1		4.096MHz	

Table 2: Recommended External Components

Recommended External Component Notes:

1. Xtal circuitry shown in inset is in accordance with the MX-COM Standard and DBS 800 Crystal Application Note.

2. External Xtal circuitry is not applicable to the 24-pin/lead version of this device. Only an externally derived clock input can be used.

3. Functions whose pins are marked with and asterisk (*) in Figure 2 are not available on the 24-pin/lead versions of this device. Pin numbers illustrated are for 28-pin versions.

4. Table 5 details the actual encoder/decoder sample rates available using the Xtal frequencies recommended above.

5. Resistor R1 is used as the DBS800 system common pull-up for the C-BUS Interrupt Request $\overline{IRQ}$ line. The optimum value will depend on the circuitry connected to the $\overline{IRQ}$. Up to 8 peripherals may be connected to this line.

6. Recommended DRAM parameters:
   256kbit x 1 or 1Mbit x 1 Dynamic Random Access Memory with "$\overline{CAS}$ before $\overline{RAS}$" refresh mode.
   Maximum Row address time = .200us.
   Example DRAM types:
   256kbit (262,144 bits)
       Texas Instruments (TMS4256-20)
       Hitachi (HM51256-15)
   1Mbit (1,048,576 bits)
       Texas Instruments (TMS4C1024-15)
       Hitachi (HM511000-15)

7. Figure 2 shows connections to 4x1 Mbit sections of DRAM. If desired, to simplify PCB layout, the DRAM inputs A0-A8 may be connected in any order to the MX802 DVSR Codec output pins A0-A8. Connections to 256kbit DRAM are similar, but A9 I left unconnected.

8. When using the MX802 "stand alone" 9Direct Access), no DRAM sections should be connected.

4   General Description

The MX802 Data/Voice Storage and Retrieval (DVSR) Codec contains a Continuously Variable Slope Delta Modulation (CVSD) encoder and decoder as well as control and timing circuitry for up to 4Mbits of external DRAM. As a member of the DBS800 series, it also contains interface and control logic for the "C-BUS" serial interface.

When used with external DRAM, theMX802 had four primary functions: Speech Storage, Speech layback, Data Storage, and Data Retrieval. The Speech Storage and Playback may be performed concurrently with data storage or retrieval.

Speech Storage:	Speech signals present at the Audio Input may be digitized by the CVSD encoder. The resulting bit stream is stored in DRAM. This process also provides readings of the speech signal power level. These readings are used by the system microcontroller for pause reduction.
Speech Playback:	Digitized speech may be read from DRAM and converted back into analog from by the CVSD decoder.
Data Storage:	Digital data derived via the C-BUS from the Modem or system data may be stored in DRAM.
Data Playback:	Digital data may be read from DRAM and sent over the C-BUS to the system microcontroller.

On-chip the Delta Codec is supported by input and output analog switched-capacitor filters and audio output switching circuitry. The DRAM control and timing circuitry provides all the necessary address, control, and refresh signals to interface to external DRAM.

The MX802 may also be used without DRAM (as a "stand alone" CVSD Codec), in which case direct access is provided to the CVSD Codec digital data and clock signals. All signals are controlled by "C-BUS" commands from the system microcontroller.

4.1 Controlling Protocol

Control of the functions of the MX802 DVSR Codec is by a group of Address/Commands (A/Cs) and appended instructions of data to and from the system microcontroller (See Figure 4). The use and content of these instructions is detailed in the following pages.

Command Assignment	Address/Command (A/C) byte		Data Bytes
	Hex	Binary	
		MSB LSB	
General Reset	01	00000001	
Write to Control Register	60	01100000	+2 byte instruction to Control Register
Read Status Register	61	01100001	+1 byte reply from Status Register
Store 'N' pages. Start page 'X'	62	01100010	+2 bytes command – Immediate
Store 'N' pages. Start page 'X'	63	01100011	+2 bytes Command – Buffered
Play 'N' pages. Start page 'X'	64	01100100	+2 bytes Command – Immediate
Play 'N' pages. Start page 'X'	65	01100101	+2 bytes Command – Buffered
Write Data. Start page 'P'	66	01100110	+2 bytes 'P' + Write Data
Read Data. Start page 'P'	67	01100111	+2 bytes 'P' + Read Data
Write Data – continue	68	01101000	+Write Data
Read Data -- Continue	69	01101001	+Read Data

Table 3: C-BUS Address/Commands

4.1.1 Address/Commands

Instruction and data transactions to and from this device consist of an Address/Command (A/C) byte followed by further instruction/data reply.

Control and configuration is by writing instructions form the microcontroller to the Control Register (60_H). Reporting of MX802 configurations is by reading the Status Register (61_H).

4.1.2 Operation with DRAM

The MX802 can operate with up to 4Mbits of Dynamic Ram (DRAM). When used with DRAM, the MX802 performs four main functions under the control of the commands received over the C-BUS interface from the microcontroller:

Stores Speech The MX802 stores speech by digitally encoding the analog input signal and writing the resulting digital data into the associated DRAM.

Plays Speech The MX802 plays back stored speech by reading the digital data stored in the DRAM and decoding it to provide and analog output signal.

Writes Data The MX802 writes data sent ver the C-BUS from the microcontroller to DRAM.

Reads Data The MX802 reads data from DRAM, sending it to the microcontroller over the C-BUS.

Data is directed to and from DRAM by the on-chip DRAM Controller.

4.1.3   Speech

The CVSD encoder and decoder sampling rates are independently set via the Control Register (See Table 4, Table 5, and Table 6) to 16, 25, 32, 50, and 64kbps. This allows the user to choose between speech quality and storage time while providing for time compression or expansion of the speech signals.

The DVSR Codec can handle from 256kbits to 4Mbits of DRAM, giving, in the case of the 32kbps sampling rate, from 8 to 131 seconds of speech storage.

For speech storage purposes, the memory is divided into 'pages' of 1024 bits each, corresponding to 32ms at 32kbps sampling rate.

<div align="center">

A 256 kbit DRAM contains   256 'pages'
A 1 Mbit DRAM contains   1024 'pages'
A 4 Mbit DRAM contains   4096 'pages'

</div>

When used without DRAM, the decoder sampling rate (8-64kbps) is determined by an external clock source applied to the Decoder Clock pin.

4.1.3.1   Store and Play Speech Commands

Speech storage and playback may take place simultaneously. These commands are transmitted, via C-BUS, to the MX802 in the following form:

STORE OR PLAY "N" (1024-bit) PAGES (of decoded speech data) STARTING AT PAGE "N".

"N" can be any number between 0 and F (1-16 pages). "X" can be any number from 405 (4Mbit DRAM), as shown below. Preceded by A/C, this command writes 16 bits (byte 1 or byte0) of data from the microcontroller to the Store or Play command Buffer.

MSB		BYTE 1						BYTE2							LSB
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
		N									X				
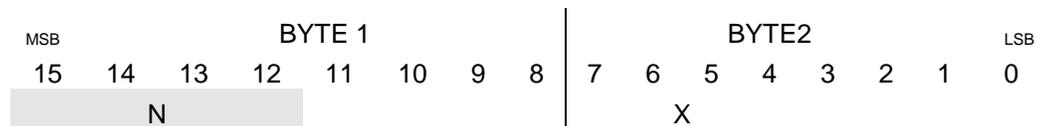
4.1.3.2   Speech Store Commands

4.1.3.2.1 62_H STORE "N" PAGES – START PAGE "X" (immediate)
63_H STORE "N" PAGES – START PAGE "X" (buffered)

The digitized speech from the CVSD encoder is stored in consecutive DRAM locations with the Speech Store Counters sequencing through the DRAM addresses and counting the number of complete pages stored since the start of the execution of the command.

As soon as the command has terminated, the following events take place:

1.   The Store Command Complete bit in the Status Register (Table 7) is set.

2.   An Interrupt Request ($\overline{IRQ}$) is sent, if enabled, to the microcontroller.

3.   The next speech storage command (if present) is immediately taken from the Store Command Buffer and execution f the new command commences.

The $\overline{IRQ}$ output is cleared by reading the Status Register:

4.1.3.2.2   61H READ STATUS REGISTER (Table 8)

To provide continuity of speech commands, both Store and Play Commands can be presented to the MX802 in one of two formats: immediate or buffered.

An immediate command will be started on completion of its loading, irrespective of the condition of the current command.

A buffered command will begin after the completion of the current Store or Play command, unless Speech Synchronization Bits (Control Register) are set.

Buffering of commands lets the DVSR Codec execute a series of commands without intervening gaps even though the microcontroller may take several milliseconds to respond to each "Command Complete" Interrupt Request.

In either case, the Store or Play Command Complete bit of the status register will be cleared.

4.1.3.3   Speech Playback

Speech playback is controlled by similar commands using the Speech Play counters and Play Command Buffer:

4.1.3.3.1   64$_H$ PLAY "N" PAGES – START PAGE "X" (immediate)
65$_H$ PLAY "N" PAGES – START PAGE "X" (buffered)

As soon as the Play Command had completed, the "Play Command Complete" bit in the Status Register is set, and an Interrupt Request is generated (if enabled).

If no "next" command is waiting in the Play Command Buffer when a speech play command finishes, a continuous idle code (0101…0101) will be fed to the delta decoder.

Speech data is stored or recovered at the selected Encode or Decode sample rate (Table 5). Store or Play Command Complete bits in the Status Register are cleared by the next Store or Play Command received from the microcontroller, or by a General Reset (01$_H$).

4.1.3.4   Store/Play Speech Synchronization (Table 6)

This capability is provided primarily for Time Domain Scrambling applications.

Speech Synchronization bits in the Control Register will produce the effects described below:

4.1.3.4.1   No Speech Sync Set:

Store and Play operations may take place completely independently.

4.1.3.4.2   Store after Play:

The next buffered store command will start on completion of a play command, while the next play command sequence (if any) continues normally.

4.1.3.4.3   Play after Store:

The next buffered play command will start on completion of a store command, while the next store command sequence (if any) continues normally.

These actions will continue while Speech Sync bits are set.

4.1.4   Data Handling

For the purpose of storing data sent via C-BUS from the microcontroller, the memory (DRAM) is divided into "data pages" of 64 bits (8 bytes).

A 256kbit DRAM contains   4096 data pages.
A 1Mbit DRAM contains 16384 data pages.
4Mbit DRAM contains   65536 data pages.

In accordance with C-BUS timing specifications, data is handled 8 bits (1 byte) at a time, although any number of 8-bit blocks of data may be written to or read from the DRAM by a single command.

Data transfer is terminated by the Chip Select line going to a logic "1."

4.1.4.1   C-BUS Data Transfer Limitations

For those commands which transfer data over the C-BUS between DRAM and the microcontroller (Write and Read data), the C-BUS serial clock rate is limited to a maximum of:

125kHz if the VSR Codec is executing store and play commands.
250kHz if no speech Store or Play commands are active.

This limitation is due to the rate at which data goes into and out of the DRAM. All other commands and replies (Control, Status, Reset) may use a maximum clock rate of 500kHz. See Figure 4.

4.1.4.2   Read Data

4.1.4.2.1   67$_H$ READ DATA -- START PAGE "P"

This command sets the Data Read Counter to "P," page, and then reads data bytes from successive DRAM locations, sending them to the microcontroller as Reply Data bytes. The Data Read Counter is incremented by 1 for each bit read.

4.1.4.2.2   69$_H$ READ DATA CONTINUE

This command reads data bytes from successive DRAM locations determined by the Data Read Counter, incrementing the counter by 1 for each bit read.

4.1.4.3   Write Data

4.1.4.3.1   66$_H$ WRITE DATA -- START PAGE "P"

This command sets the Data Write Counter to "P" page, and then writes data bytes to successive DRAM locations, incrementing the Data Write Counter by 1 for each bit received via the C-BUS.

The Start Page, "P," is indicated by loading a 2-byte word after the relevant Address/Command byte. This 16-bit word allows data page addresses from 0 to 65535 (4Mbits DRAM).

4.1.4.3.2   68$_H$ WRITE DATA CONTINUE

This command writes data bytes to successive DRAM locations determined by the Data Write Counter, incrementing the counter by 1 for each bit received over the C-BUS.

4.1.4.4   DRAM Speech Capacity

28-pin/lead versions of the MX802 may be used with a single 256kbit DRAM, or with up to 4 x 1Mbit of DRAM. 24-pin/lead versions may only be used with a single 256kbit or 1Mbit DRAM. The different encode and decode sampling clock rates available enable the user to set voice store and play times against recovered speech quality. Table 4 gives information on storage capacity and Store/Playback times. Speech data can be replayed at a different sample rate or in a reversed sequence (see Control Register for details).

DRAM Size	Available bits	Speech Pages	Nominal Sample Rates (kbps)				
			16	25	32	50	64
256kbps	262144	256	16.0	10.0	8.0	5.0	4.0
1024kbps	1048576	1024	65.0	42.0	32.0	20.0	16.0
2Mbps	2097152	2048	131.0	84.0	65.0	42.0	32.0
3Mbps	3145738	3072	196.0	126.0	98.0	63.0	49.0
4Mbps	4194304	4096	262.0	168.0	131.0	84.0	65.5

Table 4:   Sampling Clock Rates vs. Speech Storage/Playback Times

4.1.4.5   Encoder and Decoder Sampling Clocks

Encoder and decoder sampling clock rates are programmable via the Control Register. Table 5 shows the range of sampling rates available for different Xtal/clock input frequencies and the counter ratios used to produce them. Consideration should be given to the effect of different Xtal/clock frequencies upon the audio frequency performance of the device.

Control Register Byte 0, Bits				Internal Counter Division Ratio	Xtal Clock Frequency (MHz)		
5	4	3	Dec.		4.0	4.032	4.096
2	1	0	Enc.				
0	1	1		256	15.625	15.75	16.0
1	0	0		160	25.0	25.20	25.60
1	0	1		128	31.25	31.50	32.0
1	1	0		80	50.0	50.4	51.20
1	1	1		64	62.50	63.0	64.0

Table 5:   Sampling Clock Rates Available

With respect to using a single Xtal/clock frequency for all DBS 800 devices in use, it should be noted that

a.   A 4.032MHz Xtal/clock input will produce an accurate 1200-baud rate for the MX809 MSK Modem.

b.   A 4.096MHz Xtal/clock input will generate exactly 16kbps, 32kbps and 64kbps Codec sampling clock rates.

4.2 Write to Control Register

4.2.1 General Reset

Upon power-up the bits in the MX802 registers will be random (either 0 or 1). A General Reset Command (01_H) will be required to reset all devices on the C-BUS. It has the following effect on the MX802:

Control Register	Set to 00_H
Status Register	Set to 00_H
Clear Store and Play Command Buffers	

4.2.2 Direct Access

External circuitry is allowed direct access to the Delta Codec data and sampling clocks, disabling the DRAM timing circuitry. This permits the Delta Codec section of the MX802 to be used as a Delta Modulation voice encoder and decoder.

Input audio is encoded and made available at the Encoder Out (ENO) pin. Speech data input to the Decoder In (DEI) pin is decoded to give voice-band audio at the Audio Output.

Analog output switching remains under the control of the Control Register, but the decoder sampling clock rate (8kbps to 64kbps) must be provided from an external source to the Decoder Clock (DCK) pin. To ensure correct filter setting, Decoder Control bits (byte 0, bits 5, 4, 3) should be set to binary 1,1,1, where the required rate approximates to a multiple of 25kbps.

Both the encoder internal sampling clock rate and input switching (Table 7) remain under the control of the Control Register. The encoder internal sampling clock rate is available to external circuitry at the Encoder Clock Out (ECK) pin.

4.2.3 Play Counter

The Play Counter direction may be set to run backward as well as forward. This can be used in a scrambling system by replaying speech data in reverse order.

4.2.4 DRAM Control

A logic "1" will disable the DRAM Control Timing circuits and associated counters. The C-BUS Interface, Clock Generator, Delta Codec and filters remain active. This bit should be set to logic "1" when the MX802 is used in the Direct Access Mode.

Minimum DVSR Codec power consumption is achieved by setting both DRAM Control and Powersave bits to logic "1."

4.2.5 Codec Powersave

A logic "1" puts the Delta Codec and filters into Powersave Mode with V_{BIAS} maintained. The Clock Generator, C-BUS Interface, and DRAM Control and Timing remain active.

4.2.6 Command Interrupt Enable

A logic "1" set at the relevant bit will enable Interrupt Requests to the microcontroller when that command operation is complete.

4.2.7 Store and Play Speech Synchronization

This is intended primarily for Time Domain Scrambling.

4.2.8 Decoder and Encoder Control

This individually sets decoder and encoder sampling clock rates, as well as the source of the audio output.

Setting			Function
Byte 1			**First Byte for Transmission**
MSB **Bit 7**			**Not used – Set to '0'**
Bit 6			**Direct Access**
1 0			Encoder Data out to A0/ENO Encoder Clock to A3/ECK Decoder Input from A1/DEI Decoder Clock from A2/DCK Normal DVSR Operation
Bit 5			**Play Counter**
1 0			Decrement Increment
Bit 4			**DRAM Control**
1 0			Disable DRAM Enable DRAM
Bit 3			**Codec Powersave**
1 0			Powersave MX802 MX802 Enable
Bit 2			**Store Command Interrupt**
1 0			Enable Interrupt Disable
Bit 1			**Play Command Interrupt**
1 0			Enable Interrupt Disable
Bit 0			**Power Reading Interrupt**
1 0			Enable Interrupt Disable
Setting			**Function**
Byte 0			**Last Byte for Transmission**
MSB Bit 7	Bit 6		Store/Play Speech Sync.
0 0 1 1	0 1 0 1		No Sync No Sync Sync – Play after Store Sync – Store after Play
Bit 5	Bit 4	Bit 3	Decoder Control
0 0 0 0 1 1 1 1	0 0 1 1 0 0 1 1	0 1 0 1 0 1 0 1	Idle (32kbps); Aud O/P from LPF Idle (32kbps); Aud bypass Idle (32kbps); Aud O/P at high Z On-Sampling Rate 16kbps On-Sampling Rate 25kbps On-Sampling Rate 32kbps On-Sampling Rate 50kbps On-Sampling Rate 64kbps
Bit 2	Bit 1	Bit 0	Encoder Control
0 0 0 0 1 1 1 1	0 0 1 1 0 0 1 1	0 1 0 1 0 1 0 1	I/P at VBIAS; F/Idle (32kbps) I/P at high Z; F/Idle (32kbps) I/P at high Z; F/Idle (64kbps) On-Sampling Rate 16kbps On-Sampling Rate 25kbps On-Sampling Rate 32kbps On-Sampling Rate 50kbps On-Sampling Rate 64kbps

Table 6:   Control Register

4.3   Encoder and Decoder Control : Analog Input and Output Control

The Control Register, Byte 0: bits 0 to 5, are used together with the codec Powersave Bit (Byte 1: bit 3) to control codec input/output conditions and sample rates. Figure 3 shows the codec functional situation.
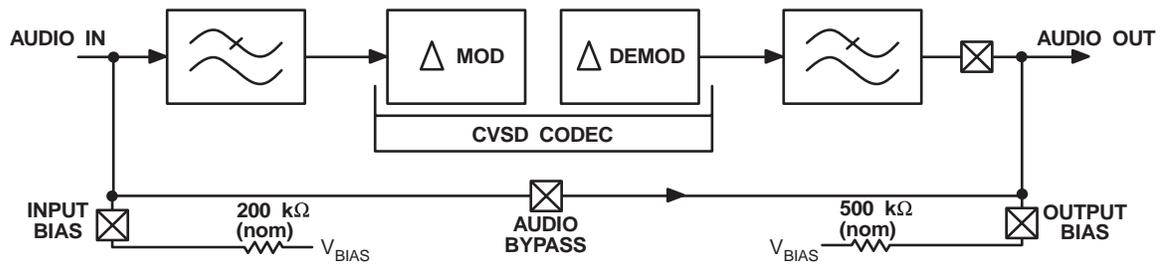
AUDIO IN → MOD DEMOD → AUDIO OUT

CVSD CODEC

INPUT BIAS   200 kΩ (nom) V_{BIAS} AUDIO BYPASS   500 kΩ (nom) V_{BIAS} OUTPUT BIAS

Figure 3: Analog Control (with reference to Figure 1)

Control Register				Circuit Switches				Note
Codec Powersave Bit	Decoder Control			Audio Bypass	Audio Out	Output Bias	*OFF = Switch Open* *ON = Switch ON*	
0	0	0	0	OFF	ON	OFF	Decoder idling fed with "1010101…" pattern at 32kbps.	1
0	0	0	1	ON	OFF	OFF		
0	0	1	0	OFF	OFF	OFF		
0	0	1	1	OFF	ON	OFF	Decoder running at the selected sampling rate.	1
–	–	–	–	–	–	–		
0	1	1	1	OFF	ON	OFF		
1	0	0	0	OFF	OFF	ON	Decoder circuits powersaved.	
1	0	0	1	ON	OFF	OFF		
1	0	1	0	OFF	OFF	ON		
1	0	1	1	OFF	OFF	ON		
–	–	–	–	-	–	-		
1	1	1	1	OFF	OFF	ON		
	Encoder Control				Input Bias			2
0	0	0	0		ON		Encoder running at 32kbps but Encoder Data O/P forced to idle pattern "01010…"	
0	0	0	1		OFF			
0	0	1	0		OFF			
0	0	1	1		OFF		Encoder running at selected sampling rate	
-	–	–	–		–			
0	1	1	1		OFF			
1	0	0	0		ON		Encoder circuits powersaved.	
-	-	-	-		-			
1	1	1	1		ON			

Table 7: Analog Control (with reference to Figure 3)

Notes

1. If the Delta Codec is in the Direct Access mode, these sampling rates will be as provided by the externally applied clock.

2. The input bias switch is operated by the Control Register Codec Powersave and Encoder Control bits to provide a relatively low impedance path for V_{BIAS} to charge the input coupling capacitor whenever the codec is powersaved, or the encoder control bits are set to 0, so that input bias can be established quickly prior to operation.

4.3.1   Time Compression of Speech

The 25kbps and 50kbps sampling rate options are provided for time compression and subsequent expansion of speech signals.

For example, 1.0 seconds of speech stored at 50kbps may be transmitted in 0.8 seconds if played out at 64kbps, and finally restored to its original speed at the receiver by storing at 64kbps and playing out at 50kbps. A similar result (with a degraded SINAD) may be achieved by using 25kbps and 32kbps sampling rates.

However, the speech frequencies are raised by time compression, and since the signal transmitted to air must be band limited to 3400 Hz, the effective end-to-end bandwidth is 0.8 x 3400 Hz, which is approximately 2700 Hz.

4.4   Read Status Register

4.4.1   Interrupts

If enabled by the Control Register, an Interrupt Request (IRQ) is produced by the MX802 to report the following actions:

> Power Reading Ready
> Store Command Complete
> Play Command Complete

When an Interrupt is produced, the Status Register must be read to determine the source of the interrupt. This action will clear the IRQ output.

The Store Command Complete bit (and an interrupt) is set on completion of a Store Command. This bit is cleared by loading the next Store Command, or by a General Reset Command (01_H).

The Play Command Complete bit (and an interrupt) is set on completion of a Play Command. This bit is cleared by loading the next Play Command, or by a General Reset Command (01_H).

The Power Reading Ready bit (and an interrupt) is set for every 1024 voice-data bits (1 page) from the Encoder. This bit is cleared after reading the Status Register, or by a General Reset Command (01_H).

4.4.2   Power Register

The power assessment element shown in Figure 1 assesses the input signal power for each encoded "page" (every 1024 encoder output bits) by counting the number of "compand bits" (000 or 111 sequences in the output bit stream) produced during that page (see Table 8) with typical encoder input power levels (dB).

At the end of each "page" the power reading ready bit of the status register is set, and an interrupt request is generated (if enabled). The resulting count is converted to a 5-bit quasi-logarithmic form. The Power Register reading is interpreted as follows:

00000 represents 0 compand bits
00001 represents 1 compand bit
11111 represents 512 compand bits, the maximum.

This power reading is placed in the status register to be read by the microcontroller. Figure 4 shows this output, indicating the input power level.

| Reading					Function	
MSB						
Bit 7					**Power Reading**	
1					Ready	
Bit 6					**Store Command**	
1					Complete	
Bit 5					**Play Command**	
1					Complete	
					Power Register	
4	**3**	**2**	**1**	**0**	Power	Compand Bits/pg.
0	0	0	0	0		0
0	0	0	0	1		1
0	0	0	1	0		2
0	0	0	1	1		3
0	0	1	0	0		4
0	0	1	0	1		5
0	0	1	1	0		6
0	0	1	1	1		7
0	1	0	0	0	-39.0dB	8
0	1	0	0	1		10
0	1	0	1	0	-36.0	12
0	1	0	1	1		14
0	1	1	0	0	33.5	16
0	1	1	0	1		18
0	1	1	1	0	-30.0	20
0	1	1	1	1		22
1	0	0	0	0	-28.0	24
1	0	0	0	1		32
1	0	0	1	0	-25.0	40
1	0	0	1	1		48
1	0	1	0	0	-22.0	56
1	0	1	0	1		64
1	0	1	1	0	-19.0	72
1	0	1	1	1		80
1	1	0	0	0	-16.0	88
1	1	0	0	1		128
1	1	0	1	0	-10.0	192
1	1	0	1	1		256
1	1	1	0	0	-6.0	320
1	1	1	0	1		384
1	1	1	1	0	0db	448
1	1	1	1	1		512

Table 8:   Status Register
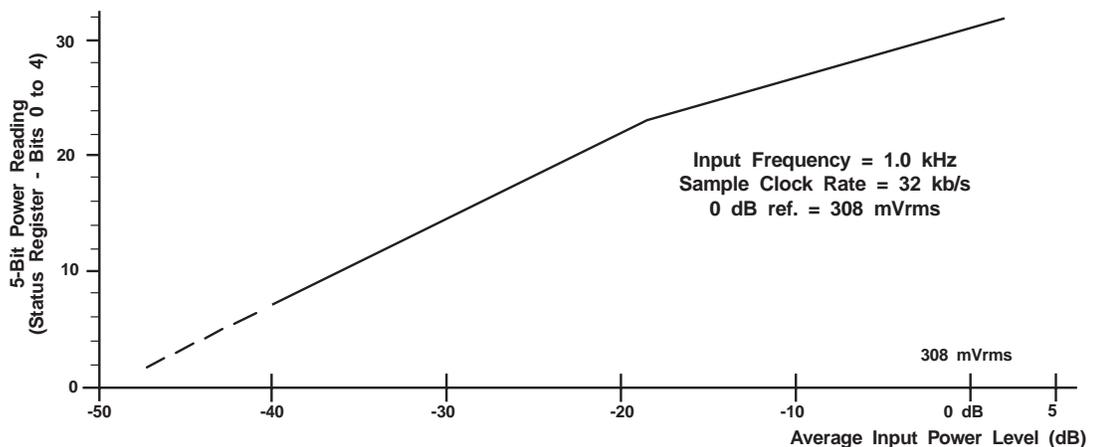
Figure 4:   Typical Power Readings vs. Input Levels

5   Application – Codec Performance

Gain (dB)

Input 0 dB Ref. = 308 mVrms
Input Level = -20 dB
Sample Rates = 16, 32 or 63 kbps

0 dB
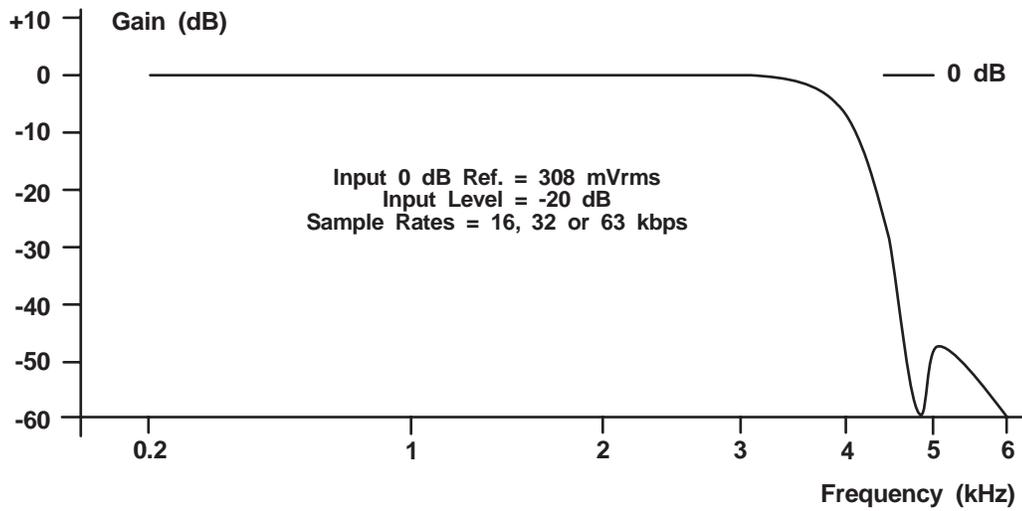
Frequency (kHz)

Figure 5:   Typical Overall;; (Encoder + Decoder) Frequency Response

SINAD (dB)

64 kbps

50 kbps

32 kbps

25 kbps

Input Frequency = 1.0 kHz
0 dB ref. = 308 mVrms

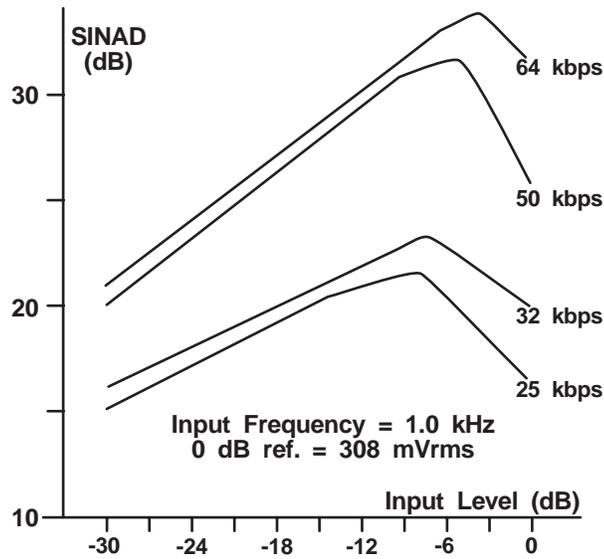Input Level (dB)

Figure 6:   SINAD vs. Input Level at Different Sample Rates
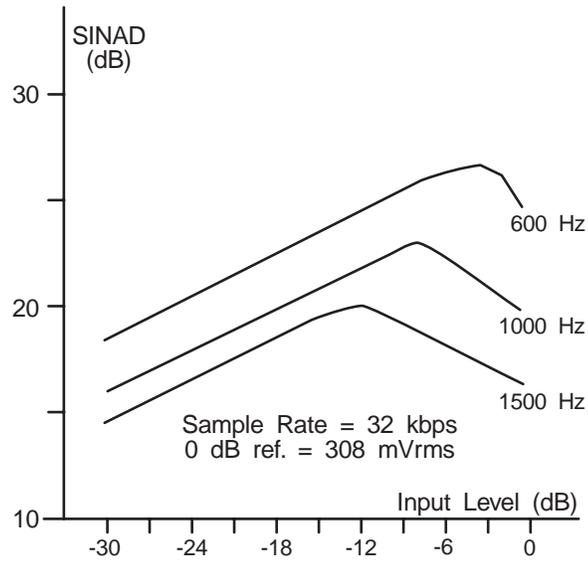
Figure 7: SINAD vs. Input Level at Different Frequencies
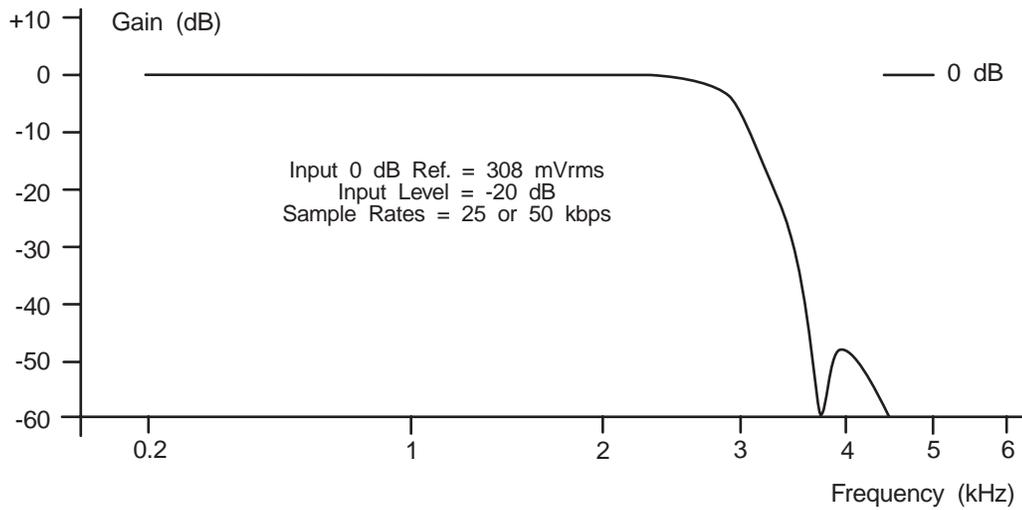

Figure 8: Typical Overall (Encoder + Decoder) Frequency Response

6   Performance Specifications

6.1   Electrical Specifications

6.1.1   Absolute Maximum Limits

Exceeding these maximum ratings can result in damage to the device.

General	Notes	Min.	Typ.	Max.	Units
Supply (V_{DD}-V_{SS})		-0.3		7.0	V
Voltage on any pin to V_{SS}		-0.3		V_{DD} + 0.3	V
Current					
V_{DD}		-30		30	mA
V_{SS}		-30		30	mA
Any other pin		-20		20	mA
J / LH / LH8 Packages					
Total allowable Power dissipation at T_{AMB} = 25°C				800	mW
Derating above 25°C			10		mW/°C above 25°C
Operating Temperature		-40		85	°C
Storage Temperature		-55		125	°C

Table 9:   Absolute Maximum Ratings

6.1.2   Operating Limits

Correct Operation of the device outside these limits is not implied.

	Notes	Min.	Typ.	Max.	Units
Supply (V_{DD}-V_{SS})		4.5	5.0	5.5	V
Operating Temperature		-40		85	°C
Xtal Frequency			4.0		MHz

Table 10:   Operating Limits

6.1.3 Operating Characteristics

For the following conditions unless otherwise specified.
V_{DD} = 5.0V @ T_{AMB} = 25°C
Xtal/Clock Frequency = 4.0MHz, Audio Level 0dB ref. = 308mV_{RMS}
Standard test signal f_0 = 820Hz,   Sample Rate 31.25kbps

Static Values	Notes	Min.	Typ.	Max.	Units
Supply Current					
I_{DD} (enabled)	1		7.0	10.0	mA
I_{DD} (powersave)	1		2.0	4.0	mA
Digital Interface					
Input Logic Level					
Logic 1 Input Level	2	3.5			V
Logic 0 Input Level	2			1.5	V
Output Logic Level					
Output Logic 1 (I_{OH} = 120µA)					
(I_{OH} = -120µA)	7	4.6			V
(I_{OH} = -50µA)	3	4.6			V
(I_{OH} = 20µA)	9	4.6			V
Output Logic 0					
(I_{OL} = 20µA)	9			0.4	V
(I_{OL} = 100µA)	3			0.4	V
(I_{OL} = 360µA)	7, 8			0.4	V
Digital Input Current					
VIN = Logic 1 or 0	2			1.0	µA
Leakage Current into $\overline{IRQ}$ 'OFF' Output	4			4.0	µA
Digital Input Capacitance	2			7.5	pF
Analog Impedance					
Input Impedance	12		500		KΩ
Output Impedance			1.5		kΩ
Dynamic Values					
Encoder					
Analog signal Input Levels	5	-24.0		4.0	dB
Passband	10, 11		3400		Hz
Decoder					
Analog Signal Output Levels	5	-24.0		4.0	dB
Passband	10, 11	300		3400	Hz

Static Values	Notes	Min.	Typ.	Max.	Units
Encoder/Decoder (Full Codec)					
Passband	10, 11	300		3400	Hz
Passband Gain	11		0		dB
Passband Ripple	11	-3.0		3.0	dB
Stopband		6.0		10	kHz
Stopband Attenuation			50.0		dB
SINAD Level			23.0		dB
Output Noise (Input Short Circuit)			-50		dBp
Idle Channel Noise (Forced)			-55		dBp
Xtal/Clock Frequency	6		4.0		MHz

Table 11: Operating Characteristics

Operating Characteristics Notes:

1. Does not include current drawn by any attached DRAM.

2. Serial Clock, Command Data, Chip Select, A1/DE1, and A2/DCK inputs

3. $\overline{CAS}$, $\overline{WE}$, and A0 to A9 inputs.

4. When the $\overline{IRQ}$ output is at V_{DD}.

5. The optimum range levels for a good Signal to Noise ratio.

6. Audio frequency response will vary with respect to Xtal/Clock frequency.

7. Reply Data output.

8. $\overline{IRQ}$ output.

9. RAS output.

10. Passband is reduced to (typically) 2700Hz when a sample rate of 25kbps or 50kbps is used.

11. Measured with a –20dB input level to avoid a codec slope-overload.

12. For optimum noise performance this input should be driven from a source impedance of less that 100Ω.

6.1.4   Timing

C-BUS Timing		Min.			Typ.	Max.	Units
		a	b	c			
t_{CSE}	Chip Select Low to First Serial Clock Rising Edge	2.0	4.0	8.0			µs
t_{CHS}	Last Serial Clock Rising Edge to Chip Select High	4.0	4.0	8.0			µs
t_{HIZ}	Chip Select High to Reply Data High – Z					2.0	µs
t_{CSOFF}	Chip Select High	2.0	4.0	8.0			µs
t_{NXT}	Command Data Inter-Byte Time	4.0	8.0	16.0			µs
t_{CK}	Serial Clock Period	2.0	4.0	8.0			µs
Direct Address Timing							
t_{CH}	Decoder or Encoder Clock High		1.0				µs
t_{CL}	Decoder or Encoder Clock Low		1.0				µs
t_{SU}	Decoder Data Set Up Time		0.45				µs
t_{H}	Decoder Data Hold Time		0.60				µs
t_{PCO}	Encoder Clock High to Encoder Data Valid					0.75	µs
$t_{SU} + t_{H}$ = Data True Time							

Table 12:   Timing Information

Notes:

1. Minimum Timing Values
    a. For all commands except "Read Data" and "Write Data" Commands.
    b. For all "Read Data" and Write Data" commands when no "Speech Store" or "Speech Play" commands are active.
    c. For "Read Data" and "Write Data" commands when "Speech Store" or "Speech Play" commands are active.

2. Depending on the command, 1 or 2 bytes of Command Data are transmitted to the peripheral MSB (bit7) first and LSB (bit0) last. Reply data is read from the peripheral MSB (bit7) first and LSB (bit0) last.

3. To allow for different microcontroller serial interface formats, C-BUS compatible ICs are able to work with either polarity Serial Clock pulses.

4. Data is clocked into and out of the peripheral on the rising Serial clock edge.

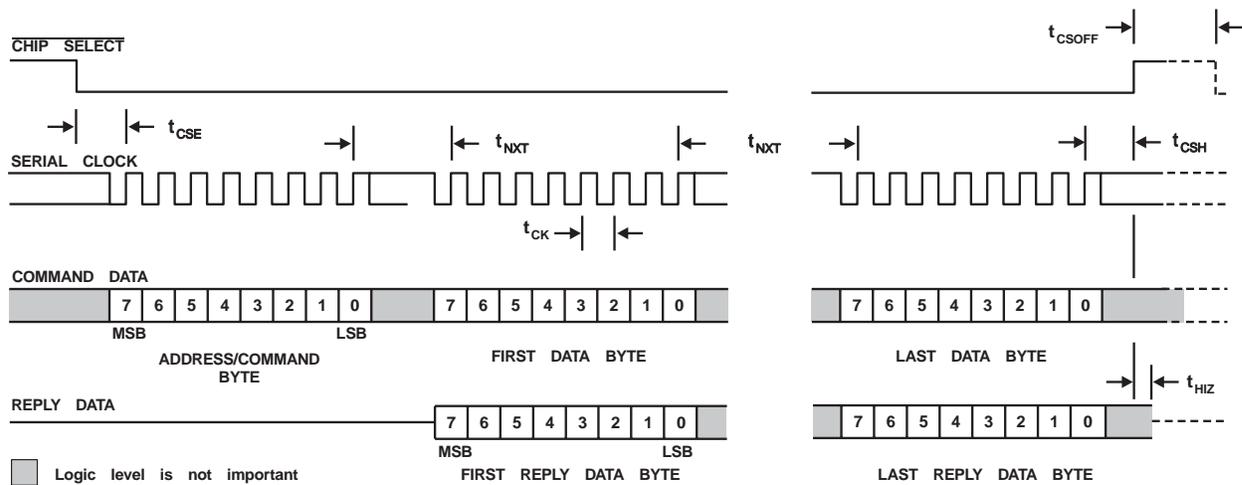5. Loaded commands are acted upon at the end each command.
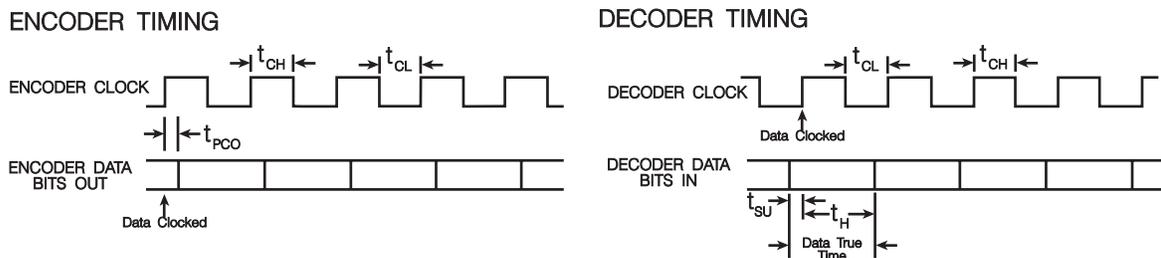
Figure 9:   C-BUS Timing Information
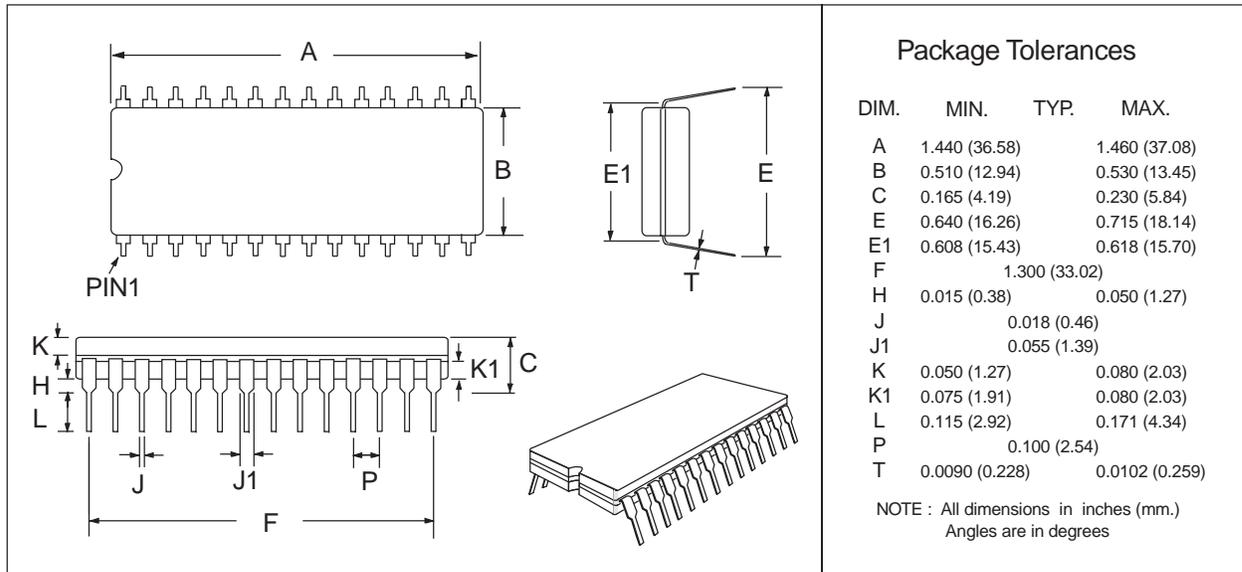
Figure 10:   Codec Direct Access Timing

6.2 Packages

DIM.	MIN.	TYP.	MAX.
A	1.440 (36.58)		1.460 (37.08)
B	0.510 (12.94)		0.530 (13.45)
C	0.165 (4.19)		0.230 (5.84)
E	0.640 (16.26)		0.715 (18.14)
E1	0.608 (15.43)		0.618 (15.70)
F		1.300 (33.02)	
H	0.015 (0.38)		0.050 (1.27)
J		0.018 (0.46)	
J1		0.055 (1.39)	
K	0.050 (1.27)		0.080 (2.03)
K1	0.075 (1.91)		0.080 (2.03)
L	0.115 (2.92)		0.171 (4.34)
P		0.100 (2.54)	
T	0.0090 (0.228)		0.0102 (0.259)

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 11: 28-pin CERDIP Mechanical Outline: *Order as part no. MX802J*

Package Tolerances

DIM.	MIN.	MAX.
A	.450 (11.43)	.453 (11.51)
B	.485 (12.32)	.495 (12.57)
C	.045x45	typical
D	.165 (4.20)	.180 (4.57)
E	.026 (0.66)	.030 (0.76)
F	.017 (0.43)	.021 (0.53)
G	.410 (10.41)	.430 (10.92)
H	.050 (1.27)	typical
J	.070 (1.78)	.085 (2.16)

NOTE : All dimensions in inches (mm.)
Angles are in degrees
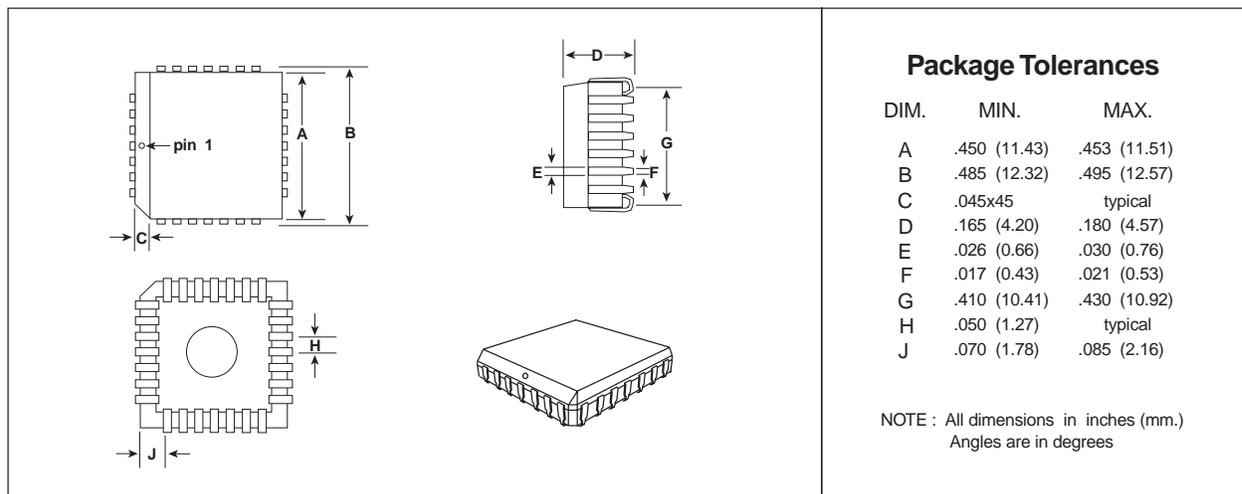
Figure 12: 28-pin PLCC Mechanical Outline: *Order as part no. MX802LH8*

Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.380 (9.61)		0.409 (10.40)
B	0.380 (9.61)		0.409 (10.40)
C	0.128 (3.25)		0.146 (3.70)
D	0.417 (10.60)		0.435 (11.05)
E	0.417 (10.60)		0.435 (11.05)
F		0.250 (6.35)	
G		0.250 (6.35)	
H		0.023 (0.58)	
J	0.018 (0.45)		0.022 (0.55)
K	0.047 (1.19)		0.048 (1.22)
P	0.049 (1.24)		0.051 (1.30)
T	0.006 (0.152)		0.009 (0.22)
W	30°	45°	
Y		6°	

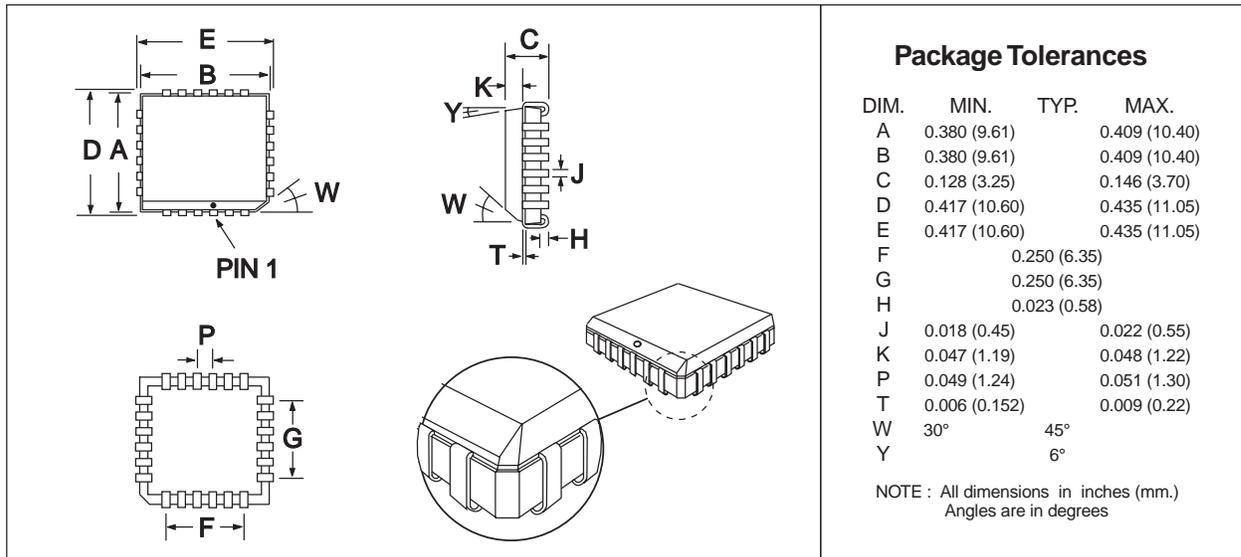NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 13: 24-pin PLCC Mechanical Outline: *Order as part no. MX802LH*