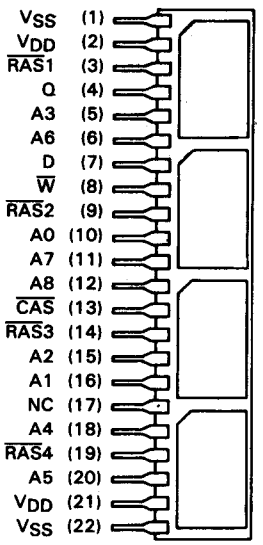
OCTOBER 1985—REVISED FEBRUARY 1988

- 1,048,576 × 1 Organization
- Single 5-V Supply (10% Tolerance)
- 22-Pin Single-In-line Package (SIP)
- Utilizes Four 256K Dynamic RAMs in Plastic Chip Carrier
- Long Refresh Period . . . 4 ms (256 Cycles)
- All Inputs, Outputs, Clocks Fully TTL Compatible
- 3-State Outputs
- Performance of Unmounted RAMs

	ACCESS TIME ROW ADDRESS (MAX)	ACCESS TIME COLUMN ADDRESS (MAX)	READ OR WRITE CYCLE (MIN)
TMS4256-10	100 ns	50 ns	200 ns
TMS4256-12	120 ns	60 ns	230 ns
TMS4256-15	150 ns	75 ns	260 ns

- Common $\overline{CAS}$ Control with Separate Data Input and Output Lines
- Low Power Dissipation
- Operating Free-Air Temperature . . . 0°C to 70°C

TM4256FC1 . . . C SINGLE-IN-LINE PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A8	Address Inputs
$\overline{CAS}$	Column-Address Strobe
D	Data Input
NC	No Connection
Q	Data Output
$\overline{RAS1}$-$\overline{RAS4}$	Row-Address Strobes
V_{DD}	5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

description

The TM4256FC1 series are 1024K, dynamic random-access memory modules organized as 1,048,576 × 1 bit in a 22-pin single-in-line package comprising four TMS4256FML, 262,144 × 1 bit dynamic RAMs in 18-lead plastic chip carriers mounted on top of a substrate together with decoupling capacitors mounted beneath the chip carriers. The onboard capacitors eliminate the need for bypassing on the motherboard and offer superior performance over equivalent leaded capacitors due to reduced lead inductance. Also, with 0.3 inch board spacing, the TM4256FC1 has a density of ten devices per square inch (approximately 4 × the density of DIPs). With the elimination of bypass capacitors on the motherboard, reduced PC board size, and fewer plated through-holes, a cost savings can be realized.

Each TMS4256FML is described in its data sheet and is fully electrically tested and processed according to TI MIL-STD-883B flows (as amended for commercial applications) prior to assembly. After assembly onto the SIP, a further set of electrical tests is performed.

The TM4256FC1 features $\overline{RAS}$ access times of 100 ns, 120 ns, and 150 ns maximum.

Refresh period is extended to 4 milliseconds, and during this period each of the 256 rows must be strobed with $\overline{RAS}$ in order to retain data. $\overline{CAS}$ can remain high during the refresh sequence to conserve power.

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All inputs and outputs, including clocks, are compatible with Series 74 TTL. All address lines and data-in are latched on-chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The TM4256FC1 is rated for operation from 0°C to 70°C.

operation

The TM4256FC1 operates as four TMS4256FMLs connected as shown in the functional block diagram. Refer to the TMS4256 data sheet for details of operation.

specifications

For TMS4256FML electrical specifications, refer to the TMS4256 data sheet.

single-in-line package and components

PC substrate: 1,27 mm (0.05 inch) nominal thickness epoxy-glass
Bypass capacitors: Multilayer ceramic
Leads: Tin/lead solder coated over phosphor-bronze

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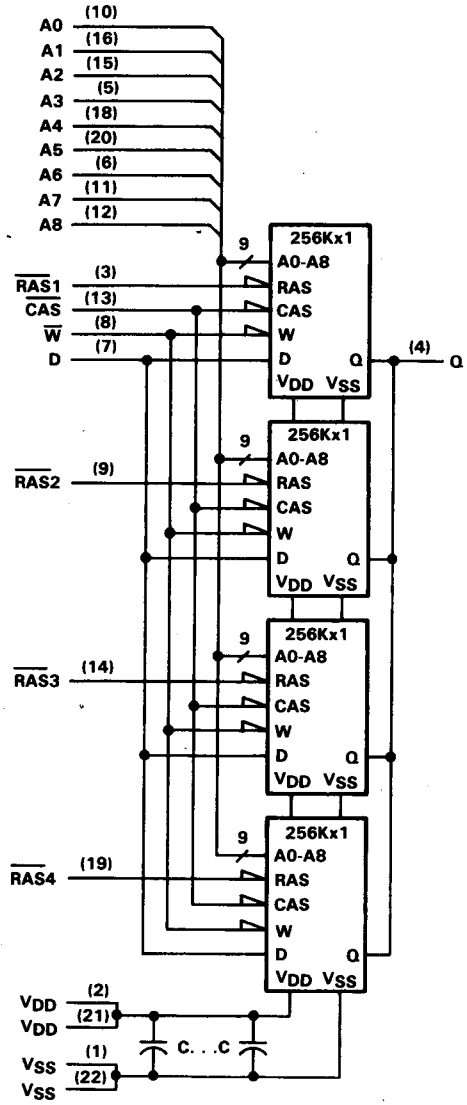
functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage range on any pin, including V_{DD} supply (see Note 1) . . . . . −1 V to 7 V
Short circuit output current for any output . . . . . 50 mA
Power dissipation . . . . . 4 W
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

†Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	−1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TM4256FC1-10		TM4256FC1-12		TM4256FC1-15		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = −5 mA	2.4	V_{DD}	2.4	V_{DD}	2.4	V_{DD}	V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA	0	0.4	0	0.4	0	0.4	V
I_I	Input current (leakage)	V_I = 0 V to 6.5 V, V_{DD} = 5 V, All other pins = 0 V		±10		±10		±10	μA
I_O	Output current (leakage)	V_O = 0.4 V to 5.5 V, V_{DD} = 5 V, $\overline{CAS}$ high		±10		±10		±10	μA
I_{DD1}	Average operating current during read or write cycle	t_c = minimum cycle Output open‡		80		75		70	mA
I_{DD2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, Output open		18		18		18	mA
I_{DD3}	Average refresh current	t_c = minimum cycle, $\overline{CAS}$ high and $\overline{RAS}$ cycling, Output open		232		212		192	mA
I_{DD4}	Average page-mode current	$t_{c(P)}$ = minimum cycle, $\overline{RAS}$ low and $\overline{CAS}$ cycling, Output open‡		50		45		40	mA

‡Assuming standard operation of one device access.

capacitance over recommended supply voltage range and operating free-air temperature range, f = 1 MHz

	PARAMETER	MIN	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs		20	pF
$C_{i(D)}$	Input capacitance, data inputs		20	pF
$C_{i(RAS)}$	Input capacitance, $\overline{RAS}$ input		5	pF
$C_{i(W)}$	Input capacitance, $\overline{W}$ input		28	pF
$C_{i(CAS)}$	Input capacitance, $\overline{CAS}$ input		20	pF
$C_{o(Q)}$	Output capacitance, data output		28	pF
$C_{o(VDD)}$	Decoupling capacitance	0.4		μF