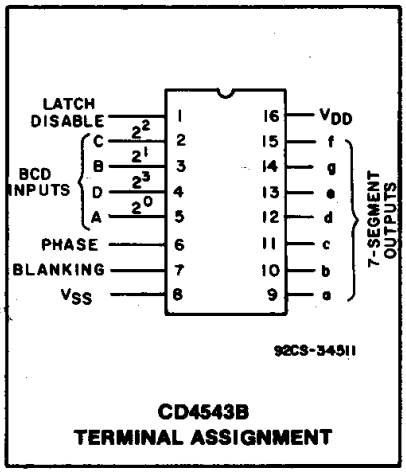
TEXAS INSTRUMENTS
Data sheet acquired from Harris Semiconductor
SCHS086A – Revised March 2002

CD4543B Types

CMOS BCD-to-Seven-Segment Latch/Decoder/Driver For Liquid-Crystal Displays

High-Voltage Types (20-Volt Rating)



CD4543B TERMINAL ASSIGNMENT

Features:
- *Display blanking of all illegal input combinations*
- *Latch storage of code*
- *Capability of driving two low power TTL loads, two HTL loads, or one low power Schottky load over the full rated-temperature range*
- *Pin-for-pin replacement for the CD4056B (with pin 7 tied to V_{SS})*
- *Direct LED driving capability*
- *100% tested for quiescent current at 20 V*
- *Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C*
- *Noise margin (full package-temperature range)= 1 V at V_{DD}=5 V; 2 V at V_{DD}=10 V; 2.5 V at V_{DD}=15 V*
- *5-V, 10-V, and 15-V parametric ratings*
- *Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"*

Applications:
- *Instrument display driver*
- *Dashboard display driver*
- *Computer/calculator display driver*
- *Timing device driver (clocks, watches, timers)*

■ CD4543B is a BCD-to-seven segment latch/decoder/driver designed primarily for liquid-crystal display (LCD) applications. It is also capable of driving light emitting diode (LED), incandescent, gas-discharge, and fluorescent displays. This device is functionally similar to and serves as direct replacement for the CD4056B when pin 7 is connected to V_{SS}. It differs from the CD4056B in that it has a display blanking capability instead of a level-shifting function and requires only one power supply. When the CD4056B is used in the level shifting mode, two power supplies are required. When the CD4543B is used for LCD applications, a square wave must be applied to the PHASE input and the backplane of the LCD device. For LED applications a logic 1 is required at the PHASE input for common-cathode devices; a logic 0 is required for common-anode devices (see truth table).

The CD4543B is supplied in hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline package (NSR suffix), and in chip form (H suffix).

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) ..... -0.5V to +20V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5V to V_{DD} +0.5V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55°C to +100°C 500mW
For T_A = +100°C to +125°C ..... Derate Linearity at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) 100mW
OPERATING-TEMPERATURE RANGE (T_A) ..... -55°C to +125°C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... -65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max ..... +265°C

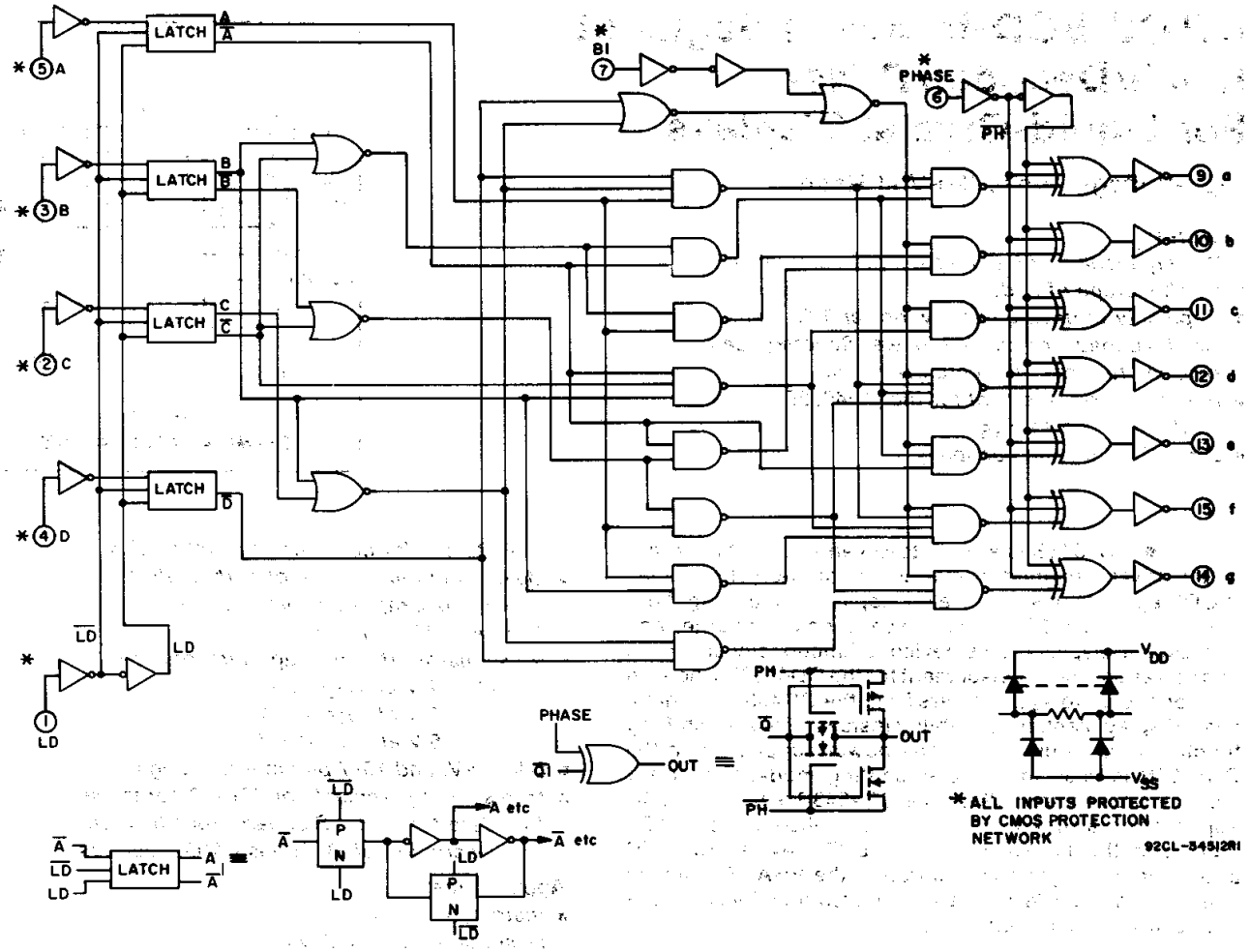


Fig. 1 - BCD-to-seven-segment latch/decoder/driver CD4543B logic circuit diagram.

RECOMMENDED OPERATING CONDITIONS at T_A=25°C, Unless Otherwise Specified
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC		V_{DD} (V)	LIMITS		UNITS
			MIN.	TYP.	
Supply-Voltage Range (For T_A=Full Package-Temperature Range)		—	3	18	V
Latch Disable Pulse Width	t_{WH}	5	250	125	ns
		10	100	50	
		15	80	40	
Minimum Data Setup Time	t_{SU}	5	60	15	
		10	20	-5	
		15	10	-5	
Minimum Data Hold Time	t_H	5	25	-5	
		10	20	10	
		15	20	10	

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC		CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
		V_O (V)	V_{IN} (V)	V_{DD} (V)	-55	-40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	
Quiescent Device Current Max.	I_{DD}	—	0, 5	5	5	5	150	150	—	0.04	5	μA
		—	0,10	10	10	10	300	300	—	0.04	10	
		—	0,15	15	20	20	600	600	—	0.04	20	
		—	0,20	20	100	100	3000	3000	—	0.08	100	
Output Low (Sink) Current Min.	I_{OL}	0.4	0, 5	5	0.64	0.61	0.42	0.36	0.51	1	—	mA
		0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	—	
		1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	—	
Output High (Source) Current Min.	I_{OH}	4.6	0, 5	5	-0.46	-0.44	-0.30	-0.26	-0.37	-0.75	—	
		2.5	0, 5	5	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	—	
		9.5	0,10	10	-0.98	-0.92	-0.68	-0.55	-0.8	-1.6	—	
		13.5	0,15	15	-3.33	-3.18	-2.2	-1.9	-2.7	-5.4	—	
Output Voltage: Low-Level Max.	V_{OL}	—	0, 5	5	0.05				—	0	0.05	V
		—	0,10	10	0.05				—	0	0.05	
		—	0,15	15	0.05				—	0	0.05	
Output Voltage: High-Level Min.	V_{OH}	—	0, 5	5	4.95				4.95	5	—	
		—	0,10	10	9.95				9.95	10	—	
		—	0,15	15	14.95				14.95	15	—	
Input Low Voltage Max.	V_{IL}	0.5,4.5	—	5	1.5				—	—	1.5	V
		1, 9	—	10	3				—	—	3	
		1.5,13.5	—	15	4				—	—	4	
Input High Voltage Min.	V_{IH}	0.5,4.5	—	5	3.5				3.5	—	—	
		1, 9	—	10	7				7	—	—	
		1.5,13.5	—	15	11				11	—	—	
Input Current Max.	I_{IN}	—	0,18	18	±0.1	±0.1	±1	±1	—	$±10^{-5}$	±0.1	μA

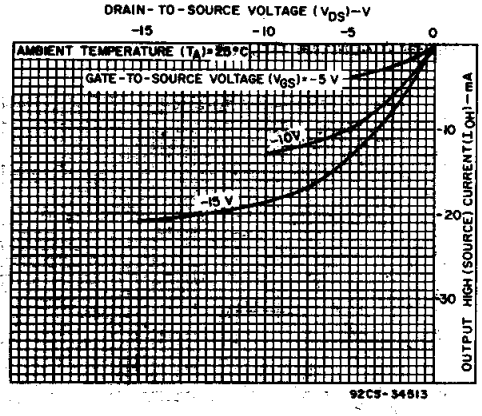


Fig. 2 - Typical output high (source) current characteristics.

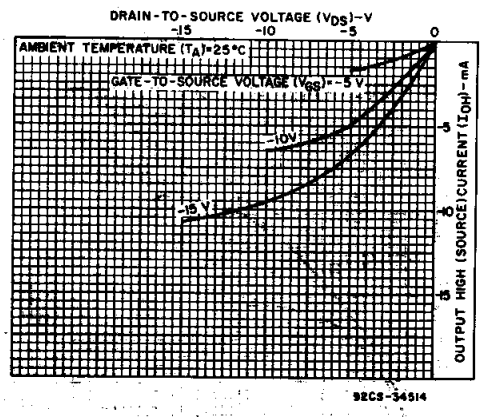


Fig. 3 - Minimum output high (source) current characteristics.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A=25° C; C_L=50 pF, Input t_r,t_f=20 ns, R_L=200 kΩ

CHARACTERISTIC		TEST CONDITIONS V_{DD} (V)	LIMITS All Packages MIN.	TYP.	MAX.	UNITS
Propagation Delay Time	t_{PHL}	5	—	600	1200	ns
		10	—	200	400	
		15	—	150	300	
	t_{PLH}	5	—	500	1000	
		10	—	200	400	
		15	—	150	300	
Transition Time	t_{THL}	5	—	180	360	
		10	—	90	180	
		15	—	65	130	
	t_{TLH}	5	—	180	360	
		10	—	90	180	
		15	—	65	130	
Latch Disable Pulse Width	t_{WH}	5	250	125	—	
		10	100	50	—	
		15	80	40	—	
Address Setup Time	t_{SU}	5	60	15	—	
		10	20	-5	—	
		15	10	-5	—	
Address Hold Time	t_H	5	25	-5	—	
		10	20	10	—	
		15	20	10	—	
Input Capacitance	C_{IN}	Any Input	—	5	7.5	pF

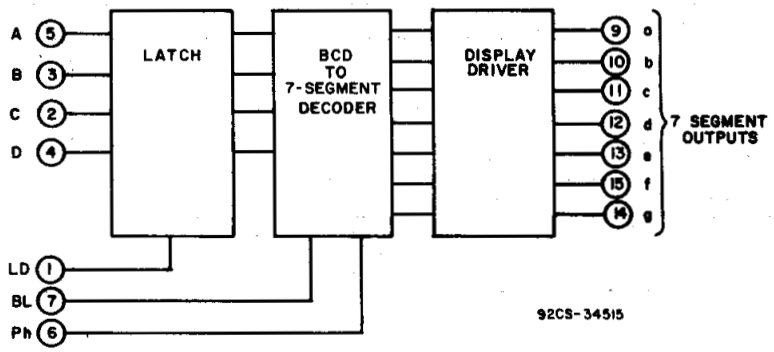


Fig. 4 - BCD-to-seven-segment latch/decoder/driver functional diagram.

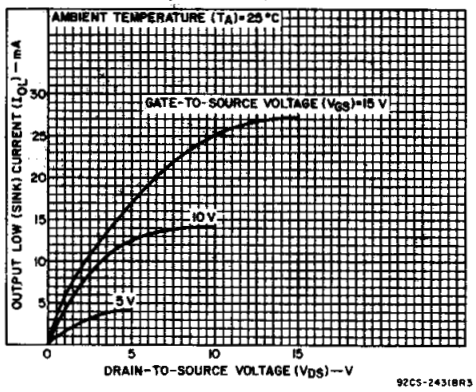


Fig. 5 - Typical output low (sink) current characteristics.

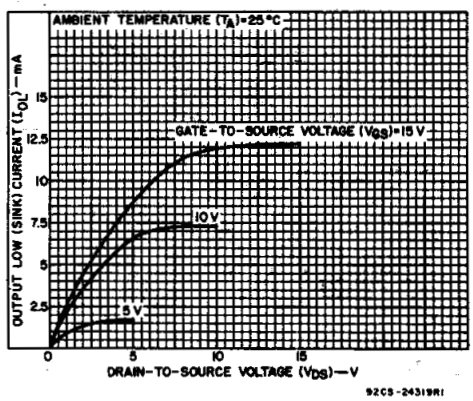


Fig. 6 - Minimum output low (sink) current characteristics.

TRUTH TABLE FOR CD4543B

INPUT CODE							OUTPUT STATE							DISPLAY CHARACTER
LD	BI	Ph*	D	C	B	A	a	b	c	d	e	f	g	
X	1	0	X	X	X	X	0	0	0	0	0	0	0	
1	0	0	0	0	0	0	1	1	1	1	1	1	0	0
1	0	0	0	0	0	1	0	1	1	0	0	0	0	1
1	0	0	0	0	1	0	1	1	0	1	1	0	1	2
1	0	0	0	0	1	1	1	1	1	1	0	0	1	3
1	0	0	0	1	0	0	0	1	1	0	0	1	1	4
1	0	0	0	1	0	1	1	0	1	1	0	1	1	5
1	0	0	0	1	1	0	1	0	1	1	1	1	1	6
1	0	0	0	1	1	1	1	1	1	0	0	0	0	7
1	0	0	1	0	0	0	1	1	1	1	1	1	1	8
1	0	0	1	0	0	1	1	1	1	1	0	1	1	9
1	0	0	1	0	1	0	0	0	0	0	0	0	0	Blank
1	0	0	1	0	1	1	0	0	0	0	0	0	0	Blank
1	0	0	1	1	0	0	0	0	0	0	0	0	0	Blank
1	0	0	1	1	0	1	0	0	0	0	0	0	0	Blank
1	0	0	1	1	1	0	0	0	0	0	0	0	0	Blank
1	0	0	1	1	1	1	0	0	0	0	0	0	0	Blank
0	0	0	X	X	X	X	**							**
†	†	1	†				Inverse of Output Combinations Above							Display as above

X=Don't care.

†=Above combinations.

*=For liquid-crystal readouts, apply a square wave to Ph.
For common cathode LED readouts, select Ph=0.
For common anode LED readouts, select Ph=1.

**=Depends upon the BCD code previously applied when LD=1.

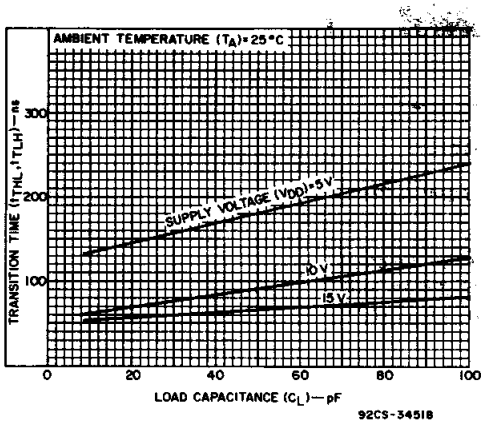


Fig. 7 - Typical transition time as a function of load capacitance.

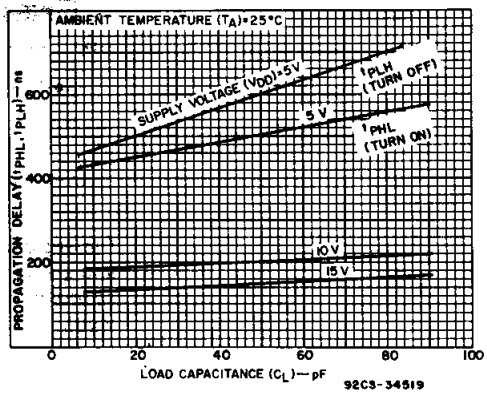


Fig. 8 - Typical propagation delay time as a function of load capacitance.

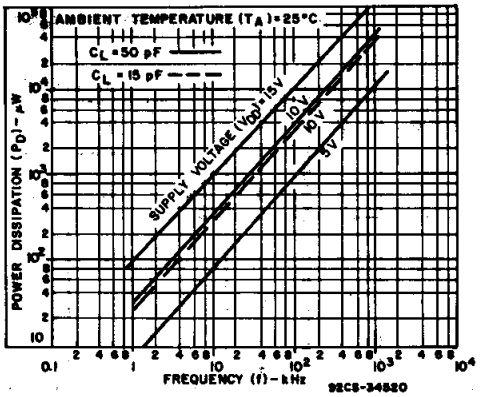


Fig. 9 – Typical dynamic power dissipation as a function of frequency.

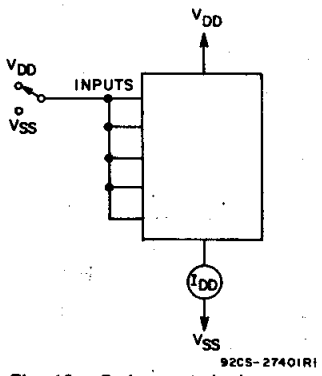


Fig. 10 – Quiescent device current test circuit.

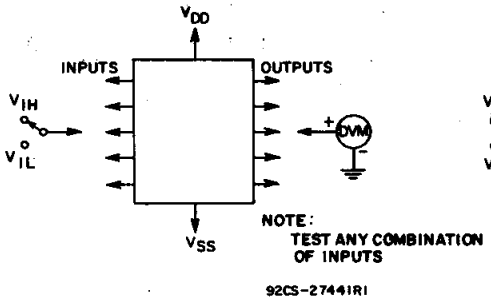


Fig. 11 – Input voltage test circuit.

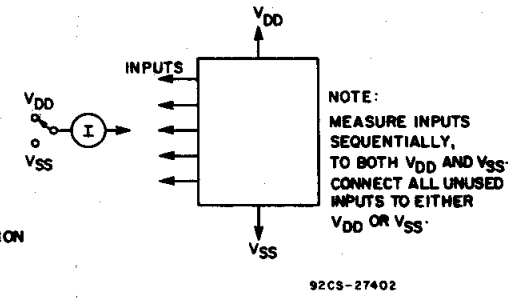
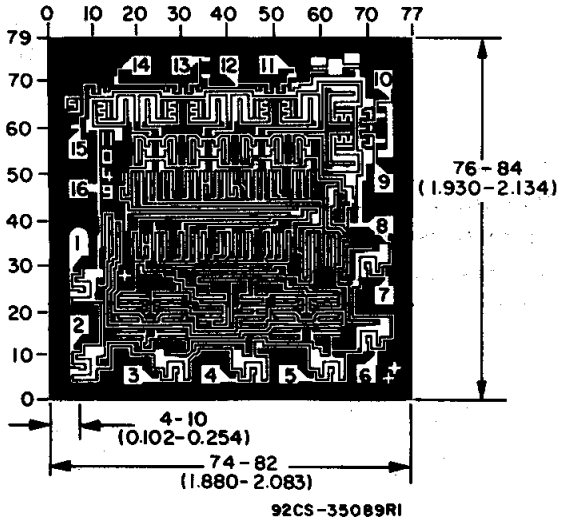


Fig. 12 – Input current test circuit.



Dimensions and pad layout for CD4543BH.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third–party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

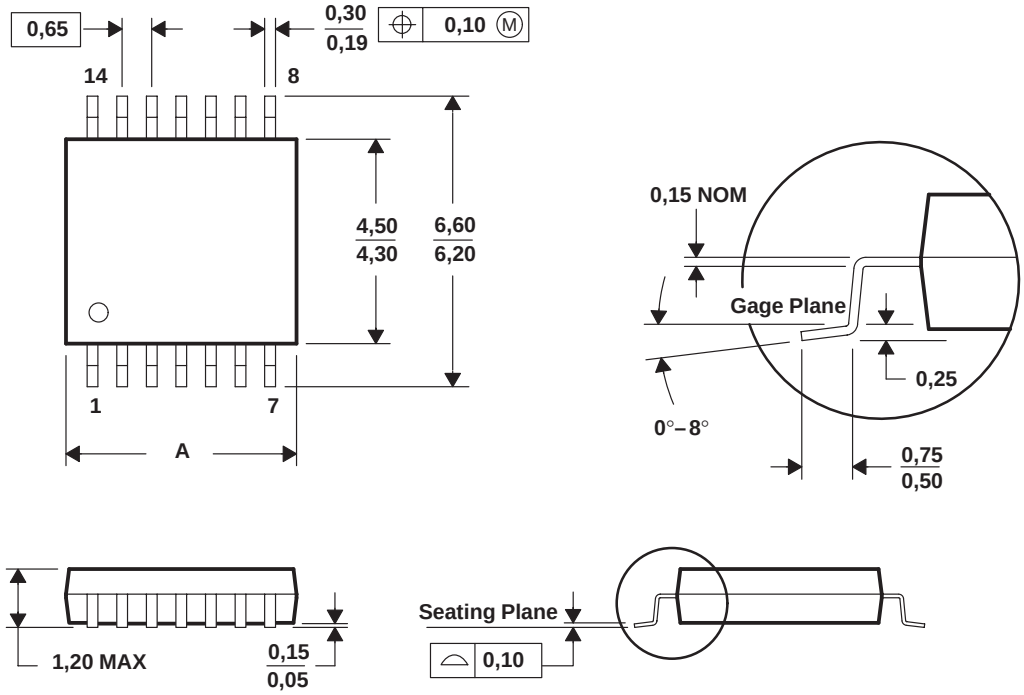
Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.

CD4543B, CMOS BCD-to-Seven-Segment Latch/Decoder/Driver for Liquid-Crystal Displays

DEVICE STATUS: **ACTIVE**

PARAMETER NAME	CD4543B
Voltage Nodes (V)	5, 10, 15

FEATURES

Back to Top

- Display blanking of all illegal input combinations
- Latch storage of code
- Capability of driving two low power TTL loads, two HTL loads, or one low power Schottky load over the full rated-temperature range
- Pin-for-pin replacement for the CD4056B (with pin 7 tied to V_{SS})
- Direct LED driving capability
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 uA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (full package-temperature range) =
  1 V at V_{DD} = 5 V
  2 V at V_{DD} = 10 V
  2.5 V at V_{DD} = 15 V
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"
- Applications:
  - Instrument display driver
  - Dashboard display driver
  - Computer/calculator display driver
  - Timing device driver (clocks, watches, timers)

DESCRIPTION

Back to Top

CD4543B is a BCD-to-seven segment latch/decoder/driver designed primarily for liquid-crystal display (LCD) applications. It is also capable of driving light emitting diode (LED), incandescent, gas-discharge, and fluorescent displays. This device is functionally similar to and serves as direct replacement for the CD4056B when pin 7 is connected to V_{SS}. It differs from the CD4056B in that it has a display blanking capability instead of a level-shifting function and requires only one power supply. When the CD4056B is used in the level shifting mode, two power supplies are required. When the CD4543B is used for LCD applications, a square wave must be applied to the PHASE input and the backplane of the LCD device. For LED applications a logic 1 is required at the PHASE input for common-cathode devices; a logic 0 is required for common-anode devices (see truth table).

The CD4543B is supplied in hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline package (NSR suffix), and in chip form (H suffix).

TECHNICAL RESOURCES

Back to Top

To view the following documents, Acrobat Reader 4.0 is required.

To download a document to your hard drive, right-click on the link and choose 'Save'.

Product Folder: CD4543B, CMOS BCD-to-Seven-Segment Latch/Decoder/Driver for Liquid-Crystal Displays

DATASHEET

Back to Top

Full datasheet in Acrobat PDF: cd4543b.pdf (256 KB,Rev.A) (Updated: 03/18/2002)

APPLICATION NOTES

Back to Top

View Application Reports for Digital Logic

- Evaluation of Nickel/Palladium/Gold-Finished Surface-Mount Integrated Circuits (SZZA026 - Updated: 06/20/2001)

RELATED DOCUMENTS

Back to Top

- Advanced Bus Interface Logic Selection Guide (SCYT126, 448 KB - Updated: 01/09/2001)
- Documentation Rules (SAP) And Ordering Information (Rev. B) (SZZU001B, 13 KB - Updated: 05/06/1999)
- Logic Selection Guide First Half 2002 (Rev. Q) (SDYU001Q, 3368 KB - Updated: 12/17/2001)
- MicroStar Junior BGA Design Summary (SCET004, 167 KB - Updated: 07/28/2000)
- Military Brief (SGYN138, 803 KB - Updated: 10/10/2000)
- Military Semiconductors Selection Guide 2002 (Rev. B) (SGYC003B, 1648 KB - Updated: 04/22/2002)
- More Power In Less Space - Technical Article (Rev. A) (SCAU001A, 850 KB - Updated: 03/01/1996)
- Overview of IEEE Std 91-1984, Explanation of Logic Symbols Training Booklet (Rev. A) (SDYZ001A, 138 KB - Updated: 07/01/1996)

SAMPLES

Back to Top

ORDERABLE DEVICE	PACKAGE	PINS	TEMP (°C)	STATUS	SAMPLES
CD4543BE	N	16	-55 TO 125	ACTIVE	Request Samples

PRICING/AVAILABILITY/PKG

Back to Top

ORDERABLE DEVICE	PACKAGE	PINS	TEMP (°C)	STATUS	BUDGETARY PRICE US$/UNIT QTY=1000+	PACK QTY	PRICING/AVAILABILITY/PKG
CD4543BE	N	16	-55 TO 125	ACTIVE	0.29	25	Check stock or order
CD4543BPWR	PW	16	-55 TO 125	ACTIVE	0.29	2000	Check stock or order

Table Data Updated on: 5/21/2002