- **Organization**
  TM124FBK32 . . . 1 048 576 × 32
  TM248GBK32 . . . 2 097 152 × 32
- **Single 5-V Power Supply**
- **72-pin Single In-Line Memory Module (SIMM) for Use With Sockets**
- **TM124FBK32 Utilizes Eight 4M-Bit Dynamic RAMs (DRAMs) in Plastic Small-Outline J-Lead (SOJ) Packages**
- **TM248GBK32 Utilizes Sixteen 4M-Bit DRAMs in Plastic SOJ Packages**
- **Long Refresh Period**
  16 ms (1024 Cycles)
- **All Inputs, Outputs, Clocks Fully TTL Compatible**
- **3-State Output**
- **Common $\overline{CAS}$ Control for Eight Common Data-In and Data-Out Lines, In Four Blocks**
- **Extended Data-Out (EDO) Operation With $\overline{CAS}$-Before-$\overline{RAS}$ (CBR), $\overline{RAS}$-Only, and Hidden Refresh**
- **JEDEC First Generation 72-Pin SIMM Pinout**
- **Presence Detect**
- **Performance Ranges:**

	ACCESS TIME t_{RAC} (MAX)	ACCESS TIME t_{AA} (MAX)	ACCESS TIME t_{CAC} (MIN)	EDO CYCLE t_{HPC} (MIN)
’124FBK32-60	60 ns	30 ns	15 ns	25 ns
’124FBK32-70	70 ns	35 ns	18 ns	30 ns
’124FBK32-80	80 ns	40 ns	20 ns	35 ns
’248GBK32-60	60 ns	30 ns	15 ns	25 ns
’248GBK32-70	70 ns	35 ns	18 ns	30 ns
’248GBK32-80	80 ns	40 ns	20 ns	35 ns

- **Low Power Dissipation**
- **Operating Free-Air Temperature Range . . . 0°C to 70°C**
- **Gold-Tabbed Versions Available:†**
  - **TM124FBK32**
  - **TM248GBK32**
- **Tin-Lead- (Solder-) Tabbed Versions Available:**
  - **TM124FBK32S**
  - **TM248GBK32S**

description

TM124FBK32

The TM124FBK32 is a 4M-byte DRAM organized as four times 1 048 576 × 8 in a 72-pin leadless SIMM. The SIMM is composed of eight TMS44409, 1 048 576 × 4-bit DRAMs, each in a 20/26-lead plastic SOJ package, mounted on a substrate together with decoupling capacitors. Each TMS44409 is described in the TMS44409 data sheet. The TM124FBK32 is available in the single-sided BK leadless module for use with sockets.

TM248GBK32

The TM248GBK32 is a 8M-byte DRAM organized as four times 2 097 152 × 8 in a 72-pin leadless SIMM. The SIMM is composed of sixteen TMS44409, 1 048 576 × 4-bit DRAMs, each in a 20/26-lead plastic SOJ package, mounted on a substrate together with decoupling capacitors. Each TMS44409 is described in the TMS44409 data sheet. The TM248GBK32 is available in the double-sided BK leadless module for use with sockets.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

† Part numbers in this data sheet are for the gold-tabbed version; the information applies to both gold-tabbed and solder-tabbed versions.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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operation

TM124FBK32

The TM124FBK32 operates as eight TMS44409DJs connected as shown in the functional block diagram. Refer to the TMS44409 data sheet for details of operation. The common I/O feature of the TM124FBK32 dictates the use of early write cycles to prevent contention on D and Q.

TM248GBK32

The TM248GBK32 operates as sixteen TMS44409DJs connected as shown in the functional block diagram. Refer to the TMS44409 data sheet for details of operation. The common I/O feature of the TM248GBK32 dictates the use of early write cycles to prevent contention on D and Q.

specifications

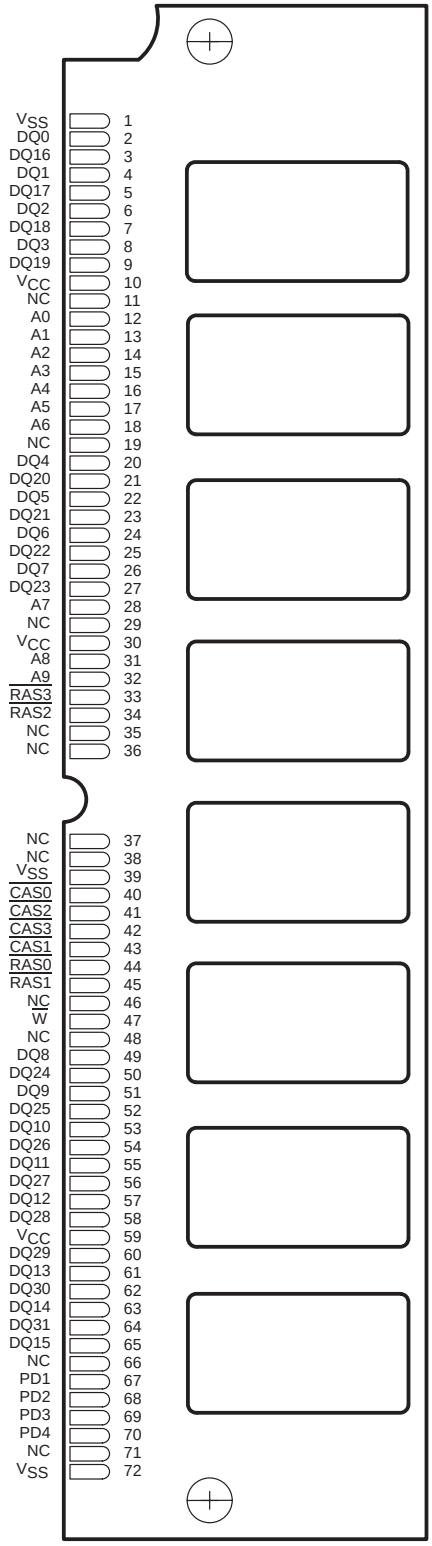
Refresh period is extended to 16 ms and, during this period, each of the 1024 rows must be strobed with $\overline{\text{RAS}}$ in order to retain data. A0–A9 address lines must be refreshed every 16 ms as required by the TMS44409 DRAM. $\overline{\text{CAS}}$ can remain high during the refresh sequence to conserve power.

single in-line memory module and components

PC substrate: 1,27 ± 0,1 mm (0.05 inch) nominal thickness; 0.005 inch/inch maximum warpage
Bypass capacitors: Multilayer ceramic
Contact area for TM124FBK32 and TM248GBK32: Nickel plate and gold plate over copper
Contact area for TM124FBK32S and TM248GBK32S: Nickel plate and tin-lead over copper

BK SINGLE IN-LINE PACKAGE†

(TOP VIEW)



TM124FBK32†

(SIDE VIEW)

TM248GBK32†

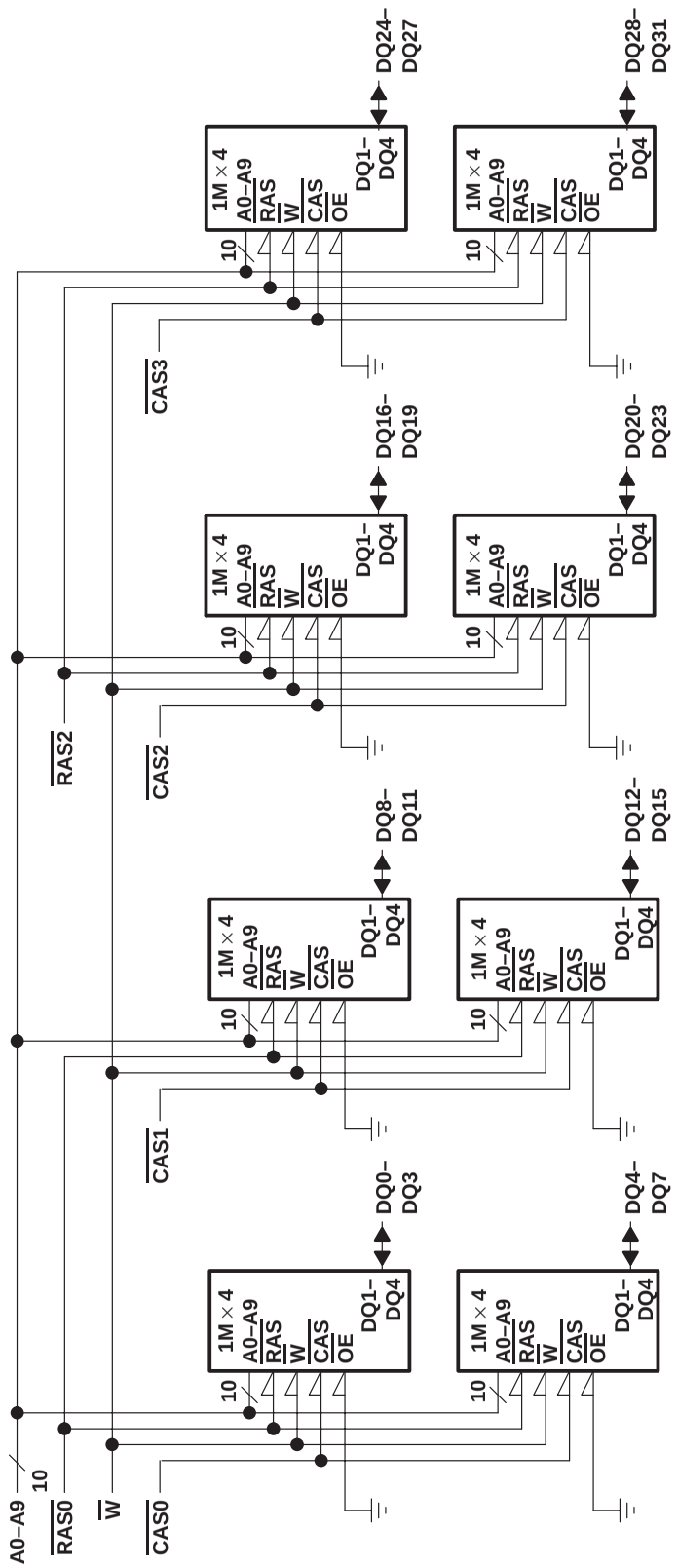
(SIDE VIEW)

PIN NOMENCLATURE	
A0–A9	Address Inputs
$\overline{CAS0}$, $\overline{CAS3}$	Column-Address Strobe
DQ0–DQ31	Data In/Data Out
NC	No Connection
PD1– PD4	Presence Detects
$\overline{RAS0}$–$\overline{RAS3}$	Row-Address Strobe
V_{CC}	5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

PRESENCE DETECT					
SIGNAL (PIN)		**PD1 (67)**	**PD2 (68)**	**PD3 (69)**	**PD4 (70)**
TM124FBK32	80 ns	V_{SS}	V_{SS}	NC	V_{SS}
	70 ns	V_{SS}	V_{SS}	V_{SS}	NC
	60 ns	V_{SS}	V_{SS}	NC	NC
TM248GBK32	80 ns	NC	NC	NC	V_{SS}
	70 ns	NC	NC	V_{SS}	NC
	60 ns	NC	NC	NC	NC

† The packages shown here are for pinout reference only and are not drawn to scale.

functional block diagram (for TM124FBK32 and TM248GBK32, Side 1)



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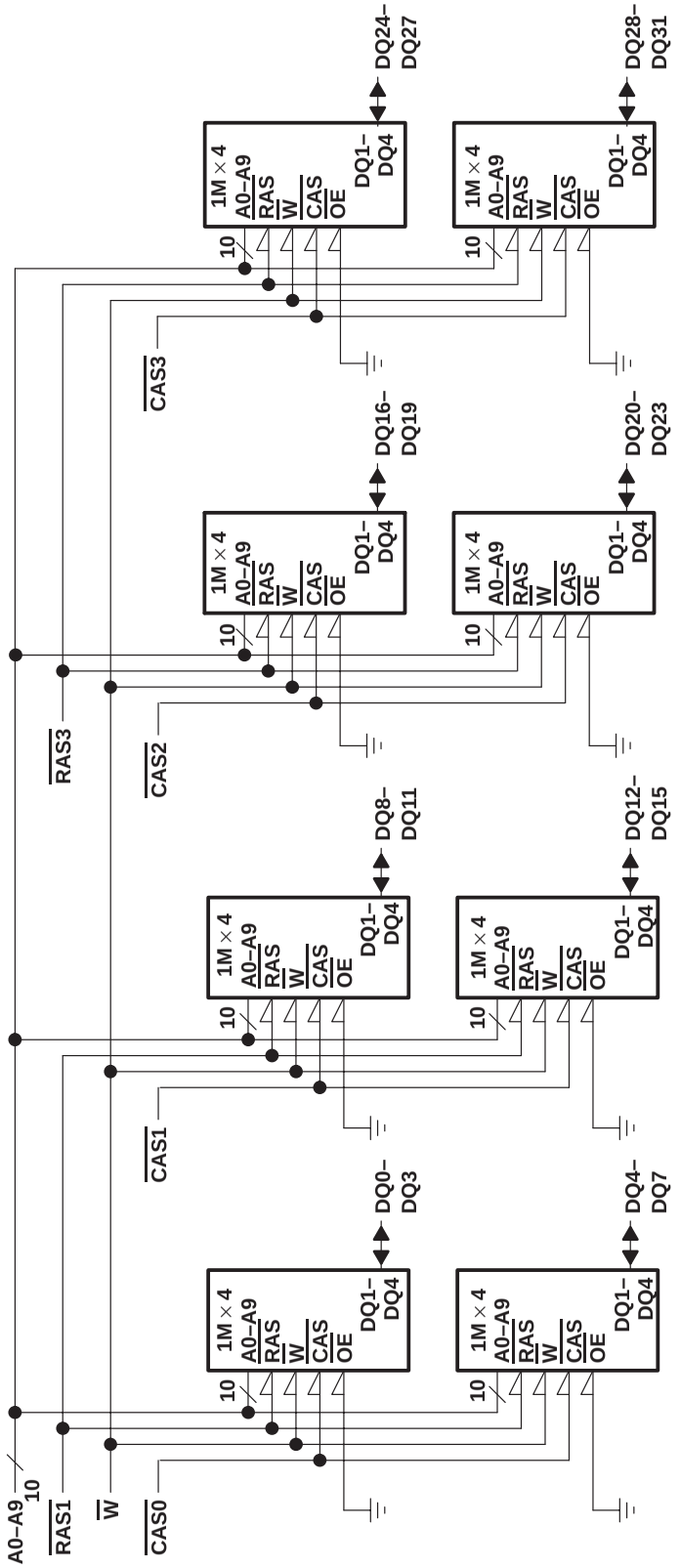
functional block diagram (for TM248GBK32, Side 2)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage range on any pin (see Note 1) . . . . . – 1 V to 7 V
Voltage range on V_{CC} (see Note 1) . . . . . – 1 V to 7 V
Short circuit output current . . . . . 50 mA
Power dissipation: TM124FBK32, TM124FBK32S . . . . . 8 W
TM248GBK32, TM248GBK32S . . . . . 16 W
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . – 55°C to 125°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	– 1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	'124FBK32-60		'124FBK32-70		'124FBK32-80		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_I = 0 to 6.5 V, V_{CC} = 5 V, All other pins = 0 to V_{CC}		±10		±10		±10	µA
I_O	Output current (leakage)	V_O = 0 to V_{CC}, V_{CC} = 5.5 V, $\overline{CAS}$ high		±10		±10		±10	µA
I_{CC1}	Read- or write-cycle current (see Note 3)	Minimum cycle, V_{CC} = 5.5 V		840		720		640	mA
I_{CC1}	Standby current	After one memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2.4 V (TTL)		16		16		16	mA
		After one memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = V_{CC} – 0.2 V (CMOS)		8		8		8	
I_{CC3}	Average refresh current ($\overline{RAS}$-only or CBR) (see Note 3)	Minimum cycle, V_{CC} = 5.5 V, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$-only), $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)		840		720		640	mA
I_{CC4}	Average page current (see Note 4)	t_{PC} = minimum, V_{CC} = 5.5 V, $\overline{RAS}$ low, $\overline{CAS}$ cycling		720		640		560	mA

NOTES: 3. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}.
4. Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	'248GBK32-60		'248GBK32-70		'248GBK32-80		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_I = 0 to 6.5 V, V_{CC} = 5 V, All other pins = 0 to V_{CC}		±20		±20		±20	µA
I_O	Output current (leakage)	V_O = 0 to V_{CC}, V_{CC} = 5.5 V, $\overline{CAS}$ high		±20		±20		±20	µA
I_{CC1}	Read- or write-cycle current (see Note 3)	Minimum cycle, V_{CC} = 5.5 V		856		736		656	mA
I_{CC1}	Standby current	After one memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2.4 V (TTL)		32		32		32	mA
		After one memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = V_{CC} – 0.2 V (CMOS)		16		16		16	
I_{CC3}	Average refresh current ($\overline{RAS}$-only or CBR) (see Note 3)	Minimum cycle, V_{CC} = 5.5 V, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$-only), $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)		1680		1440		1280	mA
I_{CC4}	Average EDO current (see Note 4)	t_{PC} = minimum, V_{CC} = 5.5 V, $\overline{RAS}$ low, $\overline{CAS}$ cycling		736		656		576	mA

NOTES: 3. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}.
4. Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}.

capacitance over recommended ranges of supply voltage and operating free-air temperature f = 1 MHz (see Note 5)

		'124FBK32		'248GBK32		UNIT
		MIN	MAX	MIN	MAX	
$C_{i(A)}$	Input capacitance, address inputs		40		80	pF
$C_{i(R)}$	Input capacitance, $\overline{RAS}$		28		28	pF
$C_{i(C)}$	Input capacitance, $\overline{CAS}$		14		28	pF
$C_{i(W)}$	Input capacitance, write-enable input		56		112	pF
$C_{o(DQ)}$	Output capacitance on DQ pins		7		14	pF

NOTE 5: V_{CC} equal to 5 V ± 0.5 V and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		'124FBK32-60 '248GBK32-60		'124FBK32-70 '248GBK32-70		'124FBK32-80 '248GBK32-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{AA}	Access time from column address		30		35		40	ns
t_{CAC}	Access time from $\overline{CAS}$ low		15		18		20	ns
t_{RAC}	Access time from $\overline{RAS}$ low		60		70		80	ns
t_{CPA}	Access time from column precharge		35		40		45	ns
t_{CLZ}	$\overline{CAS}$ to output in the low-impedance state	0		0		0		ns
t_{REZ}	Output disable time after $\overline{RAS}$ high (see Note 6)	3	15	3	18	3	20	ns
t_{WEZ}	Output disable time after $\overline{W}$ low (see Note 6)	3	15	3	18	3	20	ns

NOTE 6: t_{REZ} and t_{WEZ} are specified when the output is no longer driven.

EDO timing requirements over recommended ranges of supply voltage and operating free-air temperature

		'124FBK32-60 '248GBK32-60		'124FBK32-70 '248GBK32-70		'124FBK32-80 '248GBK32-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{HPC}	Cycle time, EDO page-mode read or write	25		30		35		ns
t_{PRWC}	Cycle time, EDO read-write	80		90		100		ns
t_{CSH}	Hold time, $\overline{CAS}$ from $\overline{RAS}$	50		55		60		ns
t_{DOH}	Hold time, output from $\overline{CAS}$	3		3		3		ns
t_{CAS}	Pulse duration, $\overline{CAS}$	10	10000	12	10000	15	10000	ns
t_{WPE}	Pulse duration, $\overline{W}$ (output disable only)	5		5		5		ns
t_{CP}	Precharge time, $\overline{CAS}$	5		5		5		ns

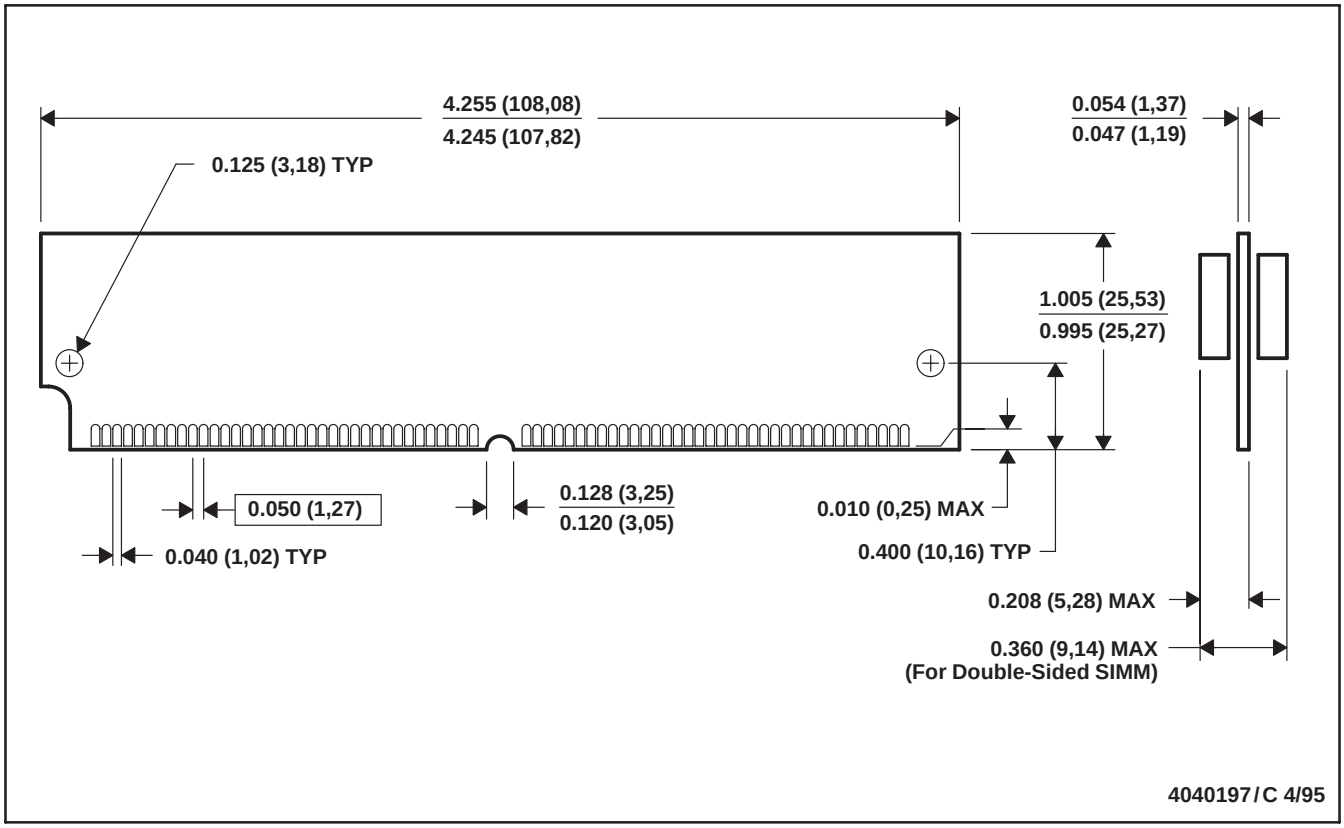
timing requirements over recommended range of supply voltage and operating free-air temperature

		'124FBK32-60 '248GBK32-60		'124FBK32-70 '248GBK32-70		'124FBK32-80 '248GBK32-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Cycle time, random read or write (see Note 7)	110		130		150		ns
t_{RWC}	Cycle time, read-write	150		175		200		ns
t_{RASP}	Pulse duration, page-mode, $\overline{RAS}$ low	60	100 000	70	100 000	80	100 000	ns
t_{RAS}	Pulse duration, non-page-mode, $\overline{RAS}$ low	60	10 000	70	10 000	80	10 000	ns
t_{RP}	Pulse duration, $\overline{RAS}$ high (precharge)	40		50		60		ns
t_{WP}	Pulse duration, $\overline{W}$ low	10		10		10		ns
t_{RASS}	Pulse duration, self-refresh entry from $\overline{RAS}$ low	100		100		100		µs
t_{RPS}	Pulse duration, $\overline{RAS}$ precharge after self-refresh	110		130		150		ns
t_{ASC}	Setup time, column address before $\overline{CAS}$ low	0		0		0		ns
t_{ASR}	Setup time, row address before $\overline{RAS}$ low	0		0		0		ns
t_{DS}	Setup time, data before $\overline{CAS}$ low	0		0		0		ns
t_{RCS}	Setup time, $\overline{W}$ high before $\overline{CAS}$ low	0		0		0		ns
t_{CWL}	Setup time, $\overline{W}$ low before $\overline{CAS}$ high	10		12		15		ns
t_{RWL}	Setup time, $\overline{W}$ low before $\overline{RAS}$ high	10		12		15		ns
t_{WCS}	Setup time, $\overline{W}$ low before $\overline{CAS}$ low	0		0		0		ns
t_{WRP}	Setup time, $\overline{W}$ high before $\overline{RAS}$ low (see Note 8)	10		10		10		ns
t_{CAH}	Hold time, column address after $\overline{CAS}$ low	10		15		15		ns
t_{DH}	Hold time, data after $\overline{CAS}$ low	10		15		15		ns
t_{RAH}	Hold time, row address after $\overline{RAS}$ low	10		10		10		ns
t_{RCH}	Hold time, $\overline{W}$ high after $\overline{CAS}$ high (see Note 9)	0		0		0		ns
t_{RRH}	Hold time, $\overline{W}$ high after $\overline{RAS}$ high (see Note 9)	0		0		0		ns
t_{WCH}	Hold time, $\overline{W}$ low after $\overline{CAS}$ low	10		15		15		ns
t_{WRH}	Hold time, $\overline{W}$ high after $\overline{RAS}$ low (see Note 8)	10		10		10		ns
t_{RHCP}	Hold time, $\overline{RAS}$ high from $\overline{CAS}$ precharge	35		40		45		ns
t_{CHS}	Hold time, $\overline{CAS}$ low after $\overline{RAS}$ high (self-refresh)	– 50		– 50		– 50		ns
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high (see Note 8)	10		10		10		ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	5		5		5		ns
t_{CSR}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low (see Note 8)	5		5		5		ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column address (see Note 10)	15	30	15	35	15	40	ns
t_{RAL}	Delay time, column address to $\overline{RAS}$ high	30		35		40		ns
t_{CAL}	Delay time, column address to $\overline{CAS}$ high	20		25		30		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 10)	20	45	20	52	20	60	ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low (CBR only)	0		0		0		ns
t_{RSH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	10		12		15		ns
t_{REF}	Refresh time interval		16		16		16	ms
t_T	Transition time	2	30	2	30	2	30	ns

NOTES: 7. All cycled times assume t_T = 5 ns.
8. $\overline{CBR}$ refresh only
9. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
10. Maximum value specified only to assure access time.

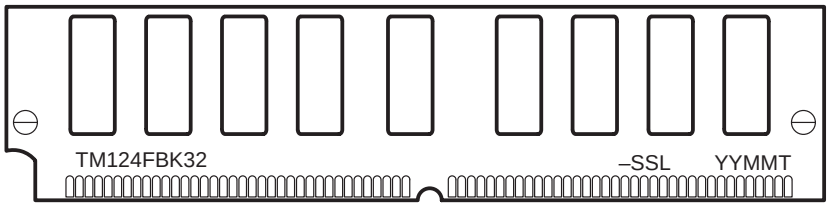
MECHANICAL DATA

BK (R-PSIM-N72) **SINGLE-IN-LINE MEMORY MODULE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.

device symbolization (TM124FBK32 illustrated)



YY = Year Code
MM = Month Code
T = Assembly Site Code
–SS = Speed Code
L = Temperature Range

NOTE: Location of symbolization may vary.

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