



GENERAL DESCRIPTION

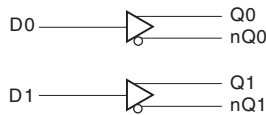


The ICS853P022 is a Dual LVCMOS / LVTTTL-to-Differential 3.3V LVPECL translator and a member of the HiPerClocks™ family of High Performance Clocks Solutions from ICS. The ICS853P022 has single ended clock inputs. The single ended clock input accepts LVCMOS or LVTTTL input levels and translate them to LVPECL levels. The small outline 8-pin TSSOP package makes this device ideal for applications where space, high performance and low power are important.

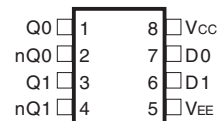
FEATURES

- 2 differential 3.3V LVPECL outputs
- LVCMOS/LVTTTL clock inputs
- Maximum output frequency: 1.1GHz
- Part-to-part skew: 650ps (maximum)
- Propagation Delay: 320ps (typical)
- Additive phase jitter, RMS: 0.03ps (typical)
- LVPECL mode operating voltage supply range:
 $V_{CC} = 3.0V$ to $3.8V$, $V_{EE} = 0V$
- ECL mode operating voltage supply range:
 $V_{CC} = 0V$, $V_{EE} = -3.8V$ to $-3.0V$
- $-40^{\circ}C$ to $85^{\circ}C$ ambient operating temperature
- Lead-Free package RoHS compliant

BLOCK DIAGRAM



PIN ASSIGNMENT



ICS853P022

8-Lead TSSOP, 118 mil

3mm x 3mm x 0.95mm package body

G Package

Top View

8-Lead SOIC, 150 mil

3.90mm x 4.90mm x 1.37mm package body

M Package

Top View



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ICS853P022
DUAL LVCMOS / LVTTTL-TO-DIFFERENTIAL
3.3V LVPECL TRANSLATOR

TABLE 1. PIN DESCRIPTIONS

| Number | Name | Type | Description |
|--------|-----------------|--------|--|
| 1, 2 | Q0, nQ0 | Output | Differential output pair. LVPECL interface levels. |
| 3, 4 | Q1, nQ1 | Output | Differential output pair. LVPECL interface levels. |
| 5 | V _{EE} | Power | Negative supply pin. |
| 6 | D1 | Input | LVCMOS / LVTTTL clock input. |
| 7 | D0 | Input | LVCMOS / LVTTTL clock input. |
| 8 | V _{CC} | Power | Positive supply pin. |



ABSOLUTE MAXIMUM RATINGS

| | |
|---|--|
| Supply Voltage, V_{CC} | 4.6V (LVPECL mode, $V_{EE} = 0$) |
| Negative Supply Voltage, V_{EE} | -4.6V (ECL mode, $V_{CC} = 0$) |
| Inputs, V_I (LVPECL mode) | -0.5V to $V_{CC} + 0.5V$ |
| Inputs, V_I (ECL mode) | 0.5V to $V_{EE} - 0.5V$ |
| Outputs, I_O | |
| Continuous Current | 50mA |
| Surge Current | 100mA |
| Operating Temperature Range, T_A | -40°C to +85°C |
| Storage Temperature, T_{STG} | -65°C to 150°C |
| Package Thermal Impedance, θ_{JA} (Junction-to-Ambient) | 101.7°C/W (0 m/s) TSSOP 112.7°C/W (0 lfpm) SOIC |

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 2A. POWER SUPPLY DC CHARACTERISTICS, $V_{CC} = 3.0V$ TO $3.8V$; $V_{EE} = 0V$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|----------|-------------------------|-----------------|---------|---------|---------|-------|
| V_{CC} | Positive Supply Voltage | | 3.0 | 3.3 | 3.8 | V |
| I_{EE} | Power Supply Current | | | | 35 | mA |

TABLE 2B. LVCMOS/LVTTTL DC CHARACTERISTICS, $V_{CC} = 3.0V$ TO $3.8V$; $V_{EE} = 0V$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|----------|--------------------|------------------------------|----------------|---------|----------------|---------|
| V_{IH} | Input High Voltage | | $0.7 * V_{CC}$ | | | V |
| V_{IL} | Input Low Voltage | | | | $0.3 * V_{CC}$ | V |
| I_{IH} | Input High Current | $V_{CC} = V_{IN} = 3.8V$ | | | 100 | μA |
| I_{IL} | Input Low Current | $V_{CC} = 3.8V, V_{IN} = 0V$ | | | -0.6 | mA |

TABLE 2C. LVPECL DC CHARACTERISTICS, $V_{CC} = 3.3V$; $V_{EE} = 0V$

| Symbol | Parameter | -40°C | | | 25°C | | | 85°C | | | Units |
|----------|-----------------------------|-------|-------|------|-------|-------|-------|-------|-------|-------|-------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| V_{OH} | Output High Voltage; NOTE 1 | 2.175 | 2.275 | 2.38 | 2.225 | 2.295 | 2.37 | 2.295 | 2.33 | 2.365 | V |
| V_{OL} | Output Low Voltage; NOTE 1 | 1.405 | 1.545 | 1.68 | 1.425 | 1.52 | 1.615 | 1.44 | 1.535 | 1.63 | V |

Output parameters vary 1:1 with V_{CC} . V_{CC} can vary +3.8V to 3.0V.

NOTE 1: Outputs terminated with 50 Ω to $V_{CC} - 2V$.



TABLE 2D. ECL DC CHARACTERISTICS, $V_{CC} = 0V$; $V_{EE} = -3.8V$ TO $-3.0V$

| Symbol | Parameter | -40°C | | | 25°C | | | 85°C | | | Units |
|----------|-----------------------------|--------|--------|-------|--------|--------|--------|--------|--------|--------|-------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| V_{OH} | Output High Voltage; NOTE 1 | -1.125 | -1.025 | -0.92 | -1.075 | -1.005 | -0.93 | -1.005 | -0.97 | -0.935 | V |
| V_{OL} | Output Low Voltage; NOTE 1 | -1.895 | -1.755 | -1.62 | -1.875 | -1.78 | -1.685 | -1.86 | -1.765 | -1.67 | V |

NOTE 1: Outputs terminated with 50Ω to $V_{CC} - 2V$.

TABLE 3. AC CHARACTERISTICS, $V_{CC} = 0V$; $V_{EE} = -3.8V$ TO $-3.0V$ OR $V_{CC} = 3.0V$ TO $3.8V$; $V_{EE} = 0V$

| Symbol | Parameter | -40°C | | | 25°C | | | 85°C | | | Units | |
|--------------|---|------------|------|-----|------|------|-----|------|------|-----|-------|----|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | | |
| f_{MAX} | Output Frequency | | | 1.1 | | | 1.1 | | | 1.1 | GHz | |
| tp_{LH} | Propagation Delay, Low to High; NOTE 1 | 125 | 320 | 600 | 180 | 320 | 475 | 190 | 300 | 410 | ps | |
| tp_{HL} | Propagation Delay, High to Low; NOTE 1 | 125 | 320 | 600 | 180 | 320 | 475 | 190 | 300 | 410 | ps | |
| $t_{sk(o)}$ | Output Skew; NOTE 2, 4 | | 12 | 55 | | 12 | 50 | | 12 | 50 | ps | |
| $t_{sk(pp)}$ | Part-to-Part Skew; NOTE 3, 4 | | | 330 | | | 225 | | | 225 | ps | |
| t_{jit} | Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter section | | 0.03 | | | 0.03 | | | 0.03 | | ps | |
| t_R/t_F | Output Rise/Fall Time | 20% to 80% | 85 | 200 | 315 | 100 | 200 | 285 | 85 | 200 | 315 | ps |

All parameters are measured $\leq 650MHz$ unless otherwise noted.

NOTE 1: Measured from the differential input crossing point to the differential output crossing point.

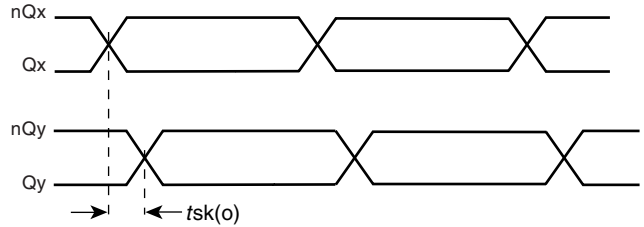
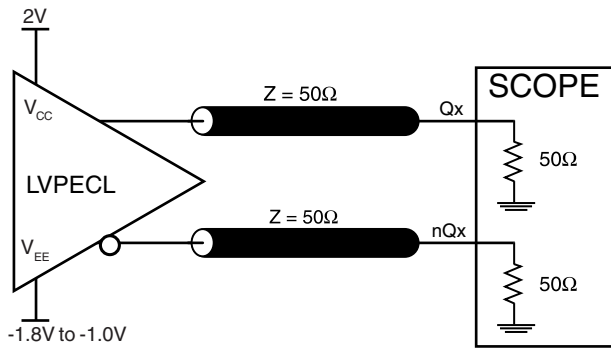
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.

NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.

NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

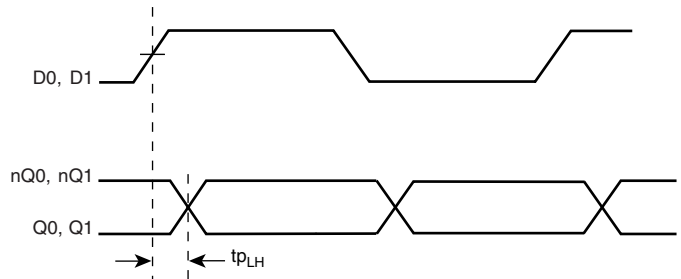
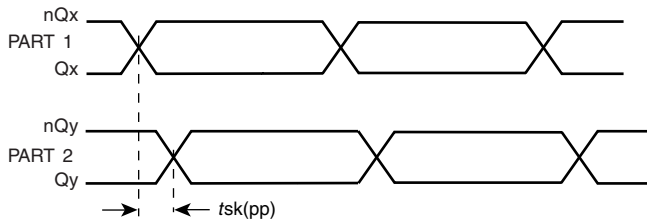


PARAMETER MEASUREMENT INFORMATION



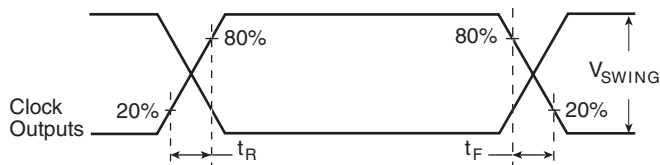
OUTPUT LOAD AC TEST CIRCUIT

OUTPUT SKEW



PART-TO-PART SKEW

PROPAGATION DELAY



OUTPUT RISE/FALL TIME



APPLICATION INFORMATION

TERMINATION FOR 3.3V LVPECL OUTPUTS

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive

50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 1A and 1B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

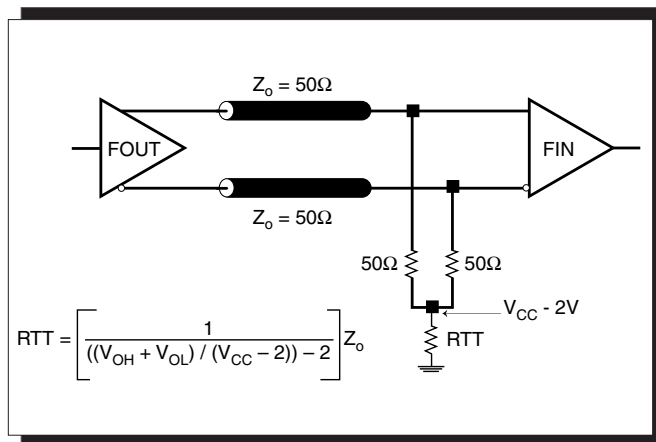


FIGURE 1A. LVPECL OUTPUT TERMINATION

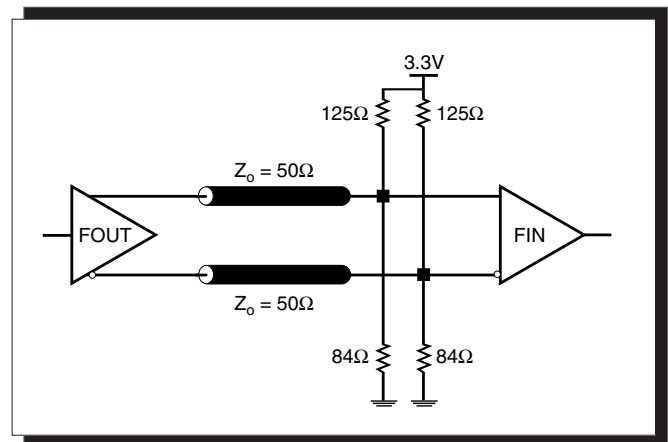


FIGURE 1B. LVPECL OUTPUT TERMINATION



POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS853P022. Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS853P022 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for $V_{CC} = 3.8V$, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)_{MAX} = $V_{CC_MAX} * I_{EE_MAX} = 3.8V * 35mA = 133mW$
- Power (outputs)_{MAX} = **30.94mW/Loaded Output pair**
If all outputs are loaded, the total power is $2 * 30.94mW = 61.88mW$

Total Power_{MAX} (3.8V, with all outputs switching) = $133mW + 61.88mW = 194.88mW$

2. Junction Temperature.

Junction temperature, T_j , is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for T_j is as follows: $T_j = \theta_{JA} * Pd_total + T_A$

T_j = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 1 meters per second and a multi-layer board, the appropriate value is 90.5°C/W per Table 4A below.

Therefore, T_j for an ambient temperature of 85°C with all outputs switching is:

$85^\circ C + 0.195W * 90.5^\circ C/W = 102.6^\circ C$. This is below the limit of 125°C.

This calculation is only an example. T_j will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

TABLE 4A. THERMAL RESISTANCE θ_{JA} FOR 8-PIN TSSOP, FORCED CONVECTION

| θ_{JA} by Velocity (Meters per Second) | | | |
|---|-----------|----------|----------|
| | 0 | 1 | 2 |
| Multi-Layer PCB, JEDEC Standard Test Boards | 101.7°C/W | 90.5°C/W | 89.8°C/W |

TABLE 4B. THERMAL RESISTANCE θ_{JA} FOR 8 LEAD SOIC

| θ_{JA} by Velocity (Linear Feet per Minute) | | | |
|--|-----------|-----------|-----------|
| | 0 | 200 | 500 |
| Single-Layer PCB, JEDEC Standard Test Boards | 153.3°C/W | 128.5°C/W | 115.5°C/W |
| Multi-Layer PCB, JEDEC Standard Test Boards | 112.7°C/W | 103.3°C/W | 97.1°C/W |

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.



3. Calculations and Equations.

LVPECL output driver circuit and termination are shown in Figure 4.

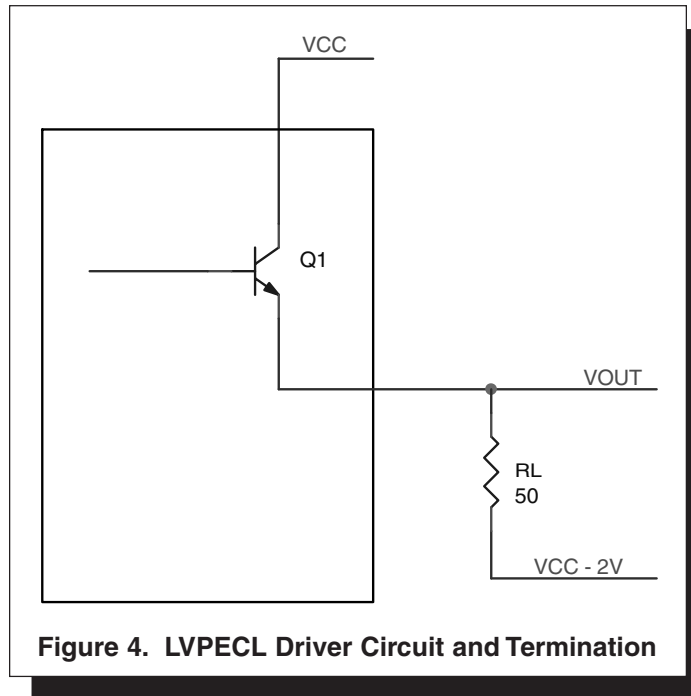


Figure 4. LVPECL Driver Circuit and Termination

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of $V_{CCO} - 2V$.

- For logic high, $V_{OUT} = V_{OH_MAX} = V_{CCO_MAX} - 0.935V$

$$(V_{CC_MAX} - V_{OH_MAX}) = 0.935V$$

- For logic low, $V_{OUT} = V_{OL_MAX} = V_{CCO_MAX} - 1.67V$

$$(V_{CCO_MAX} - V_{OL_MAX}) = 1.67V$$

$$Pd_H = [(V_{OH_MAX} - (V_{CCO_MAX} - 2V))/R_L] * (V_{CCO_MAX} - V_{OH_MAX}) = [(2V - (V_{CCO_MAX} - V_{OH_MAX}))/R_L] * (V_{CCO_MAX} - V_{OH_MAX}) = [(2V - 0.935V)/50\Omega] * 0.935V = 19.92mW$$

$$Pd_L = [(V_{OL_MAX} - (V_{CCO_MAX} - 2V))/R_L] * (V_{CCO_MAX} - V_{OL_MAX}) = [(2V - (V_{CCO_MAX} - V_{OL_MAX}))/R_L] * (V_{CCO_MAX} - V_{OL_MAX}) = [(2V - 1.67V)/50\Omega] * 1.67V = 11.02mW$$

$$\text{Total Power Dissipation per output pair} = Pd_H + Pd_L = 30.94mW$$



RELIABILITY INFORMATION

TABLE 5A. θ_{JA} vs. AIR FLOW TABLE FOR 8 LEAD TSSOP

| θ_{JA} by Velocity (Meters per Second) | | | |
|---|-----------|----------|----------|
| | 0 | 1 | 2 |
| Multi-Layer PCB, JEDEC Standard Test Boards | 101.7°C/W | 90.5°C/W | 89.8°C/W |

TABLE 5B. θ_{JA} vs. AIR FLOW TABLE FOR 8 LEAD SOIC

| θ_{JA} by Velocity (Linear Feet per Minute) | | | |
|--|-----------|-----------|-----------|
| | 0 | 200 | 500 |
| Single-Layer PCB, JEDEC Standard Test Boards | 153.3°C/W | 128.5°C/W | 115.5°C/W |
| Multi-Layer PCB, JEDEC Standard Test Boards | 112.7°C/W | 103.3°C/W | 97.1°C/W |

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

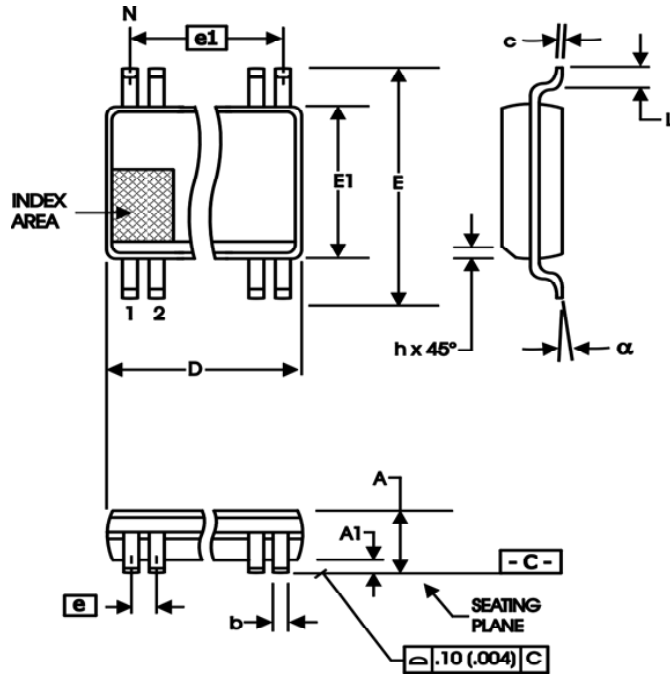
TRANSISTOR COUNT

The transistor count for ICS853P022 is: 92

Pin compatible with MC100EPT22



PACKAGE OUTLINE - G SUFFIX FOR 8 LEAD TSSOP



PACKAGE OUTLINE - M SUFFIX FOR 8 LEAD SOIC

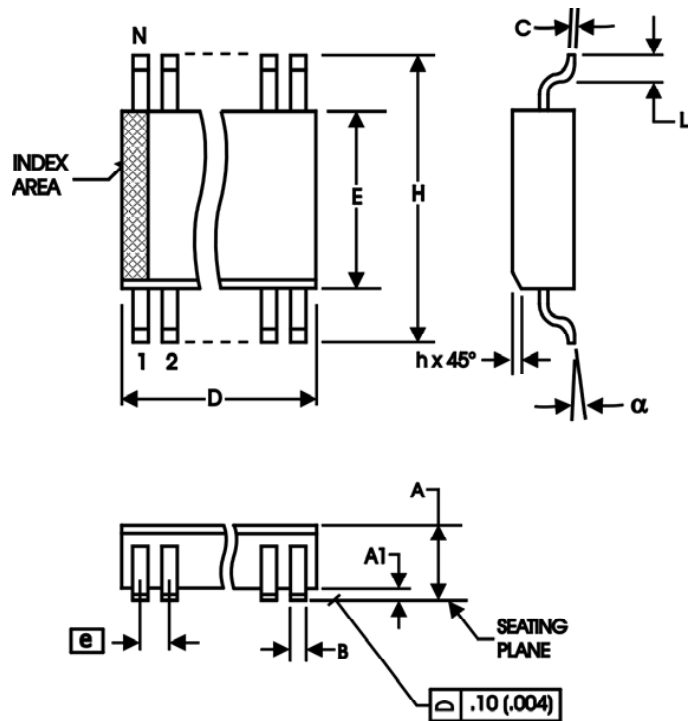


TABLE 6A. PACKAGE DIMENSIONS

| SYMBOL | Millimeters | |
|----------|-------------|---------|
| | Minimum | Maximum |
| N | 8 | |
| A | -- | 1.10 |
| A1 | 0 | 0.15 |
| A2 | 0.79 | 0.97 |
| b | 0.22 | 0.38 |
| c | 0.08 | 0.23 |
| D | 3.00 BASIC | |
| E | 4.90 BASIC | |
| E1 | 3.00 BASIC | |
| e | 0.65 BASIC | |
| e1 | 1.95 BASIC | |
| L | 0.40 | 0.80 |
| α | 0° | 8° |
| aaa | -- | 0.10 |

Reference Document: JEDEC Publication 95, MO-187

TABLE 6B. PACKAGE DIMENSIONS

| SYMBOL | Millimeters | |
|----------|-------------|---------|
| | MINIMUM | MAXIMUM |
| N | 8 | |
| A | 1.35 | 1.75 |
| A1 | 0.10 | 0.25 |
| B | 0.33 | 0.51 |
| C | 0.19 | 0.25 |
| D | 4.80 | 5.00 |
| E | 3.80 | 4.00 |
| e | 1.27 BASIC | |
| H | 5.80 | 6.20 |
| h | 0.25 | 0.50 |
| L | 0.40 | 1.27 |
| α | 0° | 8° |



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ICS853P022

DUAL LVCMOS / LVTTTL-TO-DIFFERENTIAL 3.3V LVPECL TRANSLATOR

TABLE 7. ORDERING INFORMATION

| Part/Order Number | Marking | Package | Count | Temperature |
|-------------------|----------|--|-------------|---------------|
| ICS853P022AG | P22A | 8 lead TSSOP | 96 per tube | -40°C to 85°C |
| ICS853P022AGT | P22A | 8 lead TSSOP on Tape and Reel | 2500 | -40°C to 85°C |
| ICS853P022AGLF | P2AL | 8 lead "Lead-Free" TSSOP | 96 per tube | -40°C to 85°C |
| ICS853P022AGLFT | P2AL | 8 lead "Lead-Free" TSSO on Tape and Reel | 2500 | -40°C to 85°C |
| ICS853P022AM | 53P022A | 8 lead SOIC | 96 per tube | -40°C to 85°C |
| ICS853P022AMT | 53P022A | 8 lead SOIC on Tape and Reel | 2500 | -40°C to 85°C |
| ICS853P022AMLF | 53P022AL | 8 lead "Lead-Free" SOIC | 96 per tube | -40°C to 85°C |
| ICS853P022AMLFT | 53P022AL | 8 lead "Lead-Free" SOIC on Tape and Reel | 2500 | -40°C to 85°C |

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