

# T6L52

## Gate Driver for TFT LCD Panel

The T6L52 is a 258-channel output gate driver for TFT LCD panels. In addition to three output voltage levels available, this device accepts external input of the panel drive voltage. These features make this device ideal for the S-XGA and XGA-compatible TFT LCD panel drive systems.

The T6L52 offers high integration circuit due to CMOS technology.

### Features

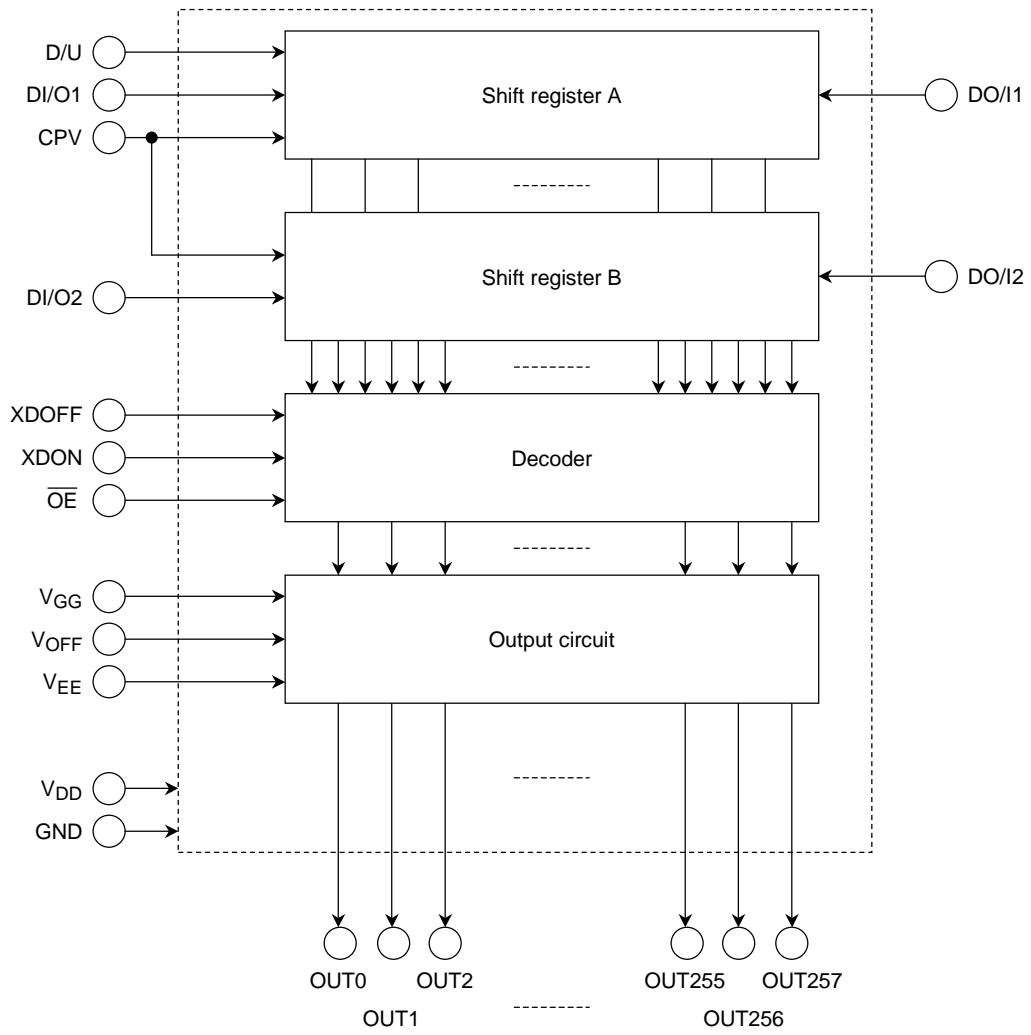
- LCD drive output pins: 258 pins (including two dummy line drive channels)
- Data transfer method : Bidirectional shift register
- Package : Tape carrier package (TCP)
- Built-in input signal level-shifting circuit

Unit: mm		
T6L52	User Area Pitch	
	IN	OUT

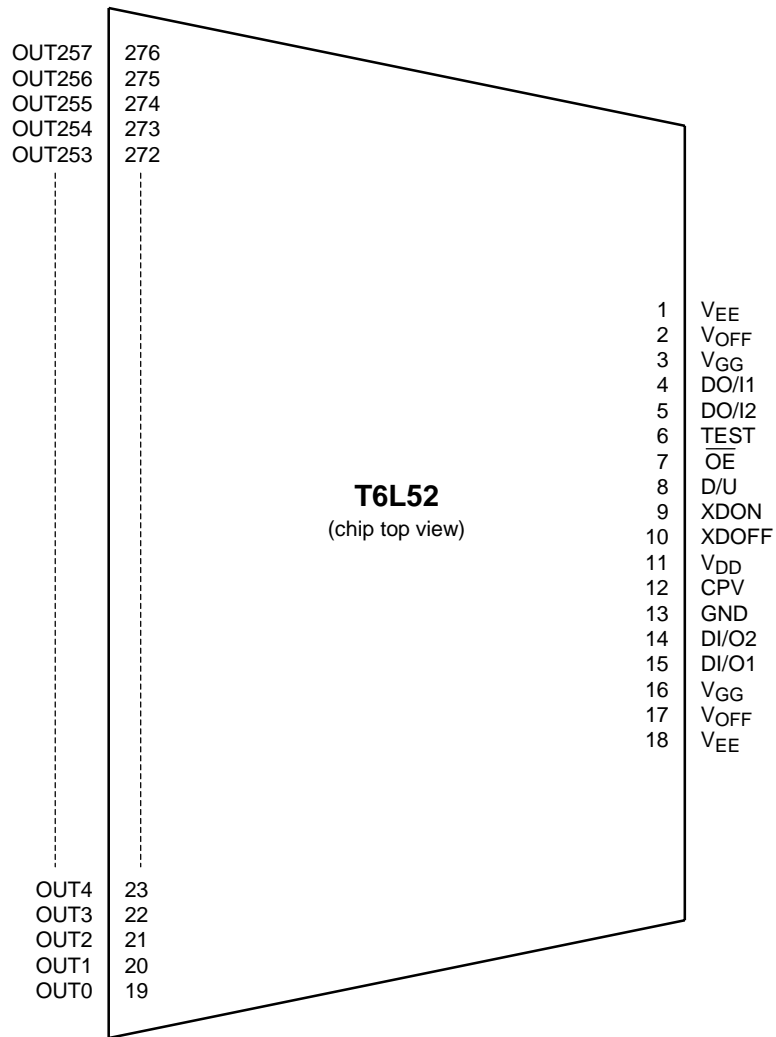
Please contact Toshiba or an authorized Toshiba dealer for the latest TCP specification and product lineup.

TCP (Tape Carrier Package)

**Block Diagram**



**Pin Assignment**



The above diagram shows the device's pin configuration only and does not necessarily correspond to the pad layout on the chip. Please contact Toshiba or our distributors for the latest TCP specification.

## Pin Description

Pin Name	I/O	Function
DI/O1 DO/I1 DI/O2 DO/I2	I/O	Vertical shift data input/output pins These pins are used to input and output shift data. The function of these pins is switched for input or output by D/U as shown below. When set for input The data is latched into the internal shift registers synchronously with the rising edge of CPV. When set for output When two or more T6L52s are cascaded, this pin outputs the data to be fed into the next stage.
D/U	I	Transfer direction select pin This pin specifies the direction in which data is transferred through the shift registers. When D/U = Low, data is shifted in the direction D/U = "L": OUT0 → OUT1 → OUT3 ... → OUT256 → OUT257 When D/U=High, the direction is reversed to give. D/U = "H": OUT257 → OUT256 → OUT255 ... → OUT1 → OUT0 The voltage applied to this pin must be a DC-level voltage that is either High (V <sub>DD</sub> ) or Low (GND).
CPV	I	Vertical shift clock This is the shift clock for the shift registers. The data in shift registers A and B are shifted synchronously with each rising edge of CPV.
$\overline{OE}$	I	Output-fixing input pin When $\overline{OE}$ = High, the LCD drive output V <sub>GG</sub> level is fixed to V <sub>EE</sub> while CPV is High. This pin is only valid during the V <sub>GG</sub> level output. The voltage applied to this pin must be a DC-level voltage that is either V <sub>DD</sub> or GND.
XDOFF	I	Display-OFF input pin When XDOFF = Low, the V <sub>OFF</sub> voltage is output all output pins irrespective of the shift data and the content of input data. However, this does not cause the contents of the shift registers to be cleared. XDOFF operates asynchronously with CPV.
XDON	I	Display-ON input pin When XDON = Low, the V <sub>GG</sub> voltage is output all output pins irrespective of the shift data and the content of input data. However, this does not cause the contents of the shift registers to be cleared. XDON does not operate asynchronously with CPV. XDON is pull-up registered to V <sub>DD</sub> . Note: If XDON = Low, it must be V <sub>GG</sub> - V <sub>EE</sub> = below 38 V. Connect the external resistor above 62 Ω to V <sub>GG</sub> line, and above 100 Ω to V <sub>OFF</sub> line. Please contact a Toshiba dealer before using this pin.
TEST	I	Test pin Leave this pin open.
OUT0 to OUT257	O	LCD panel drive pins
V <sub>GG</sub>		Power supply for LCD drive
V <sub>OFF</sub>		LCD-OFF level input pin
V <sub>EE</sub>		Power supply for LCD drive
V <sub>DD</sub>		Power supply for the internal logic
GND		Power supply for the internal logic

\*: If XDON, XDOFF, and  $\overline{OE}$  are asserted simultanceously, they are accepted in order of XDON, XDOFF, and  $\overline{OE}$ .

## Operation Description

### (1) Shift data transfer method

D/U Pin	Shift Data Input		Data Transfer Direction
	Input	Output	
L	DI/O1	DO/I1	OUT0 → OUT1 → OUT2 → OUT3 → ... → OUT256 → OUT257
	DI/O2	DO/I2	
H	DO/I1	DI/O1	OUT257 → OUT256 → OUT255 → OUT254 → ... → OUT2 → OUT1 → OUT0
	DO/I2	DI/O2	

### (2) LCD panel drive outputs

Except for the first output, the LCD panel drive outputs are controlled by the data in shift registers A and B and the input signals XDON, XDOFF, and  $\overline{OE}$  as shown below.

A	B	XDON	XDOFF	$\overline{OE}$	LCD Panel Drive Output
L	L	H	H	L	V <sub>OFF</sub>
L	H	H	H	L	V <sub>EE</sub>
H	L	H	H	L	V <sub>EE</sub>
H	H	H	H	L	V <sub>GG</sub>
X	X	H	L	X	V <sub>OFF</sub>
L	L	H	H	H	V <sub>OFF</sub>
L	H	H	H	H	V <sub>EE</sub>
H	L	H	H	H	V <sub>EE</sub>
H	H	H	H	H	V <sub>EE</sub> (When CPV = high) V <sub>GG</sub> (When CPV = low)
X	X	L	X	X	V <sub>GG</sub>

X: Don't care

### (3) First LCD panel drive output

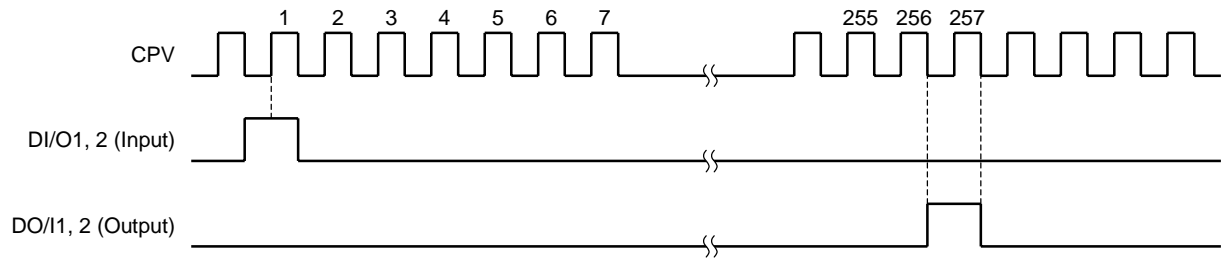
The first output (OUT0, OUT257) is output to the LCD according to the shift data (A1, B1/A256, B256) that respectively controls output 1 and output 256 as shown below.

The first output here means OUT0 when D/U = low and OUT257 when D/U = high.

D/U = "L"			D/U = "H"		
A1	B1	OUT0	A256	B256	OUT257
L	L	V <sub>OFF</sub>	L	L	V <sub>OFF</sub>
L	H	V <sub>EE</sub>	L	H	V <sub>EE</sub>
H	L	V <sub>EE</sub>	H	L	V <sub>EE</sub>
H	H	V <sub>EE</sub>	H	H	V <sub>EE</sub>

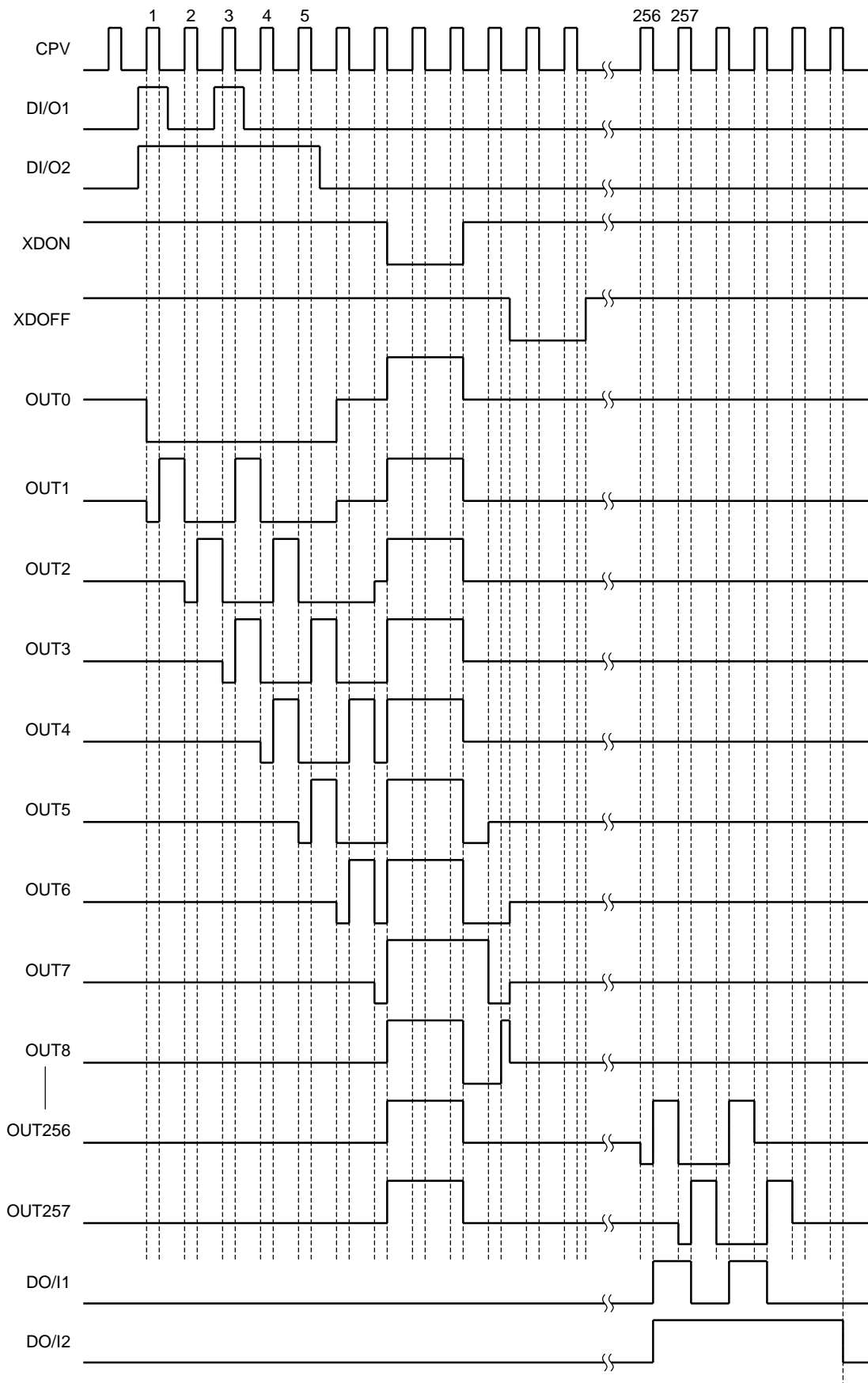
**(4) Vertical shift data output**

The vertical shift data output (When VDD = high level, when GND = low level) is latched into the LCD synchronously with the falling edge of the last valid shift data (OUT256 or OUT1).



## Timing Diagram

- When  $D/U = \text{low}$   
When  $\overline{OE} = \text{high}$



## Absolute Maximum Ratings (GND = 0 V)

Characteristics	Symbol	Rating	Unit	Relevant Pin
Supply voltage (1)	$V_{GG} - V_{EE}$	-0.3 to 48	V	
Supply voltage (2)	$V_{EE}$	-20 to 0.3		
Supply voltage (3)	$V_{DD}$	-0.3 to 6.0		
Input voltage	$V_{IN}$	GND to $V_{DD} + 0.3$	V	
Analog input voltage	$V_{OFF}$	$V_{EE} - 0.3$ to $V_{GG} + 0.3$	V	
Storage temperature	$T_{stg}$	-55 to 125	°C	

## Recommended Operating Conditions (GND = 0 V)

Characteristics	Symbol	Rating	Unit	Note
Supply voltage (1)	$V_{GG} - V_{EE}$	20 to 42	V	When XDON is fixed to high level.
		20 to 38		When XDON is enabled.
Supply voltage (2)	$V_{EE}$	-15 to -5		
Supply voltage (3)	$V_{DD}$	2.7 to 3.6		
Supply voltage (4)	$V_{GG}$	10 to 28		
Operating temperature	$T_{opr}$	-20 to 75	°C	
Operating frequency	$f_{CPV}$	DC to 100	kHz	
Output load capacitance	$C_L$	300	pF/PIN	
Analog input voltage	$V_{OFF}$	$V_{EE}$ to $V_{EE} + 10$	V	

## Electrical Characteristics

### DC Characteristics (GND = 0 V, V<sub>DD</sub> = 2.7 to 3.6 V, Ta = -20 to 75°C)

Characteristics		Symbol	Test circuit	Test Condition	Min	Max	Unit	Relevant Pin
Input voltage	Low level	V <sub>IL</sub>	—	—	GND	0.2 × V <sub>DD</sub>	V	(Note 1)
	High level	V <sub>IH</sub>		—	0.8 × V <sub>DD</sub>	V <sub>DD</sub>		
Output voltage	Low level	V <sub>OL</sub>	—	I <sub>OL</sub> = 40 μA	GND	0.4	V	DI/O1, DI/O2, DO/I1, DO/I2
	High level	V <sub>OH</sub>		I <sub>OH</sub> = -40 μA	V <sub>DD</sub> - 0.4	V <sub>DD</sub>		
Output resistance	V <sub>EE</sub> level	R <sub>EE</sub>	—	V <sub>OUT</sub> = V <sub>EE</sub> + 0.5 V (Note 2)	—	1.0	kΩ	OUT0~OUT257
	V <sub>OFF</sub> level	R <sub>OFF</sub>		V <sub>OUT</sub> = V <sub>OFF</sub> + 0.5 V (Note 2)				
	V <sub>GGV</sub>	R <sub>GG</sub>		V <sub>OUT</sub> = V <sub>GG</sub> - 0.5 V (Note 2)				
Input leakage current		I <sub>IN</sub>	—	—	-1.0	1.0	μA	(Note 1)
Current consumption (1)		I <sub>DD</sub>	—	(Note 3)	—	500	μA	V <sub>DD</sub>
Current consumption (2)		I <sub>GG</sub>	—	(Note 3)	—	100	μA	V <sub>GG</sub>
Current consumption (3)		I <sub>GND</sub>	—	(Note 3)	—	100	μA	GND

Note 1: DI/O1, DI/O2, DO/I1, DO/I2, CPV, D/U, XDON, XDOFF,  $\overline{OE}$

Note 2: V<sub>GG</sub> = 25 V, V<sub>OFF</sub> = 0 V, V<sub>EE</sub> = -10 V

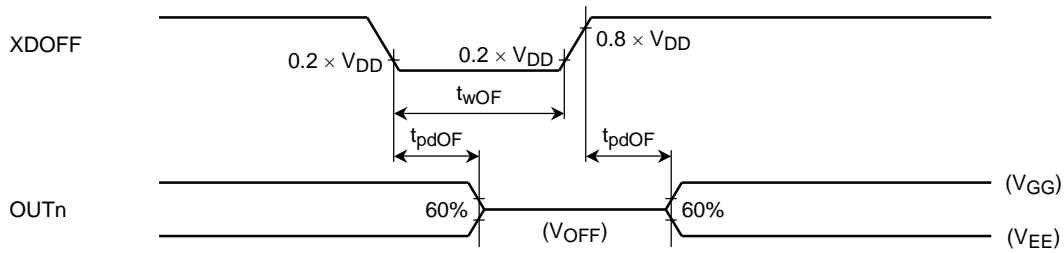
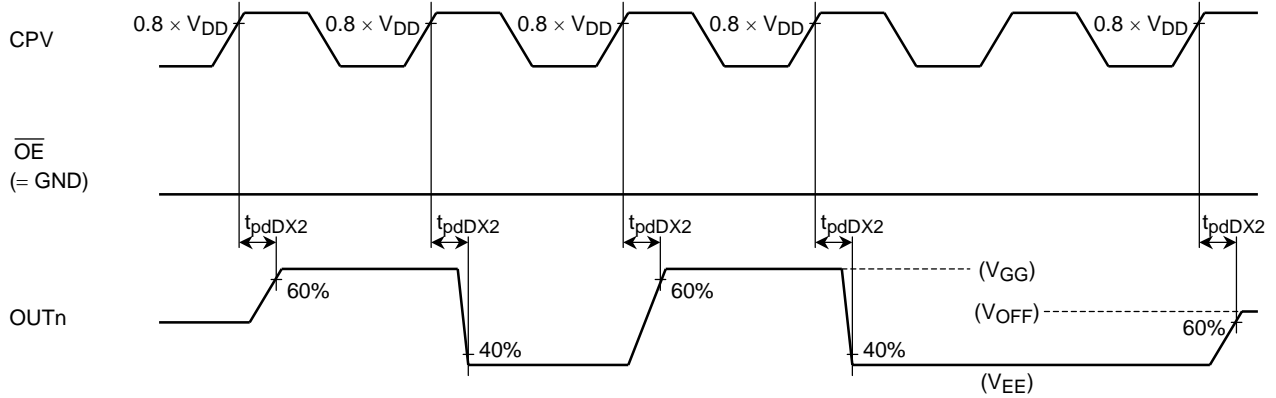
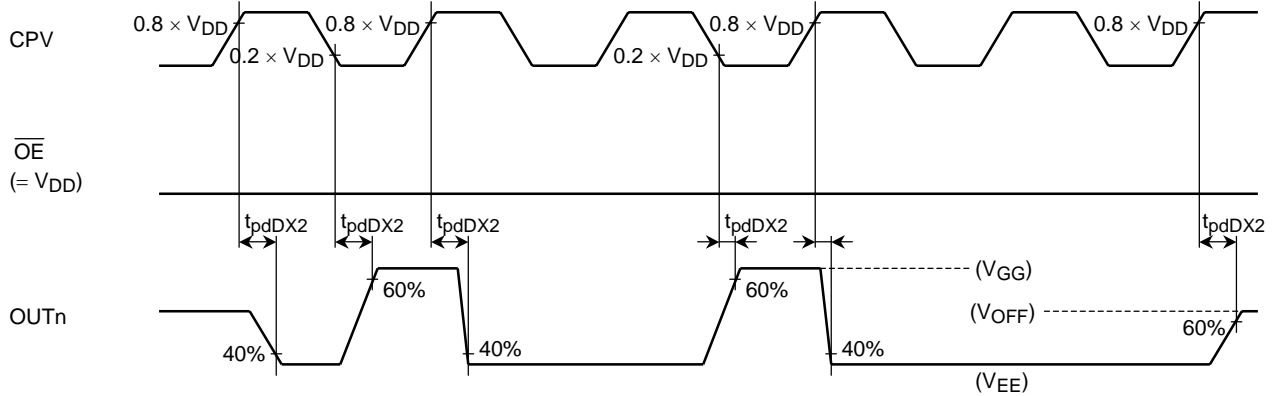
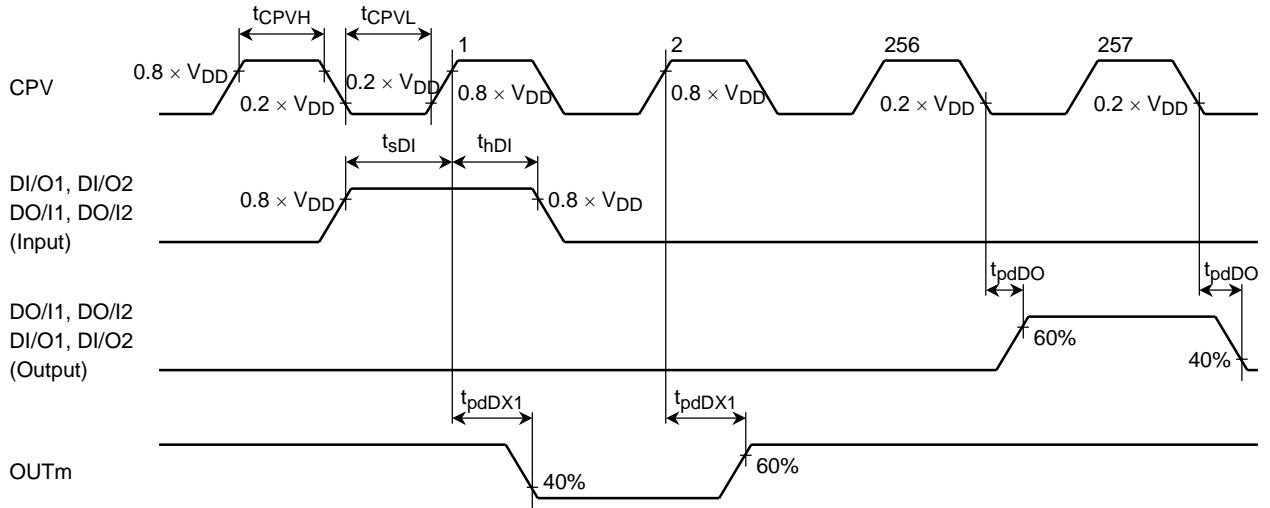
Note 3: CPV = 50 kHz, shift data input cycle = 60 Hz

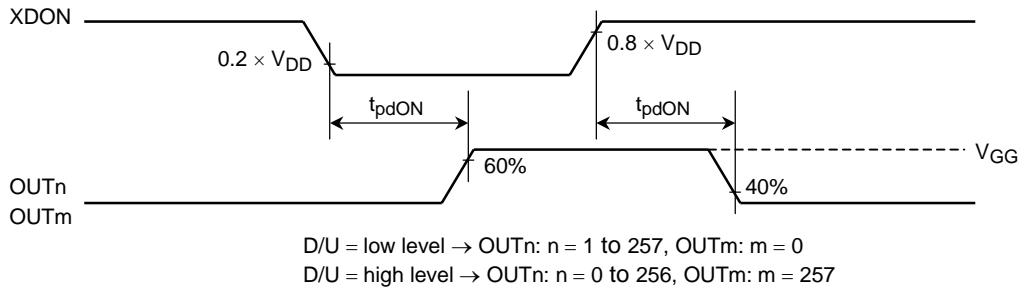
### AC Characteristics (GND = 0 V, V<sub>DD</sub> = 2.7 to 3.6 V, Ta = -20 to 75°C)

Characteristics	Symbol	Test circuit	Test Condition	Min	Max	Unit	
Clock period	t <sub>CPV</sub>	—	—	10	—	μs	
Clock pulse L	t <sub>CPVL</sub>	—	—	4	—	μs	
Clock pulse H	t <sub>CPVH</sub>	—	—	1	—	μs	
Data setup time	t <sub>sDI</sub>	—	Ta = -20°C	1.3	—	μs	
			Ta = 0°C	1.0	—		
Data setup time	t <sub>hDI</sub>	—	—	0.5	—	ns	
Output delay time (1)	t <sub>pdDO</sub>	—	C <sub>L</sub> = 15 pF (Note 4)	—	1.0	μs	
Output delay time (2)	t <sub>pdDX1</sub>	—	C <sub>L</sub> = 300 pF (Note 4)	Ta = -20°C	—		1.6
				Ta = 0°C	—		1.0
Output delay time (3)	t <sub>pdDX2</sub>	—	C <sub>L</sub> = 300 pF (Note 4)	Ta = -20°C	—		1.6
				Ta = 0°C	—		1.0
Output delay time (4)	t <sub>pdOF</sub>	—	C <sub>L</sub> = 300 pF (Note 4)	—	1.0		
Output delay time (5)	t <sub>pdON</sub>	—	C <sub>L</sub> = 300 pF (Note 4) (Note 5)	—	10		
Display-off pulse	t <sub>wOF</sub>	—	—	1	—	μs	

Note 4: V<sub>GG</sub> = 20 to 28 V, V<sub>EE</sub> = -15 to -6 V, V<sub>OFF</sub> = V<sub>EE</sub> + 3 V to V<sub>EE</sub> + 7 V, but V<sub>GG</sub> - V<sub>EE</sub> = below 42 V.

Note 5: V<sub>GG</sub> - V<sub>EE</sub> = below 38 V. Connect the external resistor above 62 Ω to V<sub>GG</sub> line, and above 100 Ω to V<sub>OFF</sub> line.

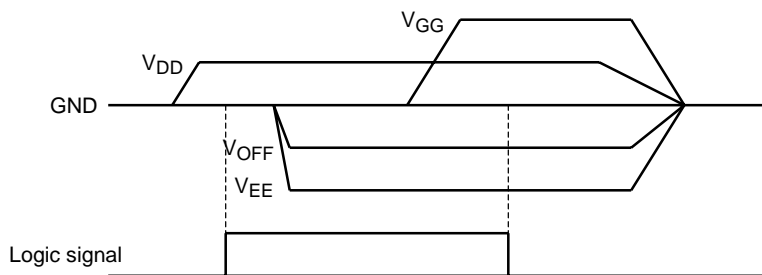




**Power Supply Sequence**

When the device is power ON,  $V_{DD} \rightarrow$  logic signal  $\rightarrow V_{EE}$ ,  $V_{OFF} \rightarrow V_{GG}$ ; when power OFF, logic signal  $V_{DD} \rightarrow V_{EE}$ ,  $V_{OFF}$ ,  $V_{GG}$ .

However, the relative potentials when the power is turned OFF are  $V_{GG} \geq V_{DD} \geq V_{OFF} \geq V_{EE}$ .



\*: The above sequence for the logic signal includes not only high and low-going transitions but also high and low levels (DC voltage levels).

**RESTRICTIONS ON PRODUCT USE**

000707EBE

- TOSHIBA is continually working to improve the quality and reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to comply with the standards of safety in making a safe design for the entire system, and to avoid situations in which a malfunction or failure of such TOSHIBA products could cause loss of human life, bodily injury or damage to property.  
In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent TOSHIBA products specifications. Also, please keep in mind the precautions and conditions set forth in the "Handling Guide for Semiconductor Devices," or "TOSHIBA Semiconductor Reliability Handbook" etc..
- The TOSHIBA products listed in this document are intended for usage in general electronics applications (computer, personal equipment, office equipment, measuring equipment, industrial robotics, domestic appliances, etc.). These TOSHIBA products are neither intended nor warranted for usage in equipment that requires extraordinarily high quality and/or reliability or a malfunction or failure of which may cause loss of human life or bodily injury ("Unintended Usage"). Unintended Usage include atomic energy control instruments, airplane or spaceship instruments, transportation instruments, traffic signal instruments, combustion control instruments, medical instruments, all types of safety devices, etc.. Unintended Usage of TOSHIBA products listed in this document shall be made at the customer's own risk.
- Polyimide base film is hard and thin. Be careful not to injure yourself on the film or to scratch any other parts with the film. Try to design and manufacture products so that there is no chance of users touching the film after assembly, or if they do, that there is no chance of them injuring themselves. When cutting out the film, try to ensure that the film shavings do not cause accidents. After use, treat the leftover film and reel spacers as industrial waste.
- Light striking a semiconductor device generates electromotive force due to photoelectric effects. In some cases this can cause the device to malfunction.  
This is especially true for devices in which the surface (back), or side of the chip is exposed. When designing circuits, make sure that devices are protected against incident light from external sources. Exposure to light both during regular operation and during inspection must be taken into account.
- The products described in this document are subject to the foreign exchange and foreign trade laws.
- The information contained herein is presented only as a guide for the applications of our products. No responsibility is assumed by TOSHIBA CORPORATION for any infringements of intellectual property or other rights of the third parties which may result from its use. No license is granted by implication or otherwise under any intellectual property or other rights of TOSHIBA CORPORATION or others.
- The information contained herein is subject to change without notice.