IM82C43
CMOS I/O Expander

DESCRIPTION

The Intersil IM82C43 is a CMOS input/output expander equivalent to the NMOS 8243. It is designed to provide I/O expansion for the CMOS IM80C48 and NMOS 8048 families of single-chip microcomputers.

The 24-pin IM82C43 provides four 4-bit bidirectional I/O ports: 8048/41 instructions control bidirectional transfers between theIM82C43 and the 8048 family microcomputers, and can execute logical AND/OR operations directly on the data contained in the IM82C43 ports.

FEATURES

- **8048/41 Compatible I/O Expander**
- **CMOS Pin-For-Pin Replacement for Standard NMOS 8243**
- **Low Power Dissipation — Maximum 25mW Active**
- **Four 4-Bit I/O Ports in 24-Pin DIP**
- **Logical AND/OR Directly to Ports**
- **High Output Drive**
- **Single +5V Supply**

ORDERING INFORMATION

PART NO.	TEMP. RANGE	PACKAGE
IM82C43CJG	0°C to +70°C	24 PIN CERDIP
IM82C43CPG	0°C to +70°C	24 PIN PLASTIC
IM82C43IJG	-40°C to +85°C	24 PIN CERDIP
IM82C43IPG	-40°C to +85°C	24 PIN PLASTIC

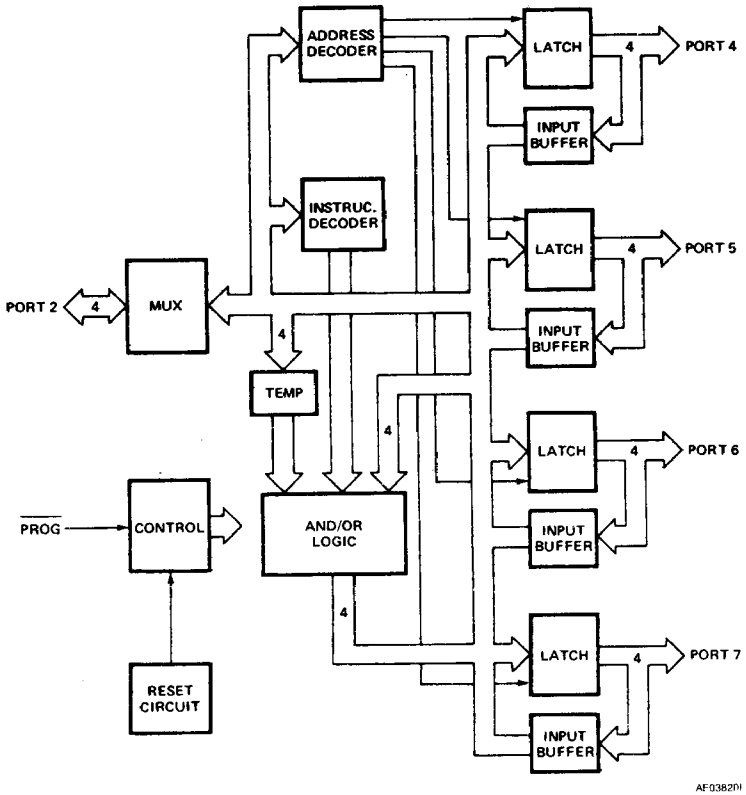

Figure 1: Functional Diagram

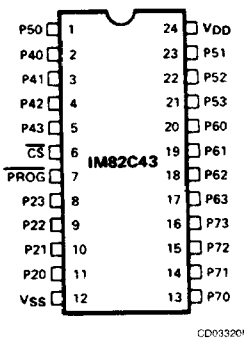

Figure 2: Pin Configuration (Outline dwgs JG, PG)

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Note: All typical values have been guaranteed by characterization and are not tested.

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage ($V_{DD} - V_{SS}$) ..... +8V
Voltage on Any Pin .....(V_{SS}-0.5V) to (V_{DD}+0.5V)
Power Dissipation 1W
Operating Temperature (C) ..... 0°C to +70°C
(I) .....-40°C to +85°C

Storage Temperature..... -65°C to +150°C
Lead Temperature (Soldering, 10sec) .....300°C

NOTE: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

DC ELECTRICAL CHARACTERISTICS (T_A = Operating Temperature Range, V_{DD}=5V±10%, V_{SS} = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IL}	Input Low Voltage		-0.5		0.8	V
V_{IH}	Input High Voltage	V_{DD} = 4.5	2.0			
		V_{DD} = 5.5	2.4			
V_{OL}	Output Low Voltage Ports 4–7	I_{OL} = 10mA			0.4	
	Output Low Voltage Port 2	I_{OL} = 20mA			0.8	
		I_{OL} = 1.6mA			0.4	
V_{OH1}	Output High Voltage Ports 4–7	I_{OH} = 3.2mA	2.8			
V_{OH2}	Output Voltage Port 2	I_{OH} = 1.6mA	2.8			
I_{ILK}	Input Leakage Ports 4–7, Port 2, $\overline{CS}$, $\overline{PROG}$	V_{IN} = V_{DD} to V_{SS}	-10		10	µA
I_{DD}	Supply Current	WRITE mode, All outputs open, t_k = 700ns		1.6	5.0	mA
I_{STBY}	Standby Current	V_{IN} = 0 or V_{DD}, $\overline{CS}$ = V_{DD}, All outputs open			100	µA
ΣI_{OL}	Sum of all I_{CL} from 16 Outputs	5mA each pin average			80	mA

AC ELECTRICAL CHARACTERISTICS (T_A = Operating Temperature Range, V_{DD} = 5V±10%, V_{SS} = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
t_a	Code Valid Before $\overline{PROG}$	80pF Load	100		ns
t_b	Code Valid After $\overline{PROG}$	20pF Load	60		
t_c	Data Valid Before $\overline{PROG}$	80pF Load	140		
t_d	Data Valid After $\overline{PROG}$	20pF Load	20		
t_h	Floating After $\overline{PROG}$	20pF Load	0	150	
t_k	$\overline{PROG}$ Negative Pulse Width		700		
t_{cs}	$\overline{CS}$ Valid Before/After $\overline{PROG}$		50		
t_{po}	Ports 4–7 Valid After $\overline{PROG}$	100pF Load		700	
t_{ip}	Ports 4–7 Valid Before/After $\overline{PROG}$		0		
t_{acc}	Port 2 Valid After $\overline{PROG}$	80pF Load		650	

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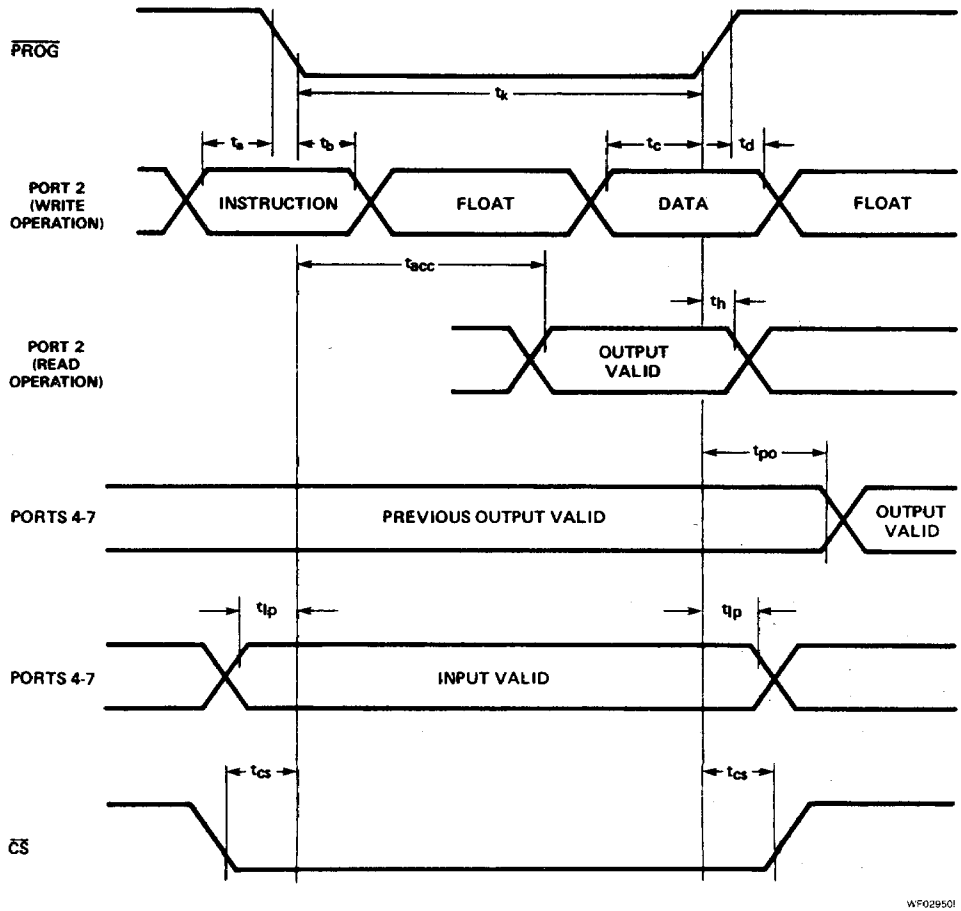

AC TEST CONDITIONS

V_{IH} = 2.8V

INPUT RISE AND FALL TIMES: 5ns (10% TO 90%)

INPUT AND OUTPUT TIMING VOLTAGE REFERENCE LEVELS: 0.8V AND 2.0V

Figure 3: Timing Diagram

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PIN DESCRIPTIONS

Designator	Pin Number	Function
$\overline{PROG}$	7	**Strobe input.** The falling edge of $\overline{PROG}$ implies valid address and control information on P20–P23, while the rising edge implies valid data on P20–P23.
$\overline{CS}$	6	**Chip select input.** When HIGH, it disables $\overline{PROG}$, thus inhibiting change in output or internal status.
P20–P23	8–11	**Four bit directional port** carrying address and control bits on the falling edge of $\overline{PROG}$ and I/O data on the rising edge of $\overline{PROG}$.
P40–43 P50–P53 P60–P63 P70–P73	2–5 1,21–23 17–20 13–16	**Four bit bidirectional I/O ports.** May be configured for input, tri-state output (READ mode) or latched output. Data on pins P20–23 may be directly written. ANDed, or ORed with previous data.
V_{SS}	12	**Circuit ground potential**
V_{DD}	24	**Positive supply.**

DETAILED DESCRIPTION

The IM82C43 has four 4-bit I/O ports, which are addressed as Ports 4 thru 7 by the processor. The following operations may be performed on these ports:

- Transfer accumulator to port (write)
- Transfer port to accumulator (read)
- AND accumulator to port
- OR accumulator to port

All communication between the microcomputer and the IM82C43 occurs over Port 2 (P20–P23) with timing provided by an output pulse on the $\overline{PROG}$ pin of the processor. Each data transfer consists of two 4-bit nibbles:

- The first contains the port address and command to the IM82C43. This is latched from Port 2 during the high-to-low transition of $\overline{PROG}$ and is encoded as shown in the table on page 3.
- The second contains the four bits of data associated with the instruction. The low-to-high transition of $\overline{PROG}$ indicates the presence of data.

Port Address And Command Format

P23	P22	INSTRUCTION CODE	P21	P20	ADDRESS CODE
0	0	Read	0	0	Port 4
0	1	Write	0	1	Port 5
1	0	ORLD	1	0	Port 6
1	1	ANLD	1	1	Port 7

Write Modes

The device has three modes. MOVD P,A directly writes new data into the selected port with old data being lost; ORLD P,A ORs the new data with the old data and writes it to the port; and ANLD P,A ANDs new data with old data and writes it to the selected port.

After the designated operation is performed, the data is latched and directed to the port. The old data remains latched until the new data is written by the rising edge of $\overline{PROG}$.

Read Mode

The device has one read mode. The command and port address are latched from port 2 on the high-to-low transition of the $\overline{PROG}$ pin. As soon as the read operation and port address are decoded, the designated port output buffers are disabled and the input buffers enabled. The read operation is terminated by the low-to-high transition of the $\overline{PROG}$ pin. The port selected is switched to the high impedance state while port 2 is returned to the input mode.

Normally a port will be in an output mode (write) or input mode (read). The first read of a port, following a mode change from write to read should be ignored; all following reads are valid. This is to allow the external driver on the port to settle after the first read instruction removes the low impedance drive from the IM82C43 output. A read of any port will leave that port in a high impedance state.

I/O Expansion

The use of a single IM82C43 with an 8048 or 8021 is shown in Figure 4. If more ports are required, more IM82C43s can be added as shown in Figure 5. Here, the upper nibble of port 2 is used to select one of the IM82C43s. Two lines could have been decoded but that would require additional hardware. Assuming that the left-most IM82C43 chip select is connected to P24, the instructions to select and de-select would be:

```
MOV A, #0EFH      P24 = 0
OUTL P2, A        Enable IM82C43
.
.
.
MOV A, #0FFH      Disable All
OUTL P2, A        Send it
```

Power On Initialization

Initial application of power to the device forces ports 4, 5, 6, and 7 to the high impedance state. Port 2 will be in an input state if $\overline{PROG}$ or $\overline{CS}$ are high when power is applied. The first high-to-low transition of $\overline{PROG}$ causes the device to exit the power-on mode. The power-on sequence is initiated if V_{DD} drops below one volt.

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TYPICAL APPLICATIONS

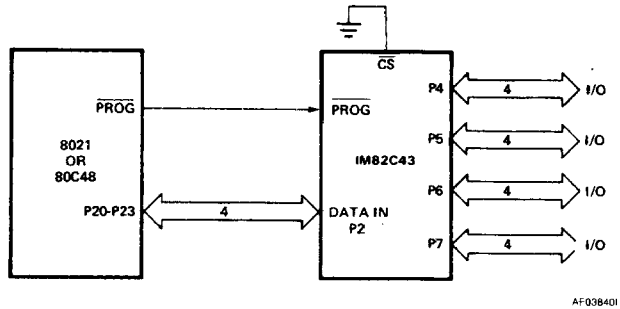

Figure 4: Expander Interface

Note: The IM82C43 does not have the same quasi-bidirectional port structure as P1/P2 of the 8048. When a "1" is written to P4–7 of the IM82C43 it is a "hard 1" (low impedance to +5V) which cannot be pulled low by an external device. All 4 bits of any port can be switched from output mode to input mode by executing a dummy read which leaves the port in a high impedance (no pullup or pulldown) state.

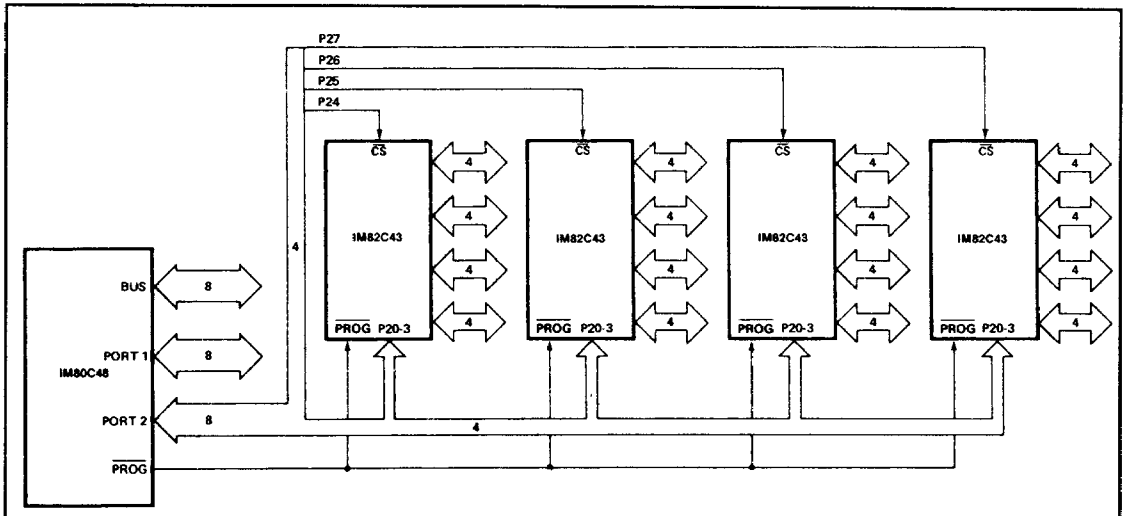

Figure 5: Using Multiple IM82C43s

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