SEPTEMBER 1998
Revision 1.1

LXT336

Quad T1/E1 Receiver

General Description

The LXT336 quad receiver is a fully-integrated, quadruple-PCM receiver for both T1 (1.544 Mbps) and E1 (2.048 Mbps) applications. It incorporates four independent receivers in a single 64-pin QFP package.

The LXT336 features a differential receiver architecture with high noise interference margin. It uses peak detection with a variable threshold for reliable recovery of data as low as 500 mV and up to 12 dB of cable attenuation.

The fully digital clock recovery system uses a low frequency master clock of 2.048 MHz or 1.544 MHz as its reference. In addition, each LXT336 receiver incorporates a Loss of Signal (LOS) detection circuit. The LOS detector is compliant with both ITU-T G.775 and ANSI T1.231 standards.

The LXT336 ports can be independently configured for either unipolar or bipolar output modes. HDB3 and AMI decoding mechanisms are available in unipolar mode.

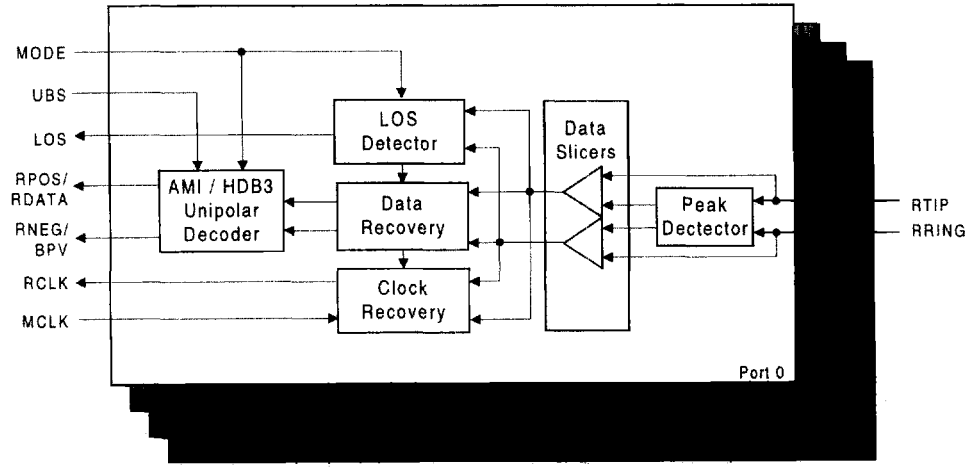
Features

- Fully integrated quad, receiver for E1 2.048 Mbps or T1 1.544 Mbps operation
- Single rail supply voltage of 5 V (typical)
- Low power consumption: 250 mW for E1; 200 mW for T1 (typical)
- High-performance receivers recover data with up to 12 dB cable attenuation
- Low frequency 1.544 or 2.048 MHz reference clock
- On-chip clock recovery function complies with ITU G.823 and Bellcore GR-499-CORE
- Programmable unipolar and bipolar PCM interface
- On-chip AMI and HDB3 decoders
- Loss of Signal processors conform to ITU G.775 and ANSI T1.231 recommendations
- Small-footprint 64-pin QFP
- Optional RZ Data recovery mode

Applications

- Test Equipment
- DSX-1 and E1 Line Monitoring
- High density T1/E1 line cards

LXT336 Block Diagram



PIN ASSIGNMENTS & SIGNAL DESCRIPTIONS

Figure 1: LXT336 Pin Assignments

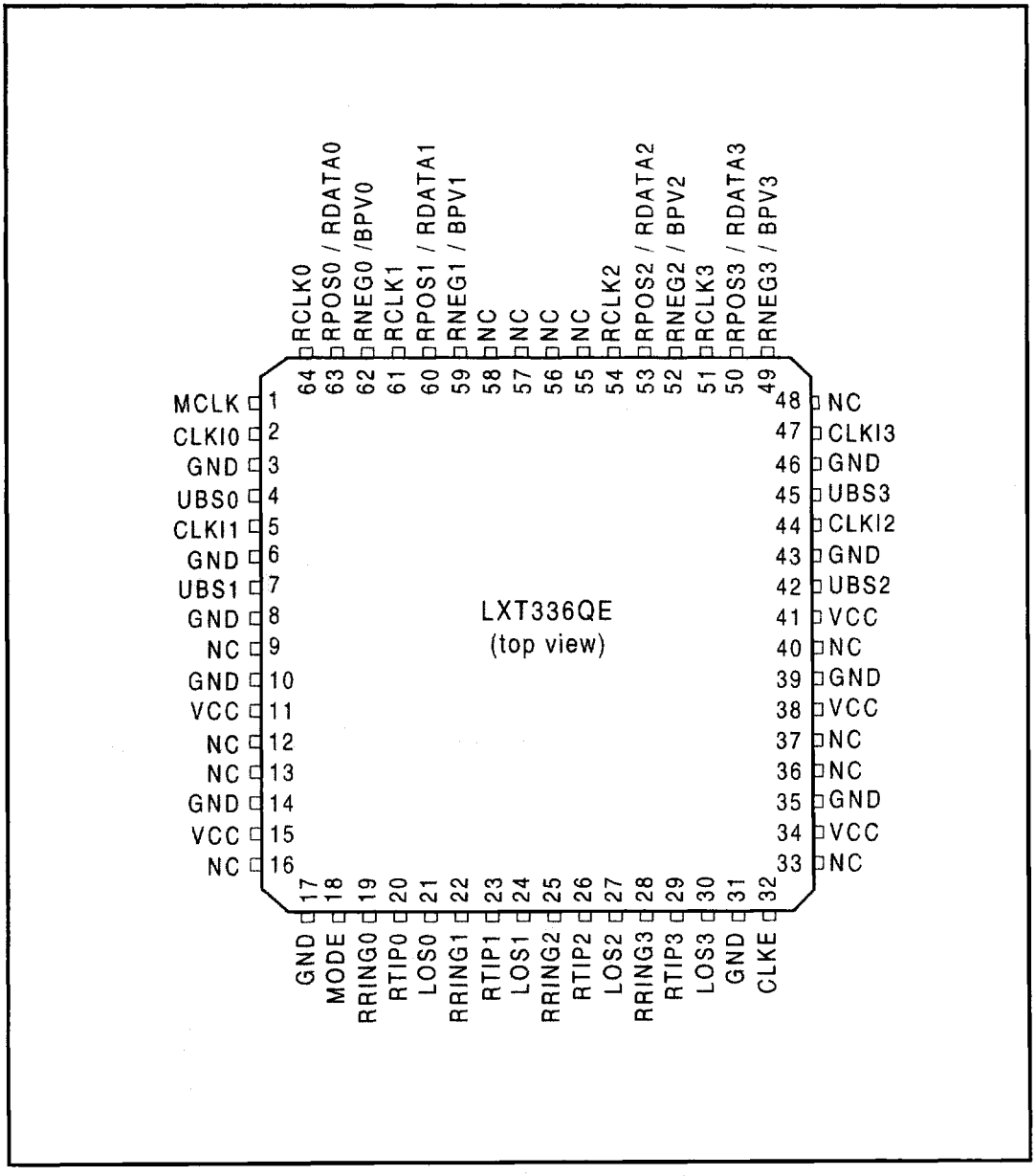


Table 1: LXT336 Pin Descriptions

Pin #	Sym	I/O[1]	Description
1	MCLK	DI	**Master Clock Input.** An independent and free-running 2.048 or 1.544 MHz clock input generates the internal reference clocks for all Receivers. On Loss of Signal (LOS), the LXT336 derives RCLKx from this master clock. With MCLK asserted High, the LXT336 disables the PLL clock recovery circuits. The Receiver then feeds RPOSx and RNEGx to an internal XOR gate that performs logically exclusive ORs for both data signals and connects this output to RCLKx for external clock recovery. In this mode, the LXT336 operates as a data recovery circuit. With MCLK asserted Low, the LXT336 powers down its clock and data recovery circuits and switches the output pins RCLKx, RPOSx and RNEGx to tri-state mode. MCLK — Operating Mode Clocked — Data/Clock Recovery L — Power Down H — Data Recovery
2	CLKI0	DI	**Clock Input - Port 0.** All CLKIx pins are identical. Connect to MCLK for unipolar operation mode (single rail plus clock). For bipolar operation mode (dual rail plus clock), CLK0 should be connected to ground.
3	GND	S	**Ground.**
4	UBS0	DI	**Unipolar-Bipolar Select Input–Port 0.** All UBSx pins are identical. If this pin is asserted High for more than 16 CLKI cycles, the LXT336 switches to unipolar mode. HDB3 or AMI decoder mode is selected by the MODE pin. The device is set to bipolar mode when this pin is asserted Low. UBSx — Operating Mode L — Bipolar Mode H — Unipolar Mode
5	CLKI1	DI	**Clock Input - Port 1.** See CLKI0, pin 2.
6	GND	S	**Ground.**
7	UBS1	DI	**Unipolar-Bipolar Select Input–Port 1.** See UBS0, pin 4.
8	GND	S	**Ground.**
9	NC	–	**Not Connected.** Must be left open.
10	GND	S	**Ground.**
11	VCC	S	**Positive Supply.** +5 VDC power supply.
12	NC	–	**Not Connected.** Must be left open.
13	NC	–	**Not Connected.** Must be left open.
14	GND	S	**Ground.**
15	VCC	S	**Positive Supply.** +5 VDC power supply.
16	NC	–	**Not Connected.** Must be left open.

1. Entries in I/O column are: DI = digital input; DO = digital output; DI/O = digital input/output; AI = analog input; AO = analog output; S = supply. Note: Do not leave digital inputs floating, with the exception of not connected (NC) pins.

Table 1: LXT336 Pin Descriptions – continued

Pin #	Sym	I/O[1]	Description
17	GND	S	**Ground.**
18	MODE	DI	**Mode Select Input.** In unipolar mode, if this pin is pulled Low, all transceivers operate in E1 mode using AMI decoding. With this pin pulled High, all transceivers enter E1 mode using HDB3 decoding. With this pin set to 2.5V, the LXT336 enters T1 mode with AMI decoding. MODE — Operating Mode L — E1 Mode with AMI Decoding H — E1 Mode with HDB3 Decoding 2.5V — T1 Mode with AMI Decoding The 2.5V reference is obtained with a resistive divider consisting of two 10 KΩ resistors across VCC and GND.
19 20	RRING0 RTIP0	AI AI	**Receive Ring Input–Port 0/Receive TIP Input–Port 0.** These pins are the inputs of the fully differential line receiver.
21	LOS0	DO	**Loss of Signal Output–Port 0.** All LOSx pins are identical. This output is High when a valid loss of signal condition is detected. See page page 187 for more information. In data recovery mode, LOSx is a pure analog energy detector.
22 23	RRING1 RTIP1	AI AI	**Receive Ring Input–Port 1/Receive TIP Input–Port 1.** See RRING0, pin 19; RTIP0, pin 20.
24	LOS1	DO	**Loss of Signal Output–Port 1.** See LOS0, pin 21.
25 26	RRING2 RTIP2	AI AI	**Receive Ring Input–Port 2/Receive TIP Input–Port 2.** See RRING0, pin 19; RTIP0, pin 20.
27	LOS2	DO	**Loss of Signal Output–Port 2.** See LOS0, pin 21.
28 29	RRING3 RTIP3	AI AI	**Receive Ring Input–Port 3/Receive TIP Input–Port 3.** See RRING0, pin 19; RTIP0, pin 20.
30	LOS3	DO	**Loss of Signal Output–Port 3.** See LOS0, pin 21.
31	GND	S	**Ground.**
32	CLKE	DI	**Clock Edge Select Input.** CLKE — Result L — RPOS, RNEG valid on falling edge of RCLK H — RPOS, RNEG valid on rising edge of RCLK
33	NC	–	**Not Connected.** Must be left open.
34	VCC	S	**Positive Supply.** +5 VDC power supply.
35	GND	S	**Ground.**
36	NC	–	**Not Connected.** Must be left open.
37	NC	–	**Not Connected.** Must be left open.

1. Entries in I/O column are: DI = digital input; DO = digital output; DI/O = digital input/output; AI = analog input; AO = analog output; S = supply. **Note:** Do not leave digital inputs floating, with the exception of not connected (NC) pins.

Table 1: LXT336 Pin Descriptions – continued

Pin #	Sym	I/O[1]	Description
38	VCC	S	**Positive Supply.** +5 VDC power supply.
39	GND	S	**Ground.**
40	NC	–	**Not Connected.** Must be left open.
41	VCC	S	**Positive Supply.** +5 VDC power supply
42	UBS2	DI	**Unipolar-Bipolar Select Input–Port 2.** See UBS0, pin 4.
43	GND	S	**Ground.**
44	CLKI2	DI	**Clock Input - Port 2.** See CLKI0, pin 2.
45	UBS3	DI	**Unipolar-Bipolar Select Input–Port 3.** See UBS0, pin 4.
46	GND	S	**Ground.**
47	CLKI3	DI	**Clock Input - Port 3.** See CLKI0, pin 2.
48	NC	–	**Not Connected.** Must be left open.
49	RNEG3/ BPV3	DO	**Receive Negative Data/Bipolar Violation Indication Output–Port 3.** All RNEGx/ BPVx pins are identical. In bipolar mode these pins act as active High bipolar non-return-to-zero (NRZ) receive signal outputs. A High signal on RNEGx corresponds to receipt of a negative pulse on RTIPx/RRINGx. A High signal on RPOSx corresponds to receipt of a positive pulse on RTIPx/RRINGx. Both signals are valid on the same edge of RCLKx, as determined by the CLKE pin. In unipolar mode, the LXT336 asserts the BPVx pin High any time it senses an In-Service Line Code violation. In data recovery mode, this pin is an active Low RZ output. See RPOS3/RDATA3, pin 50; and Functional Description.
50	RPOS3/ RDATA3	DO	**Receive Positive Data/Receive Data Output–Port 3.** A High signal on RPOSx corresponds to receipt of a positive pulse on RTIPx/RRINGx. In unipolar mode, the LXT336 asserts RDATAx High when a mark has been received. This signal is valid on the edge of RCLKx as determined by the CLKE pin. RDATAx is an NRZ receive data output. In Data Recovery mode, this pin is an active Low RZ output. See RNEG3/BPV3, pin 49.
51	RCLK3	DO	**Receive Clock Output–Port 3.** All RCLKx pins are identical. This pin provides the recovered clock from the signal received at RTIPx and RRINGx. In loss of signal conditions the LXT336 connects MCLK to this pin through internal circuitry. Asserting the MCLK pin High disables the clock recovery circuit and internally connects RPOS*x* and RNEG*x* to an XOR that is fed to the RCLK*x* output for external clock recovery applications.
52	RNEG2/ BPV2	DO	**Receive Negative Data/Violation Indication Output–Port 2.** See RNEG3/BPV3, pin 49; RPOS3/RDATA3, pin 50.

1. Entries in I/O column are: DI = digital input; DO = digital output; DI/O = digital input/output; AI = analog input; AO = analog output; S = supply. Note: Do not leave digital inputs floating, with the exception of not connected (NC) pins.

Table 1: LXT336 Pin Descriptions – continued

Pin #	Sym	I/O[1]	Description
53	RPOS2/ RDATA2	DO	**Receive Positive Data/Receive Data Output–Port 2**. See RPOS3/RDATA3, pin 50; RNEG3/BPV3, pin 49. In Data Recovery Mode, this signal is active Low.
54	RCLK2	DO	**Receive Clock Output–Port 2**. See RCLK3, pin 51.
55	NC	–	**Not connected**. Must be left open.
56	NC	–	**Not connected**. Must be left open.
57	NC	–	**Not connected**. Must be left open.
58	NC	–	**Not connected**. Must be left open.
59	RNEG1/ BPV1	DO	**Receive Negative Data/Bipolar Violation Indication Output–Port 1**. See RNEG3/ BPV3, pin 49; RPOS3/RDATA3, pin 50.
60	RPOS1/ RDATA1	DO	**Receive Positive Data/Receive Data Output–Port 1**. See RPOS3/RDATA3, pin 50; RNEG3/BPV3, pin 49.
61	RCLK1	DO	**Receive Clock Output–Port 1**. See RCLK3, pin 51.
62	RNEG0/ BPV0	DO	**Receive Negative Data/Bipolar Violation Indication Output–Port 0**. See RNEG3/BPV3, pin 49; RPOS3/RDATA3, pin 50.
63	RPOS0/ RDATA0	DO	**Receive Positive Data/Receive Data Output–Port 0**. See RPOS3/RDATA3, pin 50; RNEG3/BPV3, pin 49.
64	RCLK0	DO	**Receive Clock Output–Port 0**. See RCLK3, pin 51.

1. Entries in I/O column are: DI = digital input; DO = digital output; DI/O = digital input/output; AI = analog input; AO = analog output; S = supply. **Note**: Do not leave digital inputs floating, with the exception of not connected (NC) pins.

FUNCTIONAL DESCRIPTION

The LXT336 quad receiver is a fully-integrated, PCM receiver for both 1.544 Mbps (DSX-1) and 2.048 Mbps (E1) applications. The MCLK frequency and the MODE pin input level set the mode of operation. The LXT336 is a low-power CMOS device operating from a single +5 V power supply. Refer to the LXT336 block diagram on page 1.

Each receiver interfaces with back-end processors through bipolar or unipolar data I/O channels and allows control by hardwired pins for stand-alone operation.

Receiver Description

The four receivers in the LXT336 are identical. The following paragraphs describe the operation of a single receiver.

The LXT336 receives the input signal at RTIP/RRING via a 1:1 or 1:2 coupling transformer. Data slicers and a peak detector process the received signal. The peak detector samples the received signal and determines its maximum value. A data-rate dependent percentage of peak value goes to the data slicers as a threshold level to ensure an optimum signal-to-noise ratio.

The receiver accurately recovers signals with up to -12 dB of cable loss. The minimum receiver sensitivity signal level is approximately 500 mV peak to peak. Regardless of the received signal level, the LXT336 holds its peak detectors above a minimum level (0.225 V) to provide immunity from impulse noise.

After the data slicers process the received signal, it is fed to the data and timing recovery section, and to the receive monitor. The data and timing recovery circuits provide an input jitter tolerance significantly better than required by ITU-T G.823 and GR-499-CORE Category II. Refer to the Test Specifications section for details.

The recovered clock is output at RCLK in both bipolar and unipolar modes.

In bipolar mode, recovered data is active High and output at RPOS and RNEG; in unipolar mode recovered data is active High and output at RDATA.

If CLKE is Low, RPOS and RNEG outputs are valid on the falling edge of RCLK. If CLKE is High, RPOS and RNEG outputs are valid on the rising edge of RCLK.

Asserting MCLK High disables the clock recovery function and switches all receivers to data recovery mode. In data recovery mode, the RPOS/RNEG outputs are active Low, return-to-zero (RZ) outputs. Asserting MCLK Low powers all receivers down and holds RPOS/RNEG and RCLK in a high impedance state.

Loss Of Signal Detector

E1 LOS Detection

During E1 operation, the ITU G.775 detection criterion is employed. The Loss of Signal (LOS) detector uses a combination analog and digital detection scheme and complies with the ITU G.775 recommendation.

The receiver monitor loads a digital counter at the RCLK frequency. The monitor increments the counter with each received 0 (space), and resets it to 0 with each received 1 (mark). Any signal 21 dB below the nominal 0 dB signal for 32 consecutive pulse intervals generates a LOS condition.

The LXT336 sets the LOS flag, and replaces the recovered clock with MCLK at the RCLK output in a smooth transition. (Normal operation requires MCLK.) LOS is cleared again when the signal level rises above 21 dB (typical) below the minimum 0 dB level and the average 1s density reaches 12.5% (i.e. four marks in a 32-bit window). Another smooth transition replaces MCLK with the recovered clock at RCLK. During LOS conditions, received data is output on RPOS/RNEG (or RDATA in unipolar I/O mode).

T1 LOS Detection

During T1 operation, the ANSI T1.231 detection criterion is employed. The LXT336 asserts LOS if it receives 175 consecutive zeros, and de-asserts LOS when the signal reaches 12.5% ones density (i.e. 16 marks in a 128-bit window with no more than 99 consecutive zeros).

Data Recovery Mode LOS Detection

In data recovery mode, the LOS detector uses an analog detection scheme compliant with ITU-T G.775. Any signal 22 dB (typical) below the nominal 0 dB signal for more than approximately 16 µs generates a LOS condition. LOS is cleared when the signal level of the first 1 rises to more than 21 dB (typical) below the minimum 0 dB level. During LOS conditions, received data is output on RPOS/RNEG.

In-Service Code Violation Monitoring

In unipolar AMI I/O Mode, the LXT336 reports bipolar violations using an active High output for one RCLK cycle on the BPV output. A bipolar violation, in AMI encoding mode, is two consecutive marks of the same polarity. With the HDB3 detector enabled (MODE pulled High), the decoder will detect AMI code violations that are not part of a zero substitution code.

HDB3 code violations omit sequences of zeros that violate the coding rules. If an HDB3 code violation occurs, the decoder asserts the BPV output for one RCLK cycle during the period of the violating bit. In the event the decoder receives a sequence of four or more zeros, it asserts the BPV output during the entire sequence of violating data bits.

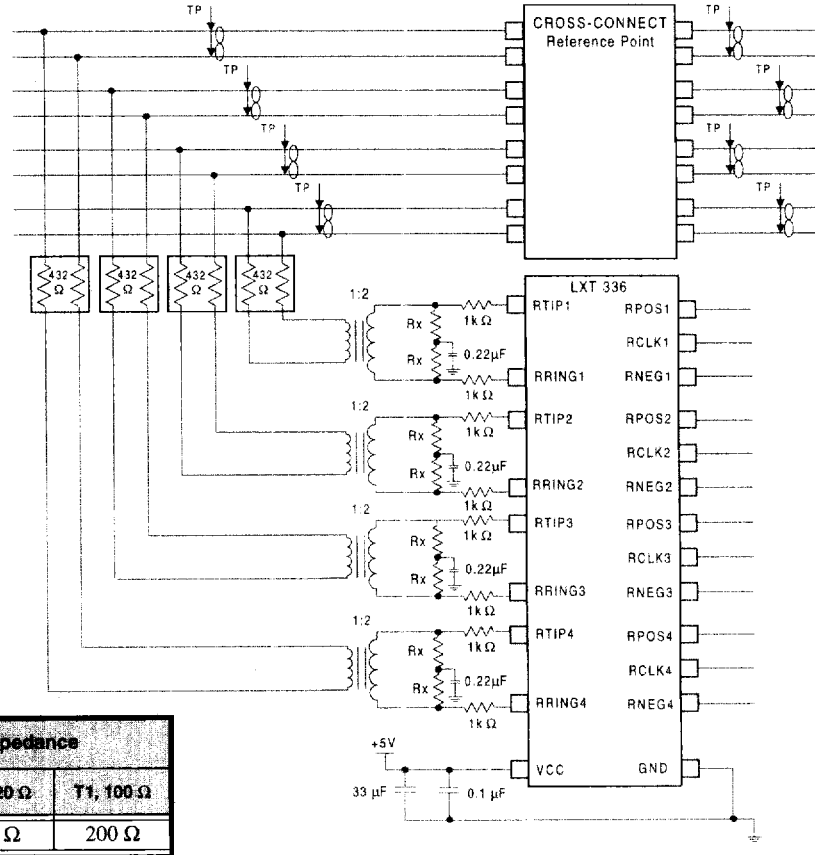
APPLICATION INFORMATION

The LXT336 is well suited for both line interface equipment and monitoring applications. The following paragraphs describe the recommended configuration for these applications.

Monitoring Applications

Figure 2 shows a typical configuration for monitoring applications. The 432Ω resistors are usually included in the monitoring jack for DSX-1 applications. These resitors provide approximately 20dB of resistive attenuation when terminated into an 100Ω impedance. The 1:2 step up transformer in the receive interface is used to boost-up the signal as seen by the LXT336. The two resistors (Rx) determine the receive termination impedance and are selected according to the nominal cable impedance as specified in the table at the bottom of Figure 2. The series 1k Ω resistors provide protection against surges coupled to the device. Due to the high input impedance of the LXT336, typically 40k Ω, these series resistors do not affect receiver sensitivity.

Figure 2: Typical Monitoring Application



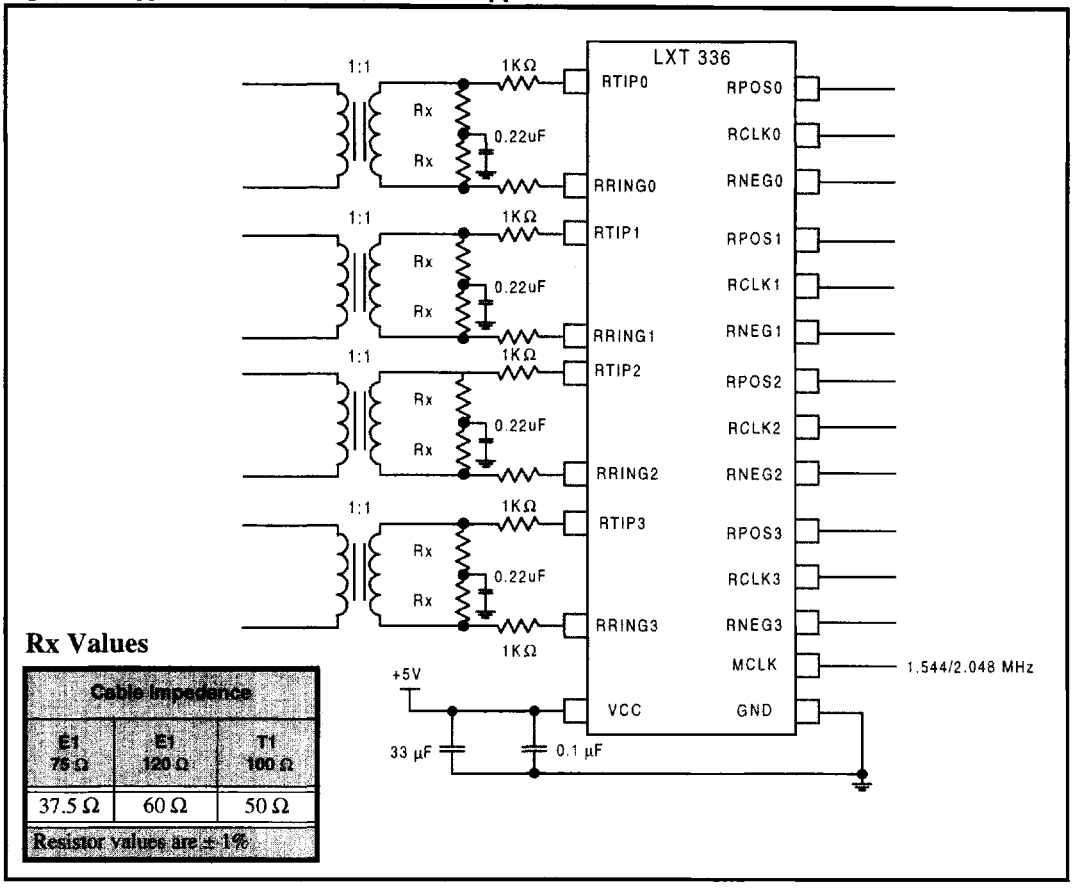
Rx Values

Cable Impedance		
E1, 75Ω	**E1, 120 Ω**	**T1, 100 Ω**
150 Ω	240 Ω	200 Ω
Resistor values are ± 1%		

Receive Line Interface Applications

Figure 3 shows the typical LXT336 configuration for receive line interface applications. A 1:1 transformer is used in combination with the appropriate termination resistors Rx. These resistors must be selected to match the line impedance as specified in the table at the bottom of Figure 3.

Figure 3: Typical Receive Line Interface Application



Rx Values

Cable Impedance		
E1 75 Ω	E1 120 Ω	T1 100 Ω
37.5 Ω	60 Ω	50 Ω
Resistor values are ± 1%		

Table 2: Transformer Specifications

Turns Ratio	Primary Inductance mH (min.)	Leakage Inductance µH (max.)	Interwinding Capacitance pF (max.)	DCR Ω (max.)	Dielectric Breakdown Voltage V[1] (min.)
1:2 or 1:1	1.2	0.60	30	1.00 pri 1.20 sec	1500 Vrms

1. This parameter is application dependent.

TEST SPECIFICATIONS

NOTE

The minimum and maximum values in Tables 3 through 9 and Figures 4 through 6 represent the performance specifications of the LXT336 and are guaranteed by test except, where noted, by design or other correlation methods.

Table 3: Absolute Maximum Ratings

Parameter	Sym	Min	Max	Unit
DC supply voltage	RVCC, RGND	-0.3	6.0	V
Input voltage on any pin[1]	V_{IN}	GND -0.3	RVCC + 0.3	V
Input voltage on RTIP/RRING	V_{IN}	-6	RVCC + 0.3	V
Transient latchup current on any pin[2]	I_{IN}	–	100	mA
Input current on any digital pin[3]	I_{IN}	-10	10	mA
DC input current on RTIP, RRING[3]	I_{IN}	–	±20	mA
Storage temperature	T_{STOR}	-65	+150	°C
Total package power dissipation	–	–	1	W

CAUTION

Exceeding these values may cause permanent damage to the device. Operation is not guaranteed under these conditions. Exposure to absolute maximum rating conditions for extended periods may adversely affect device reliability.

1. Referenced to ground.
2. Exceeding these values will cause SCR latch-up.
3. Constant input current.

Table 4: Recommended Operating Conditions

Parameter	Sym	Min	Typ	Max	Unit
DC supply voltage	V+	4.75	5.0	5.25	V
Ambient operating temperature	T_A	-40	25	+85	° C

Table 5: DC Characteristics (Over Recommended Range)

Parameter		Sym	Min	Typ[1]	Max	Unit	Test Condition
Digital I/O pins	High level input voltage	VIH	2.0	–	–	V	
	Low level input voltage	VIL	—	–	0.8	V	
	High level output voltage[2]	VOH	3.5	–	–	V	IOUT= -400µA
	Low level output voltage[2]	VOL	—	–	0.4	V	IOUT= 1.6 mA
Input leakage current (digital input pins)		IIL	-10	–	+10	µA	
Tristate leakage current		IHZ	-10		+10	µA	pins 49 - 54, 59 - 64
MODE input pin	Low level input voltage	VINL	–	–	1.5	V	pin 18
	High level input voltage	VINH	3.5	–	–	V	
	Midrange input voltage	VINM	2.3	2.5	2.7	V	
	Low level input current	IINL	–	–	50	µA	
	High level input current	IINH	–	–	50	µA	
Total power dissipation[3]	E1 operation	PD	–	250	340	mW	
	T1 operation	PD	–	200	290	mW	
Power down current		ICCO	–	–	10	mA	

1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Output Drivers will output CMOS logic levels into CMOS loads.
3. Digital outputs driving a 50 pF load; all channels receiving line signal.

Table 6: E1 Receive Characteristics (Over Recommended Range)

Parameter		Sym	Min	Typ[1]	Max	Unit	Test Condition
Permissible cable attenuation[2]		–	–	–	12	dB	@1024 kHz
Receiver dynamic range		DR	0.5	–	4.2	Vp	
Signal to noise interference margin [2, 6]		S/I	-15	–	–	dB	Per G.703, O.151, 6 dB of cable.
Signal to single tone interference margin[2]		S/X	-14	–	–	dB	O.151, 6 dB of cable
Data decision threshold		SRE	43	50	57	%	Relative to peak input voltage.
Analog loss of signal threshold		–	–	225[5]	–	mV	
Loss of signal threshold hysteresis		–	–	2.5	–	dB	
Consecutive zeros before loss of signal		–	–	32	–		G.775 recommendation
Low limit input jitter tolerance [3]	1.2E-5 Hz to 20 Hz[6]	–	36	–	–	U.I.	G.823 recommendation
	20 Hz to 2.4 kHz	–	1.5	–	–	U.I.	
	8 kHz to 100 kHz	–	0.2	–	–	U.I.	
RCLK output jitter[4, 6]	0 Hz to100 kHz	–	–	0.01	–	U.I.	peak to peak
Clock recovery PLL 3 dB bandwidth		–	–	10	–	kHz	
PLL peaking[7]		–	–	–	0	dB	
Receiver input impedance		–	–	40	–	kΩ	@1024 kHz RTIP to RRING
Receiver return loss[6]	51 kHz–102 kHz	–	20	–	–	dB	See Application Information section.
	102–2048 kHz	–	20	–	–	dB	
	2048 kHz–3072 kHz	–	20	–	–	dB	

1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Line interface application. No errors shall occur when the combined signal attenuated by the maximum specified interconnecting cable loss is applied to the input port. See ITU O.151 recommendation for further details.
3. Sine wave jitter and wander with a peak to peak amplitude that corresponds at least to what is specified in Figure 5 shall not cause either a bit error or loss of frame alignment. As test signal an HDB3-coded digital signal with an electrical characteristic that complies with what is set forth in ITU G.703 shall be used. Test sequence is pseudo-random 2^{15}-1. See also ITU O.151.
4. If the LXT336 is configured as data receiver only and if a jitter free signal is applied to RTIP and RRING the added jitter must not exceed the specified value.
5. Equal to 22 dB below the nominal 0 dB level in 120 Ω systems.
6. Guaranteed by design and other correlation methods.
7. Guaranteed by design and other correlation methods. There will be no jitter gain within the specified operating range.

Table 7: T1 Receive Characteristics (Over Recommended Range)

Parameter		Sym.	Min.	Typ[1]	Max.	Unit	Test Condition
Permissible cable attenuation		–	–	–	12	dB	@772 kHz, Line interface application
Receiver dynamic range		DR	0.5	–	4.2	Vp	
Undershoot		US	–	–	62	%	
Data decision threshold		SRT	63	70	77	%	Relative to peak input voltage.
Loss of signal threshold		–	–	0.225	–	V	
Allowable consecutive 0s before LOS		–	–	175	–		T1.231
Low limit input jitter tolerance [3]	10 Hz to 192.9 Hz[2]	–	10	–	–	U.I.	GR-499-CORE Category II equipment
	6.43KHz to 40KHz		0.3			U.I.	
Clock recovery PLL 3 dB bandwidth		–	–	10	–	kHz	
PLL peaking[4]		–	–	–	0	dB	
Receiver input impedance		–	–	40	–	kΩ	RTIP to RRING @ 772 kHz
Input return loss[2]	51 kHz–102 kHz	–	20	–	–	dB	See Application Information section.
	102–2048 kHz	–	20	–	–	dB	
	2048 kHz–3072 kHz	–	20	–	–	dB	

1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Guaranteed by design and other correlation methods.
3. Sinewave jitter with a peak-to-peak amplitude that corresponds, at minimum, with Figure 6, shall not cause bit errors or loss of frame alignment.
4. Guaranteed by design and other correlation methods. There will be no jitter gain within the specified operating range.

Table 8: Timing Characteristics (Over Recommended Range)

Parameter		Sym	Min	Typ[1]	Max	Unit	Test Condition
Master clock frequency	E1	MCLK	–	2.048	–	MHz	
	T1	MCLK	–	1.544	–	MHz	
Master clock tolerance		MCLKt	–	±50	–	ppm	
Master clock duty cycle		–	40		60	%	
Receive clock capture range [5]		–	–	±80	–	ppm	From nominal
Receive clock duty cycle [2]		RLCKd	40	50	60	%	
Receive clock pulse width [2]	E1	tPW	447	488	529	ns	
	T1	tPW	594	648	702	ns	
Receive clock pulse width low time	E1	tPWL	203	244	285	ns	
	T1	tPWL	270	324	378	ns	
Receive clock pulse width high time	E1	tPWH	–	244	–	ns	
	T1	tPWH	–	324	–	ns	
RPOS/RNEG data low time (MCLK=High)[3, 4]		tPWD1	200	244	300	ns	
RPOS/RNEG to RCLK rising setup time	E1	tSUR	50	203	–	ns	
	T1	tSUR	50	270	–	ns	
RCLK rising to RPOS/RNEG hold time	E1	tHR	50	203	–	ns	
	T1	tHR	50	270	–	ns	
Delay time between RPOS/RNEG and RCLK		–	–	5	–	ns	MCLK = High

1. Typical figures are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. RCLK duty cycle will vary depending on extent of received pulse jitter displacement. Maximum and minimum RCLK duty cycles are for worst case jitter conditions (0.2 U.I. displacement for E1 and 0.4 U.I. for T1 operation).
3. This mode disables clock recovery.
4. If MCLK is High, the PLL clock recovery circuits are disabled. RPOSx and RNEGx are fed to an internal XOR gate that connects this output to RCLKx for external clock recovery.
5. Assuming a ±50 ppm Master Clock (MCLK).

Figure 4: LXT336 Receive Timing Diagram

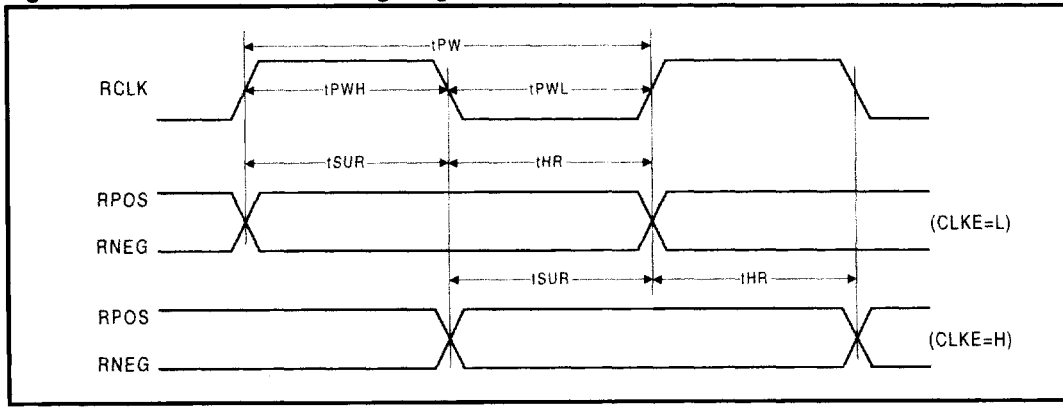


Figure 5: E1 Jitter Tolerance—G.823

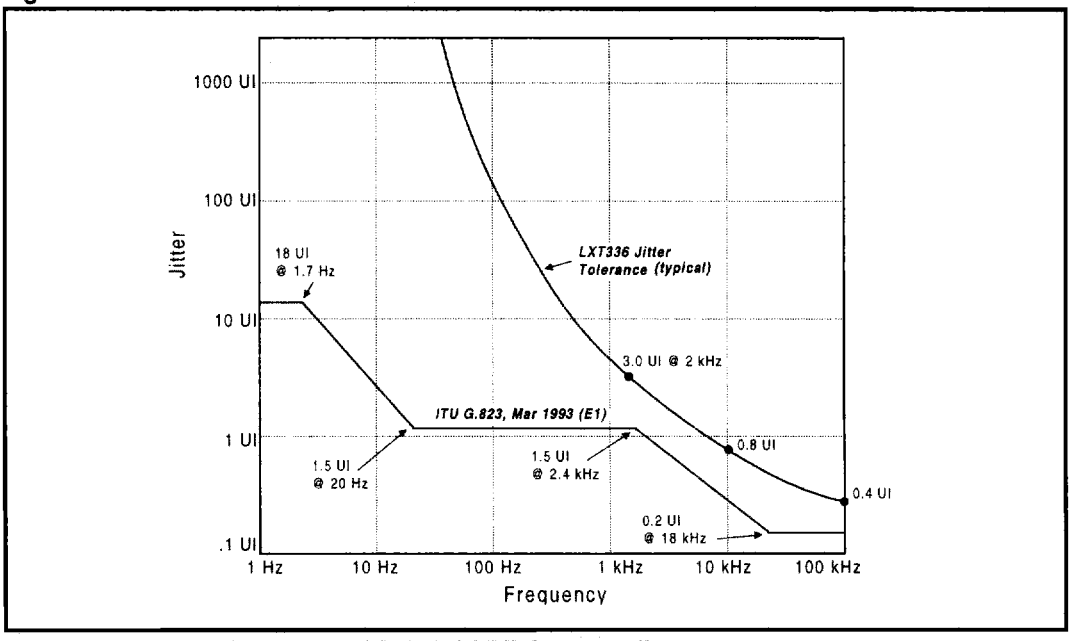


Figure 6: T1 Jitter Tolerance—GR-499-CORE Category II

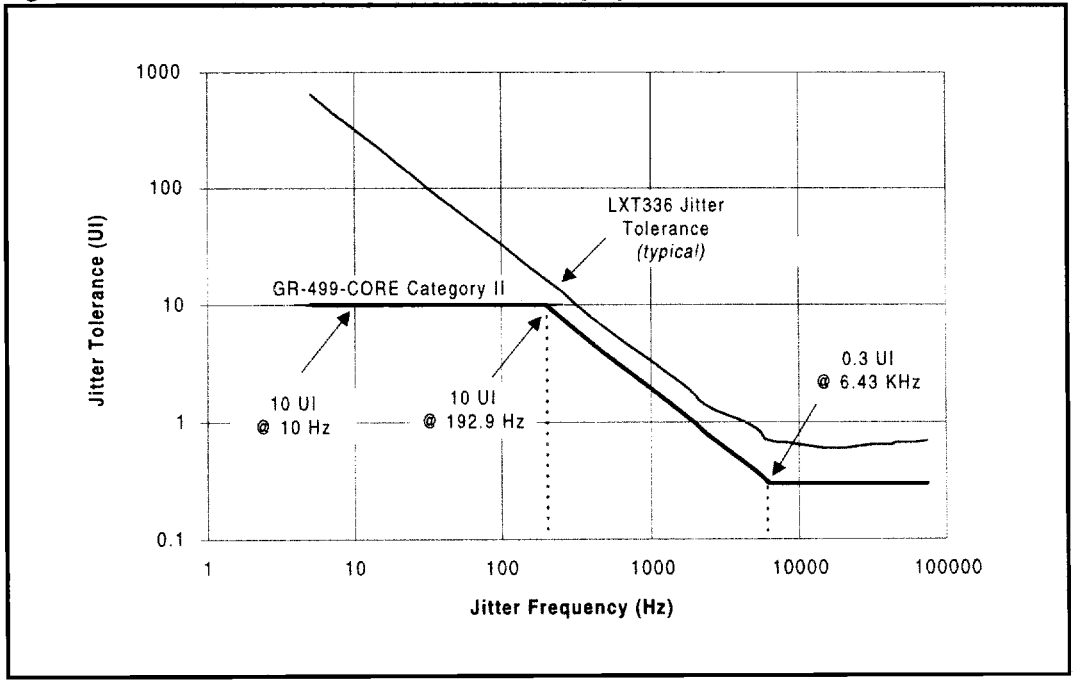


Table 9: Relevant Recommendations

Recommendation	Description
ITU	
G.703	Physical/electrical characteristics of hierarchical digital interfaces
G.704	Functional characteristics of interfaces associated with network nodes
G.735	Characteristics of Primary PCM multiple equipment operating at 2048 kbit/s and offering digital access at 384 kbit/s and/or synchronous digital access at 64 kbit/s
G.736	Characteristics of a synchronous digital multiplex equipment operating at 2048 kbit/s
G.775	Loss of signal (LOS) and alarm indication (AIS) defect detection and clearance criteria
G.823	The control of jitter and wander within digital networks which are based on the 2048 kbit/s hierarchy
O.151	Specification of instruments to measure error performance in digital systems
ANSI	
T1.102	Digital Hierarchy Electrical Interface
T1.231	Digital Hierarchy Layer 1 In-Service Digital Transmission Performance Monitoring
Bellcore	
GR-499-CORE	Transport Systems Generic Requirements

REVISION HISTORY

The following is a list of changes made to the LXT336 Data Sheet revision 0.0 to create revision 1.0. Note that minor editorial changes that have no technical significance are not included here.

Effected Info (rev. 1.0)	Page #	Description of Change
Features - Bullet	Front page	Added complies with ITU G.823 and Bellcore GR-499-CORE.
Table 1, pin 2	3	Changed pin2 from High to Clocked.
Table 1, pin 21	4	Replaced third sentence, removed forth sentence.
Fig. 2	9	Changed E1 to T1 and added connection dots.
Fig. 3	10	Changed E1 to T1, added connection dots and miscellaneous alignment.
Table 5	12	Added pin 49-54, 59-64 and all channels receiving line signals to footnote.
Table 6	13	Changed G.735 to G.823 and removed footnote 4 from middle of page.
Table 7	14	Changed footnotes middle of page and added footnote 3.
Fig. 5	16	Removed Fig. 5, E1 Pulse Mask G.703.
Fig. 6	17	Removed Fig. 6, T1 Pulse Mask, T1.102.
Fig. 7	18	Modified figure.
Fig. 9	18	Modified figure.