64K X 8 Bit CMOS Video RAM

FEATURES

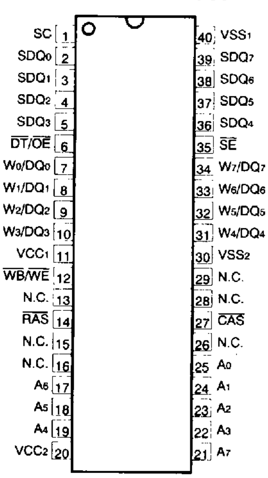
- **Dual port Architecture**
  64K x 8 bits RAM port
  256 x 8 bits SAM port
- **Performance range :**

Speed / Parameter	-7	-8	-10
RAM access time (t_{RAC})	70ns	80ns	100ns
RAM access time (t_{CAC})	20ns	20ns	25ns
RAM cycle time (t_{RC})	130ns	150ns	180ns
RAM page mode cycle (t_{PC})	45ns	50ns	60ns
SAM access time (t_{SCA})	20ns	20ns	25ns
SAM cycle time (t_{SCC})	25ns	25ns	30ns
RAM active current	85mA	80mA	70mA
SAM active current	45mA	40mA	40mA

- **Fast Page Mode**
- **RAM Read, Write, Read-Modify-Write**
- **Serial Read and Serial Write**
- **Read Transfer and Write Transfer**
- **Real time read transfer capability**
- **Write per bit masking on RAM write cycles**
- **$\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$, $\overline{\text{RAS}}$-only and Hidden Refresh**
- **Common Data I/O Using three state RAM Output control**
- **All Inputs and Outputs TTL Compatible**
- **Refresh: 256 Cycle/4ms**
- **Single +5V$\pm$ 10% Supply Voltage**
- **Plastic 40-Pin 400 mil SOJ**

PIN CONFIGURATION (TOP VIEWS)

40 Pin 400 mil SOJ



GENERAL DESCRIPTION

The Samsung KM428C64 is a CMOS 64K x 8 bit Dual Port DRAM. It consists of a 64K x 8 dynamic random access memory (RAM) port and 256 x 8 static serial access memory (SAM) port. The RAM and SAM ports operate asynchronously except during data transfer between the ports.

The RAM array consists of 256 bit rows of 2048 bits. It operates like a conventional 64K x 8 CMOS DRAM. The RAM port has a write per bit mask capability.

The SAM port consists of four 256 bit high speed shift registers that are connected to the RAM array through a 2048 bit data transfer gate. The SAM port has serial read and write capabilities.

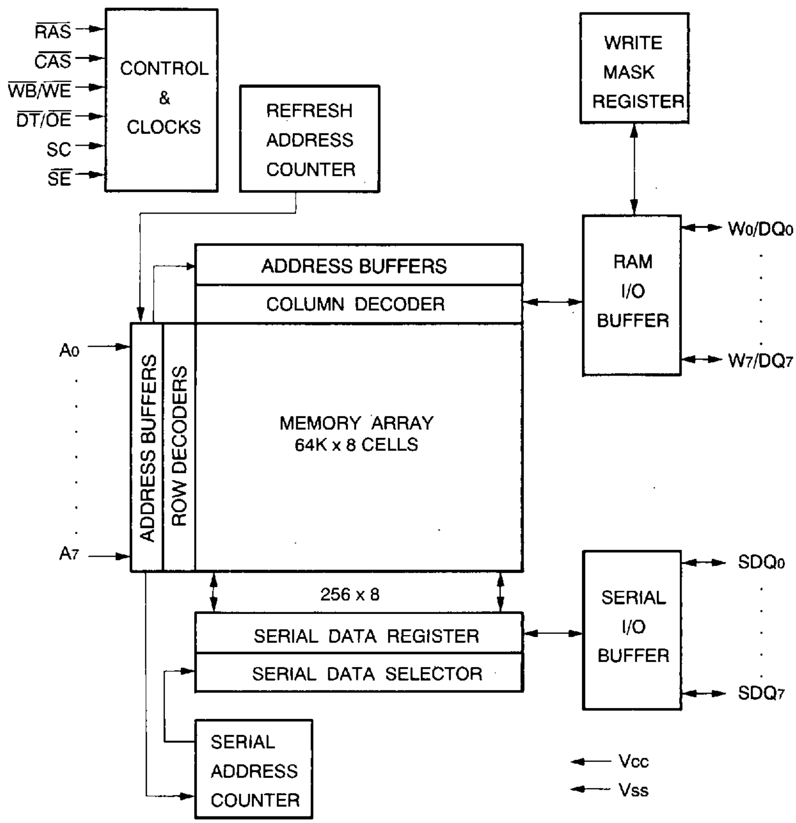
Data may be internally transferred bi-directionally between the RAM and SAM ports using read or write transfers.

Refresh is accomplished by familiar DRAM refresh modes. The KM428C64 supports $\overline{\text{RAS}}$-only, Hidden, and $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh for the RAM port. The SAM port does not require refresh.

All inputs and I/O's are TTL level compatible. All address lines and data inputs are latched on chip to simplify system design. The outputs are unlatched to allow greater system flexibility.

Pin Name	Pin Function
SC	Serial Clock
SDQ0-SDQ7	Serial Data Input / Output
$\overline{\text{DT}}/\overline{\text{OE}}$	Data Transfer / Output Enable
$\overline{\text{WB}}/\overline{\text{WE}}$	Write Per Bit / Write Enable
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{CAS}}$	Column Address Strobe
W0/DQ0-W7/DQ7	Data Write Mask / Input / Output
$\overline{\text{SE}}$	Serial Enable
A0-A7	Address Inputs
Vcc	Power (+5V)
Vss	Ground
N.C	No Connection

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	V_{IN}, V_{OUT}	-1 to + 7.0	V
Voltage on Supply Relative to Vss	V_{CC}	-1 to + 7.0	V
Storage Temperature	T_{stg}	-55 to + 150	℃
Power Dissipation	P_D	1	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to Vss, T_A = 0 to 70 ℃)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	-	6.5	V
Input Low Voltage	V_{IL}	- 1.0	-	0.8	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter (RAM Port)	SAM port	Symbol	KM428C64 -7	-8	-10	Unit
Operating Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @ tRC=min)	Standby	I_{CC1}	85	80	70	mA
	Active	$I_{CC1}A$	130	120	110	mA
Standby Current $\overline{RAS}$, $\overline{CAS}$, $\overline{DT}/\overline{OE}$, $\overline{WB}/\overline{WE}$ = V_{IH}	$\overline{SE}$ = V_{IH}, SC= V_{IL} Standby	I_{CC2}	5	5	5	mA
	$\overline{SE}$ = V_{IL}, SC= Cycling Active	$I_{CC2}A$	45	40	40	mA
$\overline{RAS}$ Only Refresh Current* ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ Cycling @ tRC=min)	Standby	I_{CC3}	85	80	70	mA
	Active	$I_{CC3}A$	130	120	110	mA
Fast Page Mode Current* ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ Cycling @ tPC=min)	Standby	I_{CC4}	65	60	50	mA
	Active	$I_{CC4}A$	110	100	90	mA
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @ tRC=min)	Standby	I_{CC5}	85	80	70	mA
	Active	$I_{CC5}A$	130	120	110	mA
Data Transfer Current* ($\overline{RAS}$ and $\overline{CAS}$ Cycling @ tRC=min)	Standby	I_{CC6}	115	110	100	mA
	Active	$I_{CC6}A$	160	150	140	mA

*NOTE: Real values are dependent on output loading and cycle rates. Specified values are obtained with the output open.

I_{CC} is specified as average current.

In I_{CC1}, I_{CC3} address transition should be changed only while $\overline{RAS}$ = V_{IL}.

In I_{CC4} address transition should be changed only once while $\overline{CAS}$ = V_{IH}.

INPUT/OUTPUT CURRENT (Recommended operating conditions unless otherwise noted.)

Item	Symbol	Min	Max	Unit
Input Leakage Current (Any Input $0 \leq V_{IN} \leq 6.5V$, all other pins not under test=0 volts.)	I_{IL}	-10	10	μA
Output Leakage Current (Data out is disabled, $0V \leq V_{OUT} \leq 5.5V$)	I_{OL}	-10	10	μA
Output High Voltage Level (RAM I_{OH}=-2mA, SAM I_{OH}=-2mA)	V_{OH}	2.4	-	V
Output Low Voltage Level (RAM I_{OL}=2mA, SAM I_{OL}=2mA)	V_{OL}		0.4	V

CAPACITANCE (T_A=25°C)

Item	Symbol	Min	Max	Unit
Input Capacitance (A_0~A_7)	C_{IN1}	2	6	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WB}/\overline{WE}$, $\overline{DT}/\overline{OE}$, SE, SC)	C_{IN2}	2	7	pF
Input/Output Capacitance (W_0/DQ_0~W_7/DQ_7)	C_{DQ}	2	7	pF
Input/Output Capacitance (SDQ_0~SDQ_7)	C_{SDQ}	2	7	pF

AC CHARACTERISTICS (0 °C $\leq T_A \leq$ 70 °C, Vcc=5.0V±10%, See notes 1,2)

Parameter	Symbol	70ns		80ns		100ns		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	130		150		180		ns	
Read-modify-write cycle time	t_{RWC}	175		200		240		ns	
Fast page mode cycle time	t_{PC}	45		50		60		ns	
Fast page mode read-modify-write	t_{PRWC}	85		90		115		ns	
Access time from $\overline{RAS}$	t_{RAC}		70		80		100	ns	3,4
Access time from $\overline{CAS}$	t_{CAC}		20		20		25	ns	4
Access time from column address	t_{AA}		35		40		50	ns	3,11
Access time from $\overline{CAS}$ precharge	t_{CPA}		40		45		55	ns	3
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	3		3		3		ns	3
Output buffer turn-off delay	t_{OFF}	3	15	3	15	3	15	ns	7
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	50		60		70		ns	
$\overline{RAS}$ pulse width	t_{RAS}	70	10K	80	10K	100	10K	ns	
$\overline{RAS}$ pulse width (fast page mode)	t_{RASP}	70	100K	80	100K	100	100K	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		20		25		ns	
$\overline{CAS}$ hold time	t_{CSH}	70		80		100		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10K	20	10K	25	10K	ns	

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SAMSUNG ELECTRONICS

AC CHARACTERISTICS (Continued)

Parameter	Symbol	70ns		80ns		100ns		Unit	Notes
		Min	Max	Min	Max	Min	Max		
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	50	25	60	25	75	ns	5,6
$\overline{RAS}$ to column addr. delay time	t_{RAD}	15	35	20	40	20	50	ns	11
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		ns	
$\overline{CAS}$ precharge time	t_{CPN}	10		10		15		ns	
$\overline{CAS}$ precharge time (fast page mode)	t_{CP}	10		10		15		ns	
Row addr. set-up time	t_{ASR}	0		0		0		ns	
Row Addr. hold time	t_{RAH}	10		15		15		ns	
Column addr. set-up time	t_{ASC}	0		0		0		ns	
Column addr. hold time	t_{CAH}	15		15		25		ns	
Column addr. hold referenced to $\overline{RAS}$	t_{AR}	55		60		75		ns	
Column addr. to $\overline{RAS}$ lead time	t_{RAL}	35		40		50		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	9
Read command hold referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	9
Write command hold time	t_{WCH}	15		15		20		ns	
Write command hold referenced to $\overline{RAS}$	t_{WCR}	55		60		75		ns	
Write command pulse width	t_{WP}	15		15		20		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	15		20		25		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	15		20		25		ns	
Data set-up time	t_{DS}	0		0		0		ns	10
Data hold time	t_{DH}	15		15		20		ns	10
Data hold referenced to $\overline{RAS}$	t_{DHR}	55		60		75		ns	
Write command set-up time	t_{WCS}	0		0		0		ns	8
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	45		45		50		ns	8
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	95		105		130		ns	8
Column addr. to $\overline{WE}$ delay time	t_{AWD}	60		65		80		ns	8
$\overline{CAS}$ set-up time (C-B-R refresh)	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ hold time (C-B-R refresh)	t_{CHR}	10		10		20		ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	10		10		10		ns	
$\overline{RAS}$ hold time referenced to $\overline{OE}$	t_{ROH}	20		20		20		ns	
Access time from output enable	t_{OEA}		20		20		25	ns	
Output enable to data input delay	t_{OED}	15		15		20		ns	
Output buffer turnoff delay from $\overline{OE}$	t_{OEZ}	3	15	3	15	3	20	ns	7
Output enable command hold time	t_{OEH}	15		15		20		ns	
Data to $\overline{CAS}$ delay	t_{DZC}	0		0		0		ns	
Data to output enable delay	t_{DZO}	0		0		0		ns	
Refresh period (256 cycle)	t_{REF}		4		4		4	ms	
$\overline{WB}$ set-up time	t_{WSR}	0		0		0		ns	

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AC CHARACTERISTICS (Continued)

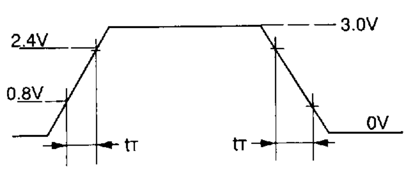
Parameter	Symbol	70ns Min	70ns Max	80ns Min	80ns Max	100ns Min	100ns Max	Unit	Notes
$\overline{\text{WB}}$ hold time	t_{RWH}	10		10		15		ns	
Write per bit mask data set-up time	t_{MS}	0		0		0		ns	
Write per bit mask data hold time	t_{MH}	10		15		15		ns	
$\overline{\text{DT}}$ high set-up time	t_{THS}	0		0		0		ns	
$\overline{\text{DT}}$ high hold time	t_{THH}	10		15		15		ns	
$\overline{\text{DT}}$ low set-up time	t_{TLS}	0		0		0		ns	
$\overline{\text{DT}}$ low hold time	t_{TLH}	10		15		15		ns	
$\overline{\text{DT}}$ low hold ref. to $\overline{\text{RAS}}$ (real time read transfer)	t_{RTH}	60		65		80		ns ns	
$\overline{\text{DT}}$ low hold ref. to $\overline{\text{CAS}}$ (real time read transfer)	t_{CTH}	20		25		30		ns	
$\overline{\text{DT}}$ low hold ref. to col. addr. (real time read transfer)	t_{ATH}	25		30		35		ns	
$\overline{\text{SE}}$ set-up time referenced to $\overline{\text{RAS}}$	t_{ESR}	0		0		0		ns	
$\overline{\text{SE}}$ hold time referenced to $\overline{\text{RAS}}$	t_{REH}	10		15		15		ns	
$\overline{\text{DT}}$ to $\overline{\text{RAS}}$ precharge time	t_{TRP}	50		60		70		ns	
$\overline{\text{DT}}$ precharge time	t_{TP}	20		25		30		ns	
$\overline{\text{RAS}}$ to first SC delay (read transfer)	t_{RSD}	70		80		100		ns	
$\overline{\text{CAS}}$ to first SC delay (read transfer)	t_{CSD}	30		35		50		ns	
Col. addr. to first SC delay (read transfer)	t_{ASD}	40		40		55		ns	
Last SC to $\overline{\text{DT}}$ lead time	t_{TSL}	5		5		5		ns	
$\overline{\text{DT}}$ to first SC delay time (read transfer)	t_{TSD}	10		15		15		ns	
Last SC to $\overline{\text{RAS}}$ set-up time (serial input)	t_{SRS}	30		30		30		ns	
$\overline{\text{RAS}}$ to first SC delay time (serial input)	t_{SRD}	20		25		25		ns	
$\overline{\text{RAS}}$ to serial input delay time	t_{SDD}	40		50		50		ns	
Serial output buffer turn-off delay from $\overline{\text{RAS}}$ (pseudo write transfer)	t_{SDZ}	10	30	10	35	10	50	ns	7
Serial input to first SC delay time	t_{SZS}	0		0		0		ns	
SC cycle time	t_{SCC}	25		25		30		ns	
SC pulse width (SC high time)	t_{SC}	7		7		10		ns	
SC precharge (SC low time)	t_{SCP}	7		7		10		ns	
Access time from SC	t_{SCA}		20		20		25	ns	4
Serial output hold time from SC	t_{SOH}	5		5		5		ns	
Serial input set-up time	t_{SDS}	0		0		0		ns	
Serial input hold time	t_{SDH}	15		15		20		ns	
Access time from $\overline{\text{SE}}$	t_{SEA}		20		20		25	ns	4
$\overline{\text{SE}}$ pulse width	t_{SE}	20		25		25		ns	
$\overline{\text{SE}}$ precharge time	t_{SEP}	20		25		25		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	70ns Min	70ns Max	80ns Min	80ns Max	100ns Min	100ns Max	Unit	Notes
Serial output turn-off from $\overline{SE}$	t_{SEZ}	3	15	3	15	3	15	ns	7
Serial input to $\overline{SE}$ delay time	t_{SZE}	0		0		0		ns	
Serial write enable set-up time	t_{SWS}	5		5		5		ns	
Serial write enable hold time	t_{SWH}	15		15		20		ns	
Serial write disable set-up time	t_{SWIS}	5		5		5		ns	
Serial write disable hold time	t_{SWIH}	15		15		20		ns	

NOTES

1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$,8SC cycles before proper device operation is achieved. If the internal refresh counter is used a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles are required instead of 8 $\overline{RAS}$ cycles.
2. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max), and are assumed to be 5ns for all inputs.
3. RAM port outputs are measured with a load equivalent to 1 TTL load and 50pF.
   D_{OUT} comparator level:V_{OH}/V_{OL} =2.0V / 0.8V
4. SAM port outputs are measured with a load equivalent to 1 TTL load and 30pF.
   Dout comparator level: V_{OH}/V_{OL}= 2.0/0.8V.
5. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. The t_{RCD}(max) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
6. Assumes that $t_{RCD} \geq t_{RCD}$(max).
7. The parameters, t_{OFF}(max), t_{OEZ}(max), t_{SDZ}(max) and t_{SEZ}(max), define the time at which the output achieves the open circuit condition and are not referenced to V_{OH} or V_{OL}.
8. The t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$(min) and $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$(min), then the cycle is a read-write cycle and the data out will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data out is indeterminate.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{WE}$ leading edge in read-write cycles.
11. Operation within the $t_{RAD(max)}$ limit insured that t_{RCD}(max) can be met. The t_{RAD}(max) is specified as a reference point only. If the t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
12. Input pulse levels are from 0.0V to 3.0Volts
    All timing measurements are referenced from V_{IL} (max) and V_{IH}(min) with transition time = 3.0ns



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DEVICE OPERATION

The KM428C64 contains 524,288 memory locations. Sixteen address bits are required to address a particular 8bit word in the memory array. Since the KM428C64 has only 8 address input pins, time multiplexed addressing is used to input 8 row and 8 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{\text{RAS}}$), the column address strobe ($\overline{\text{CAS}}$) and the valid row and column address inputs.

Operation of the KM428C64 begins by strobing in a valid row address with $\overline{\text{RAS}}$ while $\overline{\text{CAS}}$ remains high. Then the address on the 8 address input pins is changed from a row address to a column address and is strobed in by $\overline{\text{CAS}}$. This is the beginning of any KM428C64 cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationship. The cycle is terminated when both $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ have returned to the high state. Another cycle can be initiated after $\overline{\text{RAS}}$ remains high long enough to satisfy the $\overline{\text{RAS}}$ precharge time (t_{RP}) requirement.

$\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ Timing

The minimum $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ pulse widths are specified by t_{RAS} (min) and t_{CAS} (min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{\text{RAS}}$ low, it must not be aborted prior to satisfying the minimum $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ pulse widths.
In addition, a new cycle must not begin until the minimum $\overline{\text{RAS}}$ precharge time, t_{RP}, has been satisfied. Once a cycle begins, internal clocks and other circuits within the KM428C64 begin a complex sequence of events.
If the sequence is broken by violating minimum timing requirement, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining $\overline{\text{WB}}/\overline{\text{WE}}$ high during a $\overline{\text{RAS}}$ / $\overline{\text{CAS}}$ cycle. The access time is normally specified with respect to the falling edge of $\overline{\text{RAS}}$. But the access time also depends on the falling edge of $\overline{\text{CAS}}$ and on the valid column address transition.
If $\overline{\text{CAS}}$ goes low before t_{RCD} (max) and if the column address is valid before t_{RAD} (max) then the access time to valid data is specified by t_{RAC} (min). However, if $\overline{\text{CAS}}$ goes low after t_{RCD} (max) or the column address becomes valid after t_{RAD} (max), access is specified by t_{CAC} or t_{AA}.

The KM428C64 has common data I/O pins. The $\overline{\text{DT}}/\overline{\text{OE}}$ has been provided so the output buffer can be precisely controlled. For data to appear at the outputs, $\overline{\text{DT}}/\overline{\text{OE}}$ must be low for the period of time defined by t_{OEA}.

Write

The KM428C64 can perform early write and read-modify -write cycles. The difference between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{\text{WB}}/\overline{\text{WE}}$, $\overline{\text{DT}}/\overline{\text{OE}}$ and $\overline{\text{CAS}}$. In any type of write cycle. Data-in must be valid at or before the falling edge of $\overline{\text{WB}}/\overline{\text{WE}}$, whichever is later.

Fast Page Mode

Fast page mode provides high speed read,write or read-modify-write access to all memory cells within a selected row. These cycles may be mixed in any order. A fast page mode cycle begins with a normal cycle. Then, while $\overline{\text{RAS}}$ is kept low to maintain the row address, $\overline{\text{CAS}}$ is cycled to strobe in additional column addresses. This eliminates the time required to set up and strobe sequential row addresses for the same page.

Writer-Per-Bit

The write-per-bit function selectively controls the internal write-enable circuits of the RAM port. When $\overline{\text{WB}}/\overline{\text{WE}}$ is held "low" at the falling edge of $\overline{\text{RAS}}$, during a random access operation, the write-mask is enabled. At the same time, the mask data on the Wi/DQi pins is latched onto the write-mask register (WM1). When a "0" is sensed on any of the Wi/DQi pins, their corresponding write circuits are disabled and new data will not be written.

When a "1" is sensed on any of the Wi/DQi pins, their corresponding write circuits will remain enabled so that new data is written. The write mask data is valid for only one cycle the truth table of the write-per-bit function are shown in table 1.

Table 1. Truth table for write-per-bit function

$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{DT}}/\overline{\text{OE}}$	$\overline{\text{WB}}/\overline{\text{WE}}$	Wi/DQi	FUNCTION
	H	H	H	*	WRITE ENABLE
	H	H	L	1	WRITE ENABLE
				0	WRITE MASK

DEVICE OPERATION (Continued)

Data Output

The KM428C64 has a three-state output buffer which are controlled by $\overline{CAS}$ and $\overline{DT}/\overline{OE}$. When either $\overline{CAS}$ or $\overline{DT}/\overline{OE}$ is high (V_{IH}) the output is in the high impedance (Hi-Z) state. In any cycle in which valid data appears at the output goes into the low impedance state in a time specified by t_{CLZ} after the falling edge of $\overline{CAS}$. Invalid data may be present at the output during the time after t_{CLZ} and before the valid data appears at the output. The timing parameter t_{CAC}, t_{RAC} and t_{AA} specify when the valid data will be present at the output. The valid data remains at the output until $\overline{CAS}$ returns high. This is true even if a new $\overline{RAS}$ cycle occurs (as in hidden refresh). Each of the KM428C64 operating cycles is listed below after the corresponding output state produced by the cycle.

Valid Output Data: Read, Read-Modify-Write, Hidden refresh, Fast page mode Read, Fast Page Mode Read-Modify-Write.

Refresh

The data in the KM428C64 is stored on a tiny capacitor within each memory cell. Due to leakage the data may leak off after a period of time. To maintain data integrity it is necessary to refresh each of the 256 rows every 4 ms. Any operation cycle performed in the RAM port refreshes the 2048 bits selected by the row addresses or an on-chip refresh address counter.
Either a burst refresh or distributed refresh may be used. There are several ways to accomplish this.

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. This cycle must be repeated for each of the 256 row address,(A_0 ~ A_7).

$\overline{CAS}$-before-$\overline{RAS}$ Refresh: The KM428C64 has $\overline{CAS}$-before-$\overline{RAS}$ on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ is held low for the specified set up time (t_{CSR}) before $\overline{RAS}$ goes low the on-chip refresh circuitry is enabled. An internal refresh operation automatically occurs. The refresh address is supplied by the on-chip refresh address counter which is then internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{CAS}$ active time and cycling $\overline{RAS}$.

The KM428C64 hidden refresh cycle is actually a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is the preferred method.

Transfer Operation

1. Normal Write/Read Transfer.
   (SAM → RAM / RAM → SAM)
2. Pseudo Write Transfer (Switches serial port from serial Read to serial Write. No actual data transfer takes place between the RAM and the SAM).
3. Real Time Read Transfer (On the fly Read Transfer Operation).

Read-Transfer Cycle

A read-transfer consists of loading a selected row of data from the RAM array into the SAM register.
A read-transfer is accomplished by holding $\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ low and $\overline{WB}/\overline{WE}$ high at the falling edge of $\overline{RAS}$. The row address selected at the falling edge of $\overline{RAS}$ determines the RAM row to be transferred into the SAM.

The actual data transfer completed at the rising edge of $\overline{DT}/\overline{OE}$. When the transfer is completed, the SDQ lines are set into the output mode.
In a read/real-time read-transfer cycle, the transfer of a new row of data is completed at the rising edge of $\overline{DT}/\overline{OE}$ and becomes valid on the SDQ lines after the specified access time t_{SCA} from the rising edge of the subsequent serial clock (SC) cycle. The start address of the serial pointer of the SAM is determined by the column address selected at the falling edge of $\overline{CAS}$

Write Transfer Cycle

A write transfer cycle consist of loading the content of the SAM data register into a selected row of RAM array. A write transfer is accomplished by $\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ low, $\overline{WB}/\overline{WE}$ low and $\overline{SE}$ low at the falling edge of $\overline{RAS}$. The row address selected at the falling edge of $\overline{RAS}$ determines the RAM row address into which the data will be transferred. The column address selected at the falling edge of $\overline{CAS}$ determines the start address of the serial pointer of the SAM. After the write transfer is completed, the SDQ lines are in the input mode so that serial data synchronized with SC can be loaded. When consecutive write transfer operations are performed, there as a delay in availability between the last bit of the previous row and the first bit of the new row. Consequently the SC clock must be held at a constant V_{IL} or V_{IH} after the SC precharge time t_{SCP} has seen satisfied, a rising edge of the SC clock until after a specified delay t_{SRD} from the falling edge of $\overline{RAS}$.

DEVICE OPERATION (Continued)

Table 2. Truth table for Transfer operation

$\overline{RAS}$	$\overline{CAS}$	$\overline{DT}/\overline{OE}$	$\overline{WB}/\overline{WE}$	$\overline{SE}$	FUNCTION	TRANSFER DIRECTION
	H	L	H	*	Read transfer cycle	RAM → SAM
	H	L	L	L	Write transfer cycle	SAM → RAM
	H	L	L	H	Pseudo write transfer cycle	—

Pseudo Write Transfer Cycle

The pseudo write transfer cycle switches SDQ lines from serial read mode to serial write mode. It doesn't perform data transfer. A pseudo write transfer is accomplished by holding $\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ low, $\overline{WB}/\overline{WE}$ low and $\overline{SE}$ high at the falling edge of $\overline{RAS}$. The pseudo write transfer cycle must be performed after a read transfer cycle if the subsequent operation is a write transfer cycle. There is a timing delay associated with the switching of the SDQ lines from serial output mode to serial input mode. During this period, the SC clock must be held at a constant V_{IL} or V_{IH} after the t_{SC} precharge time has been satisfied. A rising edge of the SC clock must not occur until after the specified delay t_{SRD} from the rising edge of $\overline{RAS}$.

Serial Clock (SC)

All operation of the SAM port are synchronized with the serial clock SC. Data is shifted in or out of the SAM registers at the rising edge of SC. In a serial read, the output data becomes valid on the SDQ pins after the maximum specified serial access time t_{SCA} from the rising edge of SC. The serial clock SC also increments the 8 bit serial pointer which is used to select the SAM address. The pointer address is incremented in a wrap around mode to select sequential locations after the starting location which is determined by the column address in the read transfer cycle.

Serial Input / Output (SDQ0 ~ SDQ7)

Serial input and serial output share common I/O pins. Serial input or output mode is determined by the most recent transfer cycle. When a read transfer cycle is performed, the SAM port is in the output mode. When a pseudo write transfer is performed, the SAM port operation is switched from output mode to input mode. During subsequent write transfer cycle, the SAM port remains is the input mode.

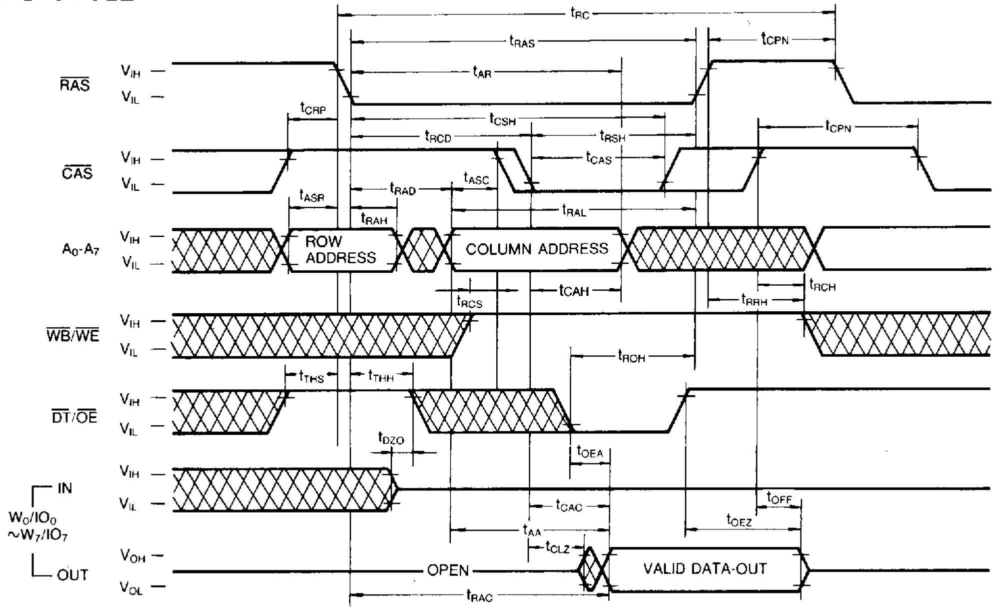
Power - up

An initial pause of 200 μsec is required, after power-up followed by 8 initialization cycles before proper device operation is assured.

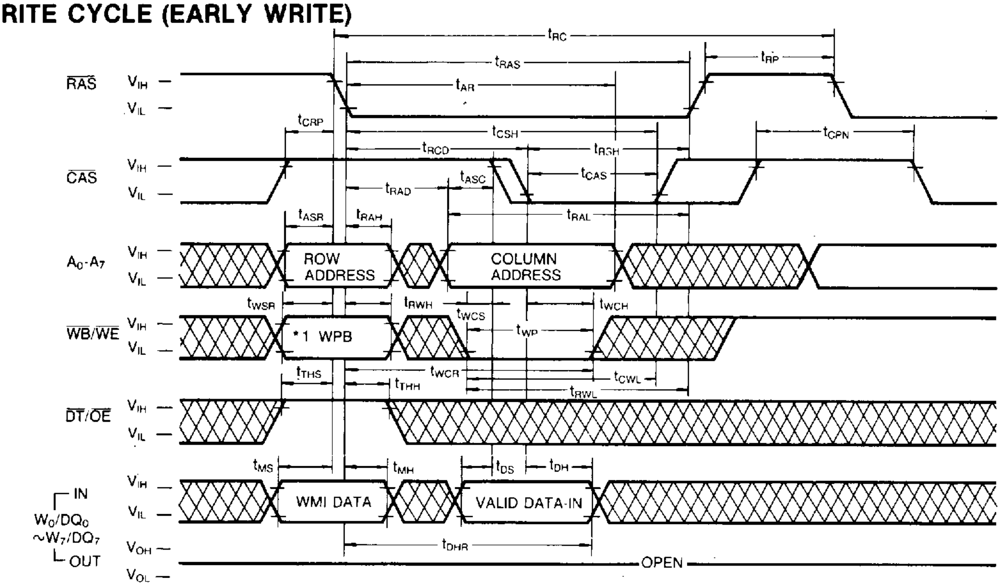
2

TIMING DIAGRAMS

READ CYCLE



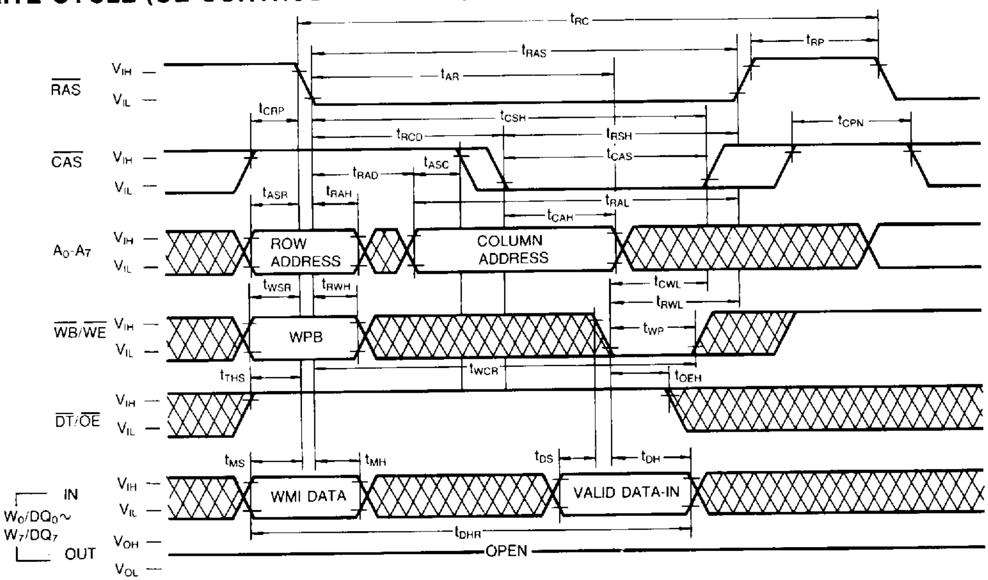
WRITE CYCLE (EARLY WRITE)



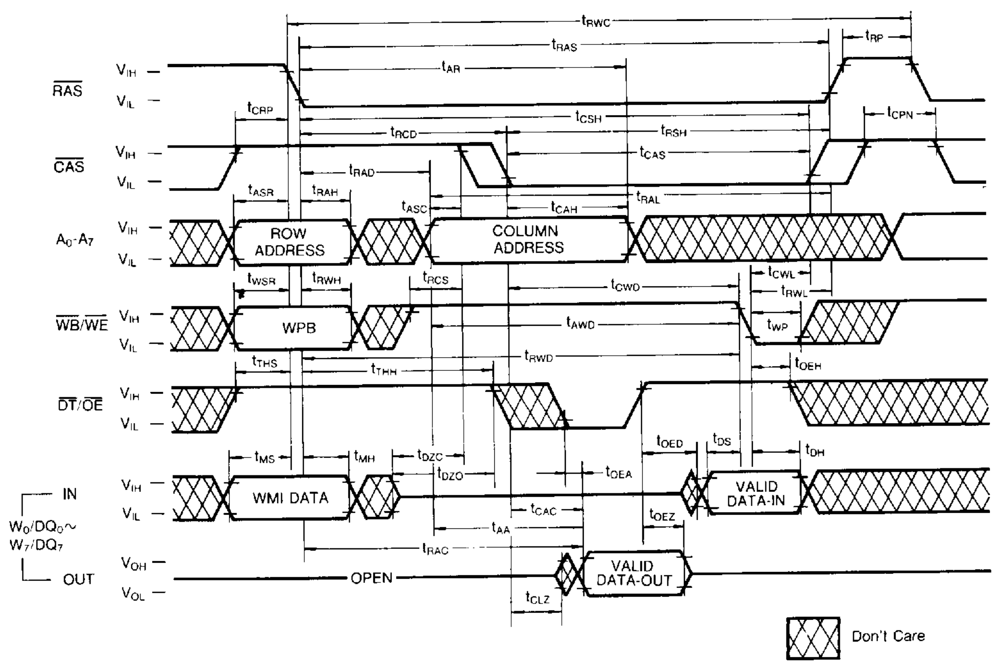
Don't Care

TIMING DIAGRAMS (Continued)

WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

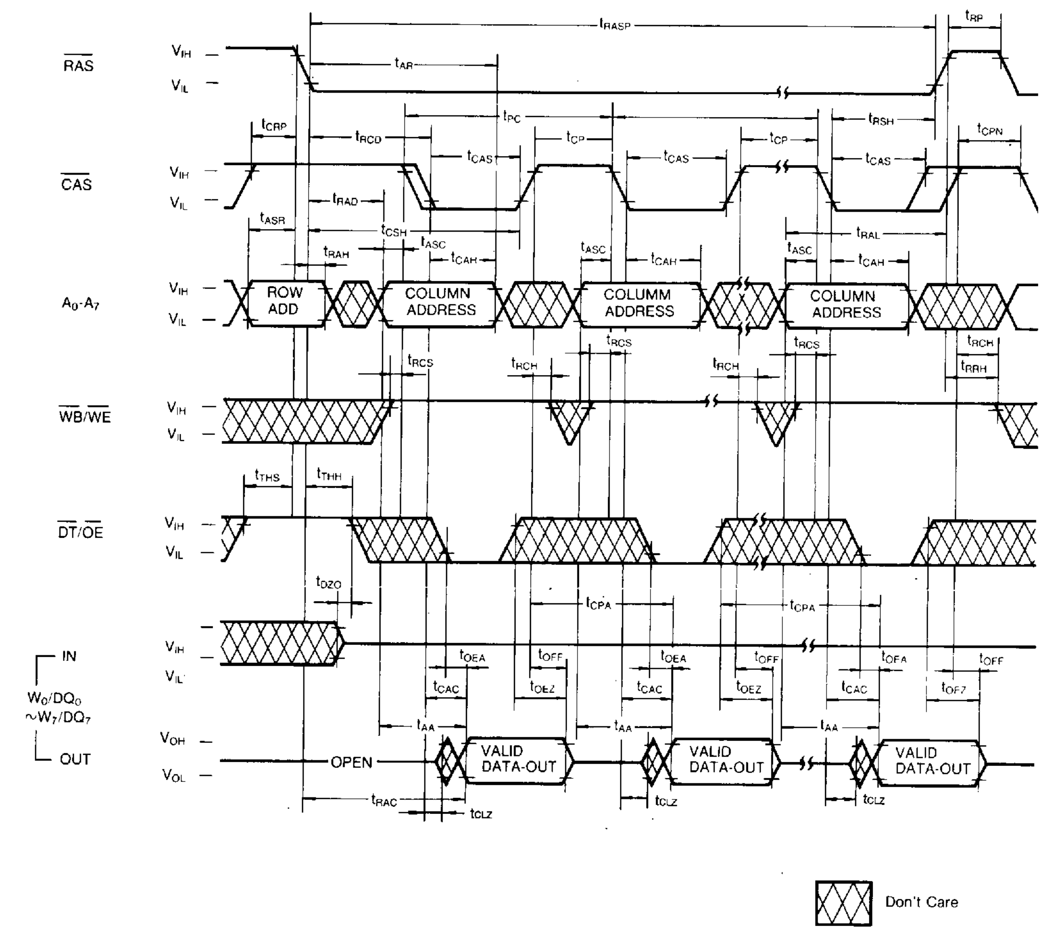


READ-WRITE/READ-MODIFY-WRITE CYCLE



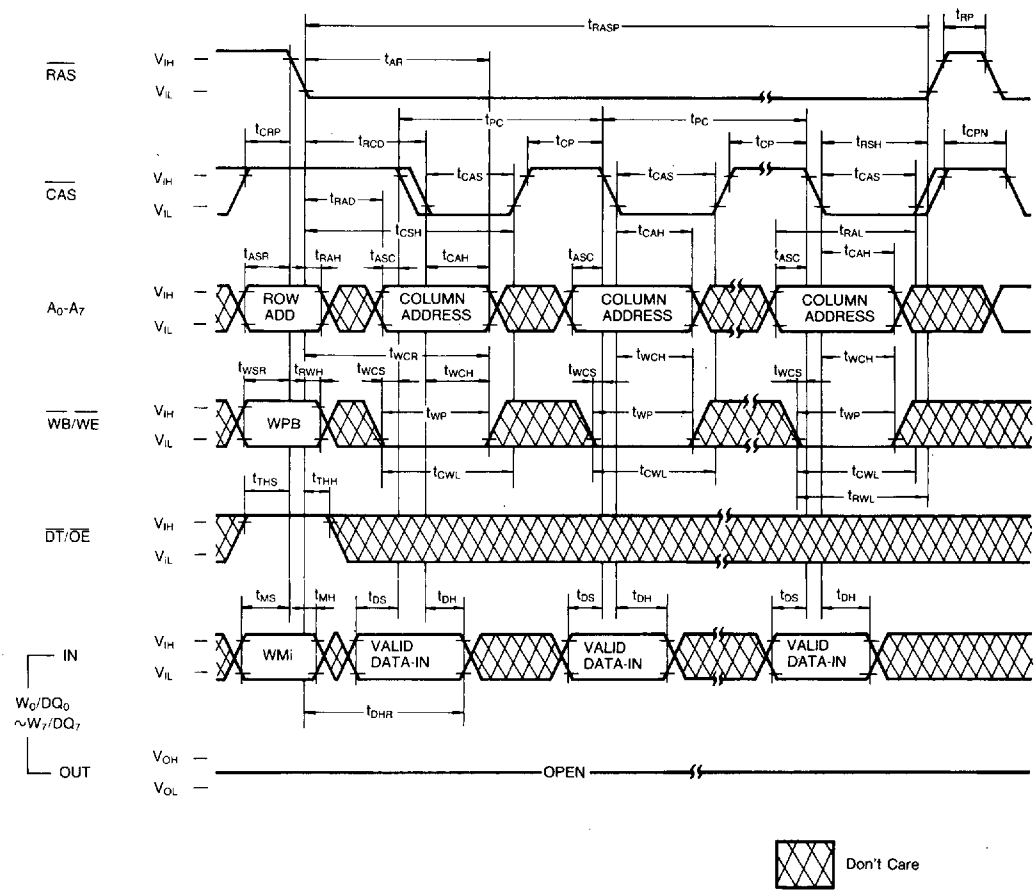
TIMING DIAGRAMS (Continued)

PAGE MODE READ CYCLE



TIMING DIAGRAMS (Continued)

PAGE MODE WRITE CYCLE (EARLY WRITE)



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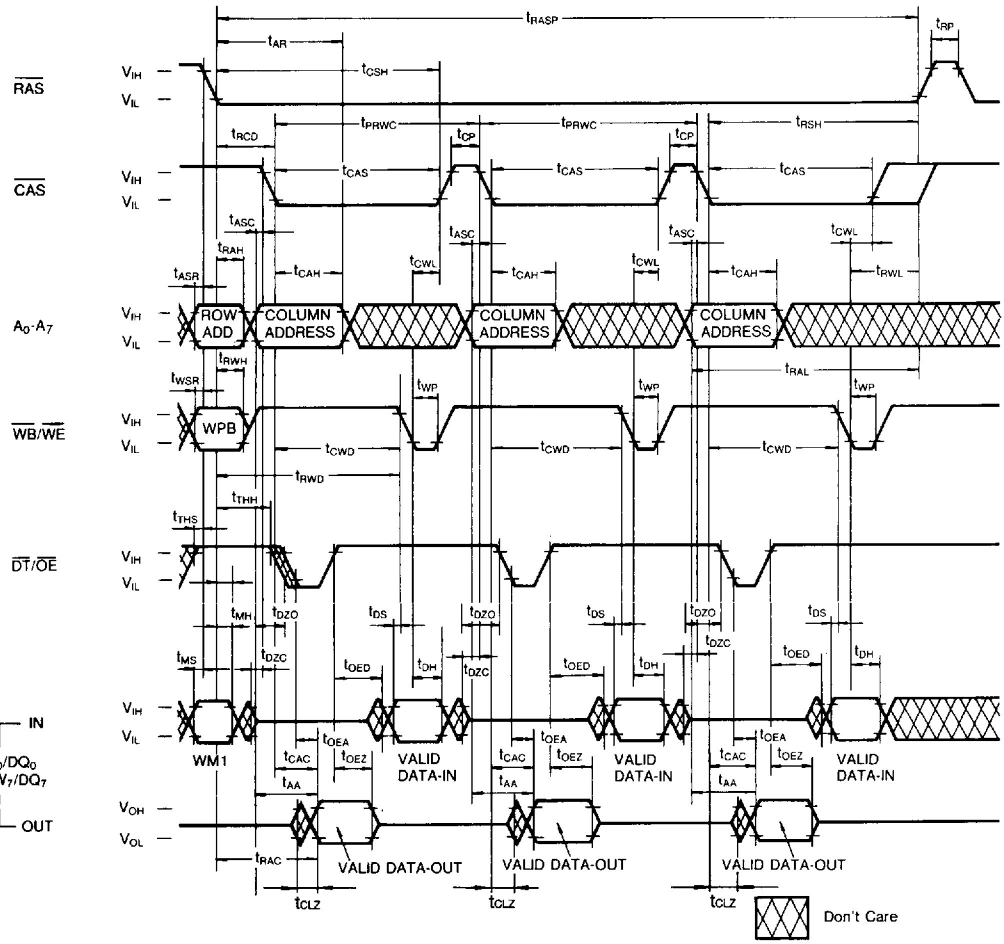
TIMING DIAGRAMS (Continued)

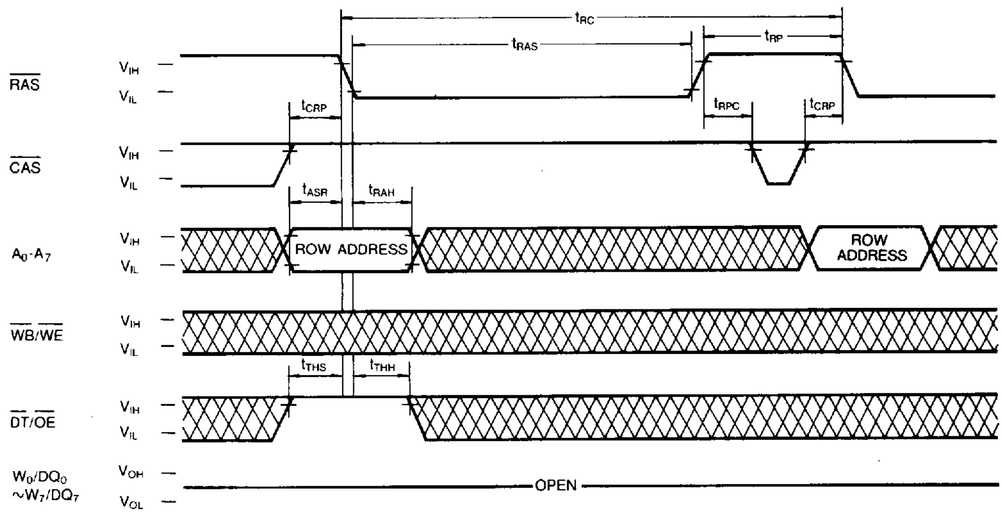
PAGE MODE READ-MODIFY-WRITY CYCLE



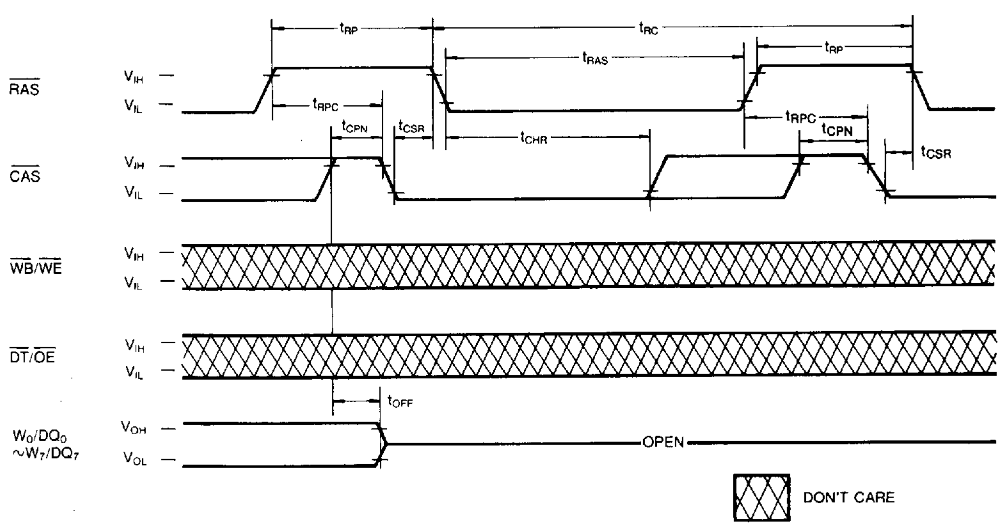
2

TIMING DIAGRAMS (Continued)

RAS ONLY REFRESH CYCLE

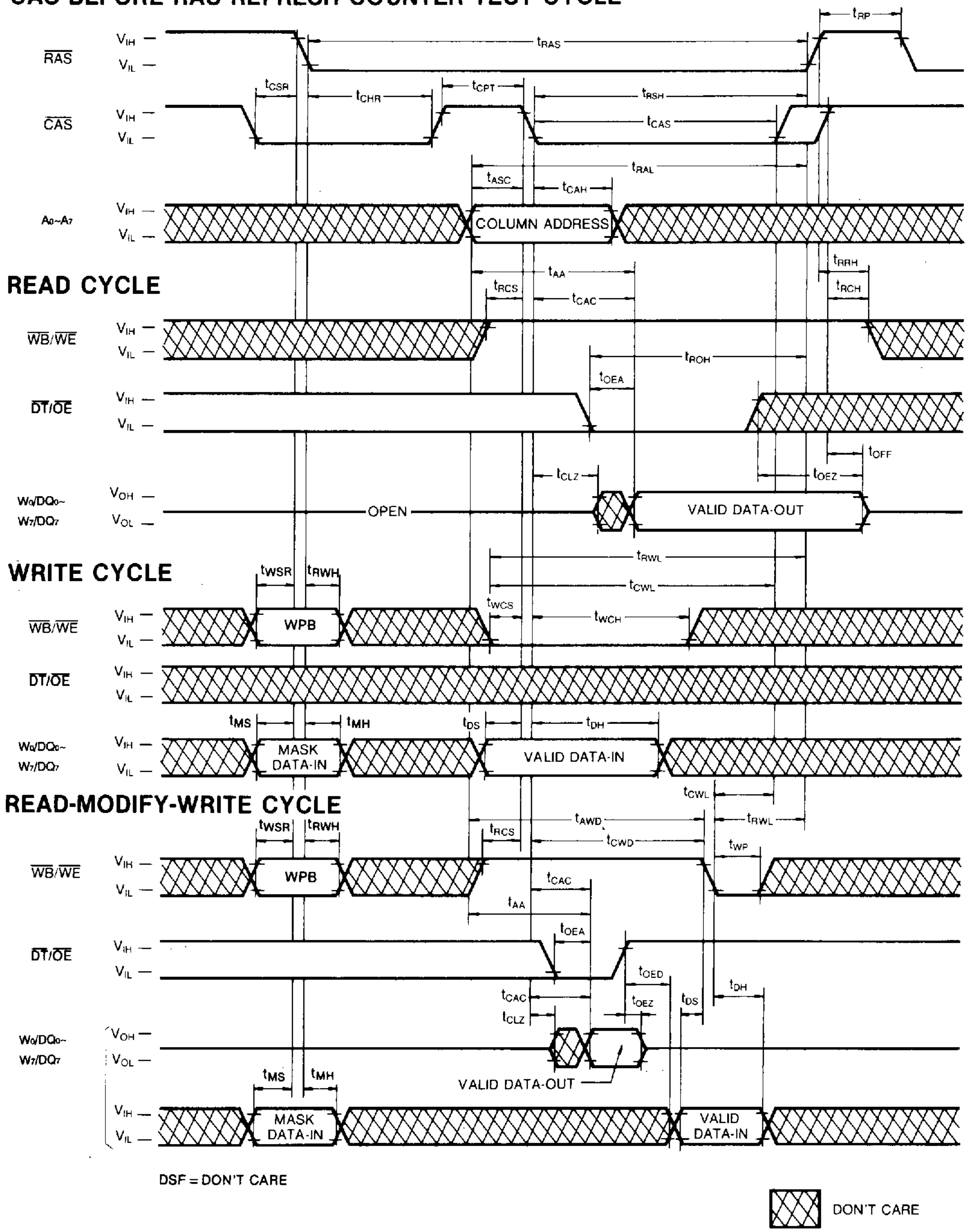


CAS BEFORE RAS REFRESH



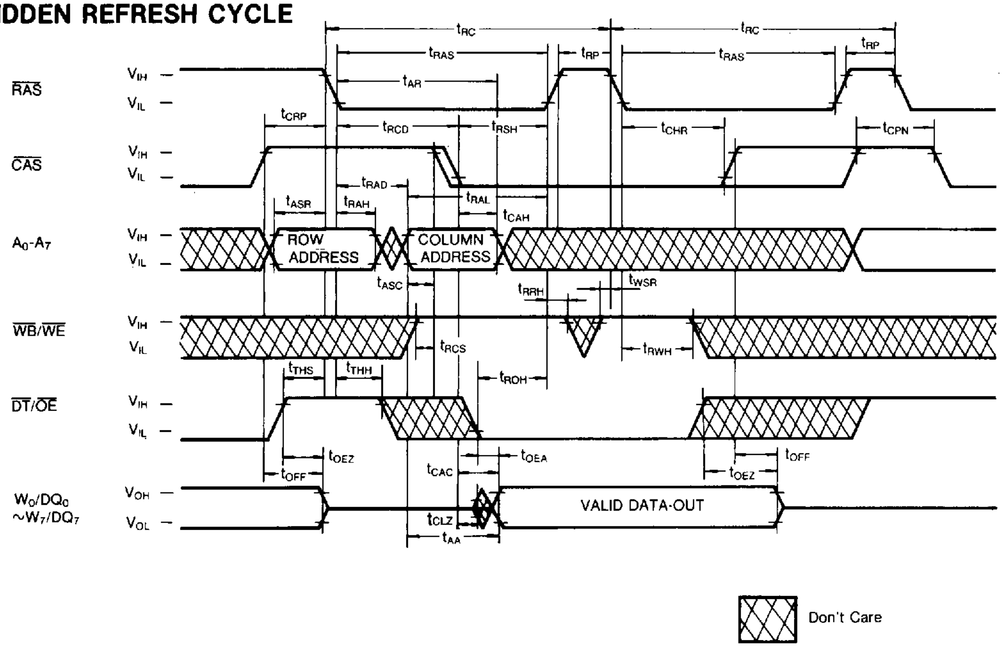
TIMING DIAGRAMS (Continued)

CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



TIMING DIAGRAMS (Continued)

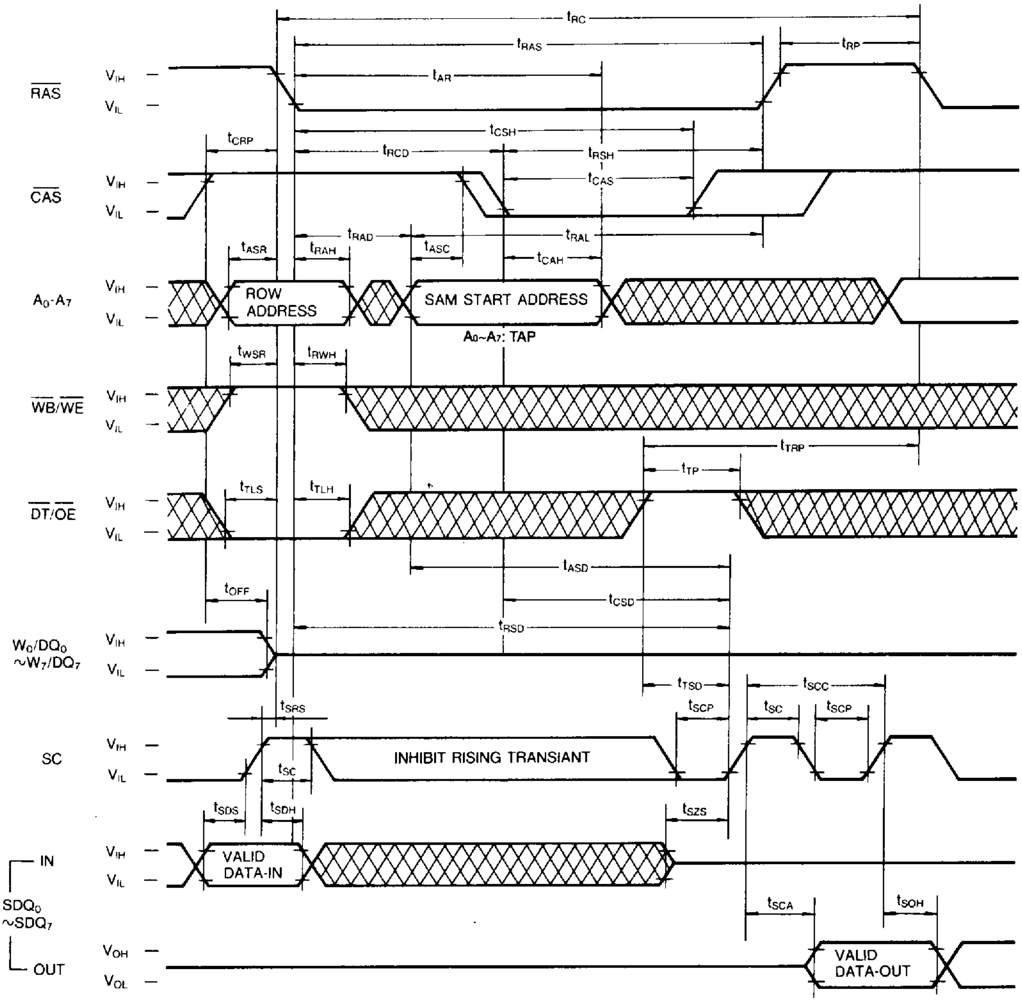
HIDDEN REFRESH CYCLE



2

TIMING DIAGRAMS (Continued)

READ TRANSFER CYCLE



Note: $\overline{SE} = V_{IL}$

Don't Care

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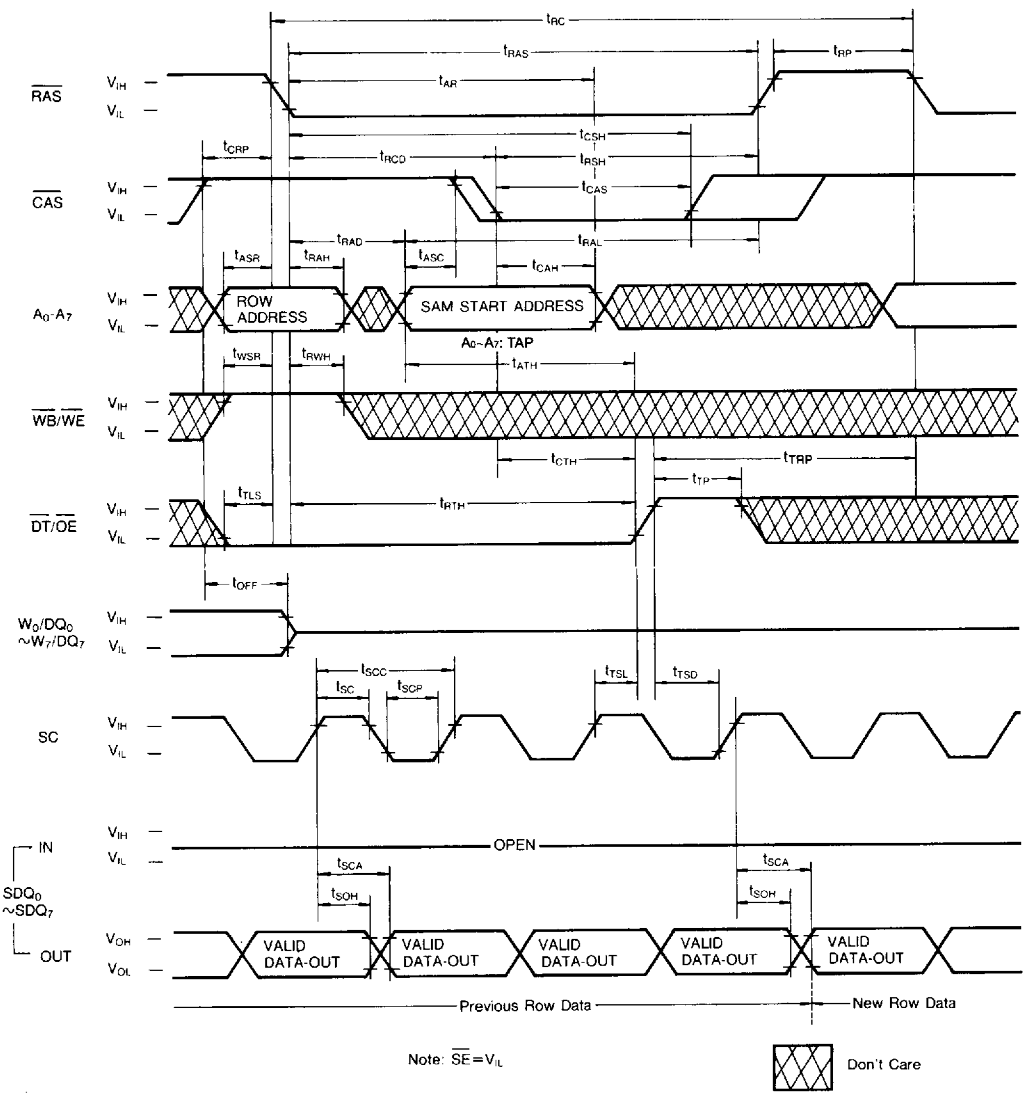
TIMING DIAGRAMS (Continued)

REAL TIME READ TRANSFER CYCLE



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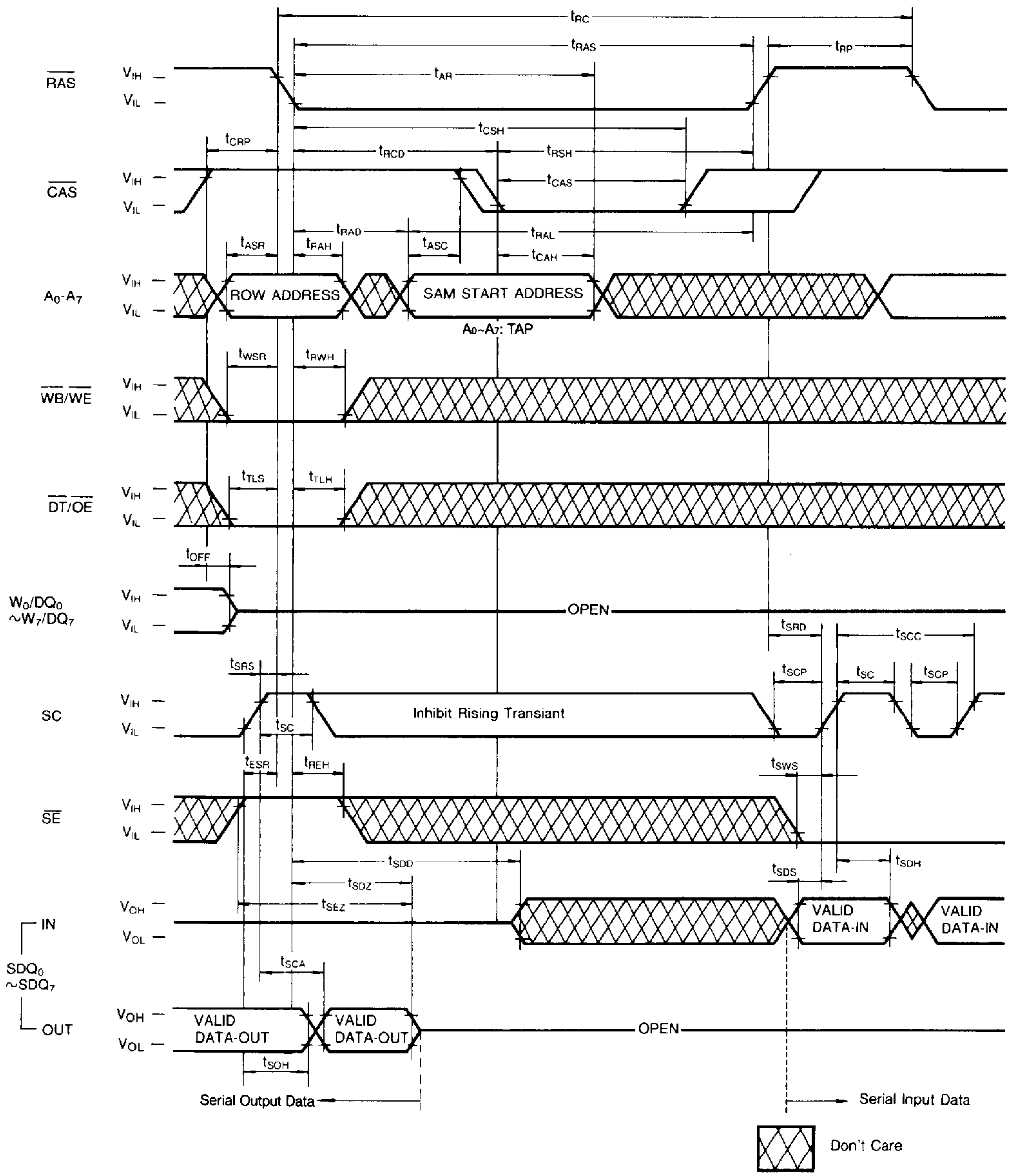
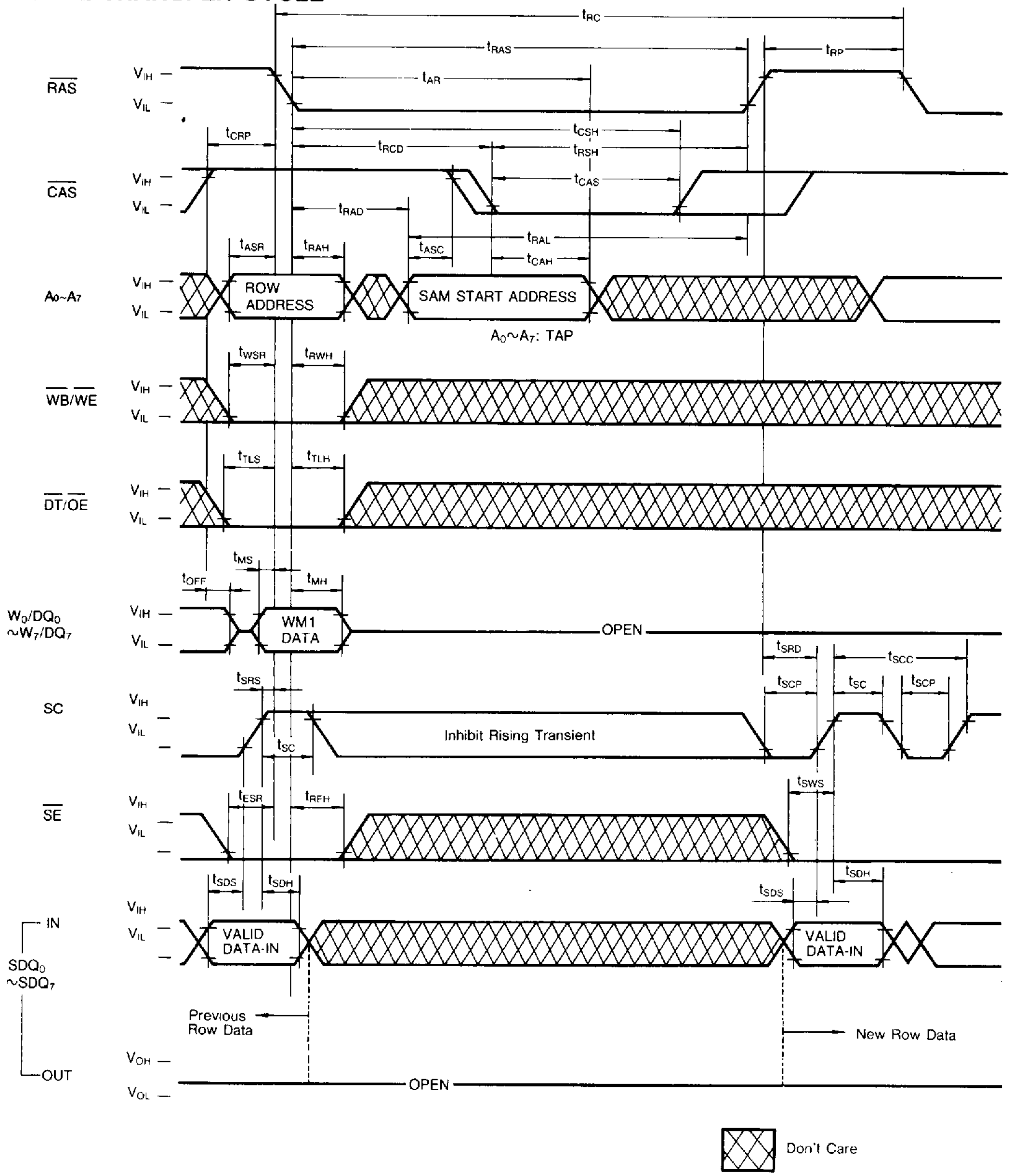
TIMING DIAGRAMS (Continued)

PSEUDO WRITE TRANSFER CYCLE



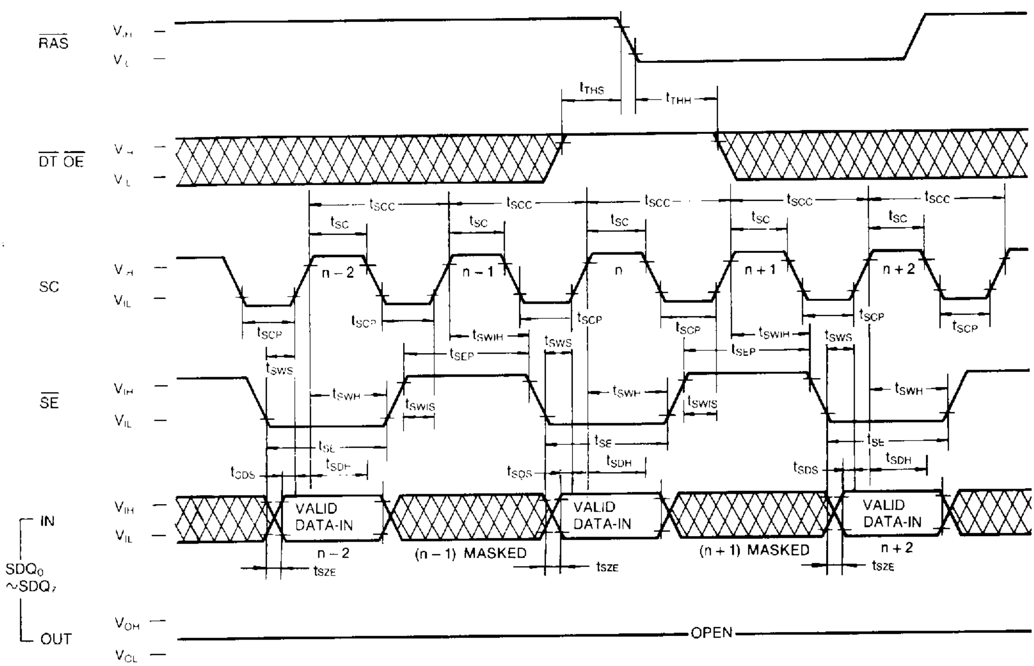
TIMING DIAGRAMS (Continued)

WRITE TRANSFER CYCLE

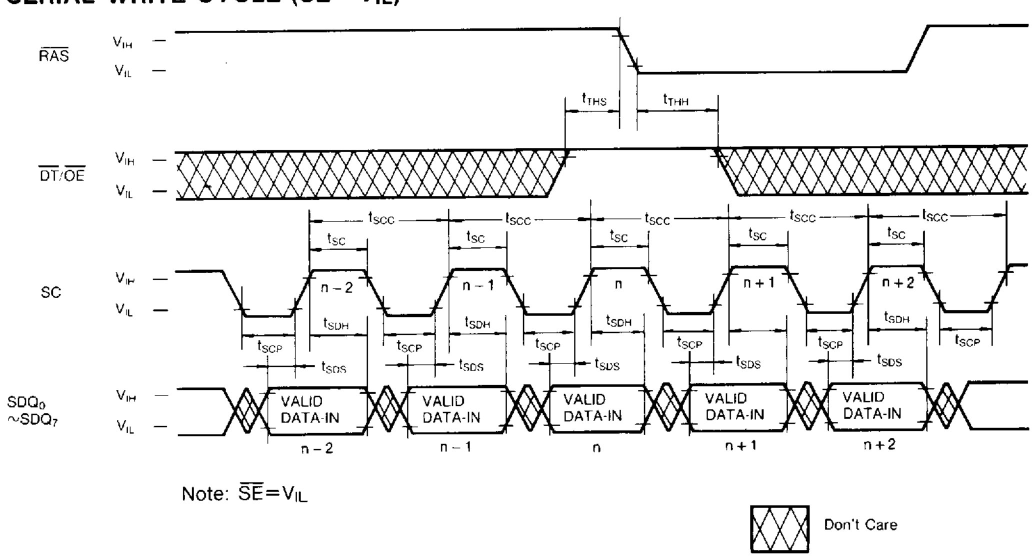


TIMING DIAGRAMS (Continued)

SERIAL WRITE CYCLE ($\overline{SE}$ Controlled Inputs)



SERIAL WRITE CYCLE ($\overline{SE}=V_{IL}$)



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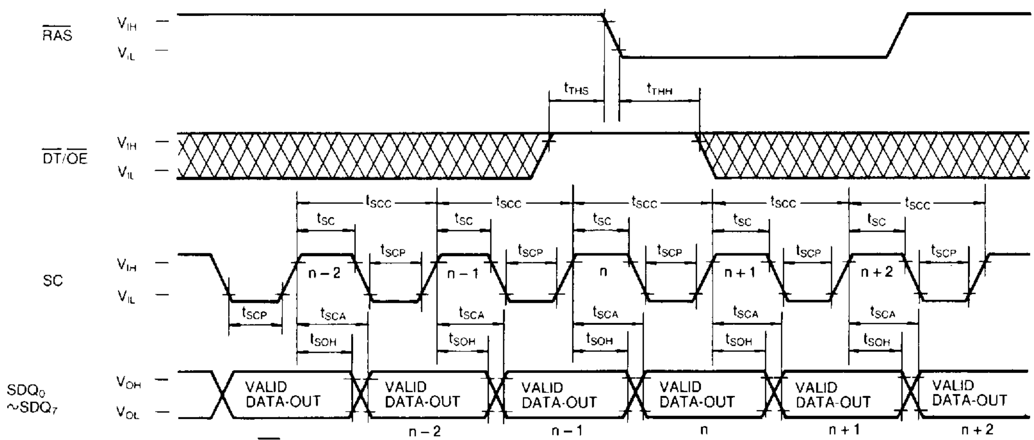
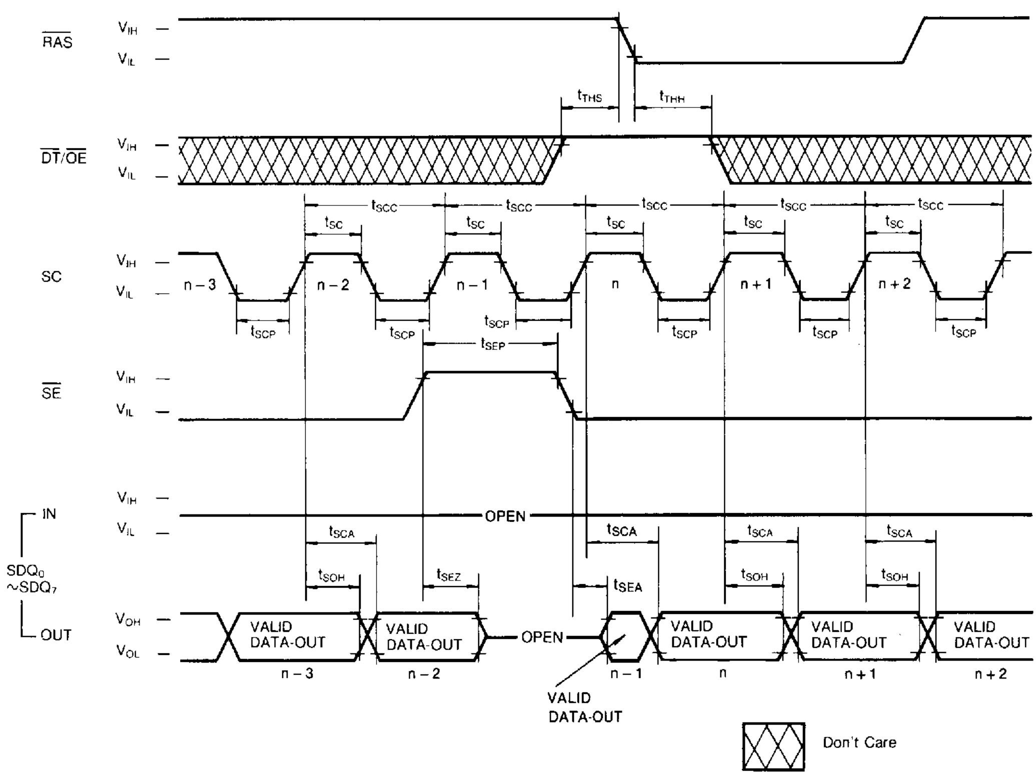
SERIAL READ CYCLE ($\overline{SE} = V_{IL}$)



Note: $\overline{SE} = V_{IL}$

SERIAL READ CYCLE ($\overline{SE}$ Controlled Outputs)



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PACKAGES DIMENSION

40 LEAD PLASTIC SMALL OUT LINE J FORM PACKAGE

Unit : Inches (millimeters)