# NN5283206 series
# CMOS 128K× 32bit × 2banks
# Synchronous Graphic Dynamic RAM

NPNX

## DESCRIPTION

**Target Specification**

The NN5283206 series is a CMOS Synchronous Graphic dynamic Random Access Memory organized as 131, 072 words x 32bits x 2banks.

The NN5283206 series features a fully synchronous operation referenced to a positive edge of clock input. The read/write operation can be performed in burst mode where data is transferred in either a 2, 4, 8 words or full page. 2 banks organization allows continual read/write operation. All operations are controlled by command setting. By having a programmable Mode register,8 column Block Write and write per bit functions provide better peformance for graphic application. Refresh is accomplished by Auto refresh and Self refresh.

The NN5283206 series is available in 100-pin QFP . All input and output are compatible with Low Voltage TTL (LVTTL).

## FEATURES

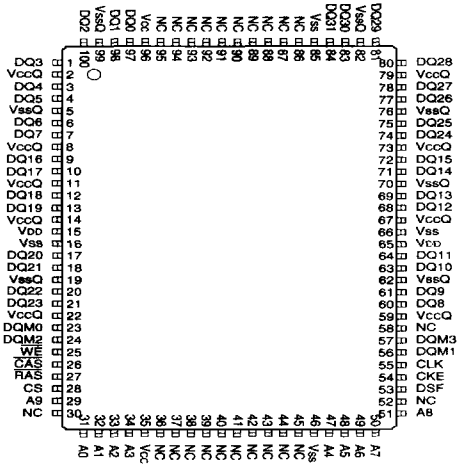
- 131,072×32bits×2banks Organization
- Single 3.3V ±0.3V Power Supply
- Performance Ranges

| Parameter | | -10 | -12 | -15 |
|---|---|---|---|---|
| Min. Clock Cycle Time | ($t_{CK}$) | 10ns | 12ns | 15ns |
| Max. $\overline{RAS}$ Access Time[1] | ($t_{RCD}$)+($t_{ACK}$) | 53ns | 65ns | 81ns |
| Max. Read Command Access Time[1] | ($t_{ACK}$) | 28ns | 35ns | 43ns |
| Max. CLK Access Time[1] | ($t_{AC}$) | 8ns | 10ns | 13ns |
| Min. Active Command Cycle Time[2] | ($t_{RC}$) | 75ns | 94ns | 112ns |

NOTE 1.CAS latency=3
2.Same Bank

- Single Pulsed $\overline{RAS}$
- 2 Banks Operation (simultaneously and independently)
- Read/Write Operation Type
  - Burst Read/Write Operation
  - Burst Read and Single Write Operation
- 8 column Block Write and write per bit capability
- Programmable Burst Sequence
  - Sequential (Wrap/Non-Wrap Mode)
  - Interleave
- Programmable Burst Length
  1, 2, 4, 8, and Full Page
- Full Page Burst Stop Capable
- Programmable $\overline{CAS}$ Latency
  1, 2, and 3
- Byte Control by DQM0,1,2 and 3
- Fully LVTTL compatible Inputs/Outputs and Clock
- 1,024 Refresh Cycles / 16ms
- Refresh Modes
  Auto Refresh
  Self Refresh
- High Reliability Package
  Plastic 100pin QFP

## PIN CONFIGURATION (TOP VIEW)




100-pin QFP

## PIN NAMES

| | | | |
|---|---|---|---|
| A0 ~A9 | Address Input<br>Row Address : A0~A8<br>Column Address: A0~A7<br>Bank Select : A9 | DQM0 ~DQM3 | Byte I/O Mask |
| | | CLK | Clock Input |
| DQ0~ DQ31 | Data Input/Output | CKE | Clock Enable |
| | | DSF | Special function Enable |
| $\overline{CS}$ | Chip Select | VDD | Power Supply (3.3V · Internal Circuit) |
| $\overline{RAS}$ | Row Address Strobe | VDDQ | Power Supply (3.3V · DQ Buffer) |
| $\overline{CAS}$ | Column Address Strobe | VSS | Power Supply (0V · Internal Circuit) |
| $\overline{WE}$ | Write Enable | VSSQ | Power Supply (0V · DQ Buffer) |
| | | NC | No Connection |