54F/74F280

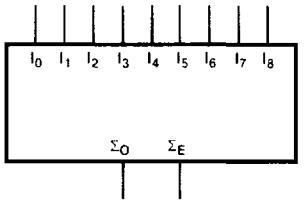
9-Bit Parity Generator/Checker

Description

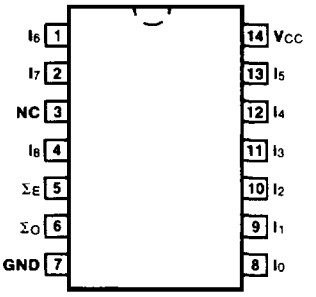
The 'F280 is a high-speed parity generator/checker that accepts nine bits of input data and detects whether an even or an odd number of these inputs is HIGH. If an even number of inputs is HIGH, the Sum Even output is HIGH. If an odd number is HIGH, the Sum Even output is LOW. The Sum Odd output is the complement of the Sum Even output.

Ordering Code: See Section 5

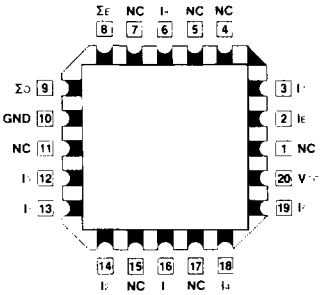
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

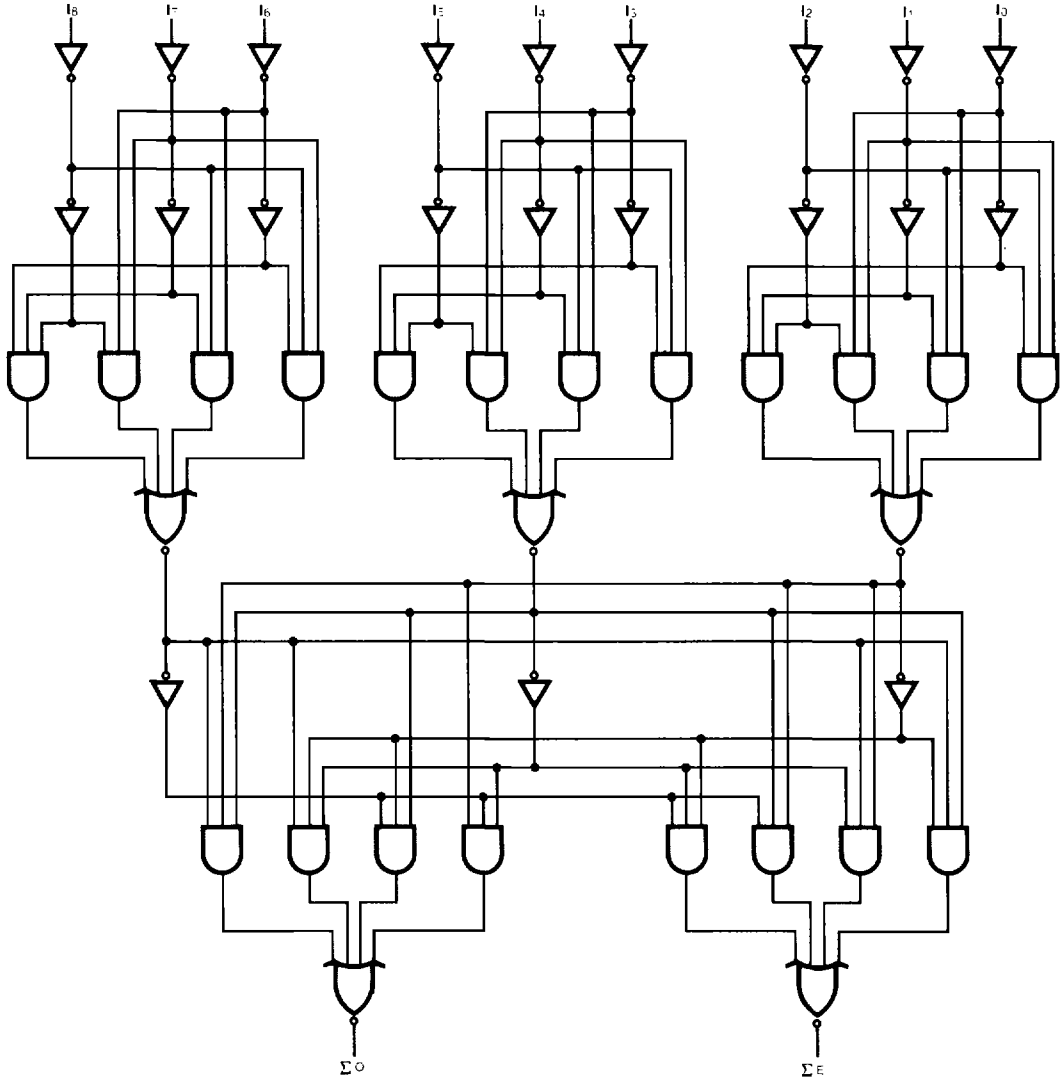
Pin Names	Description	54F/74F(U.L.) HIGH/LOW
I_0-I_8	Data Inputs	0.5/0.375
Σ_O	Odd Parity Output	25/12.5
Σ_E	Even Parity Output	25/12.5

Truth Table

Number of HIGH Inputs I_0-I_8	Outputs	
	Σ Even	Σ Odd
0, 2, 4, 6, 8	H	L
1, 3, 5, 7, 9	L	H

H = HIGH Voltage Level
L = LOW Voltage Level

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		25	38	mA	V_{CC} = Max

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F T_A = +25°C V_{CC} = +5.0 V C_L = 50 pF			54F T_A, V_{CC} = Mil C_L = 50 pF		74F T_A, V_{CC} = Com C_L = 50 pF		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay I_n to Σ_E	6.5 6.5	10.0 11.0	15.0 16.0	6.5 6.5	20.0 21.0	6.5 6.5	16.0 17.0	ns	3-1 3-10
t_{PLH} t_{PHL}	Propagation Delay I_n to Σ_O	6.5 6.5	10.0 11.0	15.0 16.0	6.5 6.5	20.0 21.0	6.5 6.5	16.0 17.0	ns	3-1 3-10