Z86018

DATA PATH CONTROLLER

FEATURES

- Low Profile 100-Pin Plastic VQFP
- Programmable Power-Down Mode
- Point and Go Automatic Disk and Host Control and Transfers

Microcontroller Port

- Access to External Switch Settings After Hardware Reset Through the Buffer RAM Data Bus
- Automatic Configuration for Microcontroller Type
- Direct, Transparent Access to all Buffer Memory, with up to 8 Kbytes of Buffer Reserved for Microcontroller Data
- Storage Such as Cache and Defect Management
- Hardware Wait State Generation or Polled Mode for Microcontroller Buffer Accesses
- Programmable Chip Select Generation for the Firmware PROM and One Other Device.

Drive Interface Port

- Full Track Read, Write, or Format Capability with no Microcontroller Intervention.
- Programmable RAM Based Sequencer with Enhanced Branching Capability
- The Sequencer is Interruptible by Either the Internal Servo Counter, or External Input to Handle Servo Fields Within a Sector
- Sequencer Data can Come From the Internal RAM Based Sequencer, or From the Buffer Memory, Allowing for Different Data Each Time a Sequencer Instruction is Executed
- Sequencer can be Updated at Any Time
- Soft and Hard Sector Drive Support
- 88-Bit Reed-Solomon with On-The-Fly Hardware Correction of a Sector Within 1/2 Sector Time
- 16-Bit CRC
- 8-Byte Stack for Pushing Header Information

Buffer Port

- DRAM Support With up to 1 Mbyte Addressing Capability
- SRAM Support With up to 64 Kbyte Addressing Capability
- 4.125 Mbytes/sec Disk Data Rate (33 MHz Read Reference Clock), and 7 Mbytes/sec Host Transfer Rate Using 80 ns Page Mode DRAMs or 50 ns SRAMs
- 8-Bit Memory Data Bus with Parity Option for DRAM Mode
- Separate Microcontroller Channel into Memory for Scratch Pad Buffer
- 6-Byte Host FIFO, 4-Byte Disk Data FIFO, and 4-Byte Formatter FIFO for Speed Matching with the Host, Disk, and Sequencer.

FEATURES (Continued)

AT Port

- True AT (IDE Connector) Interface with no Glue Logic Needed
- Direct Host Interface Through Programmable 24 mA Drives
- On-Chip Registers to Emulate the Task Files for PC AT Task File
- Provides 8- and 16-Bit Data Transfer on the Host Bus
- Provides Flexible Timing Interface to the Host Through the Ability to Insert Wait States
- Provides the Logic to Daisy Chain Two Embedded Disk Controllers on the PC AT

GENERAL DESCRIPTION

The Z86018 single-chip data path controller is a high-performance integrated device that combines the functions necessary to implement a variety of low-cost, high-performance Winchester® products. The five functions performed by this chip are:

- Disk Control and Sequencing
- Host Interface Logic
- Local Microcontroller Interface
- Reed-Solomon® ECC Correction
- Sector Buffer Interface.

Programmable power-down modes are provided for battery operated applications.

The disk controller interface features a low overhead programmable sequencer that can be programmed to transfer a full track of data from disk to buffer with no firmware intervention. The sequencer can support all types of Winchester drives, but is especially well suited to low-power sampled, or embedded servo types of drives.

The 31 x 32-bit sequencer has the ability to be interrupted, save its state, execute a servo interrupt routine, and return to the interrupted instruction. The sequencer can fetch up to 1024 bytes of format specific data per track operation, to be used as format data, to load the servo interrupt counter, or as section numbers, allowing for full track reads with no firmware intervention.

Data rates of up to 33 Mbits/sec are supported through the use of high-speed, low cost CMOS technology. Data integrity through a hardware implementation of a widely used 88-bit Reed-Solomon ECC code is provided. A 16-bit CRC is also supported in hardware for error detection on ID fields.

The microcontroller port provides for Zilog and other popular microcontroller interfaces with no need for external chip select logic. Interrupt and status registers facilitate interrupt or polling operations. Direct microcontroller access to the buffer RAM is possible even during disk and Host data transfer.

The Z86018 provides automatic host interface control which allows for full track reads from disk to host with no microcontroller intervention. The ATA signal (IRQ14) and status bits (DRQ, BSY) are regenerated by the Z86018 in hardware allowing for the fastest possible transfers over the AT bus.

The buffer controller interface arbitrates between disk, host, Reed-Solomon ECC, microcontroller, and formatter data requests. The buffer interface directly drives up to 64K of SRAM, or 1 Mbyte of DRAM. To maximize buffer bandwidth, page mode is used when accessing DRAMs. Parity generation and checking is also supported for data integrity. The buffer controller operates with an independent clock source to maximize its bandwidth.

Notes:
All Signals with a preceding front slash, "/", are active Low, e.g., B//W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

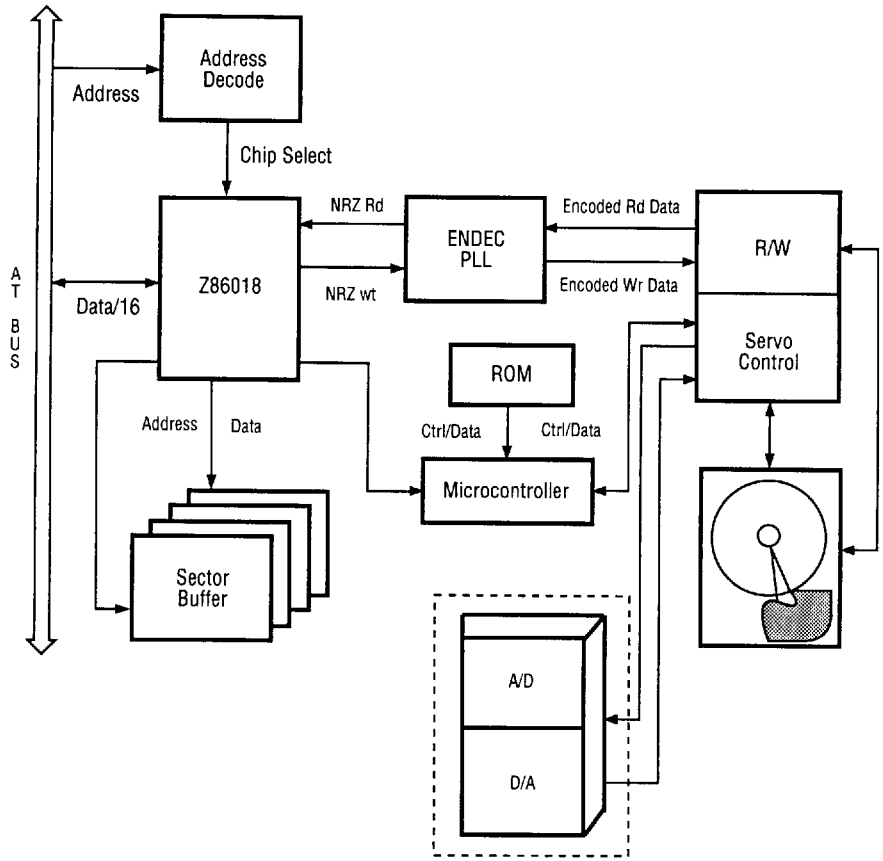

Figure 1. Z86018 IDE Block Diagram

GENERAL DESCRIPTION (Continued)

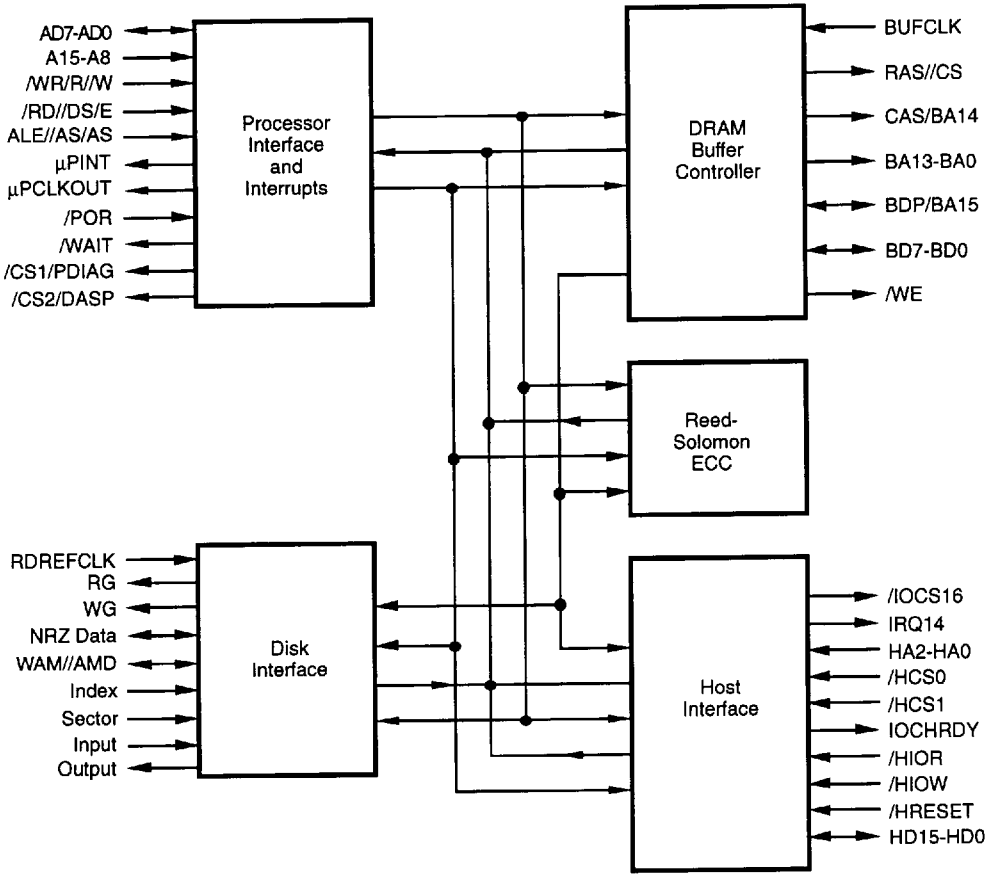

Figure 2. Z86018 Functional Block Diagram

PIN FUNCTIONS

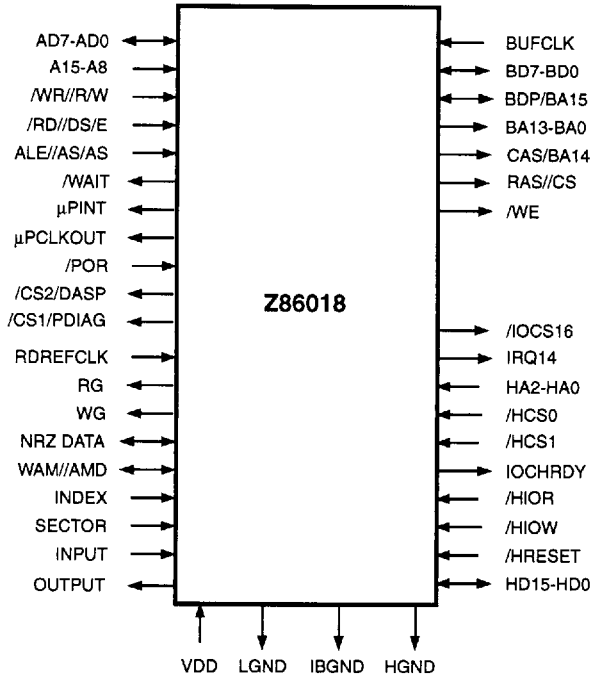

Figure 4. Z86018 Pin Function

PIN DESCRIPTION

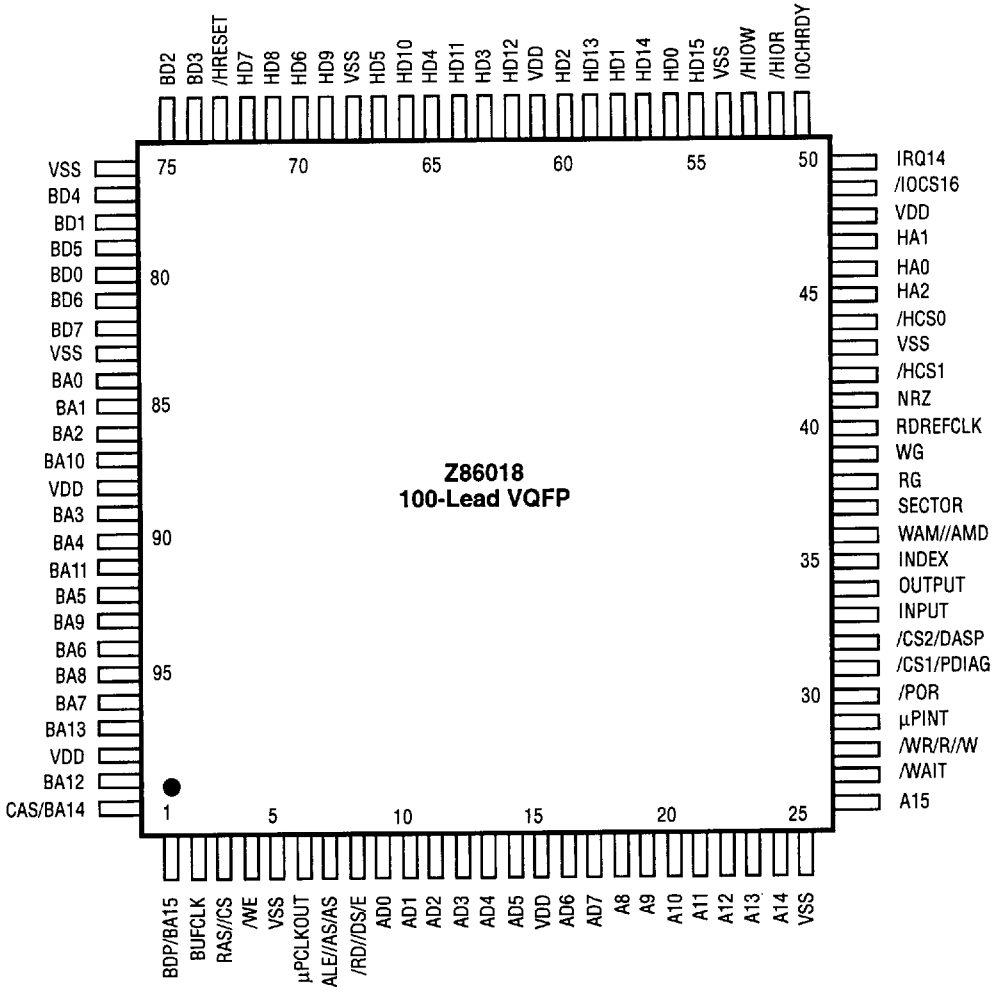

Figure 3. 100-Pin VQFP Pin Assignments

Table 1. 100-Pin VQFP Pin Descriptions

Pin #	Symbol	Function	Direction
1	BDP/BA15	Parity/Buffer Address, Bit 15	In/Output
2	BUFCLK	Buffer Clock	Input
3	RAS//CS	Row Address Strobe/Chip Select	Output
4	/WE	Write Enable	Output
5	V_{SS}	Ground	
6	µPCLKOUT	Microprocessor Clock Out	Output
7	ALE//AS/AS	Address Latch Enable/Address Strobe	Input
8	/RD//DS/E	Read Address/Data Strobe/E Clock	In/Output
9-14	AD5-AD0	Address/Data Bus	In/Output
15	V_{DD}	Power Supply	
16-17	AD7-AD6	Address/Data Bus	In/Output
18-24	A8-A14	Microprocessor Address Bus	Input
25	V_{SS}	Ground	
26	A15	Microprocessor Address Bus	Input
27	/WAIT	Wait	Output
28	/WR/R/W	Write Enable/Read/Write Strobe	Input
29	µPINT	Programmable Polarity Interrupt	Output
30	/POR	Power-On Reset	Input
31	/CS1/PDIAG	Chip Select 1/PDIAG	In/Output
32	/CS2/DASP	Chip Select 2/DASP	In/Output
33	Input	Sequence Synchronizer	Input
34	Output	Sequence Trigger	Output
35	Index	Input Index	Input
36	WAM//AMD	Write Address Mark/Address Mark Delete	In/Output
37	SECTOR	Sector	Input
38	RG	Read Gate	Output
39	WG	Write Gate	Output
40	RDREFCLK	Read Reference Clock	In/Output
41	NRZ	NRZ Data	In/Output
42	/HCS1	Host Chip Select 1	Input
43	V_{SS}	Ground	
44	/HCS0	Host Chip Select 0	Input
45	HA2	Host Address 2	Input
46	HA0	Host Address 0	Input
47	HA1	Host Address 1	Input
48	V_{DD}	Power Supply	
49	/IOCS16	16-Bit Transfer Enable	Output
50	InputRQ14	Input Interrupt Request	Output
51	InputOCHRDY	In/Output Channel Ready	Output
52	/HIOR	Host I/O Read	Input
53	/HIOW	Host I/O Write	Input
54	V_{SS}	Ground	
55	HD15	Host Data, Bit 15	In/Output

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PIN DESCRIPTIONS (Continued)

Pin #	Symbol	Function	Direction
56	HD0	Host Data, Bit 0	In/Output
57	HD14	Host Data, Bit 14	In/Output
58	HD1	Host Data, Bit 1	In/Output
59	HD13	Host Data, Bit 13	In/Output
60	HD2	Host Data, Bit 2	In/Output
61	V_{DD}	Power Supply	
62	HD12	Host Data, Bit 12	In/Output
63	HD3	Host Data, Bit 3	In/Output
64	HD11	Host Data, Bit 11	In/Output
65	HD4	Host Data, Bit 4	In/Output
66	HD10	Host Data, Bit 10	In/Output
67	HD5	Host Data, Bit 5	In/Output
68	V_{SS}	Ground	
69	HD9	Host Data, Bit 9	In/Output
70	HD6	Host Data, Bit 6	In/Output
71	HD8	Host Data, Bit 8	In/Output
72	HD7	Host Data, Bit 7	In/Output
73	/HRESET	Host Reset	Input
74-75	BD3-BD2	Buffer Data, Bits 3, 2	In/Output
76	V_{SS}	Ground	
77	BD4	Buffer Data, Bit 4	In/Output
78	BD1	Buffer Data, Bit 1	In/Output
79	BD5	Buffer Data, Bit 5	In/Output
80	BD0	Buffer Data, Bit 0	In/Output
81	BD6	Buffer Data, Bit 6	In/Output
82	BD7	Buffer Data, Bit 7	In/Output
83	V_{SS}	Ground	
84-86	BA2-BA0	Buffer Address, Bits 2, 1, 0	Output
87	BA10	Buffer Address, Bit 10	Output
88	V_{DD}	Power Supply	
89-90	BA4-BA3	Buffer Address, Bits 3, 4	Output
91	BA11	Buffer Address, Bit 11	Output
92	BA5	Buffer Address, Bit 5	Output
93	BA9	Buffer Address, Bit 9	Output
94	BA7	Buffer Address, Bit 6	Output
95-96	BA8-BA7	Buffer Address, Bits 8, 7	Output
97	BA13	Buffer Address, Bit 13	Output
98	V_{DD}	Power Supply	Output
99	BA12	Buffer Address, Bit 12	Output
100	CAS/BA14	Column Address/Buffer Address, Bit 14	Output

Microcontroller Port

ALE//AD/AS *Address Latch Enable* (input, active High), *Address Strobe* (input, active Low), *Address Strobe* (input, active High). When in Intel mode, this pin connects to the ALE pin of the microcontroller. The trailing edge of the signal is used to latch the address from AD7-AD0. In the Zilog mode this pin is the /AS signal, again the trailing edge is used to latch the address from AD7-AD0. When Motorola mode is selected, this pin is the AS signal.

/RD//DS/E *Read Enable* (input, active Low), *Data Strobe* (input, active Low), *E Clock* (input, active High). This pin is either Read Enable from Intel type microcontrollers, Data Strobe signal from the Z8 microcontroller, or the E clock from Motorola microcontrollers. In Intel mode, read data is placed on the AD7-AD0 bus when this signal is Low. In the Z8 mode, this signal, when asserted Low, signals that the data is valid, read or write, and in Motorola mode, the E clock being High signals valid data.

/WR/R//W *Write Enable* (input, active Low), *Read/Write Strobe* (input, Read, active High; Write, active Low). When in the Intel mode, Write enable, gated with the appropriate addresses, is used to write the data into the Z86018 registers. When connected to the Zilog or Motorola microcontrollers, this input establishes the direction of the transfer. This signal, along with /DS or E, determines the gating of data to or from the bus.

AD7-AD0 *Address/Data Bus* (input/output, active High). Bidirectional multiplexed microcontroller address and data bus.

A15-A8 *Microprocessor Address Bus* (input, active High). Upper byte of the microcontroller address bus.

/POR *Power-On Reset* (input, active Low). The reset condition is latched internally.

µPCLKOUT *Microprocessor Clock Out* (output, active High). This output provides the Buffer Clock oscillator divided by 1, 2, 4, or 8 for use by the microcontroller.

µPINT *Programmable Polarity Interrupt* (output, active High). Open-drain programmable polarity interrupt output signal to microcontroller. This pin requires an external pull-up resistor.

/WAIT *Wait* (output, active Low). This signal is used to add wait states to microcontroller accesses to the scratch pad RAM or the buffer RAM. In Intel mode, this is the active High RDY line of 8096 and 80196 microcontrollers (pulling this signal Low adds wait states). The 8051 must use the polled mode. In Zilog mode, this is the active High WAIT line (pulling this signal Low adds wait states) used to add wait states to microcontroller accesses to the scratch pad RAM or the buffer RAM. Motorola microcontrollers must use the polled mode as they have no external bus cycle extension signal (68HC11 and 680X family).

/CS1/PDIAG *Chip Select 1* (output, active Low), *PDIAG* (output, active High). This active Low output is the programmable chip select for the firmware PROM or can be used for PDIAG.

/CS2/DASP *Chip Select 2* (output, active Low), *DASP* (output, active High). This active Low output is the second programmable chip select or can be used for DASP.

Drive Interface Port

RDREFCLK *Read Reference Clock* (input, active High). In Read mode, this clock is used in conjunction with the NRZ signal to clock data into the chip during disk read operations. Read clock is the separated clock from the data separator. In write mode, this clock is used in conjunction with the NRZ signal to clock data out of the chip during disk write operations. The reference clock represents the source for the appropriate operating zone in a zone bit recorded format.

RG *Read Gate* (Output, active High). Read gate is asserted when the Z86018 is reading NRZ data from the disk interface.

WG *Write Gate* (output, active High). Write gate is asserted when the Z86018 is writing NRZ data to disk.

NRZ *NRZ Data* (input/output, active High). Bidirectional serial interface to an external ENDEC. It carries the read data signal from the disk when RG is asserted and the write data output to the disk when WG is asserted.

/WAM//AMD *Write Address Mark* (output, active Low), *Address Mark Detect* (input, active Low). This bidirectional signal is used in Soft Sector mode. When RG is asserted, a Low level input on this signal indicates address mark detection. With WG asserted, a Low output on this signal indicates time to write the Address Mark.

INDEX (input, active High). Index mark from the drive asserted once per revolution is used as branch control and passed to the Host in the Host Status register (58H) (host 1F7H)

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Drive Interface Port (Continued)

SECTOR (input, active High). This active High input to the programmable sequencer is available for hard sectored drives or to synchronize to the servo field for embedded servo drives.

INPUT (input, active High). This signal is used to synchronize the sequencer to external events. This pin may be used as a write fault signal.

OUTPUT (output, active High). This signal is asserted by a sequencer instruction. This pin may be used as an address mark detect enable signal or other signal that must be triggered by the sequencer.

Buffer Port DRAM/SRAM

BUFCLK *Buffer Clock* (input, active High). This pin is used to generate buffer access cycles. This clock is also used by the Reed-Solomon ECC hardware.

/WE *Write Enable* (output, active Low). The Write Enable signal ties directly to the DRAM or SRAM /WE pins.

BD7-BD0 *Buffer Data* (input/output, active High). These eight pins are bits 7-0 of the 8-bit data bus to/from the buffer memory. The weakly pulled up and pulled down configuration bits and switches are latched on these lines at Power-On Reset.

BDP/BA15 *Parity/Buffer Address, Bit 15* (input/output, active High). In DRAM mode, this is the bidirectional buffer data odd parity. In SRAM mode this is A15 to the buffer RAM.

/CAS/BA14 *Column Address Strobe* (output, active Low), *Buffer Address, Bit 14* (output, active High). In DRAM mode, this is the column address strobe directly tied to DRAM buffers. In SRAM mode, this is A14 to the buffer RAM.

/RAS//CS *Row Address Strobe/Chip Select* (output, active Low). In DRAM mode, this is the row address strobe directly tied to DRAM buffers. In SRAM mode, this is the /CS signal directly tied to the /CS pin of the buffer RAM.

BA9-BA0 *Buffer Address* (output, active High). In DRAM mode, this is the multiplexed row and column address for 1M addressing range. In SRAM mode these are A9-A0 of the buffer RAM.

BA13-BA10 *Buffer Address* (output, active High). In DRAM mode, this is the multiplexed row and column address for 1M addressing range. In SRAM mode, these are A9-A0 of the buffer RAM.

Host Interface

/IOCS16 *16-Bit Transfer Enable* (output, active Low). This open-drain output signal indicates to the host that a 16-bit sector buffer transfer is active on the PC bus.

IRQ14 *Interrupt Request* (output, active High). This signal is asserted to indicate to the Host that the disk controller needs attention. The interrupt is cleared by either reading the Host Status Register (1F7H), or writing the Host Command Register (1F7H).

HA2-HA0 *Host Address* (input, active High). Host Address lines A9-A0 are used to access the various PC AT control, status, and data registers.

/HCS1 *Host Chip Select 1* (input, active Low). This pin, decoded from the Host Address bus, is used to select three of the registers in the task file (3F0-3F7).

/HCS0 *Host Chip Select 0* (input, active Low). This pin, decoded from the Host Address bus, is used to select some of the host accessible register (1F0-1F7).

IOCHRDY *I/O Channel Ready* (output, active High). I/O Channel Ready is asserted low to extend Host transfer cycles when the disk controller is not ready to respond.

/HRESET *Host Reset* (input, active Low). When this signal is Low, it initializes the control and status registers and stops any command in process.

/HIOR *Host I/O Read* (input, active Low). This input is asserted Low by the host during a host read operation. When this signal is asserted with /HCS0//HCS1 status or data from this chip is enabled on the host data bus.

/HIOW *Host I/O Write* (input, active Low). This input is asserted Low by the host during a host write operation. When this signal is asserted with /HCS0//HCS1 data, the host is strobed into this chip at the rising edge of /HIOW.

/HRESET *Host Reset* (input, active Low). When this signal is Low, it initializes the control and status registers and stops any command in process.

HD15-HD0 *Host Data* (input/output, active High). These signals are the data bits HD15-HD0 used for disk data transfers.

Power and Ground

V_{DD} 5 Volt Power Supply
V_{SS} Logic Ground

FUNCTIONAL DESCRIPTION

The Z86018 allows for the use of lower cost microcontrollers by providing close synchronization with the data to and from the disk and host interface and the ability to do full track reads with no microcontroller intervention.

Using the Z86018 provides the low parts count and the high performance required for today's small form factor disk drive subsystems. A complete drive is realized using the Z86018, a microcontroller, ROM code, local DRAM/SRAM buffer, ENDEC/data separator, the read/write and servo circuitry.

The Z86018 is divided into five major blocks:

- Microcontroller interface
- AT Host interface
- Disk formatter/sequencer
- Buffer memory interface
- Reed-Solomon ECC

Microcontroller Interface

The microcontroller communication path to the Z86018 is a multiplexed, 8-bit address and data bus compatible with that provided by the Intel, Zilog, and Motorola class of controllers. This interface is designed to work with these controllers with no external circuitry. Microcontroller selection is accomplished at the end of a hardware reset, by appropriately pulling up or down the Buffer Data lines 7-6.

The Intel-type interface provides a multiplexed address/data bus which carries the address in the first half of the cycle. The falling edge of ALE is used to capture the microcontroller address inside the Z86018's address latch. This address is decoded to provide external chip selects, access the buffer RAM, or to access any one of the internal registers. When an address match with the relocatable registers occurs, data is written into the Z86018 on the rising edge of /WR. With /RD asserted the Z86018's internal data bus will drive the AD7-AD0 data bus. This chip can also provide wait states to the microcontroller through its READY signal, as well as support a polled data ready mode for microcontrollers that do not support a ready line.

The Zilog-type interface latches the address on the trailing edge of the /AS signal. The data is written to the Z86018 with the R/W direction signal Low, at the trailing edge of the /DS signal. Similarly data is read by the microcontroller when R/W is High. The Z86018 will start driving the AD7-AD0 data bus with its data when /DS is asserted. Wait states to the microcontroller are provided by the WAIT signal, as well as support of a polled data ready.

The Motorola-type interface latches the address on the trailing edge of the AS signal. The data is written to the Z86018 when the R/W direction signal is Low, at the trailing edge of the E signal. Similarly, data is read by the microcontroller when R/W is High. The Z86018 will start driving the AD7-AD0 data bus with its data when E is asserted. The 68HCxx family does not support the wait mode, and must use the polled mode.

The Z86018 registers and scratch pad memory are relocatable to one of four microcontroller address ranges, for compatibility with different types of microcontrollers, and flexibility in PCB design. Two programmable external chip selects are also provided for overall system simplicity, one for the firmware ROM, and a second user-definable chip select.

In addition to internal register access the Z86018 is designed to allow direct random access to the external DRAM/SRAM buffer. Microcontroller access to large amounts of external DRAM/SRAM buffer memory provides the firmware with a flexible and inexpensive method of scratch pad memory access. This memory is used to store sequencer data (up to 1024 bytes) and for any other variable storage needed (up to 8 Kbytes). Buffer data access is performed by selecting a microcontroller segment, and reading or writing the desired memory location. The microcontroller scratch pad space is automatically protected from accidental access by the host or disk by rolling over to the top of the scratch pad area instead of 0.

When segmentation is enabled, the memory is divided into either two or four equal segments based upon the size of the buffer memory. (**Note:** Segment 0 is smaller by the scratch pad size.)

FUNCTIONAL DESCRIPTION (Continued)

Host Interface

The Host interface supports the AT task file register set and hardware signals. The Z86018 contains all of the command, control, status, and data registers necessary to perform automatic host transfers of up to 256 sectors with no microcontroller intervention. This includes automatic updating of cylinder, head, sector and number of sector registers, as well as the status register. This, coupled with the sequencer's ability to perform full track reads with no microcontroller intervention, is called "Point and Go" disk control.

The Z86018 provides the capability for direct connection to the Host bus. The data bus drive capability is programmable between 12 mA and 24 mA current sink capability, and can drive loads up to 300 pF.

The Z86018 also provides circuitry to extend the Host I/O cycles and insert wait states by deasserting the IOCHRDY signal. This circuit is only active for to or from the data register (Host 1F0H). The Z86018 inserts wait states when the buffer controller is not ready for the transfer.

The Host transfer will not interfere with disk read ahead, as the buffer bandwidth is high enough to keep up with both, and disk and Host transfer directions are independent.

Disk Sequencer

At the heart of the Z86018 chip is the programmable formatter/sequencer. The formatter can be subdivided into three different blocks: a RAM based sequencer, data path, and CRC logic. Using this unique sector format and desired operation; read, write, verify, or format can be loaded into the programmable sequencer's writable control store at any time.

The sequencer's ability to be interrupted makes the Z86018 well suited for use with sampled servo drives. It can be interrupted to remain idle during the servo field, and, when the servo field is passed, read or write a VFO field and sync byte, then continue where it left off.

The time to the next servo interrupt can be loaded from the buffer or a register, freeing the ID field from containing this information and giving more space on the disk for data. For evenly spaced servo fields, the value to the next servo burst is loaded into the Servo Interrupt Count registers (R75 and R76). A byte count fragment must be loaded from the sector buffer when the sync byte is read in an ID field.

The RAM based writable control store contains 31 four-byte words. The word is further subdivided into two control bytes, a count field, and branch/data field. These fields direct the operation of the disk controller block in a sequential manner.

The Z86018 sequencer differs from other sequencers currently available in that it can fetch data from the external RAM buffer, and also that it can be interrupted and return to where it left off. These two features are to simplify full track operations with no microcontroller intervention, in that the sector numbers can be stored in the RAM buffer and automatically read and compared by the sequencer.

The sequencer's clock source is the RDREFCLK, coming from the disk interface. During read operations this clock is the separated clock synchronized to the NRZ data. During write or format operations, the RDREFCLK is the write clock. RDREFCLK is further divided-by-eight to establish the byte clock, which is the minimum instruction delay time.

The sequencer consists of four different fields: control, count, branch, and data. The count field simply specifies the number of times an instruction is repeated. The count field can be programmed to specify a maximum count of 4096, with 0 equal to execute the instruction 1 time. The upper two bits specify modules (1, 4, 16, or 64), and the lower six bits are the count.

The data and branch fields are multiplexed into the same sequencer byte. There are two reasons for this. First it reduces the required area of RAM by 20%, and, secondly the instruction set is specially tailored to eliminate the need for simultaneous data and branch requirements. When the data field is selected in an instruction, then the next instruction is the current instruction plus one. When the branch field is selected in an instruction, the next instruction is either a branch address programmed in the lower five bits of the branch field, or the current instruction plus one.

One of thirteen different branch conditions is specified to synchronously direct the program flow. Many instructions require a data operand, which is supplied by the data source of the current instruction. The source of data while the branch field is enabled is either from the buffer or the formatter buffer area, while the data source is from the sequencer's data field. when the branch field is disabled.

A two-byte control field is used to synchronize external signals (RG, WG, OUTPUT, WAM) to the sequencer's program flow.

Sequencer Instruction Flow

The sequencer is designed to receive internal or external events and synchronize itself to these events in order to properly direct the flow of NRZ data. Internal signals like ECC error, data miscompare, or WG can be sampled to direct the program flow. External signals like Index, Sector, or Input can also direct program flow after synchronization.

The Servo Counter can also be used to direct program flow to a pre-determined location (Sequencer Vector Address 76H). This sequencer has been designed to handle these interrupts by saving its state, sequencing through the interrupt handling routine, and continuing from the exact location prior to the interrupt. This powerful feature enables the sequencer to be used in embedded/sampled servo formats, as well as other more traditional formats. A bit maskable flag byte compare provides the ability for sophisticated defect management schemes embedded in the ID field. 16 bit CRC capability is also provided for ID field integrity.

Buffer Controller

The buffer control functional logic block controls the flow of data between the external SRAM/DRAM buffer, and the host, disk, Reed-Solomon ECC logic, and microcontroller. The Z86018 provides all the necessary signals to interface directly to page mode nibble-wide DRAMs with internal refresh counters, or static RAM. Using DRAMs, page mode accessing is necessary to sustain the buffer bandwidth, and allow the microcontroller access to the buffer with as few wait states as possible. The Z86018 has a 6-byte FIFO for host transfers and a 4-byte FIFO for disk and sequencer data transfers, to sustain the buffer bandwidth.

A programmable 10-bit counter is provided to time the refresh interval appropriately. Refresh cycles are performed by CAS before RAS accesses in the background every time the refresh counter rolls over. The DRAM interface has an optional parity bit in addition to the byte wide data. When enabled, the parity error status bit is set after a detected parity error. If interrupts are enabled the Microprocessor interrupt output signal is also set.

In SRAM mode, parity data is not available, since the parity pin also provides the A15 signal to the buffer RAM.

To allow for different speed memories, the Buffer Size register (26H) contains two bits (cycle length 1:0) to control the number of clock pulses used for each memory access.

Disk accesses to the buffer are initiated by updating the Disk Pointer registers. During a disk read operation the data from the disk's NRZ interface, after going through the Serial/deserializer, will get stored in a 4-byte staging FIFO. A 2-byte page mode transfer will be initiated when the FIFO is 2 bytes full. The Disk Pointer will increment to the next sequential location in the buffer memory in preparation for the next burst.

During a disk write operation, the buffer controller maintains a full FIFO, while data from the staging FIFO is serialized and sent as NRZ data.

The mechanism for host accesses to or from the buffer occurs in a similar fashion. During a disk read operation the buffer controller maintains a full FIFO while the host interface tries to empty the staging FIFO. The buffer controller is designed to maintain the highest possible bandwidth to ensure that it will not starve either the host or the disk interface.

The Host Pointer register and the Sectors Available registers control the host access. During a read operation, data is read from the disk into the sector buffer. Assuming automatic host transfers are enabled, after the ECC logic checks the sector, the Sectors Available counter is incremented, indicating that a transfer from the buffer to the host is ready. The Z86018 automatically transfers the sector to the host, updates the sector, head, cylinder, and number of sector registers, and decrements the sectors available counter. When another sector is available, the process continues until either an uncorrectable error occurs or all of the requested sectors are transferred.

During a disk write operation data from the host interface is staged in the 6-byte FIFO and written to buffer memory when the FIFO has four bytes of data.

To initiate automatic host write operations the firmware sets the Sector Available register to the number of sectors that are allocated in the buffer. The Host Pointer and Disk Pointer are set to the address of the first byte in the buffer. As sectors are written into the buffer the Sectors Available register is decremented. As sectors are written to the disk the Sectors Available register is incremented, thus maintaining the process without microcontroller intervention.

In order for the buffer pointers to work correctly, and in DRAM mode, the proper addressing generated, the Buffer Size register must be programmed for the correct buffer size (26H bits 3-0).

Buffer Controller (Continued)

The buffer can be segmented by setting the Segmentation Enable bit. If segmentation is enabled, the memory is divided into two or four equal segments (segment 0 is smaller by the size of the microcontroller scratch pad RAM). The Host and Disk pointers can point to different segments, allowing for flexibility in caching.

As previously discussed there is a mechanism available for microcontroller access to the buffer. The microcontroller access can be made in one of two modes. First and simplest is the ready mode, where the ready line is used to hold the microcontroller if necessary until the data is available. The second way is to poll 2AH bit 3. In the polled mode all reads must be performed twice, the first one returning incorrect data, and the second read (after the busy/done bit indicates done, 2AH bit 3) as valid data.

The scratch pad area is either disabled, 2 Kbytes, 4 Kbytes, or 8 Kbytes, and the buffer can be 2 Kbytes up to 1 Mbyte. (**Note:** Disabling the scratch pad area also disables the sequencer format data.) There are two registers that control the upper address bits to allow access to any area of the buffer. The sequencer format data area is always at location 0 of the physical buffer memory, and is contained within the scratch pad memory, which also starts at location 0 in the physical buffer memory. This allows for easy updating of the sequencer data by the microcontroller. Care must be taken to ensure that these two are kept separate by the firmware.

Another feature of the buffer controller is access to external switch settings (resistor pull ups or pull downs) when exiting a power on reset condition. The Buffer data bus is latched and stored in the Switches register (20H) bits 7-5 are reserved for microcontroller type, and PROM chip select/Z86018 registers location. Bits 4-0 are available to the user for any purpose.

Reed-Solomon Error Detection and Correction

The Z86018 contains a hardware implementation of an 88-bit Reed-Solomon ECC algorithm. This logic generates 11 bytes of syndrome for disk writes, and checks and corrects errors on disk reads.

The detection capabilities of this algorithm are to detect single burst errors up to 71 bits in length, and double burst errors up to 31 bits in length. It can also detect four bursts up to 11 bits in length.

The correction capabilities are up to four 10-bit symbols (including three and four random bit errors), or single burst errors up to 31 bits, and double burst errors up to 11 bits (firmware correction).

The Reed-Solomon ECC logic can operate on one of two sector sizes (512, or 1024 bytes) (60H bit 5). The correction length capabilities are also firmware selectable (60H bits 4-3). A shorter correction length will improve the probability of miscorrection.

The Reed-Solomon ECC logic is initialized by setting the INIT CRC/R-S field in Sequencer Control Field 0, and specifying either Data Time, or ECC Time in the Data Type field.

If a correctable ECC error is detected, the R-S ECC circuit will automatically perform the XOR of the data in the buffer, and keep going, requiring no intervention from the microcontroller. If an uncorrectable error is detected, the Uncorrectable bit in the R-S ECC Control and Status register (60H bit 0) will be set, and after appropriate retries, the firmware can read the syndrome bytes from the R-S Syndrome Data register (61H) and perform multiple burst corrections.

ABSOLUTE MAXIMUM RATINGS

Symbol	Description	Min	Max	Units
V_{CC}	Supply Voltage (*)	–0.3	+7.0	V
T_{STG}	Storage Temp	–65°	+150°	C
T_A	Oper Ambient Temp		†	C
	Power Dissipation		2.2	W

Notes:
* Voltage on all pins with respect to GND.
† See Ordering Information.

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (Figure 5).

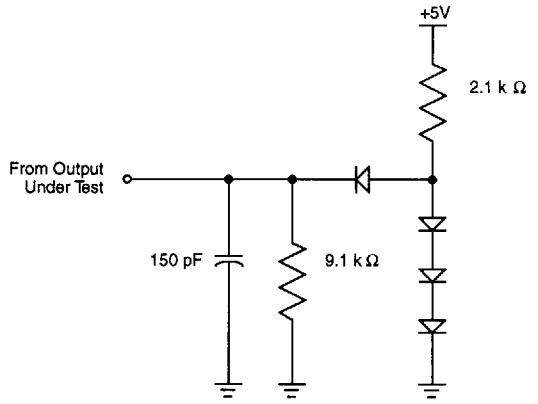


Figure 5. Test Load Diagram

DC CHARACTERISTICS

T_A = 0°C to +70°C, V_{DD} = 5V ± –5%, V_{SS} = 0V

Symbol	Parameter	Min	Max	Unit	Comments
V_{OL}	Output Low Voltage		0.45	V	
V_{IH}	Input High Voltage	2.0	V_{DD}+0.5	V	
V_{IL}	Input Low Voltage	–0.5	0.8	V	
I_{LI}	Input Leakage Current	–10	10	µA	
O_{LI}	Output Leakage Current	–10	10	µA	
I_{CC}	Operating Current		45	mA	40 MHz BUFCLK
I_{CC}	Operating Current		43	mA	36 MHz BUFCLK
I_{CC}	Operating Current		38	mA	32 MHz BUFCLK
I_{CC}	Operating Current		33	mA	24 MHz BUFCLK
I_{CCSB}	Standby Current		300	µA	
C_I	Input Capacitance		8	pF	
C_O	Output Capacitance		8	pF	

6

AC CHARACTERISTICS AND TIMING DIAGRAMS (Continued)

T_A = 0°C to +70°C, V_{DD} = 5V ± –5%, V_{SS} = 0V

The following timing parameters assume that all output pins will drive one TTL load in parallel with 50 pF, except host bus pins will drive 300 pF load and buffer address and data lines will drive 30 pF loads

Buffer Memory Timing - SRAM

40 MHz Buffer Clock (Figures 6 and 7)

No.	Symbol	Parameter	Min	Max	Unit
1	TpC	BUFCLK Period	25		ns
2	TwCH	BUFCLK High		10	ns
3	TwCL	BUFCLK Low		10	ns
4	TrC, TfC	BUFCLK Rise and Fall		5	ns
5	TrC(Av)	BUFCLK to Address Valid		32	ns
6	TrC(CS)	BUFCLK to CS		28	ns
7	TsDI(CS)	Data Setup to CS	10		ns
8	ThDI(CS)	Data Hold Time	5		ns
9	TwCS	CS Pulse Width	25		ns
10	TwAv(CS)	Address Valid to CS	20		ns
11	ThA(WE)	Address Hold Time from WE	7		ns
12	TwWE	WE Pulse Width	25		ns
13	TrC(WE)	BUFCLK to WE		25	ns
14	ThD(WE)	Data Hold Time	0		ns
15	TdWE(Dv)	WE to Data Valid	0		ns
16	TdCS(WE)	CS to WE	–2	2	ns
17	TdWE(CS)	WE to CS	–2	2	ns

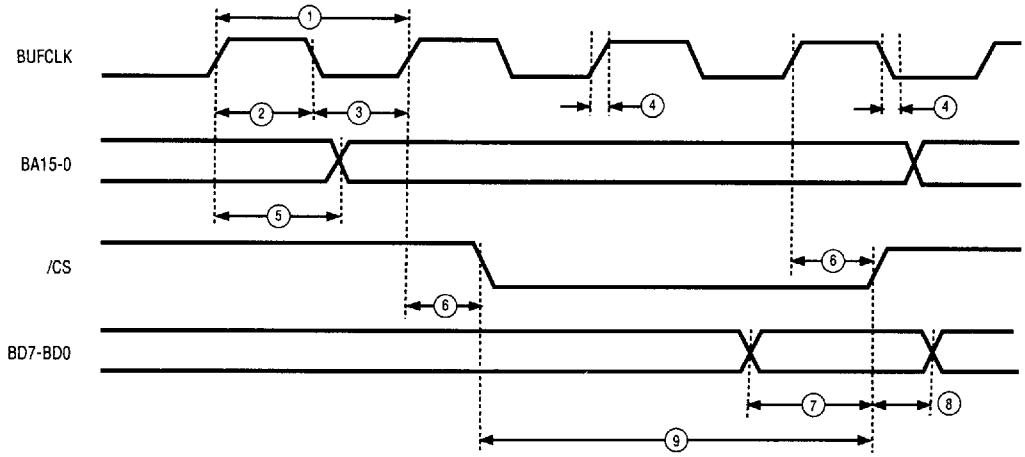


Figure 6. SRAM Buffer Memory Read Timing

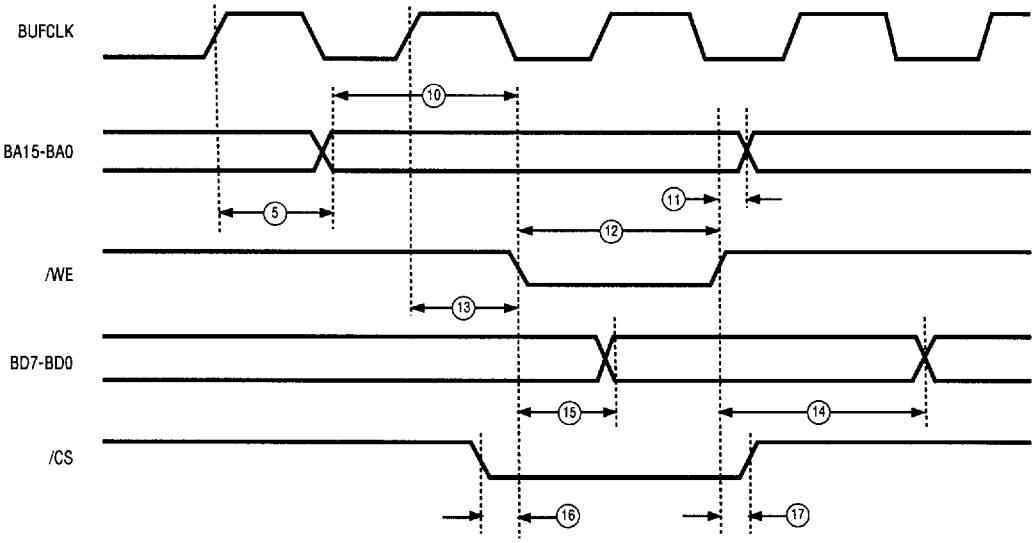


Figure 7. SRAM Buffer Memory Write Timing

AC CHARACTERISTICS AND TIMING DIAGRAMS (Continued)

T_A = 0°C to +70°C, V_{DD} = 5V ± –5%, V_{SS} = 0V

Disk Interface Timing (Figures 8 and 9)

No.	Symbol	Parameter	Min	Max	Unit
18	TpC	RDREFCLK Period	30		ns
19	TwCH	RDREFCLK High	10		ns
20	TwCL	RDREFCLK Low	10		ns
21	TrC, TfC	RDREFCLK Rise & Fall		5	ns
22	TsNRZ	NRZ Setup Time	9		ns
23	ThNRZ	NRZ Hold Time	6		ns
24	TsAMD	AMD Setup Time	7		ns
25	ThAMD	AMD Hold Time	7		ns
26	TdC(RG/WG)	RDREFCLK to RG/WG		28	ns
27	TdC(NRZ)	RDREFCLK to NRZ Data		17	ns
28	TdC(AMD/WAM)	RDREFCLK to AMD/WAM		28	ns

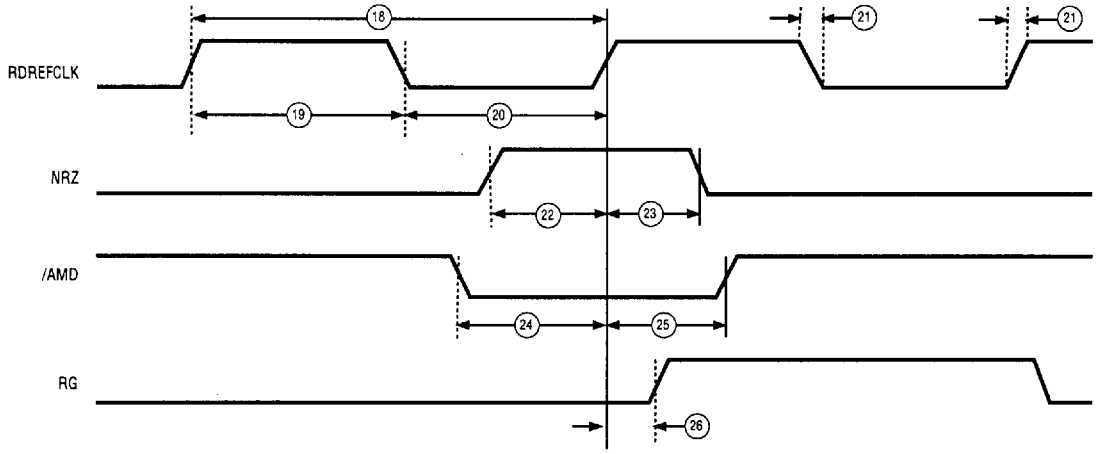


Figure 8. Disk Read Timing

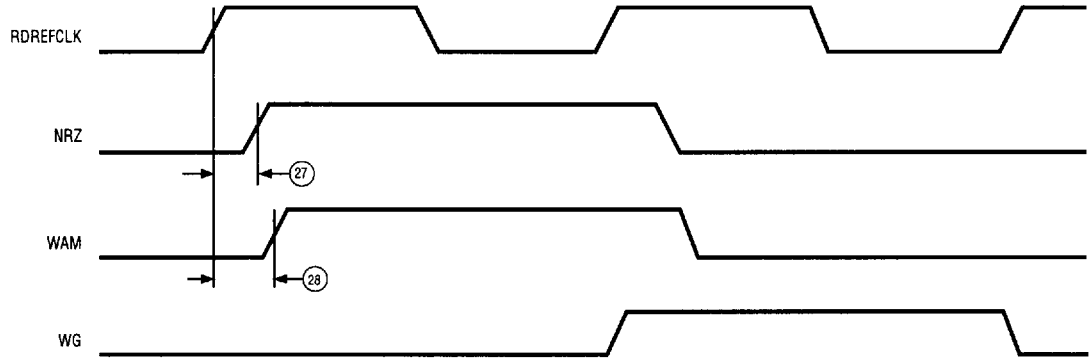


Figure 9. Disk Write Timing

AC CHARACTERISTICS AND TIMING DIAGRAMS (Continued)

T_A = 0°C to +70°C, V_{DD} = 5V ± –5%, V_{SS} = 0V

Microcontroller Write Access Timing (Figure 10)

No.	Symbol	Parameter	Min	Max	Unit
29	TwAS	AS Enable Time	20		ns
30	TsMCU(A)	Microprocessor Address Setup Time	5		ns
31	ThMCU(A)	Microprocessor Address Hold Time	6		ns
32	TsMCU(D)	Microprocessor Data Setup Time	0		ns
33	ThMCU(D)	Microprocessor Data Hold Time	5		ns
34	TdAS(WR)	AS to WR	12		ns
35	TwWR	WR Strobe Width	60		ns
36	TdWR(WT)	WR Active to WAIT Active		15	ns
37	TdWT(WR)	WAIT Inactive to WR Inactive	0		ns

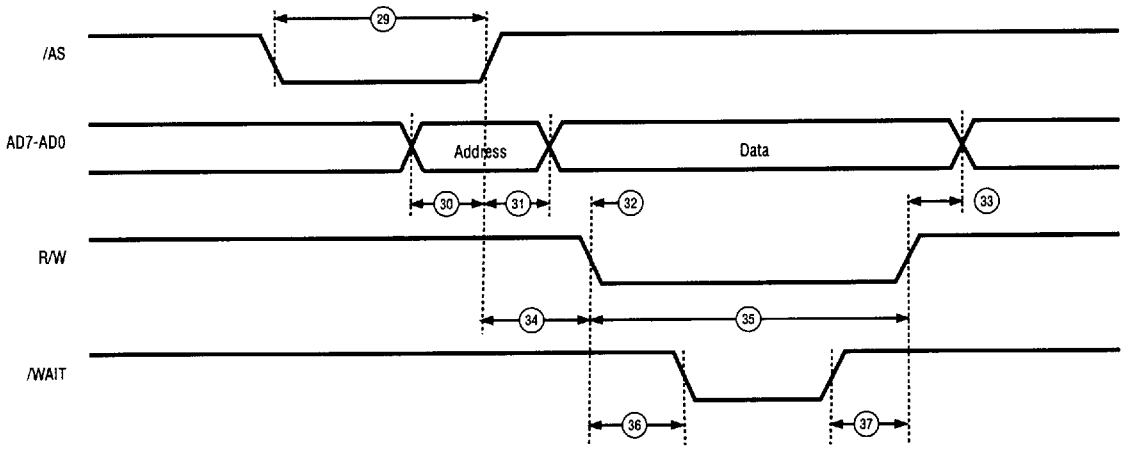


Figure 10. Zilog Z8® Write Microcontroller Access Timing

Microcontroller Read Access Timing (Figure 11)

No.	Symbol	Parameter	Min	Max	Unit
38	TdDS(Dv)	DS to Data Valid		35	ns
39	ThD(DS)	Data Hold Time After DS	14		ns
40	TdAS(DS)	AS to DS	11		ns
41	TwDS	DS Strobe Width	70		ns
42	TdDS(WT)	DS Active to WAIT Active		15	ns
43	TdWT(Dv)	WAIT Rise to Data Valid	5		ns
44	TdWT(DS)	WAIT Inactive to DS Inactive	0		ns

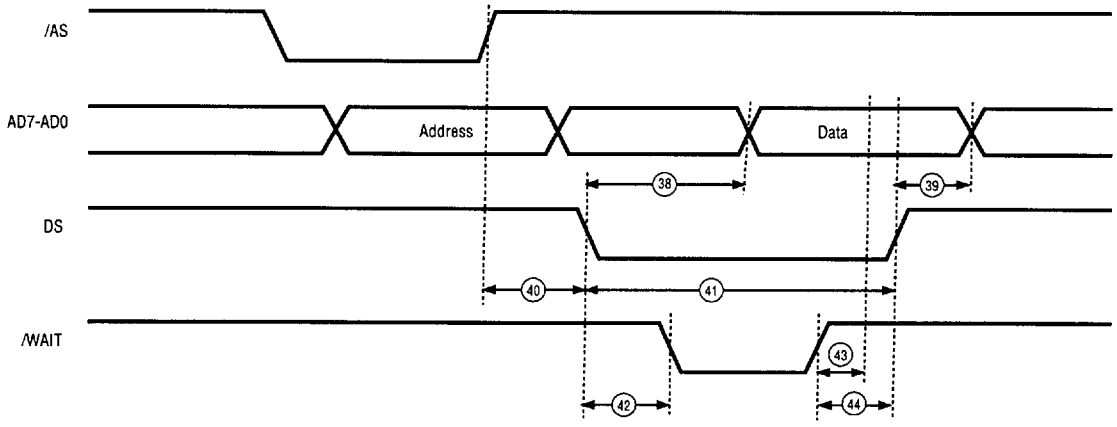


Figure 11. Zilog Z8® Read Microcontroller Access Timing

AC CHARACTERISTICS AND TIMING DIAGRAMS (Continued)

T_A = 0°C to +70°C, V_{DD} = 5V ± –5%, V_{SS} = 0V

Host Access Timing (Figure 12)

No.	Symbol	Parameter	Min	Max	Unit
45	TdAv(IOCS)	Address Valid to IOCS16		15	ns
46	TwHIOR/W	HIOR/HIOW Strobe Width	50		ns
47	TdIOCH(HIOR/W)	IOCHRDY Delay from HIOR/HIOW		10	ns
48	TdHIOR(Da)	HIOR to Data Available		20	ns
49	ThD	Data Hold Time	9		ns
50	TsHW	Host Write Setup Time	5		ns
51	ThHW	Host Write Hold Time	10		

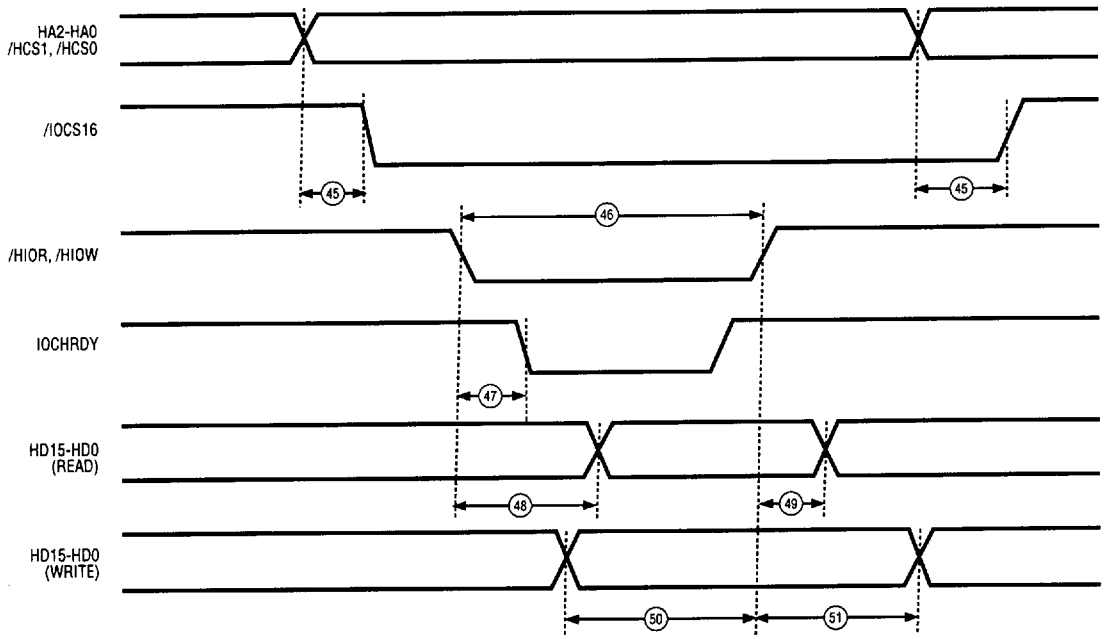


Figure 12. Host Access Timing

DRAM Memory Timing (Figures 13 and 14)

No.	Symbol	Parameter	Min	Max	Unit
52	TdC(Av)	BUFCLK to Address Valid		35	ns
53	TdRAS(Av)	RAS to Address Valid		28	ns
54	TsRAS	RAS Address Setup Time	20		ns
55	TwRAS	RAS Pulse Width	75		ns
56	TdDs(RAS)	Data Setup Time to RAS	10		ns
57	TsCAS	CAS Setup Time	15		ns
58	TdRAS(CAS)	RAS to CAS		40	ns
59	TwCAS	CAS Pulse Width	25		ns
60	TdRAS(WE)	RAS to WE		40	ns
61	TdDs(WE)	Data Setup to WE	3		ns
62	ThCAS	CAS Address Hold Time	20		ns
63	ThRAS	RAS Address Hold Time	7		ns
64	ThD	Data Hold Time	10		ns

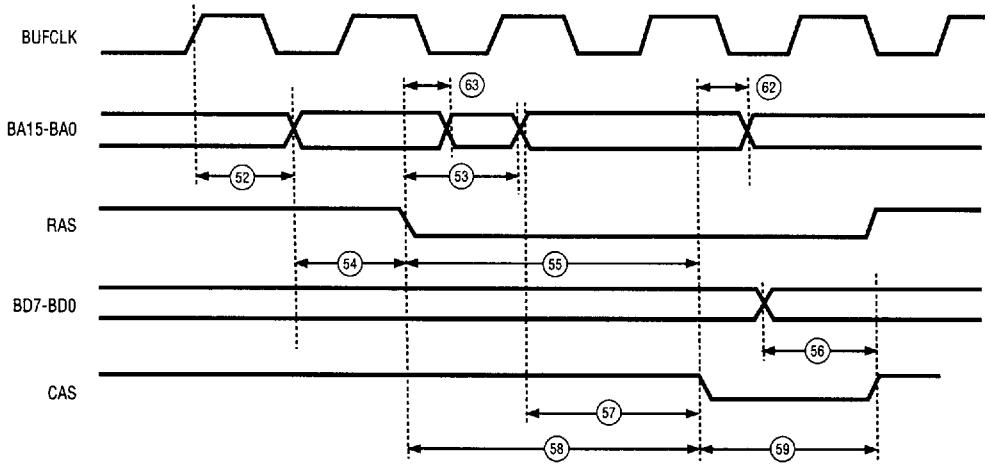


Figure 13. Buffer Memory Read Timing

AC CHARACTERISTICS AND TIMING DIAGRAMS (Continued)

T_A = 0°C to +70°C, V_{DD} = 5V ± –5%, V_{SS} = 0V

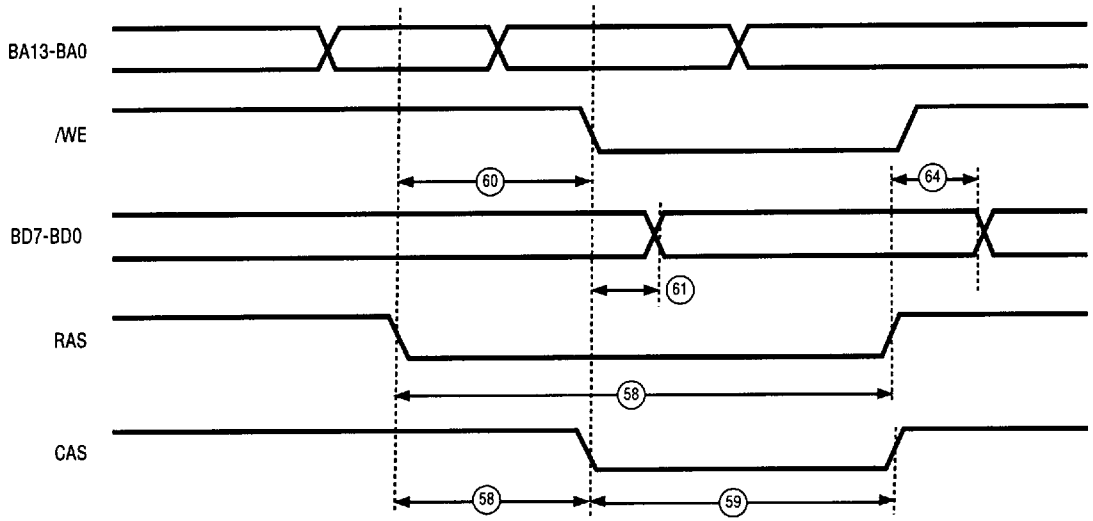
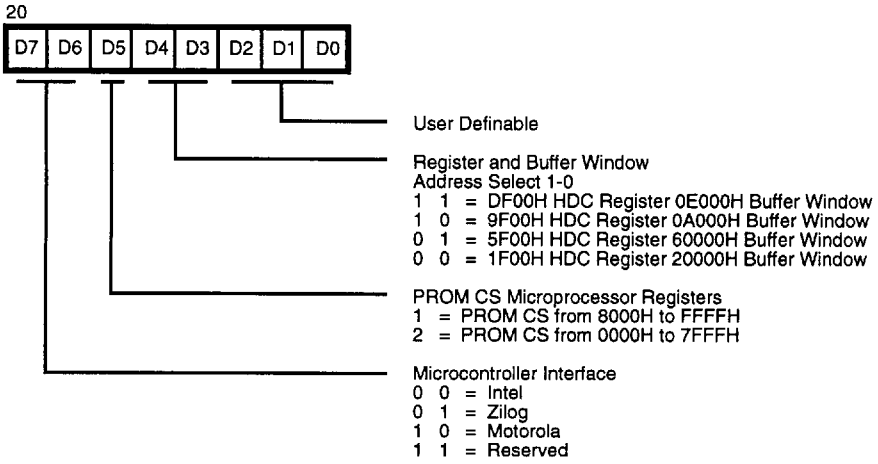


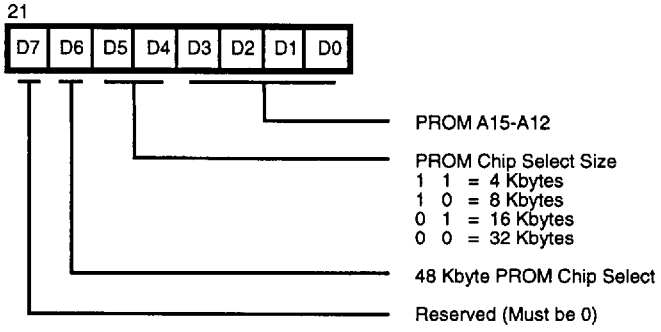
Figure 14. DRAM Buffer Memory Write Timing

REGISTER DESCRIPTION



Reset Condition = (Register Settings for BD7-BD0)

Figure 15. Switches (20H: Read Only)



Reset Condition = 00H if Register 20H bit 5 = 0.
Reset Condition = 08H if Register 20H bit 5 = 1.

Figure 16. PROM Chip Select (CS1) (21H: Read/Write)

6

REGISTER DESCRIPTION (Continued)

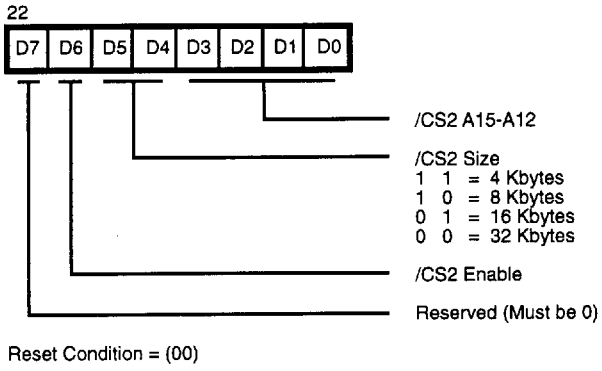


Figure 17. Chip Select 2 (CS2)
(22H: Read/Write)

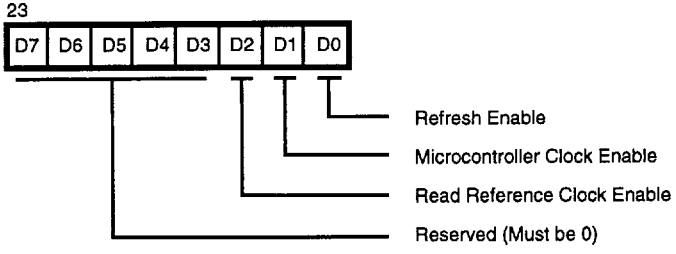


Figure 18. Power-Down Options
(23H: Write Only)

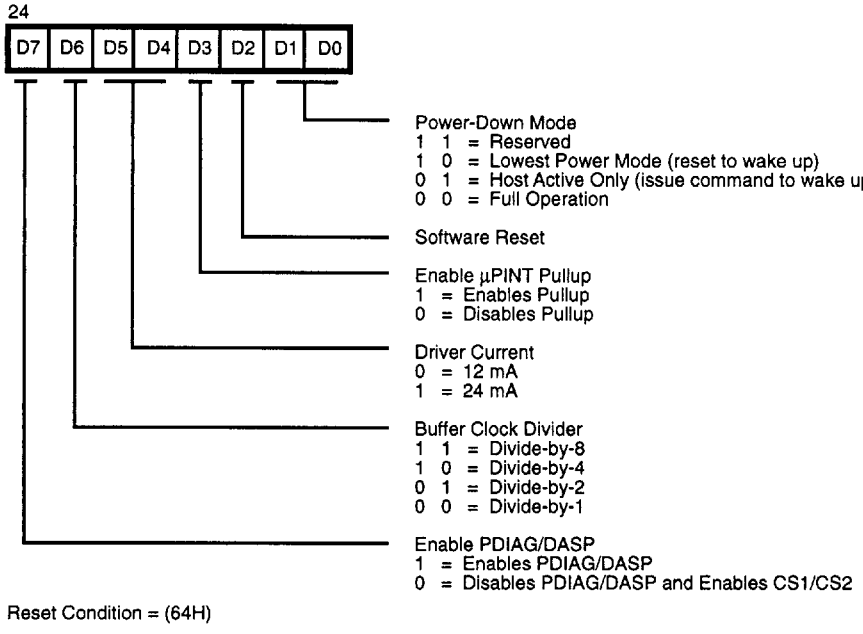


Figure 19. System Operation Control (24H: Read/Write)

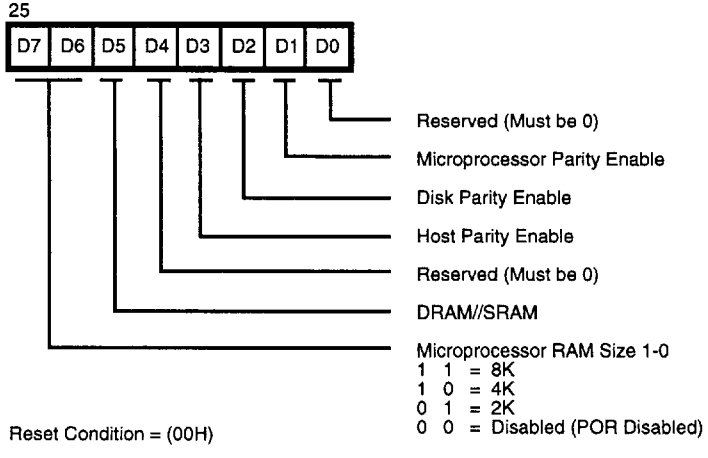


Figure 20. Buffer Mode Control (25H: Read/Write)

6

REGISTER DESCRIPTION (Continued)

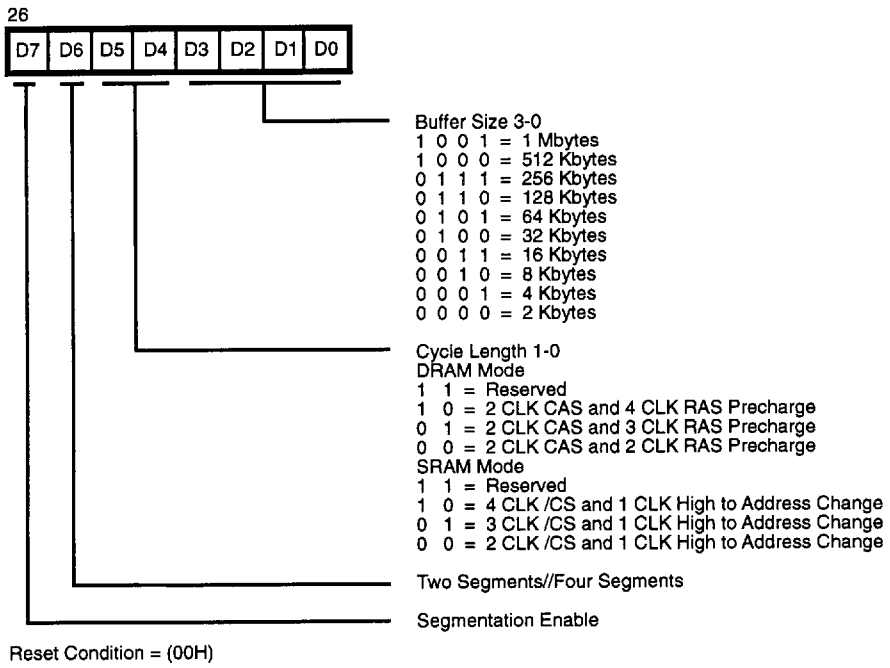


Figure 21. Buffer Size (26H: Read/Write)

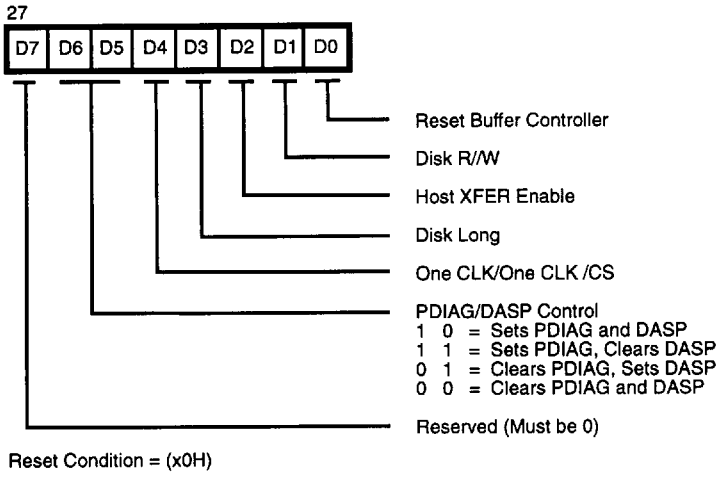


Figure 22. Buffer Operation Control (27H: Read/Write)

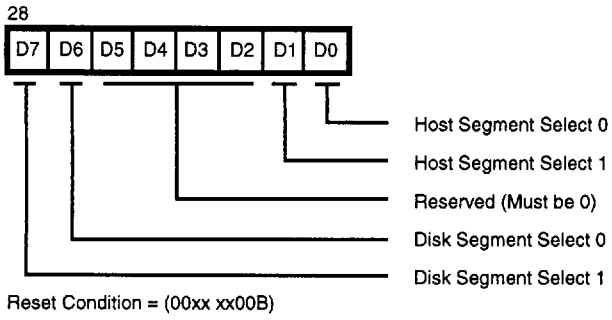


Figure 23. Segment Select (28H: Read/Write)

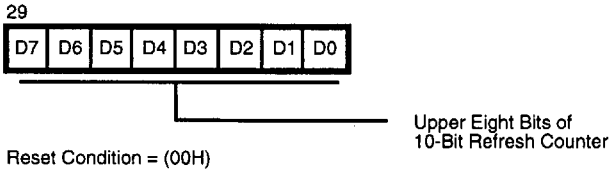


Figure 24. Refresh Period (29H: Read/Write)

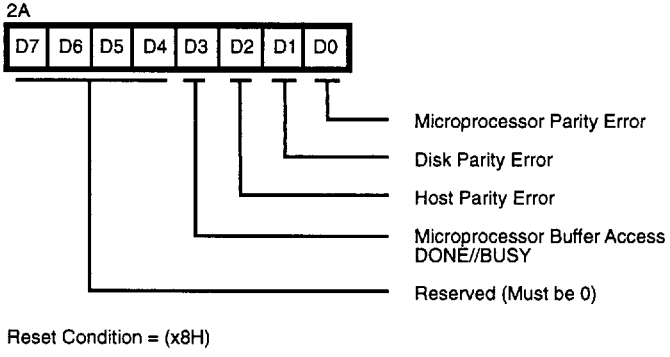


Figure 25. Buffer Interrupt Status/Status Clear (2AH: Read/Write)

6

REGISTER DESCRIPTION (Continued)

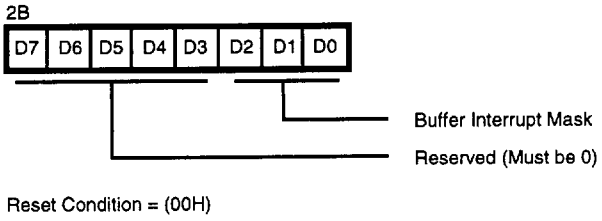


Figure 26. Buffer Interrupt Mask (2BH: Read/Write)

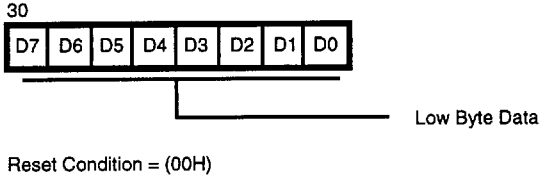


Figure 27. Disk Pointer Low Byte (30H: Read/Write)

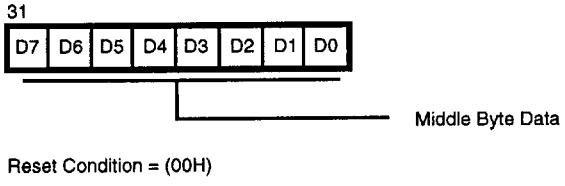


Figure 28. Disk Pointer Middle Byte (31H: Read/Write)

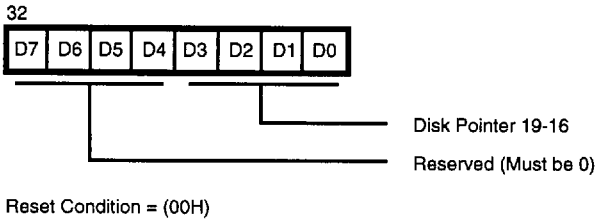


Figure 29. Disk Pointer High Nibble (32H: Read/Write)

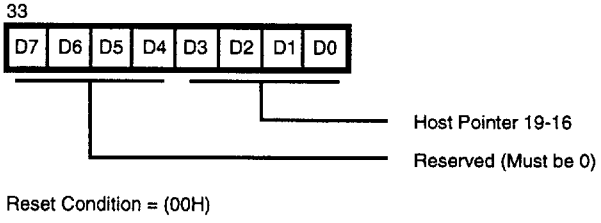


Figure 30 Host Pointer High Nibble (33H: Read/Write)

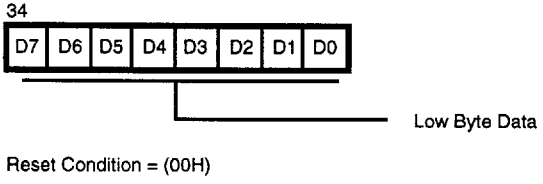
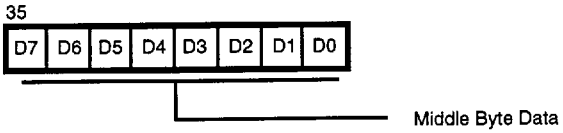


Figure 31. Host Pointer Low Byte (34H: Read/Write)

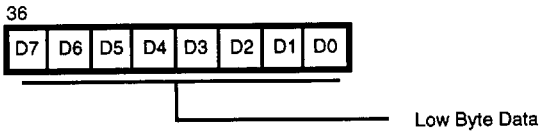
6

REGISTER DESCRIPTION (Continued)



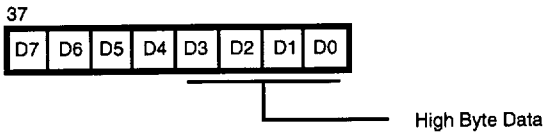
Reset Condition = (00H)

Figure 32. Host Pointer Middle Byte (35H: Read/Write)



Reset Condition = (00H)

Figure 33. Formatter Current Pointer Low (36H: Read/Write)



Reset Condition = (00H)

Figure 34. Formatter Current Pointer High (37H: Read/Write)

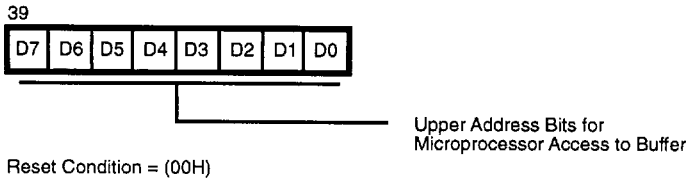


Figure 35. Microprocessor Address 19:12 (39H: Read/Write)

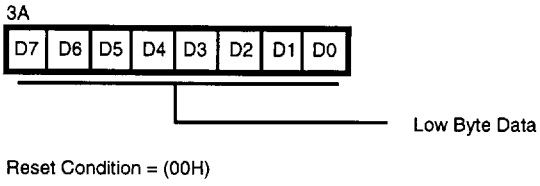


Figure 36. Formatter Pointer Start Low (3AH: Read/Write)

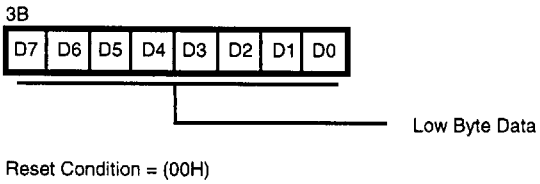


Figure 37. Formatter Pointer End Low (3BH: Read/Write)

6

REGISTER DESCRIPTION (Continued)

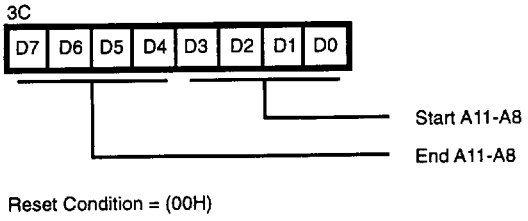


Figure 38. Formatter Pointer Start/End High (3CH: Read/Write)

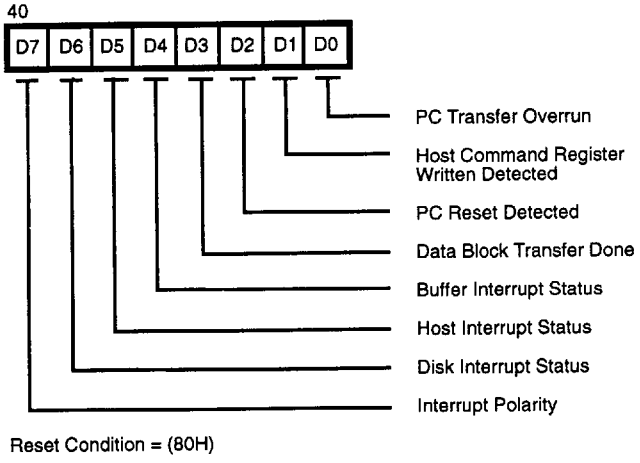


Figure 39. Host Interrupt Status/Status Clear (40H: Read/Write)

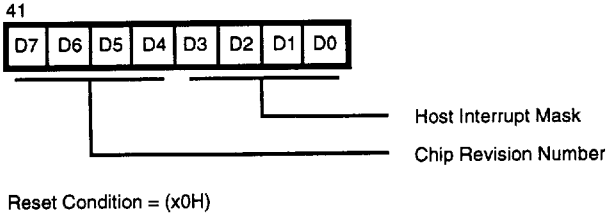


Figure 40. Host Interrupt Mask (41H: Read/Write)

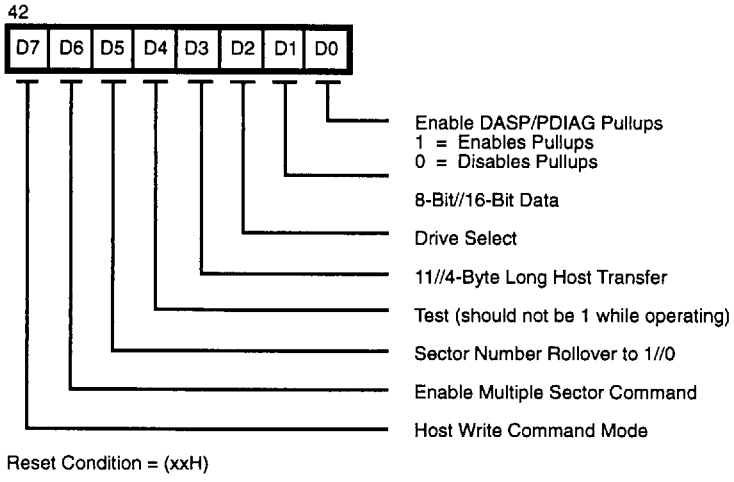


Figure 41. PC Mode Control 1 (42H: Read/Write)

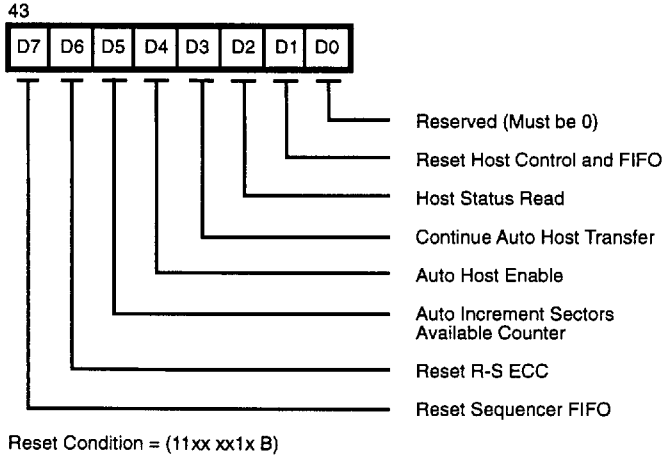


Figure 42. PC Mode Control 2 (43H: Read/Write)

6

REGISTER DESCRIPTION (Continued)

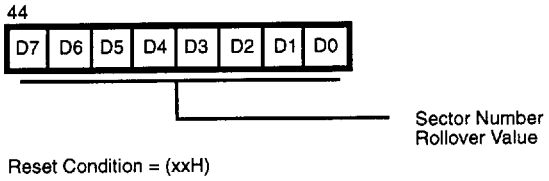


Figure 43. Sector Rollover (44H: Read/Write)

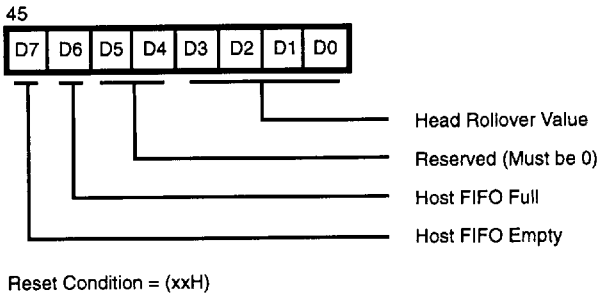


Figure 44. Head Rollover (45H: Read/Write)

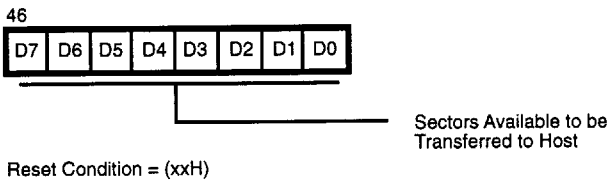


Figure 45. Sectors Available (46H: Read/Write)

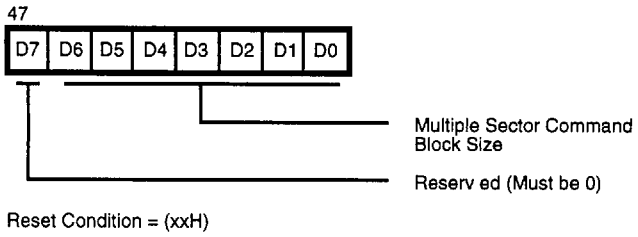


Figure 46. Multiple Sector Size (47H: Read/Write)

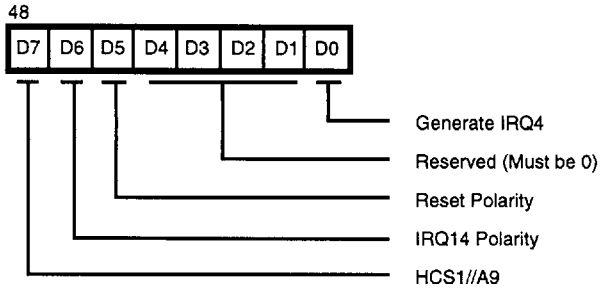


Figure 47. Generate IRQ Register (48H: Read/Write)

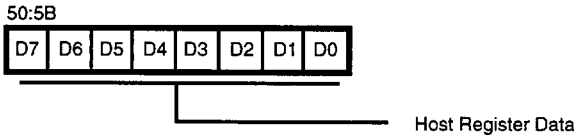


Figure 48. Host Register File (Command/General) (50:5BH: Read/Write)

6

REGISTER DESCRIPTION (Continued)

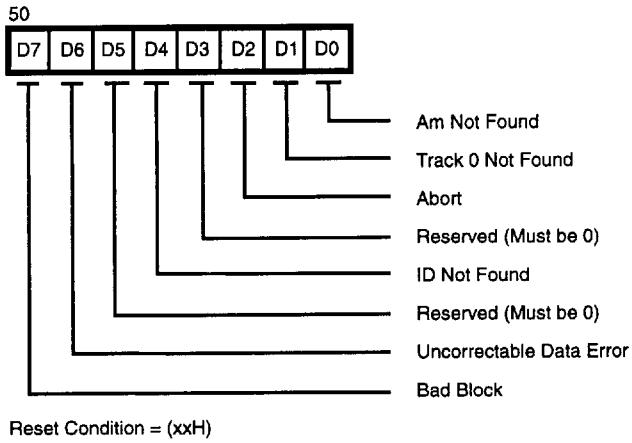


Figure 49. Error Register (Host Read Only 1F1) (50H: Read/Write)

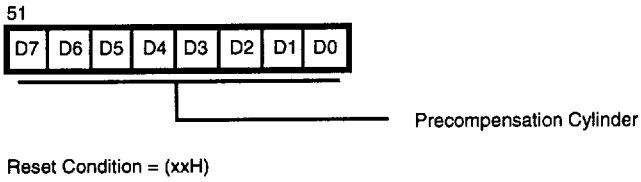


Figure 50. Write Precompensation (Host Write Only 1F1) (51H: Read/Write)

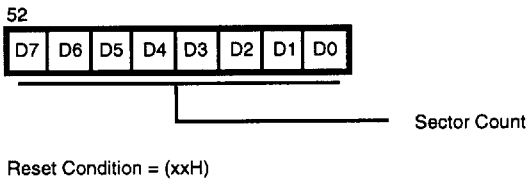


Figure 51. Sector Count (Host Read/Write 1F2) (52H: Read/Write)

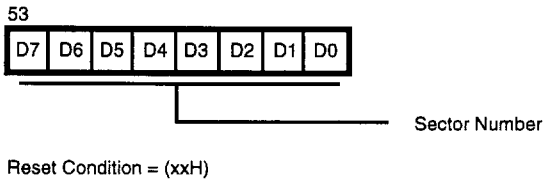


Figure 52. Sector Number (Host Read/Write 1F3) (53H: Read/Write)

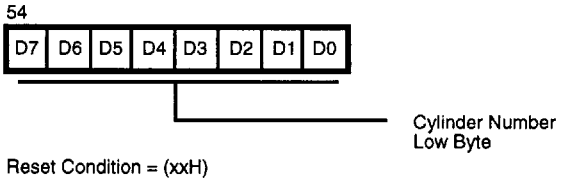


Figure 53. Cylinder Low (Host Read/Write 1F4) (54H: Read/Write)

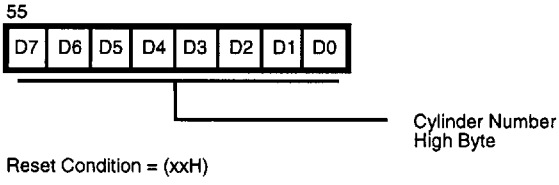


Figure 54. Cylinder High (Host Read/Write 1F5) (55H: Read/Write)

6

REGISTER DESCRIPTION (Continued)

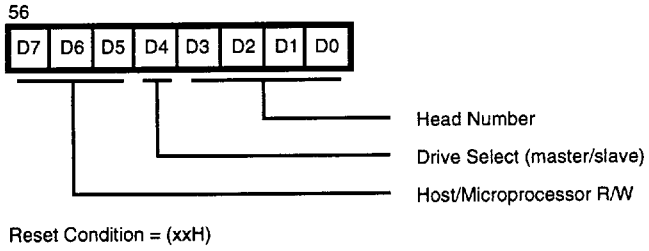


Figure 55. Drive/Head Register (Host Read/Write 1F6 and Read Only 3F7) (56H: Read/Write)

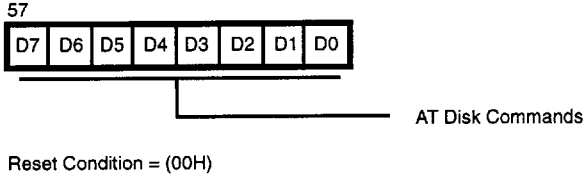


Figure 56. Command Register (Host Write Only 1F7) (57H: Read/Write)

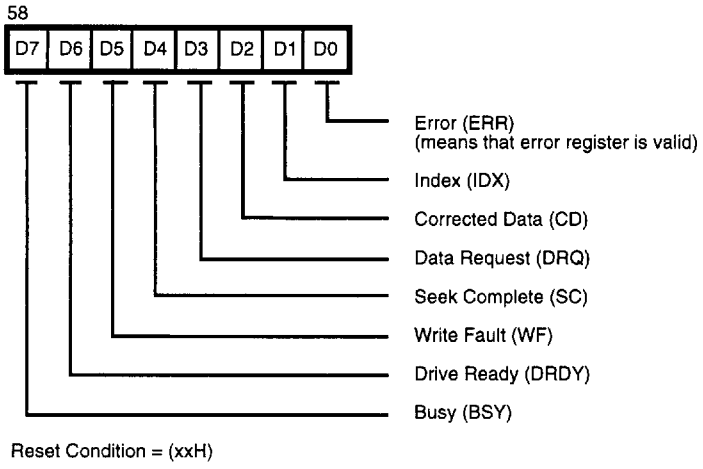


Figure 57. Status Register and Alternate Status Register (Host Read Only 1F7 and 3F6) (58H: Read/Write)

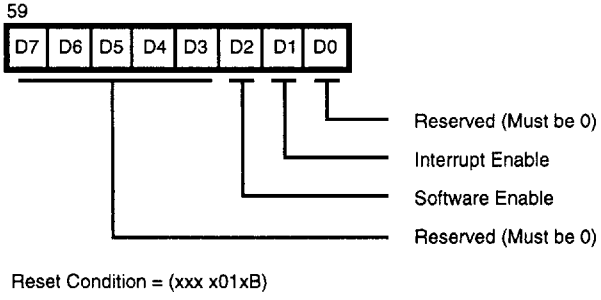
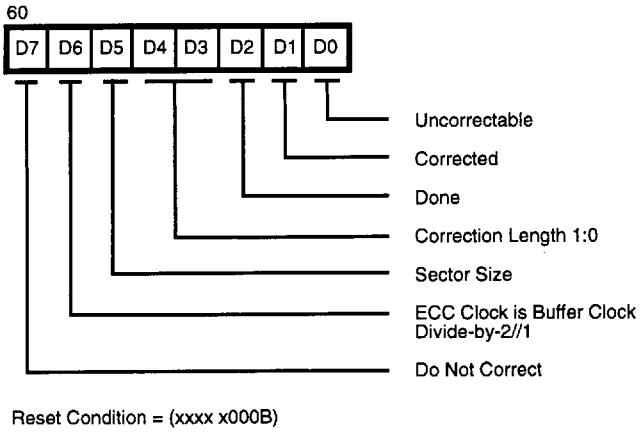


Figure 58. Digital Output Register (Host Write Only 3F6) (59H: Read/Write)

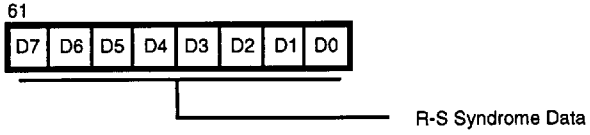
6

REGISTER DESCRIPTION (Continued)



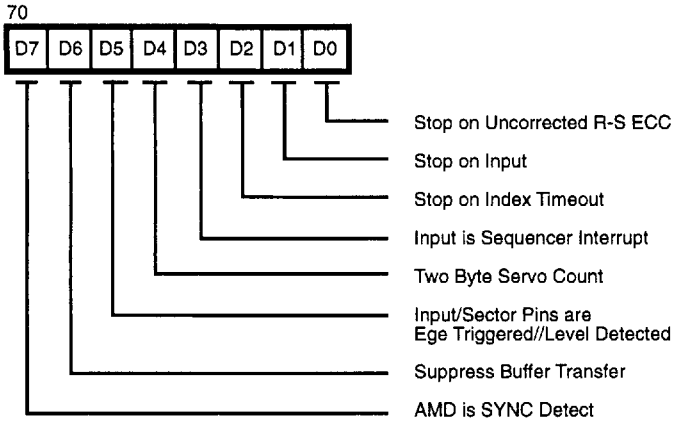
Reset Condition = (xxxx x000B)

Figure 59. R-S ECC Control and Status (60H: Read/Write)



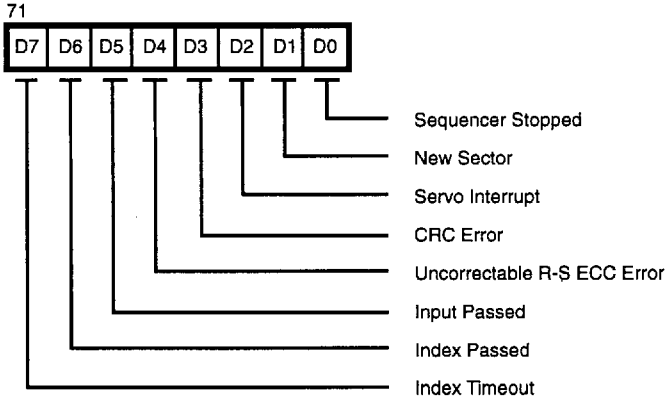
Reset Condition = (xxH)

Figure 60. R-S Syndrome Data (61H: Read Only)



Reset Condition = (00H)

Figure 61. Sequencer Mode Register (70H: Read/Write)



Reset Condition = (01H)

Figure 62. Disk Interrupt Status/Clear Status (71H: Read/Write)

6

REGISTER DESCRIPTION (Continued)

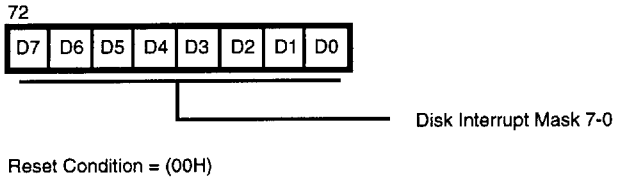


Figure 63. Disk Interrupt Mask (72H: Read/Write)

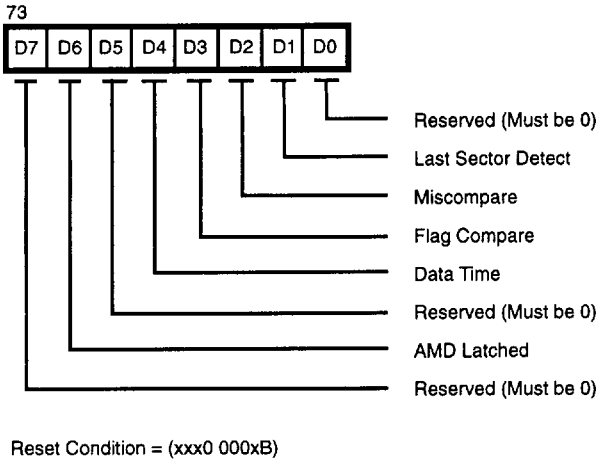


Figure 64. Disk Sequencer Status/Control (73H: Read/Write)

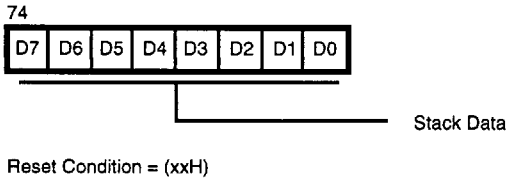


Figure 65. Top Of Stack (74H: Read Only)

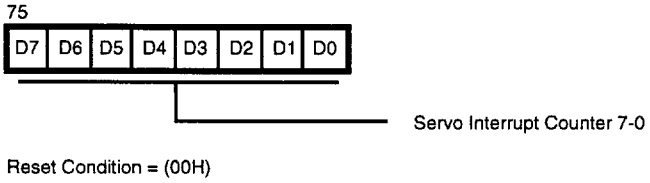


Figure 66. Servo Interrupt Count Lower (75H: Read/Write)

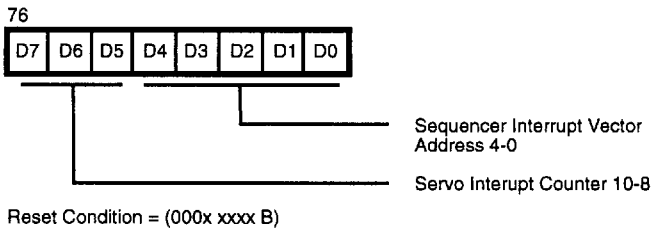


Figure 67. Servo Interrupt Count Upper/Sequencer Vector Address (76H: Read/Write)

6

REGISTER DESCRIPTION (Continued)

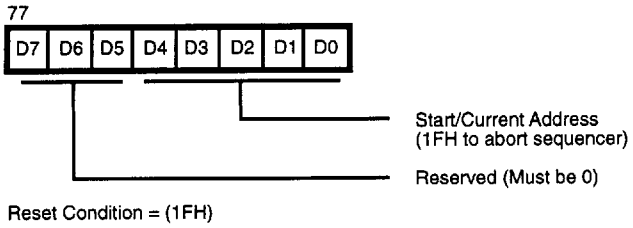


Figure 68. Sequencer Start Address/Current Address (77H: Read/Write)

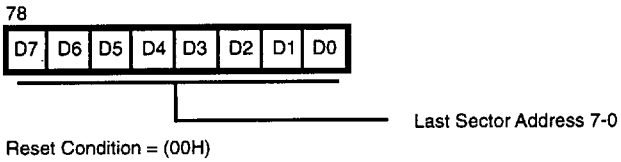


Figure 69. Last Sector Address (78H: Read/Write)

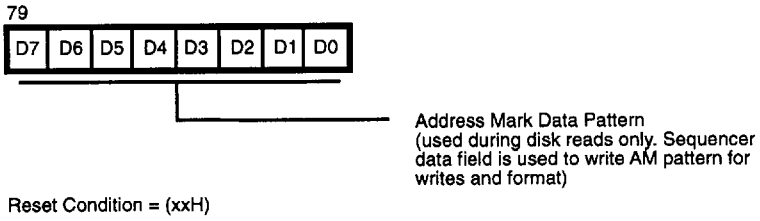


Figure 70. SYNC Pattern (79H: Read/Write)

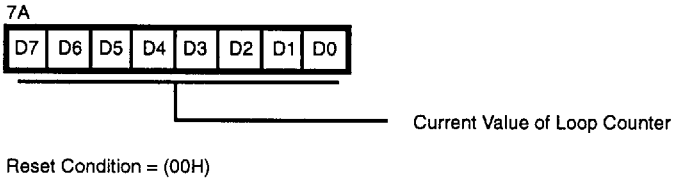


Figure 71. Loop Count Register (7AH: Read Only)

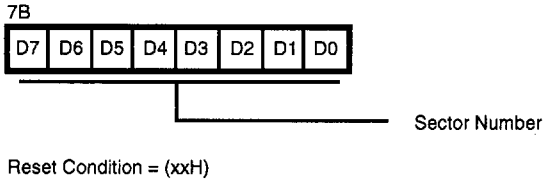


Figure 72. Sequencer Sector Number Register (7BH: Read/Write)

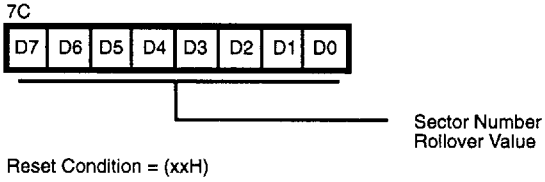


Figure 73. Sequencer Sector Number Rollover (7CH: Read/Write)

6

REGISTER DESCRIPTION (Continued)

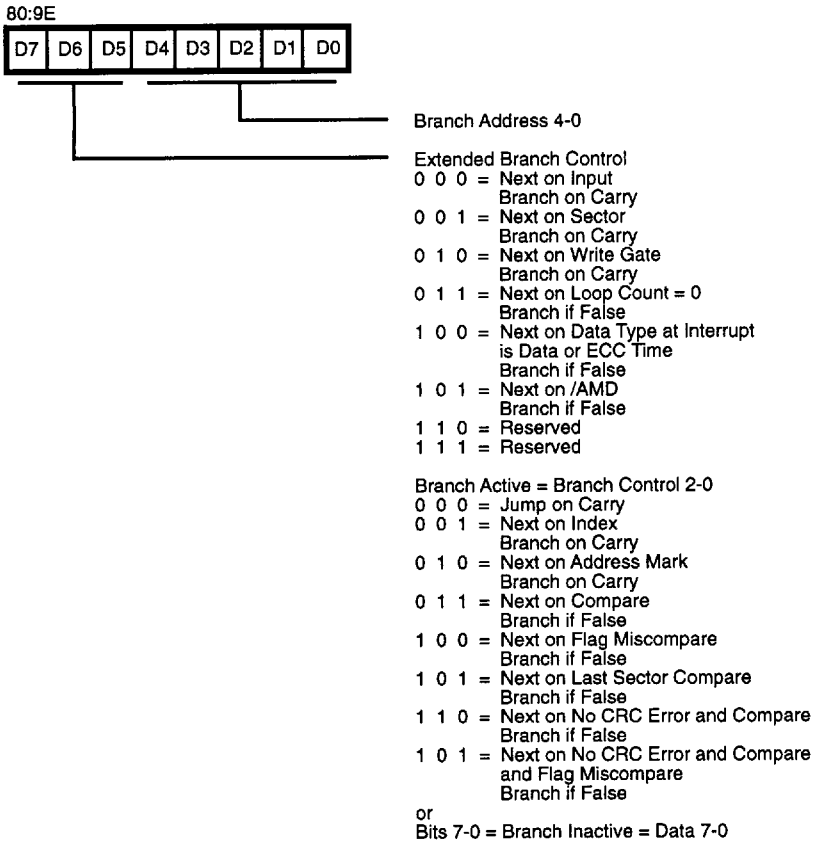


Figure 74. Data/Branch Control/Jump Address (80:9EH: Read/Write)

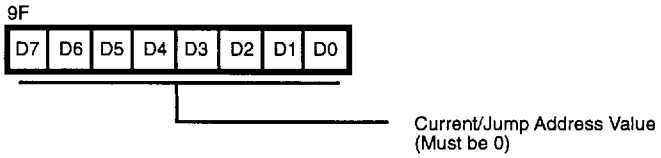


Figure 75. Current Data/Branch (9FH)

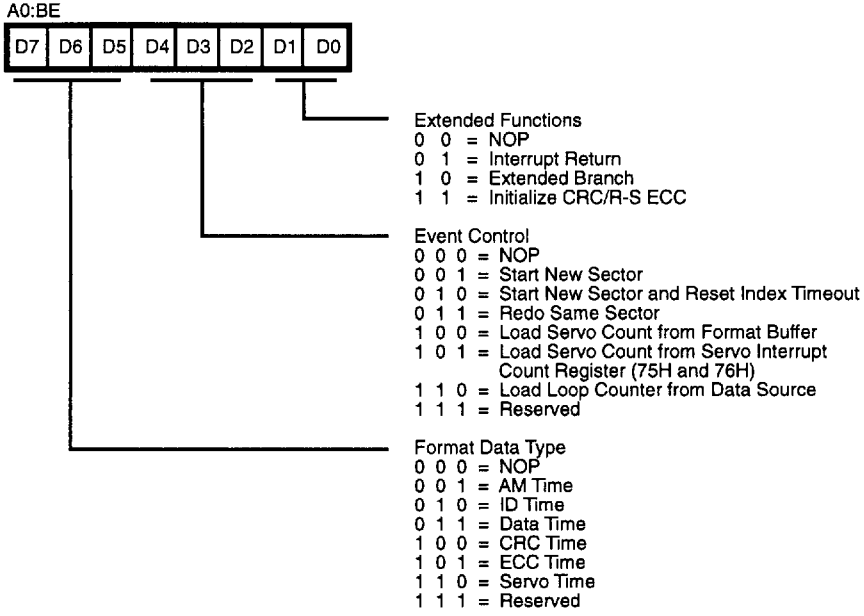


Figure 76. Sequencer Control Field 0 (A0-BEH: Read/Write)

REGISTER DESCRIPTION (Continued)

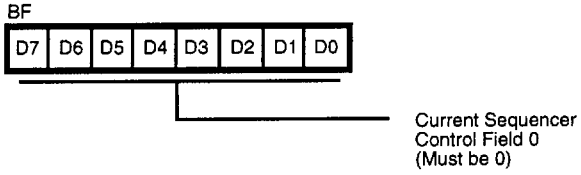


Figure 77. Current Sequencer Control Field 0 (BFH)

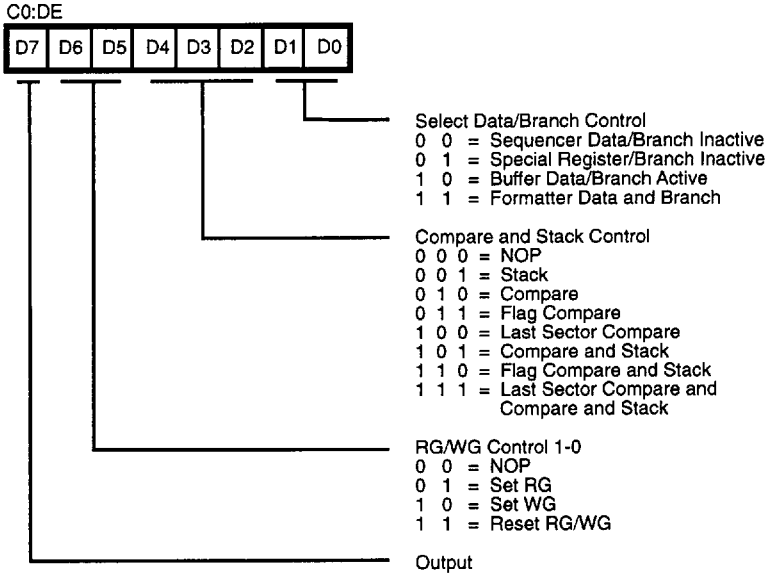


Figure 78. Sequencer Control Field 1 (C0:DEH: Read/Write)

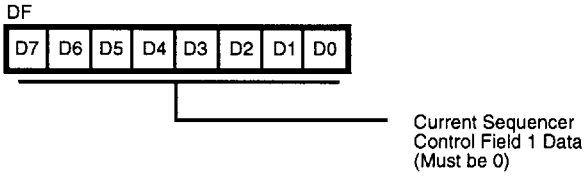


Figure 79. Sequencer Sector Number (DFH: Read/Write)

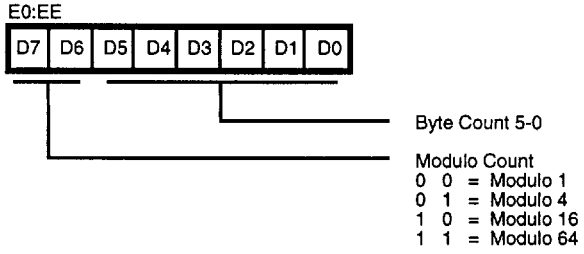


Figure 80. Sequencer Count Field (E0:EEH: Read/Write)

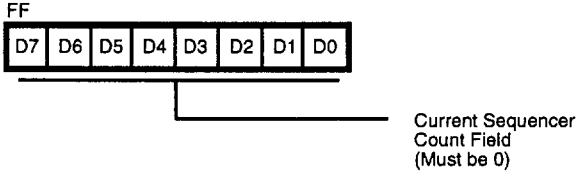
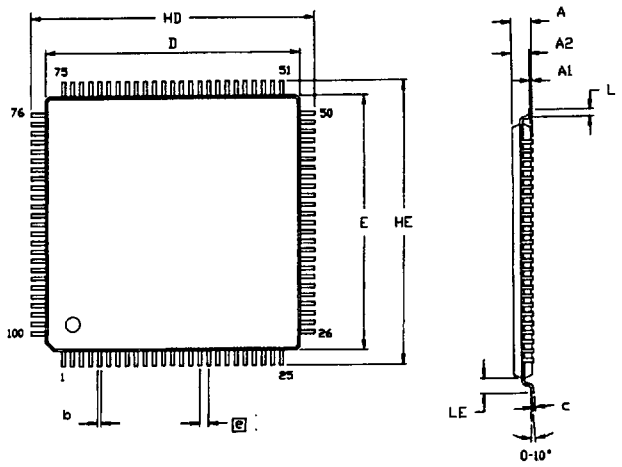


Figure 81. Sequencer Count Field (FFH)

PACKAGE INFORMATION



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	1.35	1.60	.053	.063
A1	0.05	0.20	.002	.008
A2	1.30	1.50	.051	.059
b	0.15	0.26	.006	.010
c	0.10	0.20	.004	.008
HD	15.85	16.15	.624	.636
D	13.90	14.10	.547	.555
HE	15.85	16.15	.624	.636
E	13.90	14.10	.547	.555
e	0.50 TYP		.020 TYP	
L	0.35	0.65	.014	.026
LE	0.90	1.10	.035	.043

1. CONTROLLING DIMENSIONS : MM
2. MAX COPLANARITY : .10mm / .004"

100-Pin VQFP Package Diagram

ORDERING INFORMATION

Z86018

40 MHz (Buffer Clock)
100-Pin VQFP
Z8601840ASC

For fast results, contact your local Zilog sales office for assistance in ordering the part desired.

Package
A = Very Small VQFP

Temperature
S = 0°C to +70°C

Speed
40 = 40 MHz

Environmental
C = Plastic Standard

Example:

Z 86018 40 A S C is a Z86018, 40 MHz, VQFP, 0°C to +70°C, Plastic Standard Flow