

TM2SR72EPH 2097152 BY 72-BIT TM4SR72EPH 4194304 BY 72-BIT SYNCHRONOUS DYNAMIC RAM MODULES

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- **Organization**
 - TM2SR72EPH . . . 2097152 x 72 Bits
 - TM4SR72EPH . . . 4194304 x 72 Bits
- **Single 3.3-V Power Supply**
(±10% Tolerance)
- **Designed for 66-MHz 4-Clock Systems**
- **JEDEC 168-Pin Dual-In-Line Memory Module (DIMM) Without Buffer for Use With Socket**
- **TM2SR72EPH — Uses Nine 16M-Bit Synchronous Dynamic RAMs (SDRAMs) (2M × 8-Bit) in Plastic Thin Small-Outline Packages (TSOPs)**
- **TM4SR72EPH — Uses 18 16M-Bit SDRAMs (2M × 8-Bit) in Plastic TSOPs**
- **Performance Ranges:**
- **High-Speed, Low-Noise Low-Voltage TTL (LVTTTL) Interface**
- **Byte-Read/Write Capability**
- **Read Latencies 2 and 3 Supported**
- **Support Burst-Interleave and Burst-Interrupt Operations**
- **Burst Length Programmable to 1, 2, 4, and 8**
- **Two Banks for On-Chip Interleaving (Gapless Access)**
- **Ambient Temperature Range 0°C to 70°C**
- **Gold-Plated Contacts**
- **Pipeline Architecture**
- **Serial Presence Detect (SPD) Using EEPROM**

| | SYNCHRONOUS CLOCK CYCLE TIME | | ACCESS TIME (CLOCK TO OUTPUT) | | REFRESH INTERVAL |
|--|------------------------------------|------------------------------|-------------------------------------|------------------------------|---------------------|
| | t _{CK3} (CL = 3)† | t _{CK2} (CL = 2) | t _{AC3} (CL = 3) | t _{AC2} (CL = 2) | |
| | TM2SR72EPH-10 | 10 ns | 15 ns | 7 ns | |

† CL = CAS latency

description

The TM2SR72EPH is a 16M-byte, 168-pin dual-in-line memory module (DIMM). The DIMM is composed of nine TMS626812BDGE, 2097152 × 8-bit SDRAMs, each in a 400-mil, 44-pin plastic thin small-outline package (TSOP) mounted on a substrate with decoupling capacitors. See the TMS626812B data sheet (literature number SMOS693).

The TM4SR72EPH is a 32M-byte, 168-pin DIMM. The DIMM is composed of eighteen TMS626812BDGE, 2097152 × 8-bit SDRAMs, each in a 400-mil, 44-pin plastic TSOP mounted on a substrate with decoupling capacitors. See the TMS626812B data sheet (literature number SMOS693).

operation

The TM2SR72EPH operates as nine TMS626812BDGE devices that are connected as shown in the TM2SR72EPH functional block diagram. The TM4SR72EPH operates as eighteen TMS626812BDGE devices connected as shown in the TM4SR72EPH functional block diagram.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



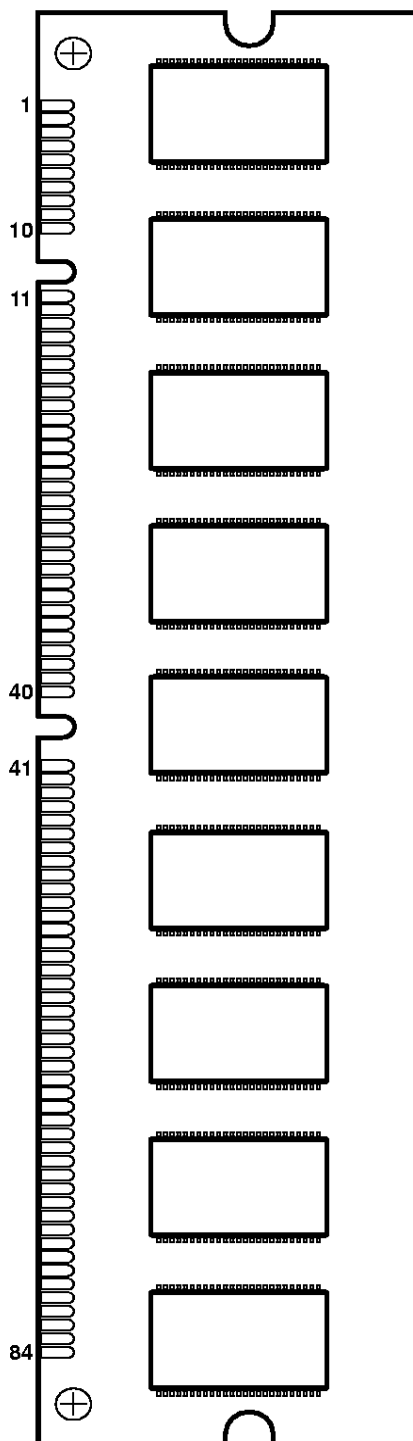
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**DUAL-IN-LINE MEMORY MODULE
(TOP VIEW)**



**TM2SR72EPH
(SIDE VIEW)**



**TM4SR72EPH
(SIDE VIEW)**



PIN NOMENCLATURE

| | |
|---------------|------------------------------|
| A[0:10] | Row-Address Inputs |
| A[0:8] | Column-Address Inputs |
| A11/BA0 | Bank-Select Zero |
| <u>CAS</u> | Column-Address Strobe |
| CB[0:7] | Data In/Data Out |
| CKE[0:1] | Clock Enable |
| CK[0:3] | System Clock |
| DQ[0:63] | Data In/Data Out |
| DQMB[0:7] | Data-In/Data-Out |
| | Mask Enable |
| <u>NC</u> | No Connect |
| <u>RAS</u> | Row-Address Strobe |
| <u>S[0:3]</u> | Chip-Select |
| SA[0:2] | Serial Presence Detect (SPD) |
| | Device Address Input |
| SCL | SPD Clock |
| SDA | SPD Address/Data |
| VDD | 3.3-V Supply |
| <u>VSS</u> | Ground |
| <u>WE</u> | Write Enable |

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Pin Assignments

| NO. | PIN NAME | NO. | PIN NAME | NO. | PIN NAME | NO. | PIN NAME |
|-----|-----------------|-----|-----------------|-----|------------------|-----|-----------------|
| 1 | V _{SS} | 43 | V _{SS} | 85 | V _{SS} | 127 | V _{SS} |
| 2 | DQ0 | 44 | NC | 86 | DQ32 | 128 | CKE0 |
| 3 | DQ1 | 45 | $\overline{S2}$ | 87 | DQ33 | 129 | $\overline{S3}$ |
| 4 | DQ2 | 46 | DQMB2 | 88 | DQ34 | 130 | DQMB6 |
| 5 | DQ3 | 47 | DQMB3 | 89 | DQ35 | 131 | DQMB7 |
| 6 | V _{DD} | 48 | NC | 90 | V _{DD} | 132 | NC |
| 7 | DQ4 | 49 | V _{DD} | 91 | DQ36 | 133 | V _{DD} |
| 8 | DQ5 | 50 | NC | 92 | DQ37 | 134 | NC |
| 9 | DQ6 | 51 | NC | 93 | DQ38 | 135 | NC |
| 10 | DQ7 | 52 | CB2 | 94 | DQ39 | 136 | CB6 |
| 11 | DQ8 | 53 | CB3 | 95 | DQ40 | 137 | CB7 |
| 12 | V _{SS} | 54 | V _{SS} | 96 | V _{SS} | 138 | V _{SS} |
| 13 | DQ9 | 55 | DQ16 | 97 | DQ41 | 139 | DQ48 |
| 14 | DQ10 | 56 | DQ17 | 98 | DQ42 | 140 | DQ49 |
| 15 | DQ11 | 57 | DQ18 | 99 | DQ43 | 141 | DQ50 |
| 16 | DQ12 | 58 | DQ19 | 100 | DQ44 | 142 | DQ51 |
| 17 | DQ13 | 59 | V _{DD} | 101 | DQ45 | 143 | V _{DD} |
| 18 | V _{DD} | 60 | DQ20 | 102 | V _{DD} | 144 | DQ52 |
| 19 | DQ14 | 61 | NC | 103 | DQ46 | 145 | NC |
| 20 | DQ15 | 62 | NC | 104 | DQ47 | 146 | NC |
| 21 | CB0 | 63 | CKE1 | 105 | CB4 | 147 | NC |
| 22 | CB1 | 64 | V _{SS} | 106 | CB5 | 148 | V _{SS} |
| 23 | V _{SS} | 65 | DQ21 | 107 | V _{SS} | 149 | DQ53 |
| 24 | NC | 66 | DQ22 | 108 | NC | 150 | DQ54 |
| 25 | NC | 67 | DQ23 | 109 | NC | 151 | DQ55 |
| 26 | V _{DD} | 68 | V _{SS} | 110 | V _{DD} | 152 | V _{SS} |
| 27 | \overline{WE} | 69 | DQ24 | 111 | \overline{CAS} | 153 | DQ56 |
| 28 | DQMB0 | 70 | DQ25 | 112 | DQMB4 | 154 | DQ57 |
| 29 | DQMB1 | 71 | DQ26 | 113 | DQMB5 | 155 | DQ58 |
| 30 | $\overline{S0}$ | 72 | DQ27 | 114 | $\overline{S1}$ | 156 | DQ59 |
| 31 | NC | 73 | V _{DD} | 115 | \overline{RAS} | 157 | V _{DD} |
| 32 | V _{SS} | 74 | DQ28 | 116 | V _{SS} | 158 | DQ60 |
| 33 | A0 | 75 | DQ29 | 117 | A1 | 159 | DQ61 |
| 34 | A2 | 76 | DQ30 | 118 | A3 | 160 | DQ62 |
| 35 | A4 | 77 | DQ31 | 119 | A5 | 161 | DQ63 |
| 36 | A6 | 78 | V _{SS} | 120 | A7 | 162 | V _{SS} |
| 37 | A8 | 79 | CK2 | 121 | A9 | 163 | CK3 |
| 38 | A10 | 80 | NC | 122 | A11/BA0 | 164 | NC |
| 39 | NC | 81 | NC | 123 | NC | 165 | SA0 |
| 40 | V _{DD} | 82 | SDA | 124 | V _{DD} | 166 | SA1 |
| 41 | V _{DD} | 83 | SCL | 125 | CK1 | 167 | SA2 |
| 42 | CK0 | 84 | V _{DD} | 126 | NC | 168 | V _{DD} |



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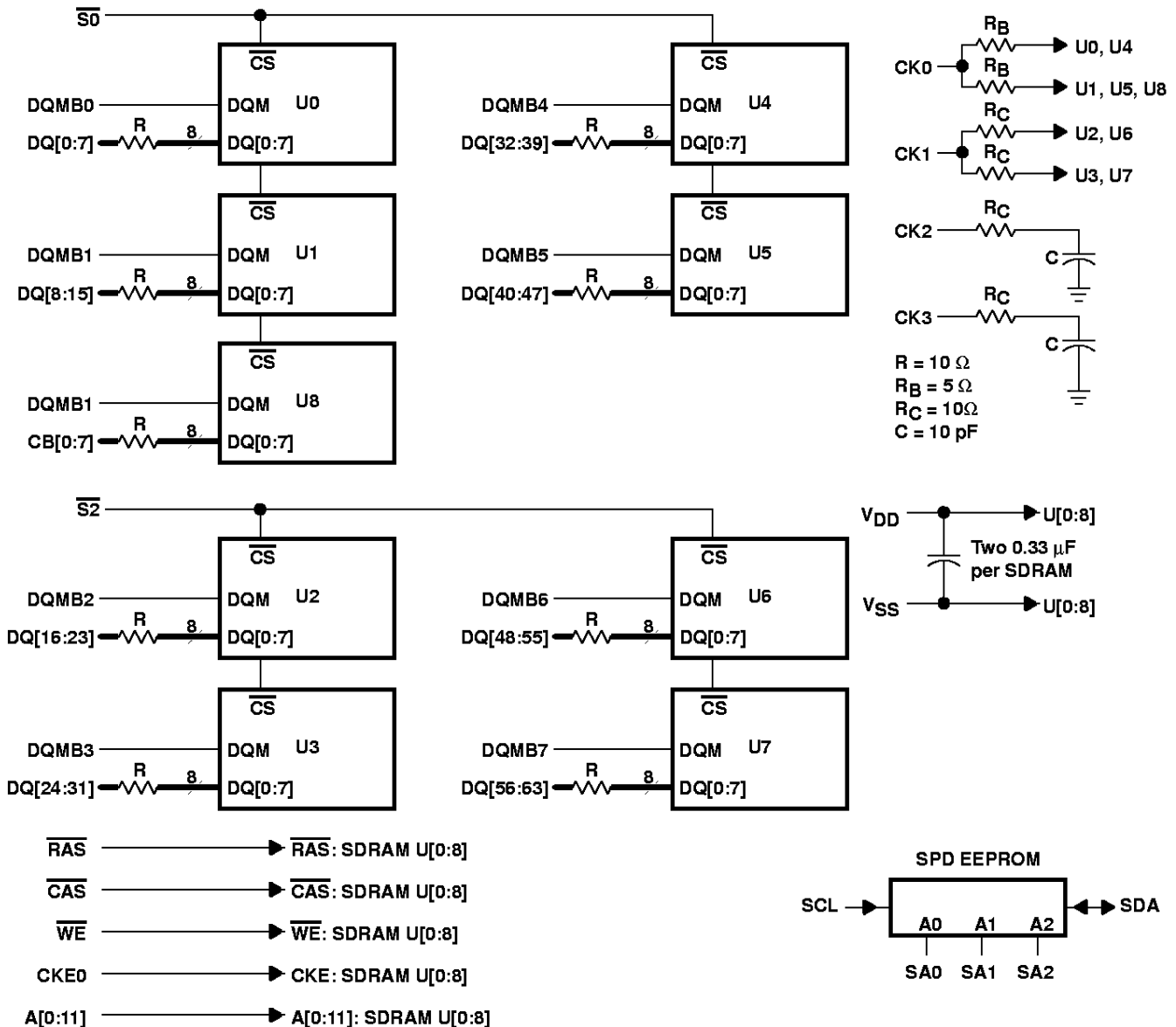
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dual-in-line memory module and components

The dual-in-line memory module and components include:

- PC substrate: $1,27 \pm 0,1$ mm (0.05 inch) nominal thickness; 0.005 inch/inch maximum warpage
- Bypass capacitors: Multilayer ceramic
- Contact area: Nickel plate and gold plate over copper

functional block diagram for the TM2SR72EPH



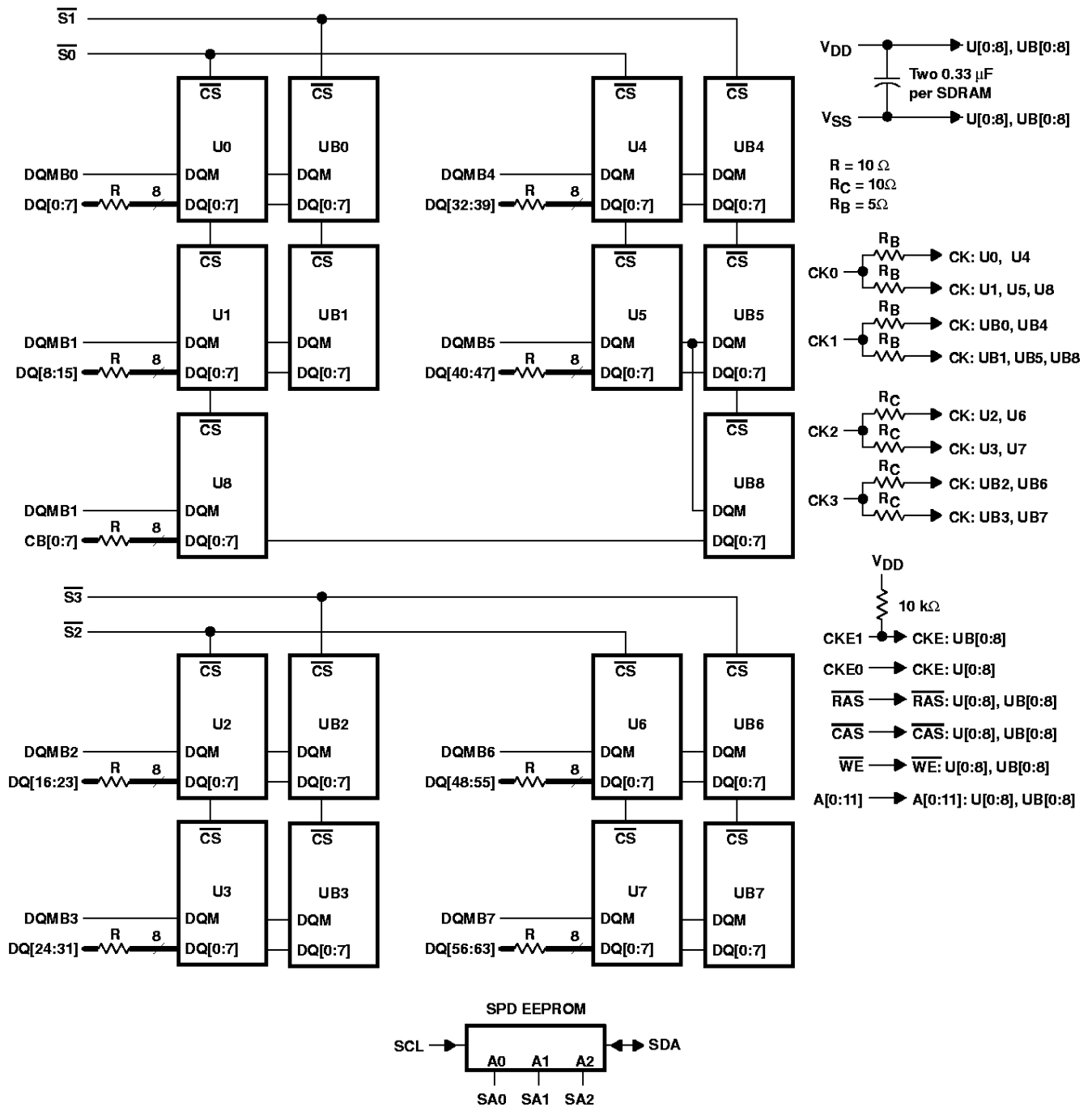
LEGEND: \overline{CS} = Chip Select
 SPD = Serial Presence Detect



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functional block diagram for the TM4SR72EPH



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absolute maximum ratings over operating ambient temperature range (unless otherwise noted)†

| | |
|--|------------------|
| Supply voltage range, V_{DD} | –0.5 V to 4.6 V |
| Voltage range on any pin (see Note 1) | – 0.5 V to 4.6 V |
| Short-circuit output current | 50 mA |
| Power dissipation: TM2SR72EPH | 9 W |
| TM4SR72EPH | 18 W |
| Operating ambient temperature range, T_A | 0°C to 70°C |
| Storage temperature range, T_{stg} | – 55°C to 150°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS} .

recommended operating conditions

| | MIN | NOM | MAX | UNIT |
|--|------|-----|----------------|------|
| V_{DD} Supply voltage | 3 | 3.3 | 3.6 | V |
| V_{SS} Supply voltage | | 0 | | V |
| V_{IH} High-level input voltage | 2 | | $V_{DD} + 0.3$ | V |
| V_{IH-SPD} High-level input voltage for SPD device | 2 | | 5.5 | V |
| V_{IL} Low-level input voltage ‡ | –0.3 | | 0.8 | V |
| T_A Operating ambient temperature | 0 | | 70 | °C |

‡ V_{IL} MIN = –1.5 V ac (pulse width \leq 5 ns)

capacitance over recommended ranges of supply voltage and ambient temperature, $f = 1$ MHz (see Note 2)§

| PARAMETER | TMxSR72EPH | | UNIT |
|--|------------|-----|------|
| | MIN | MAX | |
| $C_i(CK)$ Input capacitance, CK input | 2.5 | 4 | pF |
| $C_i(AC)$ Input capacitance, address and control inputs: A0–A11, \overline{RAS} , \overline{CAS} , \overline{WE} | 2.5 | 5 | pF |
| $C_i(CKE)$ Input capacitance, CKE input | | 5 | pF |
| C_o Output capacitance | 4 | 6.5 | pF |
| $C_i(DQMBx)$ Input capacitance, DQMBx input | 2.5 | 5 | pF |
| $C_i(Sx)$ Input capacitance, \overline{Sx} input | 2.5 | 5 | pF |
| $C_i(o)(SDA)$ Input/output capacitor, SDA input | | 9 | pF |
| $C_i(SPD)$ Input capacitor, SA0, SA1, SA2, SCL inputs | | 7 | pF |

§ Specifications in this table represent a single SDRAM device.

NOTE 2: $V_{DD} = 3.3$ V \pm 0.3 V. Bias on pins under test is 0 V.



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electrical characteristics over recommended ranges of supply voltage and ambient temperature (unless otherwise noted) (see Note 3)†

| PARAMETER | | TEST CONDITIONS | 'xSR72EPH-10 | | UNIT |
|--------------------|--|---|-----------------|------|------|
| | | | MIN | MAX | |
| V _{OH} | High-level output voltage | I _{OH} = -2 mA | 2.4 | | V |
| V _{OL} | Low-level output voltage | I _{OL} = 2 mA | | 0.4 | V |
| I _I | Input current (leakage) | 0 V < V _I < V _{DD} + 0.3 V, All other pins = 0 V to V _{DD} | | ± 10 | μA |
| I _O | Output current (leakage) | 0 V < V _O < V _{DD} + 0.3 V, Output disabled | | ± 10 | μA |
| I _{CC1} | Operating current | Burst length = 1, t _{RC} ≥ t _{RC} MIN I _{OH} /I _{OL} = 0 mA, one bank activated (see Note 4) | CAS latency = 2 | 85 | mA |
| | | | CAS latency = 3 | 90 | |
| I _{CC2P} | Precharge standby current in power-down mode | CKE ≤ V _{IL} MAX, t _{CK} = 15 ns (see Note 5) | | 1 | mA |
| I _{CC2PS} | | CKE and CK ≤ V _{IL} MAX, t _{CK} = ∞ (see Note 6) | | 1 | |
| I _{CC2N} | Precharge standby current in non-power-down mode | CKE ≥ V _{IH} MIN, t _{CK} = 15 ns (see Note 5) | | 30 | mA |
| I _{CC2NS} | | CKE ≥ V _{IH} MIN, CK ≤ V _{IL} MAX, t _{CK} = ∞ (see Note 6) | | 2 | |
| I _{CC3P} | Active standby current in power-down mode | CKE ≤ V _{IL} MAX, t _{CK} = 15 ns (see Note 5) | | 3 | mA |
| I _{CC3PS} | | CKE and CK ≤ V _{IL} MAX, t _{CK} = ∞ (see Note 6) | | 3 | |
| I _{CC3N} | Active standby current in non-power-down mode | CKE ≥ V _{IH} MIN, t _{CK} = 15 ns (see Note 5) | | 40 | mA |
| I _{CC3NS} | | CKE ≥ V _{IH} MIN, CK ≤ V _{IL} MAX, t _{CK} = ∞ (see Note 6) | | 10 | |
| I _{CC4} | Burst current | Page burst, I _{OH} /I _{OL} = 0 mA All banks activated, n _{CCD} = one cycle (see Note 7) | CAS latency = 2 | 130 | mA |
| | | | CAS latency = 3 | 140 | |
| I _{CC5} | Auto-refresh current | t _{RC} ≤ t _{RC} MIN | CAS latency = 2 | 80 | mA |
| | | | CAS latency = 3 | 85 | |
| I _{CC6} | Self-refresh current | CKE ≤ V _{IL} MAX | | 0.4 | mA |

† Specifications in this table represent a single SDRAM device.

- NOTES: 3. All specifications apply to the device after power-up initialization. All control and address inputs must be stable and valid.
4. Control, DQ, and address inputs change state only twice during t_{RC}.
5. Control, DQ, and address inputs change state only once every 30 ns.
6. Control, DQ, and address inputs do not change (stable).
7. Control, DQ, and address inputs change only once every cycle.



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ac timing requirements†‡

| | 'xSR72EPH-10 | | UNIT |
|---|--|--------|-------|
| | MIN | MAX | |
| t _{CK2} Cycle time, CLK, CAS latency = 2 | 15 | | ns |
| t _{CK3} Cycle time, CLK, CAS latency = 3 | 10 | | ns |
| t _{CH} Pulse duration, CLK high | 3 | | ns |
| t _{CL} Pulse duration, CLK low | 3 | | ns |
| t _{AC2} Access time, CLK high to data out, CAS latency = 2 (see Note 8) | | 7 | ns |
| t _{AC3} Access time, CLK high to data out, CAS latency = 3 (see Note 8) | | 7 | ns |
| t _{OH} Hold time, CLK high to data out | 3 | | ns |
| t _{LZ} Delay time, CLK high to DQ in low-impedance state (see Note 9) | 2 | | ns |
| t _{HZ} Delay time, CLK high to DQ in high-impedance state (see Note 10) | | 8 | ns |
| t _{IS} Setup time, address, control, and data input | 2 | | ns |
| t _{IH} Hold time, address, control, and data input | 1 | | ns |
| t _{QESP} Power-down/self-refresh exit time | 10 | | ns |
| t _{RAS} Delay time, ACTV command to DEAC or DCAB command | 50 | 100000 | ns |
| t _{RC} Delay time, ACTV, REFR, or SLFR exit to ACTV, MRS, REFR, or SLFR command | 80 | | ns |
| t _{RCD} Delay time, ACTV command to READ, READ-P, WRT, or WRT-P command (see Note 11) | 20 | | ns |
| t _{RP} Delay time, DEAC or DCAB command to ACTV, MRS, REFR, or SLFR command | 30 | | ns |
| t _{RRD} Delay time, ACTV command in one bank to ACTV command in the other bank | 30 | | ns |
| t _{RSA} Delay time, MRS command to ACTV, MRS, REFR, or SLFR command | 20 | | ns |
| t _{APR} Final data out of READ-P operation to ACTV, MRS, SLFR, or REFR command | t _{RP} – (CL – 1) * t _{CK} | | ns |
| t _{APW} Final data in of WRT-P operation to ACTV, MRS, SLFR, or REFR command | t _{RP} + t _{CK} | | ns |
| t _{WR} Delay time, final data in of WRT operation to DEAC or DCAB command | 10 | | ns |
| t _T Transition time (see Note 12) | 1 | 5 | ns |
| t _{REF} Refresh interval | | 64 | ms |
| n _{CCD} Delay time, READ or WRT command to an interrupting command | 1 | | cycle |
| n _{CDD} Delay time, $\overline{\text{CS}}$ low or high to input enabled or inhibited | 0 | 0 | cycle |
| n _{CLE} Delay time, CKE high or low to CLK enabled or disabled | 1 | 1 | cycle |
| n _{CWL} Delay time, final data in of WRT operation to READ, READ-P, WRT, WRT-P | 1 | | cycle |
| n _{DID} Delay time, ENBL or MASK command to enabled or masked data in | 0 | 0 | cycle |
| n _{DOD} Delay time, ENBL or MASK command to enabled or masked data out | 2 | 2 | cycle |
| n _{HZP2} Delay time, DEAC or DCAB command to DQ in high-impedance state, CAS latency = 2 | | 2 | cycle |
| n _{HZP3} Delay time, DEAC or DCAB command to DQ in high-impedance state, CAS latency = 3 | | 3 | cycle |
| n _{WCD} Delay time, WRT command to first data in | 0 | 0 | cycle |

† All references are made to the rising transition of CK_x, unless otherwise noted.

‡ Specifications in this table represent a single SDRAM device.

NOTES: 8. t_{AC} is referenced from the rising transition of CK that precedes the data-out cycle. For example, the first data out t_{AC} is referenced from the rising transition of CK_x that is CAS latency – one cycle after the READ command. Access time is measured at output reference level 1.4 V.

9. t_{LZ} is measured from the rising transition of CK_x that is CAS latency – one cycle after the READ command.

10. t_{HZ} MAX defines the time at which the outputs are no longer driven and is not referenced to output voltage levels.

11. For read or write operations with automatic deactivate, t_{RCD} must be set to satisfy minimum t_{RAS}.

12. Transition time, t_T, is measured between V_{IH} and V_{IL}.



serial presence detect

The serial presence detect (SPD) is contained in a 2K-bit serial EEPROM located on the module. The SPD nonvolatile EEPROM contains various data such as module configuration, SDRAM organization, and timing parameters (see Table 1 and Table 2). Only the first 128 bytes are programmed by Texas Instruments; the remaining 128 bytes are available for customer use. Programming is done through a IIC bus using the clock (SCL) and data (SDA) signals. All Texas Instruments modules comply with the current JEDEC SPD Standard. See the Texas Instruments *Serial Presence Detect Technical Reference* (literature number SMMU001) for further details.

SPD contents for the TMxSR72EPH devices are listed in the following tables:

Table 1–TM2SR72EPH Table 2–TM4SR72EPH

Table 1. Serial Presence Detect Data for the TM2SR72EPH

| BYTE NO. | DESCRIPTION OF FUNCTION | TM2SR72EPH-10 | |
|----------|--|--------------------------|------|
| | | ITEM | DATA |
| 0 | Defines number of bytes written into serial memory during module manufacturing | 128 bytes | 80h |
| 1 | Total number of bytes of SPD memory device | 256 bytes | 08h |
| 2 | Fundamental memory type (FPM, EDO, SDRAM, . . .) | SDRAM | 04h |
| 3 | Number of row addresses on this assembly | 11 | 0Bh |
| 4 | Number of column addresses on this assembly | 9 | 09h |
| 5 | Number of module rows on this assembly | 1 bank | 01h |
| 6 | Data width of this assembly | 72 bits | 48h |
| 7 | Data width continuation | | 00h |
| 8 | Voltage interface standard of this assembly | LVTTTL | 01h |
| 9 | SDRAM cycle time at maximum supported CAS latency (CL), CL = X | t _{CK} = 10 ns | A0h |
| 10 | SDRAM access from clock at CL = X | t _{AC} = 7 ns | 70h |
| 11 | DIMM configuration type (non-parity, parity, error correcting code [ECC]) | ECC | 02h |
| 12 | Refresh rate/type | 15.6 μs/ self-refresh | 80h |
| 13 | SDRAM width, primary DRAM | x8 | 08h |
| 14 | Error-checking SDRAM data width | x8 | 08h |
| 15 | Minimum clock delay, back-to-back random column addresses | 1 CK cycle | 01h |
| 16 | Burst lengths supported | 1, 2, 4, 8 | 0Fh |
| 17 | Number of banks on each SDRAM device | 2 banks | 02h |
| 18 | CAS latencies supported | 2, 3 | 06h |
| 19 | CS latency | 0 | 01h |
| 20 | Write latency | 0 | 01h |

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serial presence detect (continued)

Table 1. Serial Presence Detect Data for the TM2SR72EPH (Continued)

| BYTE NO. | DESCRIPTION OF FUNCTION | TM2SR72EPH-10 | |
|----------|--|---|------------|
| | | ITEM | DATA |
| 21 | SDRAM module attributes | Non-buffered/ Non-registered | 00h |
| 22 | SDRAM device attributes: general | VDD tolerance = (+10%), Burst read/write, precharge all, auto precharge | 0Eh |
| 23 | Minimum clock cycle time at CL = X – 1 | t _{CK} = 15 ns | F0h |
| 24 | Maximum data-access time from clock at CL = X – 1 | t _{AC} = 7 ns | 70h |
| 25 | Minimum clock cycle time at CL = X – 2 | N/A | 00h |
| 26 | Maximum data-access time from clock at CL = X – 2 | N/A | 00h |
| 27 | Minimum row-precharge time | t _{RP} = 20 ns | 14h |
| 28 | Minimum row-active to row-active delay | t _{RRD} = 20 ns | 14h |
| 29 | Minimum $\overline{\text{RAS}}$ -to- $\overline{\text{CAS}}$ delay | t _{RCD} = 30 ns | 1Eh |
| 30 | Minimum $\overline{\text{RAS}}$ pulse width | t _{RAS} = 50 ns | 32h |
| 31 | Density of each bank on module | 16M Bytes | 04h |
| 32 | Command and address signal input setup time | t _{IS} = 2 ns | 20h |
| 33 | Command and address signal input hold time | t _{IH} = 1 ns | 10h |
| 34 | Data signal input setup time | t _{IS} = 2 ns | 20h |
| 35 | Data signal input hold time | t _{IH} = 1 ns | 10h |
| 36–61 | Superset features (may be used in the future) | | |
| 62 | SPD revision | Rev. 1.2 | 12h |
| 63 | Checksum for byte 0–62 | 2 | 02h |
| 64–71 | Manufacturer's JEDEC ID code per JEP – 106E | 97h | 9700...00h |
| 72 | Manufacturing location† | TBD | |
| 73–90 | Manufacturer's part number† | TBD | |
| 91 | Die revision code† | TBD | |
| 92 | PCB revision code† | TBD | |
| 93–94 | Manufacturing date† | TBD | |
| 95–98 | Assembly serial number† | TBD | |
| 99–125 | Manufacturer-specific data† | TBD | |
| 126–127 | Vendor-specific data† | TBD | |
| 128–166 | System-integrator-specific data† | TBD | |
| 167–255 | Open | | |

† TBD indicates that values are determined at manufacturing time and are module-dependent.

‡ These TBD values are determined and programmed by the customer (optional).



serial presence detect (continued)

Table 2. Serial Presence Detect Data for the TM4SR72EPH

| BYTE NO. | DESCRIPTION OF FUNCTION | TM4SR72EPH-10 | |
|----------|--|---|------|
| | | ITEM | DATA |
| 0 | Defines number of bytes written into serial memory during module manufacturing | 128 bytes | 80h |
| 1 | Total number of bytes of SPD memory device | 256 bytes | 08h |
| 2 | Fundamental memory type (FPM, EDO, SDRAM, . . .) | SDRAM | 04h |
| 3 | Number of row addresses on this assembly | 11 | 0Bh |
| 4 | Number of column addresses on this assembly | 9 | 09h |
| 5 | Number of module banks on this assembly | 2 banks | 02h |
| 6 | Data width of this assembly | 72 bits | 48h |
| 7 | Data width continuation | | 00h |
| 8 | Voltage interface standard of this assembly | LVTTTL | 01h |
| 9 | SDRAM cycle time at maximum supported CAS latency (CL), CL = X | t _{CK} = 10 ns | A0h |
| 10 | SDRAM access from clock at CL = X | t _{AC} = 7 ns | 70h |
| 11 | DIMM configuration type (non-parity, parity, error correcting code [ECC]) | ECC | 02h |
| 12 | Refresh rate/type | 15.6 μs/ self-refresh | 80h |
| 13 | SDRAM width, primary DRAM | x8 | 08h |
| 14 | Error-checking SDRAM data width | x8 | 08h |
| 15 | Minimum clock delay, back-to-back random column addresses | 1 CK cycle | 01h |
| 16 | Burst lengths supported | 1, 2, 4, 8 | 0Fh |
| 17 | Number of banks on each SDRAM device | 2 banks | 02h |
| 18 | CAS latencies supported | 2, 3 | 06h |
| 19 | CS latency | 0 | 01h |
| 20 | Write latency | 0 | 01h |
| 21 | SDRAM module attributes | Non-buffered/ Non-registered | 00h |
| 22 | SDRAM device attributes: general | VDD tolerance = (+10%), Burst read/write, precharge all, auto precharge | 0Eh |
| 23 | Minimum clock cycle time at CL = X – 1 | t _{CK} = 15 ns | F0h |
| 24 | Maximum data-access time from clock at CL = X – 1 | t _{AC} = 7 ns | 70h |
| 25 | Minimum clock cycle time at CL = X – 2 | N/A | 00h |
| 26 | Maximum data-access time from clock at CL = X – 2 | N/A | 00h |
| 27 | Minimum row-precharge time | t _{RP} = 20 ns | 14h |
| 28 | Minimum row-active to row-active delay | t _{RRD} = 20 ns | 14h |
| 29 | Minimum <u>RAS</u> -to- <u>CAS</u> delay | t _{RCD} = 30 ns | 1Eh |
| 30 | Minimum <u>RAS</u> pulse width | t _{RAS} = 50 ns | 32h |
| 31 | Density of each bank on module | 16M Bytes | 04h |

TM2SR72EPH 2097 152 BY 72-BIT
TM4SR72EPH 4194 304 BY 72-BIT
SYNCHRONOUS DYNAMIC RAM MODULES

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serial presence detect (continued)

Table 2. Serial Presence Detect Data for the TM4SR72EPH (Continued)

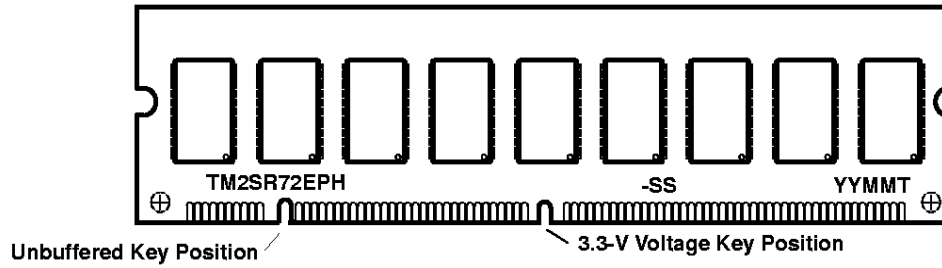
| BYTE NO. | DESCRIPTION OF FUNCTION | TM4SR72EPH-10 | |
|----------|---|-------------------------|------------|
| | | ITEM | DATA |
| 32 | Command and address signal input setup time | $t_{IS} = 2 \text{ ns}$ | 20h |
| 33 | Command and address signal input hold time | $t_{IH} = 1 \text{ ns}$ | 10h |
| 34 | Data signal input setup time | $t_{IS} = 2 \text{ ns}$ | 20h |
| 35 | Data signal input hold time | $t_{IH} = 1 \text{ ns}$ | 10h |
| 36–61 | Superset features (may be used in the future) | | |
| 62 | SPD revision | Rev. 1.2 | 12h |
| 63 | Checksum for byte 0–62 | 3 | 03h |
| 64–71 | Manufacturer's JEDEC ID code per JEP-106E | 97h | 9700...00h |
| 72 | Manufacturing location [†] | TBD | |
| 73–90 | Manufacturer's part number [†] | TBD | |
| 91 | Die revision code [†] | TBD | |
| 92 | PCB revision code [†] | TBD | |
| 93–94 | Manufacturing date [†] | TBD | |
| 95–98 | Assembly serial number [†] | TBD | |
| 99–125 | Manufacturer-specific data [†] | TBD | |
| 126–127 | Vendor-specific data [†] | TBD | |
| 128–166 | System-integrator-specific data [‡] | TBD | |
| 167–255 | Open | | |

[†] TBD indicates that values are determined at manufacturing time and are module-dependent.

[‡] These TBD values are determined and programmed by the customer (optional).



device symbolization (TM2SR72EPH)



YY = Year Code
MM = Month Code
T = Assembly Site Code
-SS = Speed Code

NOTE A: Location of symbolization may vary.

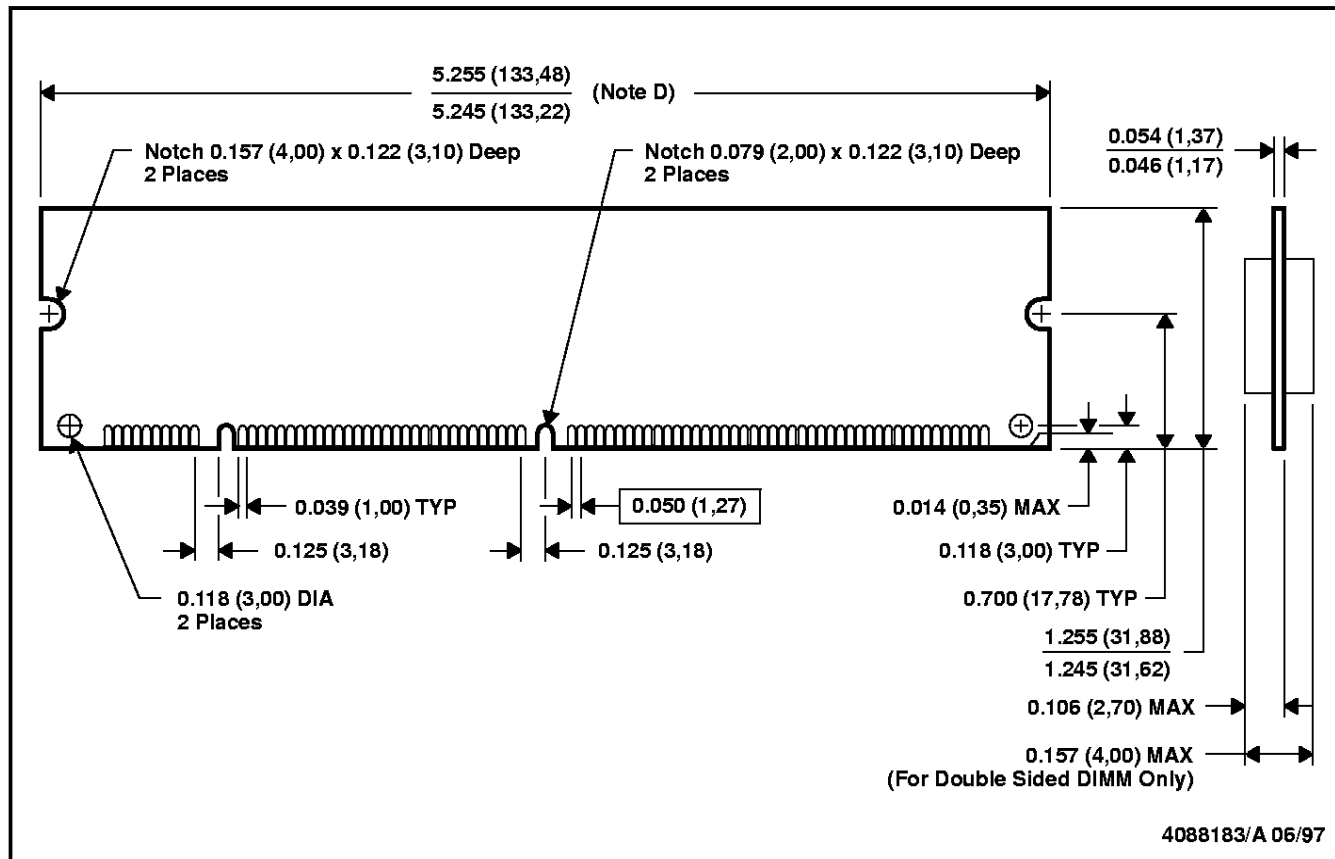
TM2SR72EPH 2097 152 BY 72-BIT
TM4SR72EPH 4194 304 BY 72-BIT
SYNCHRONOUS DYNAMIC RAM MODULES

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MECHANICAL DATA

BU (R-PDIM-N168)

DUAL IN-LINE MEMORY MODULE



4088183/A 06/97

- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MO-161
 D. Dimension includes de-panelization variations; applies between notch and tab edge.
 E. Outline may vary above notches to allow router/panelization irregularities.



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