Supertex inc.

HV87
HV88

32-Channel Serial To Parallel Converter With High Voltage Push-Pull Outputs

Ordering Information

Device	Package Options		
	44 J-Lead Quad Ceramic Chip Carrier	44 J-Lead Quad Plastic Chip Carrier	Die in waffle pack
HV87	HV8708DJ	HV8708PJ	HV8708X
HV88	HV8808DJ	HV8808PJ	HV8808X

Features

- ☐ Processed with HVCMOS® technology
- ☐ CMOS compatible outputs
- ☐ Output voltages up to 80V
- ☐ Low power level shifting
- ☐ Source/sink current minimum 20mA
- ☐ Shift register speed 8MHz
- ☐ Latched data outputs
- ☐ Forward and reverse shifting options
- ☐ Diode to V_{PP} allows efficient power recovery

Absolute Maximum Ratings[1]

Supply voltage, V_{DD}[2]		-0.5V to +15V
Output voltage, V_{PP}		-0.5V to +80V
Logic input levels[2]		-0.5V to V_{DD} +0.5V
Ground currrent[3]		1.5A
Continuous total power dissipation[4]	Ceramic	1500mW
	Plastic	1200mW
Operating temperature range	Commercial	-40°C to +85°C
	Military	-55°C to +125°C
Storage temperature range		-65°C to +150°C
Lead temperature 1.6mm (1/16 inch) from case for 10 seconds		260°C

Notes:
1. Device will survive (but operation may not be specified or guaranteed) at these extremes.
2. All voltages are referenced to GND.
3. Duty cycle is limited by the total power dissipated in the package.
4. For operation above 25°C ambient, derate linearly to 70°C at 12mW/°C.

General Description

The HV87 and HV88 are low-voltage serial to high-voltage parallel converters wtih push-pull outputs.These devices have been designed for use as drivers for AC-electroluminescent displays. They can also be used in any application requiring multiple output high-voltage current sourcing and sinking capabilities such as driving plasma panels, vacuum fluorescent displays, or large matrix LCD displays. The inputs are fully CMOS compatible.

These devices consist of a 32-bit shift register, 32 latches, and control logic to perform the polarity select and blanking of the outputs. HVout1 is connected to the first stage of the shift register through the polarity and blanking logic. Data is shifted through the shift register on the logic low to high transition of the clock. The HV87 shifts data in the clockwise direction when viewed from the top of the package and the HV88 shifts in the counterclockwise direction. A data output buffer is provided for cascading devices. This output reflects the current status of the last bit of the shift register ($HV_{OUT}32$). Operation of the shift register is not affected by the $\overline{LE}$ (latch enable), $\overline{BL}$ (blanking), or the $\overline{POL}$ (polarity) inputs. Transfer of data from the shift register to the latch occurs when the $\overline{LE}$ (latch enable) input is high. The data in the latch is stored when $\overline{LE}$ is low.

Electrical Characteristics (over recommended operating conditions unless noted)

DC Characteristics

Symbol	Parameter		Min	Max	Units	Conditions
I_{DD}	V_{DD} supply current			15	mA	$V_{DD} = V_{DD}$ max f_{CLK} = 8MHz
I_{PP}	High voltage supply current			100	µA	Outputs high
				100	µA	Outputs low
I_{DDQ}	Quiescent V_{DD} supply current			0.5	mA	All $V_{IN} = V_{SS}$ or V_{DD}
V_{OH}	High-level output	HV_{OUT}	52		V	I_O= -20mA
		Data out	10		V	I_O= -100µA
V_{OL}	Low-level output	HV_{OUT}		8	V	I_O= 20mA
		Data out		1.0	V	I_O= 100µA
I_{IH}	High-level logic input current			1	µA	$V_{IH} = V_{DD}$
I_{IL}	Low-level logic input current			-1	µA	V_{IL} = 0V

AC Characteristics (V_{DD} = 5V, T_C = 25°C)

Symbol	Parameter	Min	Max	Units	Conditions
f_{CLK}	Clock frequency		8	MHz	
t_W	Clock width high or low	62		ns	
t_{SU}	Data set-up time before clock rises	25		ns	
t_H	Data hold time after clock rises	10		ns	
t_{ON}, t_{OFF}	Time from latch enable to HV_{OUT}		500	ns	
t_{DHL}	Delay time clock to data high to low		100	ns	C_L = 15pF
t_{DLH}	Delay time clock to data low to high		100	ns	C_L = 15pF
t_{DLE}	Delay time clock to $\overline{LE}$ low to high	50		ns	
t_{WLE}	Width of $\overline{LE}$ pulse	50		ns	
t_{SLE}	$\overline{LE}$ set-up time before clock rises	50		ns	

Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{DD}	Logic supply voltage		10.8	13.2	V
V_{PP}	Output off voltage		8	75	V
V_{IH}	High-level input voltage		V_{DD} -2.0V	V_{DD}	V
V_{IL}	Low-level input voltage		0	2.0	V
f_{CLK}	Clock frequency			8	MHz
T_A	Operating free-air temperature	Commercial	-4.0	+85	°C

Note:

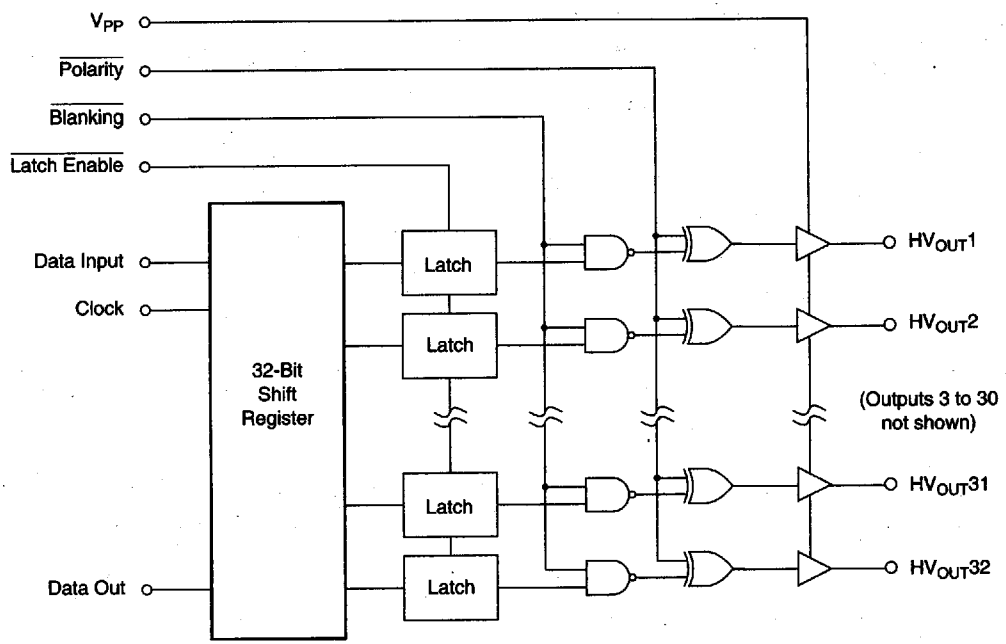
Power-up sequence should be the following:

1. Connect ground.
2. Apply V_{DD}.
3. Set all inputs (Data, CLK, Enable, etc.) to a known state.
4. Apply V_{PP}.

Power-down sequence should be the reverse of the above.

5. V_{PP} is not allowed to float during operation.
6. The V_{PP} should not drop below V_{DD} during operations.

Functional Block Diagram



Function Table

Function	Inputs					Outputs		
						Shift Reg	HV Outputs	Data Out
	Data	CLK	$\overline{LE}$	$\overline{BL}$	$\overline{POL}$	1 2...32	1 2...32	*
All on	X	X	X	L	L	* *...*	H H...H	*
All off	X	X	X	L	H	* *...*	L L...L	*
Invert mode	X	X	L	H	L	* *...*	$\overline{*}$ $\overline{*...*}$	*
Load S/R	H or L	↑	L	H	H	H or L *...*	* *...*	*
Load latches	X	H or L	↑	H	H	* *...*	* *...*	*
	X	H or L	↑	H	L	* *...*	$\overline{*}$ $\overline{*...*}$	*
Transparent latch mode	L	↑	H	H	H	L *...*	L *...*	*
	H	↑	H	H	H	H *...*	H *...*	*

Notes:
H = high level, L = low level, X = irrelevant, ↑ = low-to-high transition.
* = dependent on previous stage's state before the last CLK or last LE high.

Input and Output Equivalent Circuits

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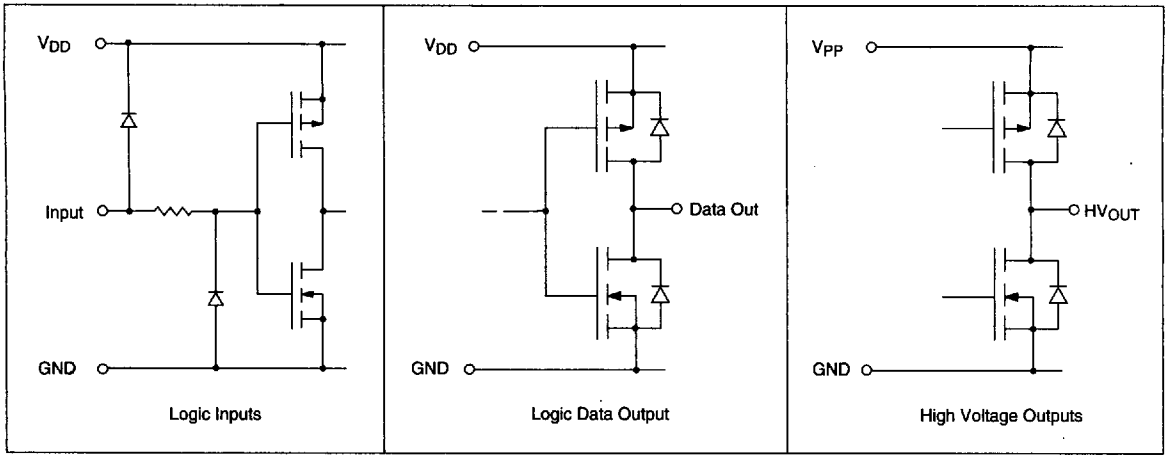
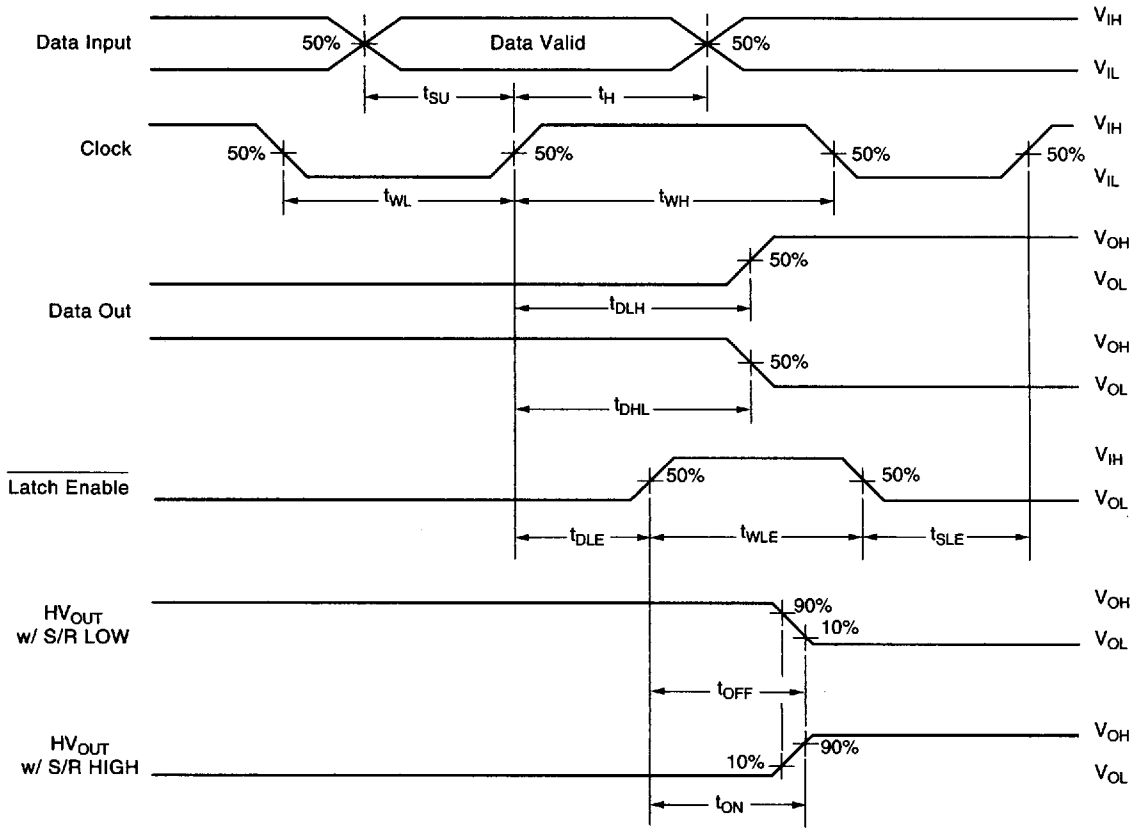


Switching Waveforms



Pin Configurations

HV87
44 Pin J-Lead Package

Pin	Function	Pin	Function
1	HV_{OUT} 17	23	GND
2	HV_{OUT} 16	24	V_{PP}
3	HV_{OUT} 15	25	V_{DD}
4	HV_{OUT} 14	26	Latch Enable
5	HV_{OUT} 13	27	Data In
6	HV_{OUT} 12	28	Blanking
7	HV_{OUT} 11	29	N/C
8	HV_{OUT} 10	30	HVout 32
9	HV_{OUT} 9	31	HV_{OUT} 31
10	HV_{OUT} 8	32	HV_{OUT} 30
11	HV_{OUT} 7	33	HV_{OUT} 29
12	HV_{OUT} 6	34	HV_{OUT} 28
13	HV_{OUT} 5	35	HV_{OUT} 27
14	HV_{OUT} 4	36	HV_{OUT} 26
15	HV_{OUT} 3	37	HV_{OUT} 25
16	HV_{OUT} 2	38	HV_{OUT} 24
17	HV_{OUT} 1	39	HV_{OUT} 23
18	Data Out	40	HV_{OUT} 22
19	N/C	41	HV_{OUT} 21
20	N/C	42	HV_{OUT} 20
21	Polarity	43	HV_{OUT} 19
22	Clock	44	HV_{OUT} 18

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1	HV_{OUT} 16	23	GND
2	HV_{OUT} 17	24	V_{PP}
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4	HV_{OUT} 19	26	Latch Enable
5	HV_{OUT} 20	27	Data In
6	HV_{OUT} 21	28	Blanking
7	HV_{OUT} 22	29	N/C
8	HV_{OUT} 23	30	HV_{OUT} 1
9	HV_{OUT} 24	31	HV_{OUT} 2
10	HV_{OUT} 25	32	HV_{OUT} 3
11	HV_{OUT} 26	33	HV_{OUT} 4
12	HV_{OUT} 27	34	HV_{OUT} 5
13	HV_{OUT} 28	35	HV_{OUT} 6
14	HV_{OUT} 29	36	HV_{OUT} 7
15	HV_{OUT} 30	37	HV_{OUT} 8
16	HV_{OUT} 31	38	HV_{OUT} 9
17	HV_{OUT} 32	39	HV_{OUT} 10
18	Data Out	40	HV_{OUT} 11
19	N/C	41	HV_{OUT} 12
20	N/C	42	HV_{OUT} 13
21	Polarity	43	HV_{OUT} 14
22	Clock	44	HV_{OUT} 15

Package Outline

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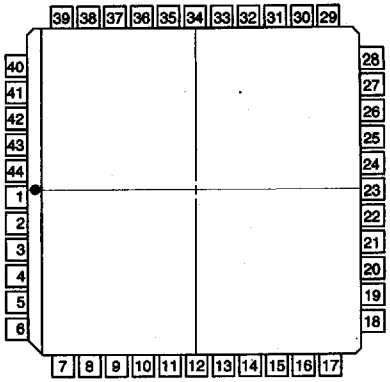

top view
44-pin J-Lead Package