

Radiation Hardened Inverting 8-Bit Parallel-Input/Serial Output Shift Register

September 1995

Features

- 3 Micron Radiation Hardened SOS CMOS
- Total Dose 200K RAD (Si)
- SEP Effective LET No Upsets: $>100 \text{ MEV-cm}^2/\text{mg}$
- Single Event Upset (SEU) Immunity $< 2 \times 10^{-9}$ Errors/Bit-Day (Typ)
- Dose Rate Survivability: $>1 \times 10^{12}$ RAD (Si)/s
- Dose Rate Upset $>10^{10}$ RAD (Si)/s 20ns Pulse
- Latch-Up Free Under Any Conditions
- Fanout (Over Temperature Range)
 - Standard Outputs - 10 LSTTL Loads
- Military Temperature Range: -55°C to $+125^\circ\text{C}$
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range: 4.5V to 5.5V
- Input Logic Levels
 - $V_{IL} = 0.3 \text{ VCC Max}$
 - $V_{IH} = 0.7 \text{ VCC Min}$
- Input Current Levels $I_i \leq 5\mu\text{A}$ at VOL, VOH

Description

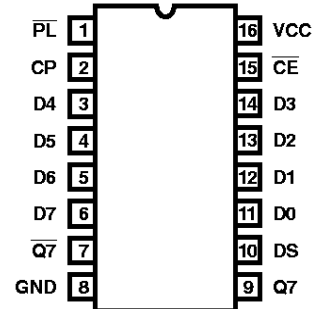
The Harris HCS165MS is a Radiation Hardened 8-Bit Parallel-In/Serial-Out Shift Register with complementary serial outputs and an asynchronous parallel load input.

The HCS165MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family.

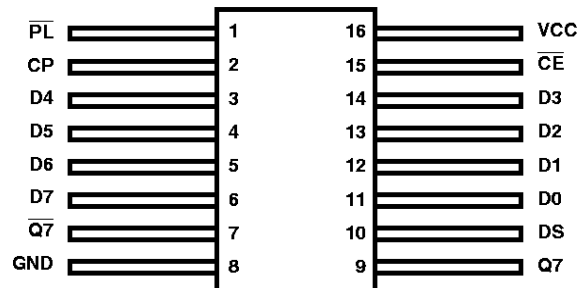
The HCS165MS is supplied in a 16 lead Ceramic flatpack (K suffix) or a SBDIP Package (D suffix).

Pinouts

16 LEAD CERAMIC DUAL-IN-LINE
METAL SEAL PACKAGE (SBDIP)
MIL-STD-1835 CDIP2-T16, LEAD FINISH C
TOP VIEW



16 LEAD CERAMIC METAL SEAL
FLATPACK PACKAGE (FLATPACK)
MIL-STD-1835 CDFF4-F16, LEAD FINISH C
TOP VIEW

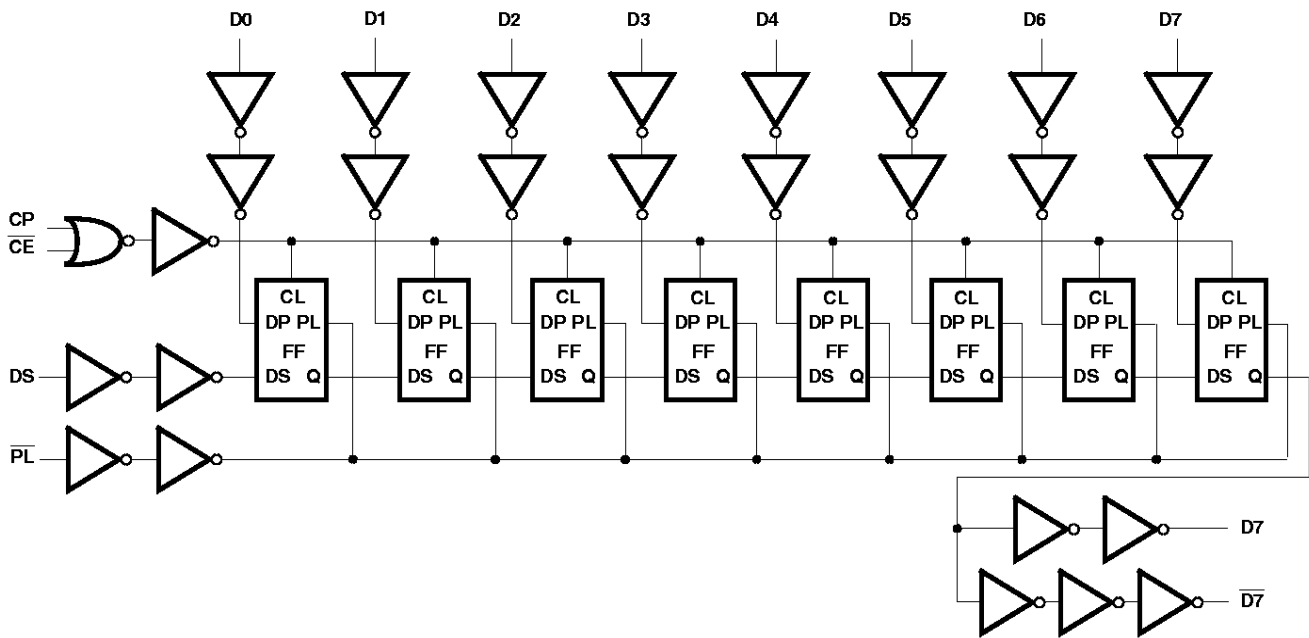


Ordering Information

PART NUMBER	TEMPERATURE RANGE	SCREENING LEVEL	PACKAGE
HCS165DMSR	-55°C to $+125^\circ\text{C}$	Harris Class S Equivalent	16 Lead SBDIP
HCS165KMSR	-55°C to $+125^\circ\text{C}$	Harris Class S Equivalent	16 Lead Ceramic Flatpack
HCS165D/Sample	$+25^\circ\text{C}$	Sample	16 Lead SBDIP
HCS165K/Sample	$+25^\circ\text{C}$	Sample	16 Lead Ceramic Flatpack
HCS165HMSR	$+25^\circ\text{C}$	Die	Die

HCS165MS

Functional Diagram



TRUTH TABLE

OPERATING MODES	INPUTS					Qn REGISTER		OUTPUTS	
	\overline{PL}	\overline{CE}	CP	DS	D0 - D7	Q0	Q1 - Q6	Q7	$\overline{Q7}$
Parallel Load	L	X	X	X	L	L	L - L	L	H
	L	X	X	X	H	H	H - H	H	L
Serial Shift	H	L	\nearrow	l	X	L	Q0 - Q5	Q6	$\overline{Q6}$
	H	L	\nearrow	h	X	H	Q0 - Q5	Q6	$\overline{Q6}$
Hold "Do Nothing"	H	H	X	X	X	Q0	Q1 - Q6	Q7	$\overline{Q7}$

H = HIGH voltage level

h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition

L = LOW voltage level

l = LOW voltage level one setup time prior to the LOW-to-High clock transition

Qn = Lower case letters indicate the state of the referenced output one set-up time prior to the LOW-to-HIGH clock transition.

X = Don't Care

\nearrow = LOW-to-HIGH clock transition.

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Absolute Maximum Ratings

Supply Voltage (VCC)	-0.5V to +7.0V
Input Voltage Range, All Inputs	-0.5V to VCC +0.5V
DC Input Current, Any One Input	±10mA
DC Drain Current, Any One Output (All Voltage Reference to the VSS Terminal)	±25mA
Storage Temperature Range (TSTG)	-65°C to +150°C
Lead Temperature (Soldering 10sec)	+265°C
Junction Temperature (TJ)	+175°C
ESD Classification	Class 1

Reliability Information

Thermal Resistance	θ_{JA}	θ_{JC}
SBDIP Package	73°C/W	24°C/W
Ceramic Flatpack Package	114°C/W	29°C/W
Maximum Package Power Dissipation at +125°C Ambient		
SBDIP Package		0.68W
Ceramic Flatpack Package		0.44W
If device power exceeds package dissipation capability, provide heat sinking or derate linearly at the following rate:		
SBDIP Package		13.7mW/°C
Ceramic Flatpack Package		8.8mW/°C

CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation..

Operating Conditions

Supply Voltage (VCC)	+4.5V to +5.5V	Input Low Voltage (VIL)	0.0V to 30% of VCC
Input Rise and Fall Times at VCC = 4.5V (TR, TF)	.500ns Max	Input High Voltage (VIH)	70% of VCC to VCC
Operating Temperature Range (TA)	-55°C to +125°C		

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUB- GROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	40	μA
			2, 3	+125°C, -55°C	-	750	μA
Output Current (Sink)	IOL	VCC = 4.5V, VIH = 4.5V, VOUT = 0.4V, VIL = 0V	1	+25°C	4.8	-	mA
			2, 3	+125°C, -55°C	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIH = 4.5V, VOUT = VCC -0.4V, VIL = 0V	1	+25°C	-4.8	-	mA
			2, 3	+125°C, -55°C	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V, VIH = 3.15V, IOL = 50μA, VIL = 1.35V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
		VCC = 5.5V, VIH = 3.85V, IOL = 50μA, VIL = 1.65V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V, VIH = 3.15V, IOH = -50μA, VIL = 1.35V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
		VCC = 5.5V, VIH = 3.85V, IOH = -50μA, VIL = 1.65V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	±0.5	μA
			2, 3	+125°C, -55°C	-	±5.0	μA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) (Note 2)	7, 8A, 8B	+25°C, +125°C, -55°C	-	-	-

NOTES:

1. All voltages reference to device GND.
2. For functional tests $VO \geq 4.0V$ is recognized as a logic "1", and $VO \leq 0.5V$ is recognized as a logic "0".

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TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB- GROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
CP or \overline{CE} to Q7 or $\overline{Q7}$	TPLH TPHL	VCC = 4.5V	9	+25°C	2	35	ns
			10, 11	+125°C, -55°C	2	41	ns
PEN to Q7 or $\overline{Q7}$	TPLH TPHL	VCC = 4.5V	9	+25°C	2	40	ns
			10, 11	+125°C, -55°C	2	46	ns
D7 to Q7	TPLH TPHL	VCC = 4.5V	9	+25°C	2	27	ns
			10, 11	+125°C, -55°C	2	31	ns
D7 to $\overline{Q7}$	TPLH TPHL	VCC = 4.5V	9	+25°C	2	29	ns
			10, 11	+125°C, -55°C	2	35	ns

NOTES:

- All voltages referenced to device GND.
- AC measurements assume $R_L = 500\Omega$, $C_L = 50pF$, Input $T_R = T_F = 3ns$, $V_{IL} = GND$, $V_{IH} = V_{CC}$.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	TEMPERATURE	LIMITS		UNITS
				MIN	MAX	
Capacitance Power Dissipation	CPD	VCC = 5.0V, VIH = 5.0V, VIL = 0.0V, f = 1MHz	+25°C	-	41	pF
			+125°C, -55°C	-	56	pF
Input Capacitance	CIN	VCC = 5.0V, VIH = 5.0V, VIL = 0.0V, f = 1MHz	+25°C	-	10	pF
			+125°C, -55°C	-	10	pF
Output Capacitance	COUT	VCC = 5.0V, VIH = 5.0V, VIL = 0.0V, f = 1MHz	+25°C	-	20	pF
			+125°C, -55°C	-	20	pF
Pulse Width Time CP, PL	TW	VCC = 4.5V, VIH = 4.5V, VIL = 0.0V	+25°C	16	-	ns
			+125°C, -55°C	24	-	ns
Setup Time DS to CP, \overline{CE} to CP, Dn to PL	TSU	VCC = 4.5V, VIH = 4.5V, VIL = 0.0V	+25°C	16	-	ns
			+125°C, -55°C	24	-	ns
Hold Time DS to CP, \overline{CE}	TH	VCC = 4.5V, VIH = 4.5V, VIL = 0.0V	+25°C	7	-	ns
			+125°C, -55°C	11	-	ns
Hold Time \overline{CE} to CP	TH	VCC = 4.5V, VIH = 4.5V, VIL = 0.0V	+25°C	0	-	ns
			+125°C, -55°C	0	-	ns
Recovery Time PL to CP	TREC	VCC = 4.5V, VIH = 4.5V, VIL = 0.0V	+25°C	20	-	ns
			+125°C, -55°C	30	-	ns
Maximum Frequency	FMAX	VCC = 4.5V, VIH = 4.5V, VIL = 0.0V	+25°C	30	-	MHz
			+125°C, -55°C	20	-	MHz
Output Transition Time	TTHL TTLH	VCC = 4.5V, VIH = 4.5V, VIL = 0.0V	+25°C	1	15	ns
			+125°C, -55°C	1	22	ns

NOTE:

- The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.

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TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMPERATURE	200K RAD LIMITS		UNITS
				MIN	MAX	
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	+25°C	-	0.75	mA
Output Current (Sink)	IOL	VCC = 4.5V, VIN = VCC or GND, VOUT = 0.4V	+25°C	4.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIN = VCC or GND, VOUT = VCC - 0.4V	+25°C	-4.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V or 5.5V, VIH = 0.70(VCC), VIL = 0.30(VCC), IOL = 50μA	+25°C	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V or 5.5V, VIH = 0.70(VCC), VIL = 0.30(VCC), IOH = -50μA	+25°C	VCC - 0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	+25°C	-	±5	μA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 0.70(VCC), VIL = 0.30(VCC), (Note 3)	+25°C	-	-	-
CP or CEN to Q7 or Q7N	TPLH TPHL	VCC = 4.5V	+25°C	2	41	ns
PEN to Q7 or Q7N	TPLH TPHL	VCC = 4.5V	+25°C	2	46	ns
D7 to Q7	TPLH TPHL	VCC = 4.5V	+25°C	2	31	ns
$\overline{D7}$ to $\overline{Q7N}$	TPLH TPHL	VCC = 4.5V	+25°C	2	35	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = VCC.
3. For functional tests VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 5. BURN-IN AND OPERATING LIFE TEST, DELTA PARAMETERS (+25°C)

PARAMETER	GROUP B SUBGROUP	DELTA LIMIT
ICC	5	12μA
IOL/IOH	5	-15% of 0 Hour

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TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test I (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test II (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Interim Test III (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11, (Note 2)
	Subgroup B-6	Sample/5005	1, 7, 9	
Group D		Sample/5005	1, 7, 9	

NOTES:

1. Alternate Group A testing in accordance with method 5005 of MIL-STD-883 may be exercised.
2. Table 5 parameters only.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE RAD	POST RAD	PRE RAD	POST RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1,9	Table 4 (Note 1)

NOTE:

1. Except FN test which will be performed 100% Go/No-Go.

TABLE 8. STATIC AND DYNAMIC BURN-IN TEST CONNECTIONS

OPEN	GROUND	1/2 VCC = 3V ± 0.5V	VCC = 6V ± 0.5V	OSCILLATOR	
				50kHz	25kHz
STATIC BURN-IN I TEST CONNECTIONS (Note 1)					
7, 9	1 - 6, 8, 10 - 15	-	16	-	-
STATIC BURN-IN II TEST CONNECTIONS (Note 1)					
7, 9	8	-	1 - 6, 10 - 16	-	-
DYNAMIC BURN-IN TEST CONNECTIONS (Note 2)					
-	3 - 6, 8, 11 - 15	7, 9	1, 16	2	10

NOTES:

1. Each pin except VCC and GND will have a resistor of 10kΩ ± 5% for static burn-in
2. Each pin except VCC and GND will have a resistor of 1kΩ ± 5% for dynamic burn-in

TABLE 9. IRRADIATION TEST CONNECTIONS

OPEN	GROUND	VCC = 5V ± 0.5V
7, 9	8	1 - 6, 10 - 16

NOTE: Each pin except VCC and GND will have a resistor of 47kΩ ± 5% for irradiation testing.
Group E, Subgroup 2, sample size is 4 dice/wafer 0 failures.

HCS165MS

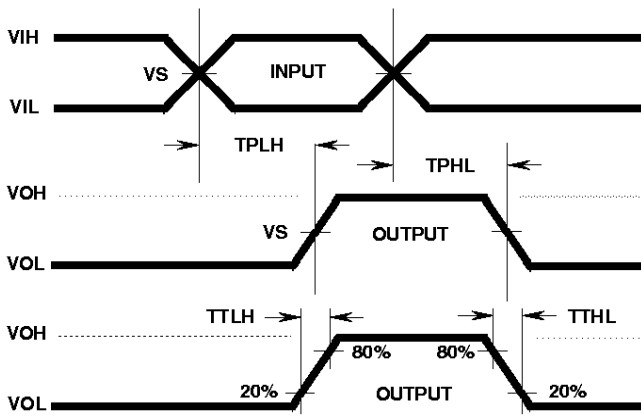
Harris Space Level Product Flow - 'MS'

Wafer Lot Acceptance (All Lots) Method 5007 (Includes SEM)	100% Interim Electrical Test 1 (T1) 100% Delta Calculation (T0-T1)
GAMMA Radiation Verification (Each Wafer) Method 1019, 4 Samples/Wafer, 0 Rejects	100% Static Burn-In 2, Condition A or B, 24 hrs. min., +125°C min., Method 1015
100% Nondestructive Bond Pull, Method 2023	100% Interim Electrical Test 2 (T2)
Sample - Wire Bond Pull Monitor, Method 2011	100% Delta Calculation (T0-T2)
Sample - Die Shear Monitor, Method 2019 or 2027	100% PDA 1, Method 5004 (Notes 1 and 2)
100% Internal Visual Inspection, Method 2010, Condition A	100% Dynamic Burn-In, Condition D, 240 hrs., +125°C or Equivalent, Method 1015
100% Temperature Cycle, Method 1010, Condition C, 10 Cycles	100% Interim Electrical Test 3 (T3)
100% Constant Acceleration, Method 2001, Condition per Method 5004	100% Delta Calculation (T0-T3)
100% PIND, Method 2020, Condition A	100% PDA 2, Method 5004 (Note 2)
100% External Visual	100% Final Electrical Test
100% Serialization	100% Fine/Gross Leak, Method 1014
100% Initial Electrical Test (T0)	100% Radiographic, Method 2012 (Note 3)
100% Static Burn-In 1, Condition A or B, 24 hrs. min., +125°C min., Method 1015	100% External Visual, Method 2009 Sample - Group A, Method 5005 (Note 4) 100% Data Package Generation (Note 5)

NOTES:

1. Failures from Interim electrical test 1 and 2 are combined for determining PDA 1.
2. Failures from subgroup 1, 7, 9 and deltas are used for calculating PDA. The maximum allowable PDA = 5% with no more than 3% of the failures from subgroup 7.
3. Radiographic (X-Ray) inspection may be performed at any point after serialization as allowed by Method 5004.
4. Alternate Group A testing may be performed as allowed by MIL-STD-883, Method 5005.
5. Data Package Contents:
 - Cover Sheet (Harris Name and/or Logo, P.O. Number, Customer Part Number, Lot Date Code, Harris Part Number, Lot Number, Quantity).
 - Wafer Lot Acceptance Report (Method 5007). Includes reproductions of SEM photos with percent of step coverage.
 - GAMMA Radiation Report. Contains Cover page, disposition, Rad Dose, Lot Number, Test Package used, Specification Numbers, Test equipment, etc. Radiation Read and Record data on file at Harris.
 - X-Ray report and film. Includes penetrometer measurements.
 - Screening, Electrical, and Group A attributes (Screening attributes begin after package seal).
 - Lot Serial Number Sheet (Good units serial number and lot number).
 - Variables Data (All Delta operations). Data is identified by serial number. Data header includes lot number and date of test.
 - The Certificate of Conformance is a part of the shipping invoice and is not part of the Data Book. The Certificate of Conformance is signed by an authorized Quality Representative.

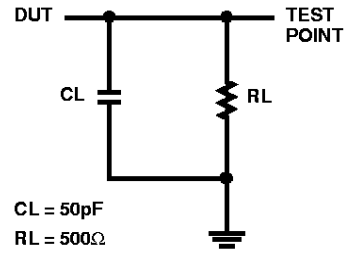
AC Timing Diagram



AC VOLTAGE LEVELS

PARAMETER	HCS	UNITS
VCC	4.50	V
V_{IH}	4.50	V
V_S	2.25	V
V_{IL}	0	V
GND	0	V

AC Load Circuit



HCS165MS

Die Characteristics

DIE DIMENSIONS:

95 x 94 mils

METALLIZATION:

Type: AlSi

Metal Thickness: $11\text{k}\text{\AA} \pm 1\text{k}\text{\AA}$

GLASSIVATION:

Type: SiO_2

Thickness: $13\text{k}\text{\AA} \pm 2.6\text{k}\text{\AA}$

WORST CASE CURRENT DENSITY:

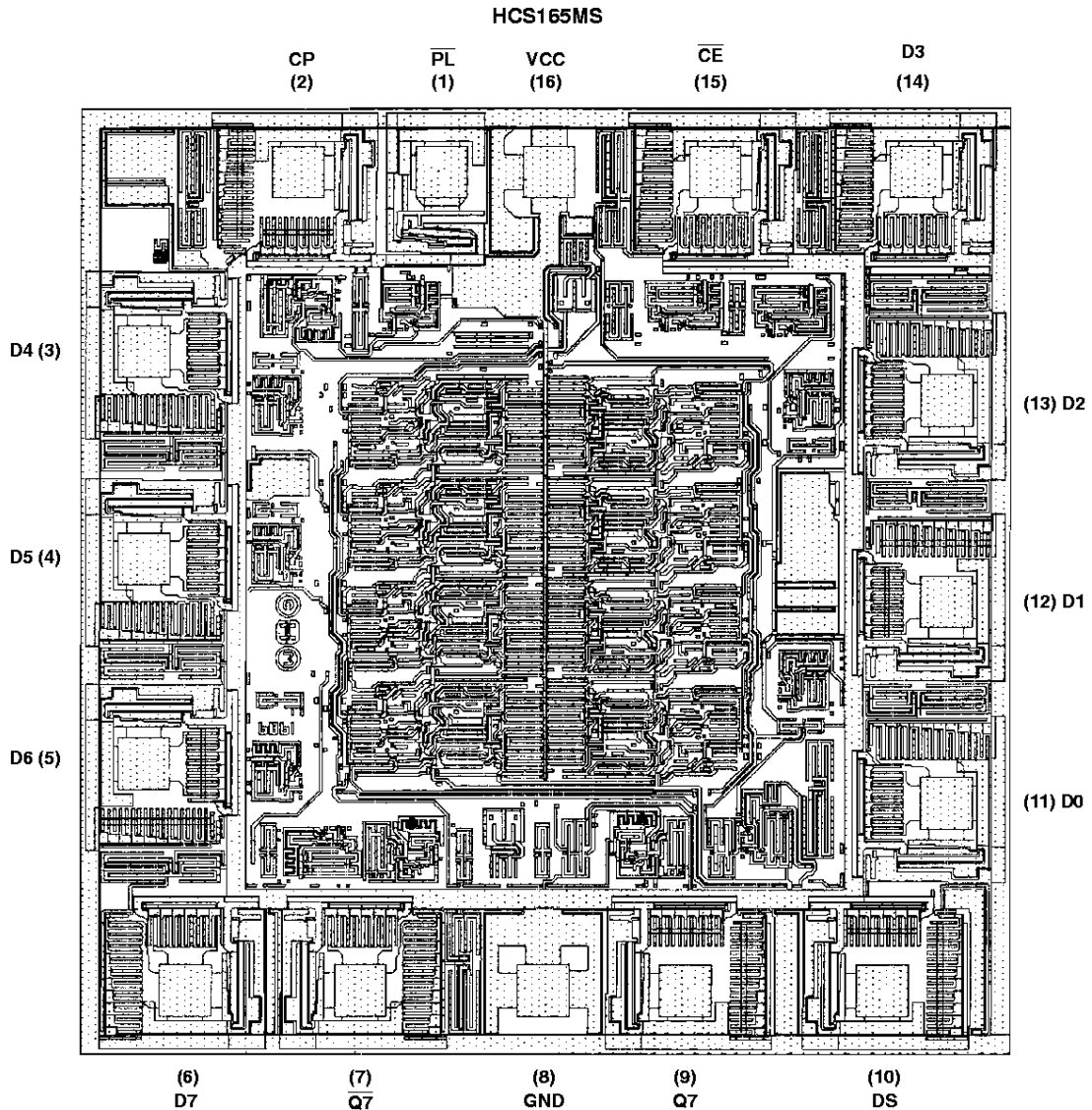
$< 2.0 \times 10^5 \text{A/cm}^2$

BOND PAD SIZE:

$100\mu\text{m} \times 100\mu\text{m}$

4 x 4 mils

Metallization Mask Layout



NOTE: The die diagram is a generic plot from a similar HCS device. It is intended to indicate approximate die size and bond pad location. The mask series for the HCS165 is TA14385A.