VIA BCM® Bus Converter

BCM4914xD1E5135yzz

Fixed-Ratio DC-DC Converter

Features & Benefits

- Up to 35 A continuous output current
- Fixed transformation ratio(K) of 1/8
- 695 W/in^3 power density
- 97.6% peak efficiency
- 2121 Vdc isolation
- Built-in EMI filtering and In-rush limiting circuit
- Suitable for hot swap applications
- Parallel operation for multi-kW arrays
- OV, OC, UV, short circuit and thermal protection
- 4914 package
- High MTBF
- Thermally enhanced VIA™ package
- PMBus™ management interface

Typical Applications

- 380 DC Power Distribution
- Green Buildings and Microgrids
- Information and Communication Technology (ICT) Equipment
- High End Computing Systems
- Automated Test Equipment
- Industrial Systems
- High Density Energy Systems
- Transportation

Product Description

The VIA BCM is a high efficiency Bus Converter, operating from a 260 to 410 V_{DC} primary bus to deliver an isolated 32.5 to 51.3 V_{DC} unregulated, Safety Extra Low Voltage (SELV) secondary output.

This unique ultra-low profile module incorporates DC-DC conversion, integrated filtering, transient surge protection and PMBus™ commands and controls in a chassis or PCB mount form factor.

The VIA BCM offers low noise, fast transient response and industry leading efficiency and power density. A secondary referenced PMBus™ compatible telemetry and control interface provides access to the VIA BCM's internal controller configuration, fault monitoring, and other telemetry functions.

Leveraging the thermal and density benefits of Vicor's VIA packaging technology, the VIA BCM module offers flexible thermal management options with very low top and bottom side thermal impedances.

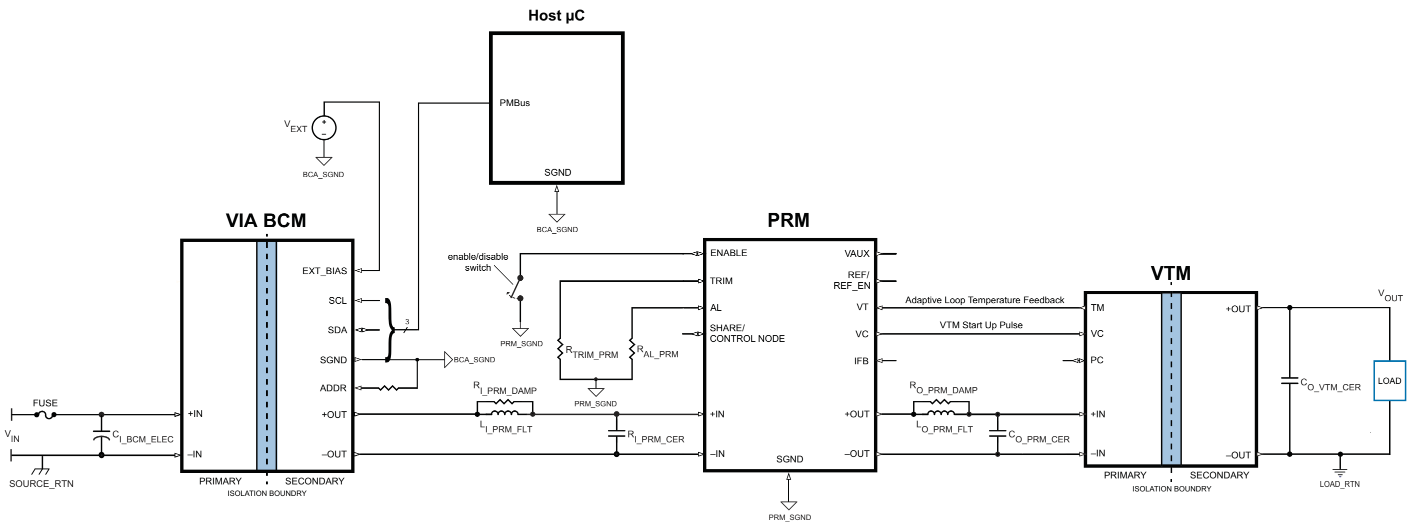
When combined with downstream Vicor DC-DC conversion components and regulators, the VIA BCM allows the Power Design Engineer to employ a simple, low-profile design which will differentiate his end system without compromising on cost or performance metrics.

Size:
4.91 x 1.40 x 0.37 in
124.77 x 35.54 x 9.30 mm

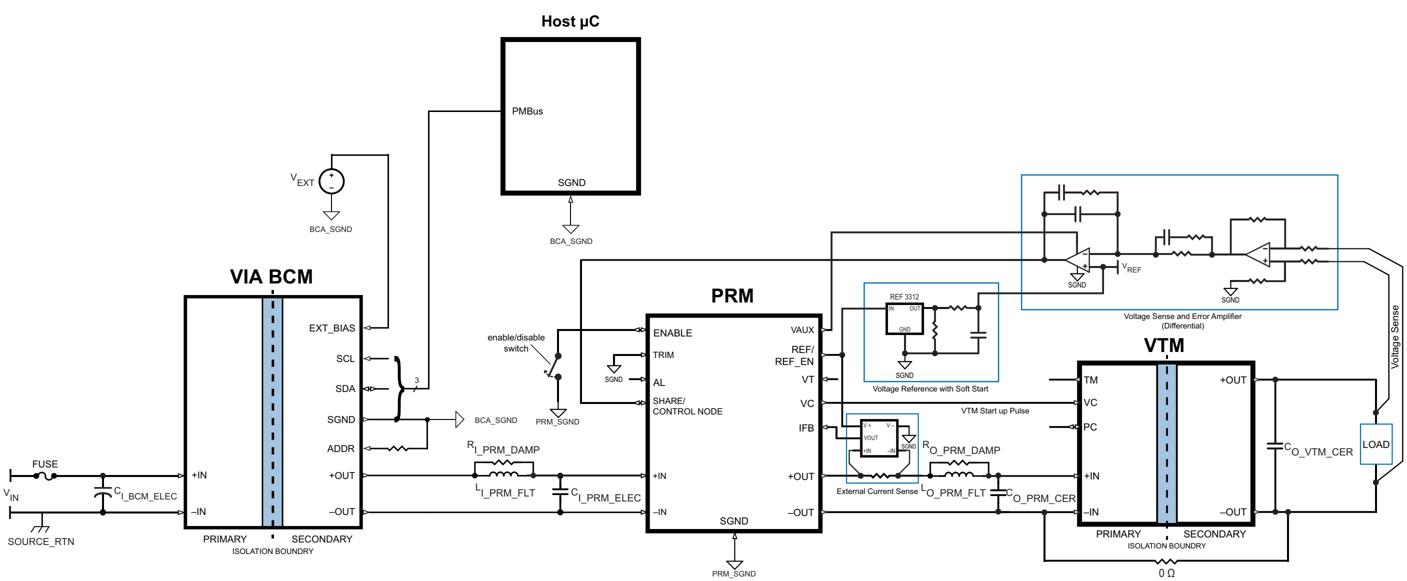
Part Ordering Information

Product Function			Package Length		Package Width		Package Type	Input Voltage		Range Ratio	Output Voltage (Range)		Max Output Current		Product Grade	Option Field	
B	C	M	4	9	1	4	x	D	1	E	5	1	3	5	y	z	z
BCM = Bus Converter Module			Length in Inches x 10		Width in Inches x 10		B = Board VIA V = Chassis VIA	Internal Reference							C = -20 to 100°C T = -40 to 100°C	02 = Chassis/PMBus 06 = Short Pin/PMBus 10 = Long Pin/PMBus	

Typical Application

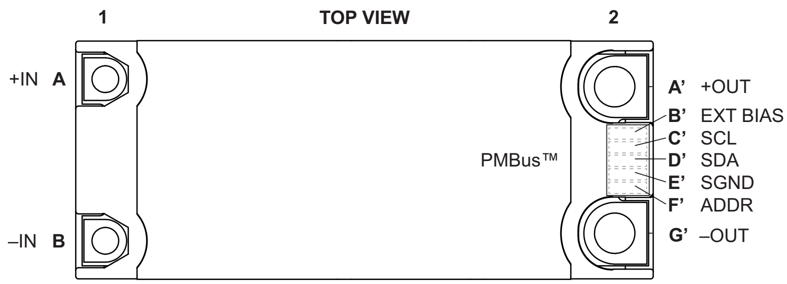


VIA BCM BCM4914xD1E5135yzz + PRM + VTM, Adaptive Loop Configuration

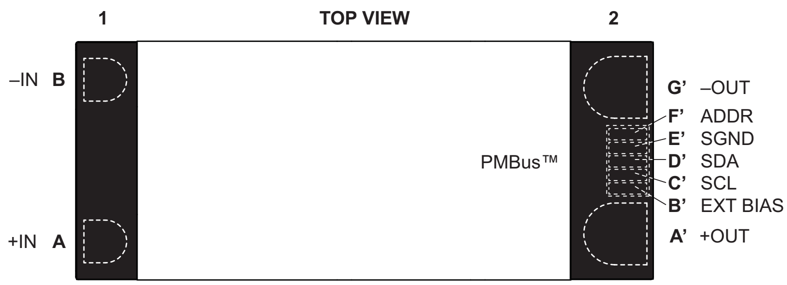


BCM4914xD1E5135yzz + PRM + VTM, Remote Sense Configuration

Pin Configuration



4914 VIA BCM - Chassis Mount



4914 VIA BCM - PCB Mount

Pin Descriptions

Pin Number	Signal Name	Type	Function
A1	+IN	INPUT POWER	Positive input power terminal
B1	–IN	INPUT POWER RETURN	Negative input power terminal
A'2	+OUT	OUTPUT POWER	Positive output power terminal
B'2	EXT BIAS	INPUT	5 V Unregulated supply input
C'2	SCL	INPUT	I^2C Clock, PMBus Compatible
D'2	SDA	INPUT/OUTPUT	I^2C Data, PMBus Compatible
E'2	SGND	POWER	Signal Ground
F'2	ADDR	INPUT	Address assignment - Resistor based
G'2	–OUT	OUTPUT POWER RETURN	Negative output power terminal

Absolute Maximum Ratings

The absolute maximum ratings below are stress ratings only. Operation at or beyond these maximum ratings can cause permanent damage to the device.

Parameter	Comments	Min	Max	Unit
+IN to –IN		-1	450	V
+OUT to –OUT		-1	60	V
EXT BIAS to SGND		-0.3	10	V
			0.15	A
SCL to SGND		-0.3	5.5	V
SDA to SGND		-0.3	5.5	V
ADDR to SGND		-0.3	3.6	V
Dielectric Withstand*	See note below			
Input-Case	Basic Insulation	2121		Vdc
Input-Output	Reinforced Insulation	2121		Vdc
Output-Case	Functional Insulation	707		Vdc

* Please see Dielectric Withstand section.

Electrical Specifications

Specifications apply over all line and load conditions, unless otherwise noted; **Boldface** specifications apply over the temperature range of -40°C ≤ T_{CASE} ≤ 100°C (T-Grade); All other specifications are at T_{CASE} = 20°C unless otherwise noted.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Powertrain						
Input voltage range, continuous	V_{IN_DC}		**260**		**410**	V
Input voltage range, transient	V_{IN_TRANS}		**260**		**410**	V
V_{IN} µController Active	$V_{\mu C\_ACTIVE}$	V_{IN} voltage where µC is initialized			120	V
Quiescent current	I_Q	Disabled, V_{IN} = 400 V		2		mA
		T_{CASE} ≤ 100°C			4	
No load power dissipation	P_{NL}	V_{IN} = 400 V, T_{CASE} = 20°C		10.5	17	W
		V_{IN} = 400 V	**6**		**21**	
		V_{IN} = 260 V to 410 V, T_{CASE} = 20°C			18	
		V_{IN} = 260 V to 410 V			**22**	
Inrush current peak - EN	$I_{INR\_P\_EN}$	V_{IN} = 410 V, C_{OUT} = 56 µF, R_{LOAD} = 25% of full load current, Application of Enable		6		A
		T_{CASE} ≤ 100°C			**12**	
Inrush current peak - V_{IN}	$I_{INR\_P\_VIN}$	V_{IN} = 410 V, C_{OUT} = 56 µF, R_{LOAD} = 25% of full load current, Application of V_{IN}		7		
		T_{CASE} ≤ 100°C			**13**	
DC input current	I_{IN_DC}	At P_{OUT}= 1750 W, T_{CASE} ≤ 70°C			4.5	A
Transformation ratio	K	K = V_{OUT}/V_{IN}, at no load		1/8		V/V
Output power (continuous)	P_{OUT_DC}	See specified electrical and thermal operating area			1750	W
Output power (pulsed)	P_{OUT_PULSE}	10 ms pulse, 25% Duty cycle			2000	W
Output current (continuous)	I_{OUT_DC}	See specified electrical and thermal operating area			35	A
Output current (pulsed)	I_{OUT_PULSE}	10 ms pulse, 25% Duty cycle			40	A
Efficiency (ambient)	η_{AMB}	V_{IN} = 400 V, I_{OUT} = 35 A	96.5	97.2		%
		V_{IN} = 260 V to 410 V, I_{OUT} = 35 A	95.3			
		V_{IN} = 400 V, I_{OUT} = 17.5 A	96.8	97.6		
Efficiency (hot)	η_{HOT}	V_{IN} = 400 V, I_{OUT} = 35 A, T_{CASE} = 70°C	95.7	96.2		%
Efficiency (over load range)	$\eta_{20\%}$	7 A < I_{OUT} < 35 A, T_{CASE} ≤ 70°C	94.5			%
Output resistance	R_{OUT_COLD}	V_{IN} = 400 V, I_{OUT} = 35 A, T_{CASE} = -40°C	20	24	28	mΩ
	R_{OUT_AMB}	V_{IN} = 400 V, I_{OUT} = 35 A	20	25.5	31	
	R_{OUT_HOT}	V_{IN} = 400 V, I_{OUT} = 35 A, T_{CASE} = 70°C	32	38	42	
Switching frequency	F_{SW}	Frequency of the Output Voltage Ripple = 2x F_{SW}	**1.05**	1.10	**1.14**	MHz
Output voltage ripple	V_{OUT_PP}	C_{OUT} = 0 F, I_{OUT} = 35 A, V_{IN} = 400 V, 20 MHz BW		250		mV
		T_{CASE} ≤ 100°C			550	
Effective Output capacitance (internal)	C_{OUT_INT}	Effective value at 50 V_{OUT}		37.6		µF
Effective Output capacitance (external)	C_{OUT_EXT}	Excessive capacitance may drive module into SC protection	**0**		**56**	µF
Array Maximum external output capacitance	C_{OUT_AEXT}	C_{OUT_AEXT} Max = N * 0.5*C_{OUT_EXT} Max				

Electrical Specifications (Cont.)

Specifications apply over all line and load conditions, unless otherwise noted; **Boldface** specifications apply over the temperature range of -40°C ≤ T_{CASE} ≤ 100°C (T-Grade); All other specifications are at T_{CASE} = 20°C unless otherwise noted

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Powertrain Protection						
Auto Restart Time	$t_{AUTO\_RESTART}$	Startup into a persistent fault condition. Non-Latching fault detection given $V_{IN} > V_{IN\_UVLO+}$, Module will ignore attempts to re-enable during time off	**292.5**		**357.5**	ms
Input overvoltage lockout threshold	V_{IN_OVLO+}		430	440	450	V
Input overvoltage recovery threshold	V_{IN_OVLO-}		420	430	440	V
Input overvoltage lockout hysteresis	$V_{IN\_OVLO\_HYST}$			10		V
Overvoltage lockout response time	t_{OVLO}			10		µs
Soft-Start time	$t_{SOFT\text{-}START}$	From powertrain active Fast Current limit protection disabled during Soft-Start		1		ms
Output overcurrent trip threshold	I_{OCP}		**37.5**	47	**59**	A
Overcurrent Response Time Constant	t_{OCP}	Effective internal RC filter		3.6		ms
Short circuit protection trip threshold	I_{SCP}		**52**			A
Short circuit protection response time	t_{SCP}			1		µs
Overtemperature shutdown threshold	t_{OTP}	Temperature sensor located inside controller IC (Internal Temperature)	125			°C
Powertrain Supervisory Limits						
Input overvoltage lockout threshold	V_{IN_OVLO+}		**420**	436	**450**	V
Input overvoltage recovery threshold	V_{IN_OVLO-}		**405**	426	**440**	V
Input overvoltage lockout hysteresis	$V_{IN\_OVLO\_HYST}$			10		V
Overvoltage lockout response time	t_{OVLO}			100		µs
Input undervoltage lockout threshold	V_{IN_UVLO-}		**200**	226	**250**	V
Input undervoltage recovery threshold	V_{IN_UVLO+}		**225**	244	**259**	V
Input undervoltage lockout hysteresis	$V_{IN\_UVLO\_HYST}$			15		V
Undervoltage lockout response time	t_{UVLO}			100		µs
Undervoltage startup delay	t_{UVLO+_DELAY}	From $V_{IN} = V_{IN\_UVLO+}$ to powertrain active, EN floating, (i.e One time Startup delay from application of V_{IN} to V_{OUT})		20		ms
Output Overcurrent Trip Threshold	I_{OCP}		42.5	45	47.5	A
Overcurrent Response Time Constant	t_{OCP}			2		ms
Overtemperature shutdown threshold	t_{OTP}	Temperature sensor located inside controller IC (Internal Temperature)	**125**			°C
Undertemperature shutdown threshold	t_{UTP}	Temperature sensor located inside controller IC (Internal Temperature)			-45	°C
Undertemperature restart time	$t_{UTP\_RESTART}$	Startup into a persistent fault condition. Non-Latching fault detection given $V_{IN} > V_{IN\_UVLO+}$		3		s

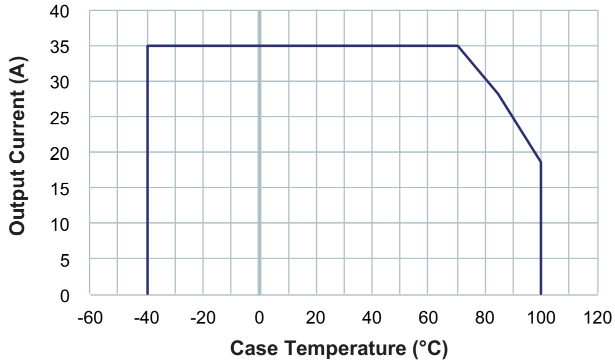


Figure 1 — *Specified thermal operating area*

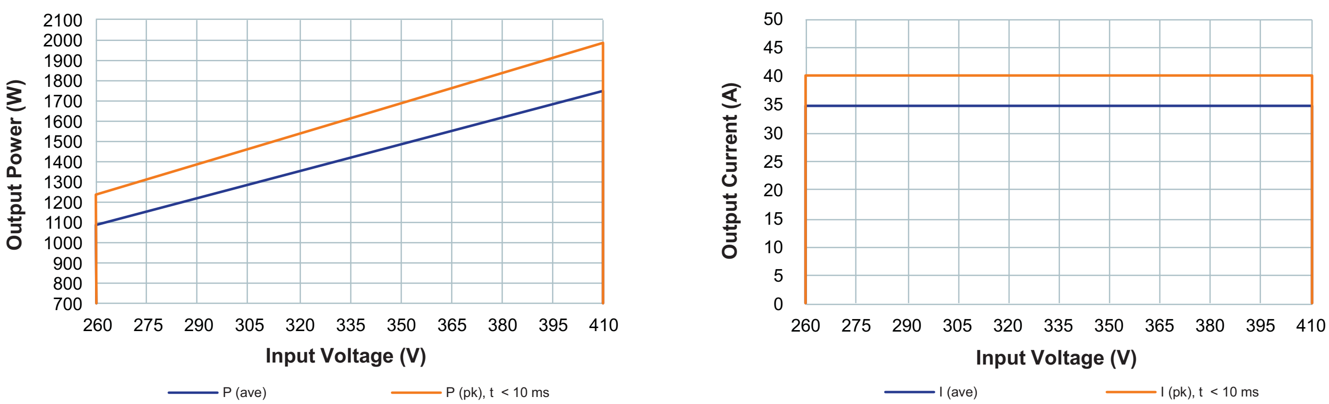


Figure 2 — *Specified electrical operating area using rated R_{OUT_HOT}*

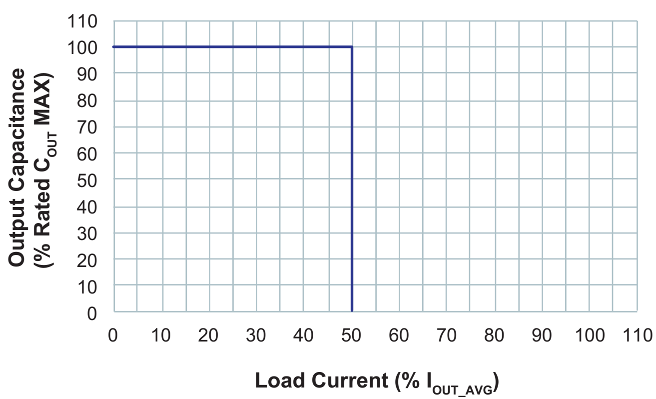


Figure 3 — *Specified Primary start-up into load current and external capacitance*

Reported Characteristics

Specifications apply over all line and load conditions, unless otherwise noted; **Boldface** specifications apply over the temperature range of -40°C ≤ T_{CASE} ≤ 100°C (T-Grade); All other specifications are at T_{CASE} = 20°C unless otherwise noted

Monitored Telemetry

• The VIA BCM communication version is not intended to be used without a external µC.

ATTRIBUTE	INTERNAL µC PMBus™ READ COMMAND	ACCURACY (RATED RANGE)	FUNCTIONAL REPORTING RANGE	UPDATE RATE	REPORTED UNITS
Input voltage	(88h) READ_VIN	± 5% (LL - HL)	130 V to 450 V	100 µs	$V_{ACTUAL} = V_{REPORTED} \times 10^{-1}$
Input current	(89h) READ_IIN	± 5% (10 - 133% of FL)	- 0.85 A to 5.9 A	100 µs	$I_{ACTUAL} = I_{REPORTED} \times 10^{-3}$
Output voltage[1]	(8Bh) READ_VOUT	± 5% (LL - HL)	16.25 V to 56.25 V	100 µs	$V_{ACTUAL} = V_{REPORTED} \times 10^{-1}$
Output current	(8Ch) READ_IOUT	± 5% (10 - 133% of FL)	- 7 A to 47.5 A	100 µs	$I_{ACTUAL} = I_{REPORTED} \times 10^{-2}$
Output resistance	(D4h) READ_ROUT	± 5% (50 - 100% of FL)	10 µΩ to 40 µΩ	100 ms	$R_{ACTUAL} = R_{REPORTED} \times 10^{-5}$
Temperature[2]	(8Dh) READ_TEMPERATURE_1	± 7°C (Full Range)	- 55°C to 130°C	100 ms	$T_{ACTUAL} = T_{REPORTED}$

[1] Default READ Output Voltage returned when unit is disabled = -300 V.
[2] Default READ Temperature returned when unit is disabled = -273°C.

Variable Parameter

• Factory setting of all below Thresholds and Warning limits are 100% of listed protection values.
• Variables can be written only when module is disabled either EN pulled low or $V_{IN} < V_{IN\_UVLO-}$.
• Module must remain in a disabled mode for 3 ms after any changes to the below variables allowing ample time to commit changes to EEPROM.

ATTRIBUTE	INTERNAL µC PMBus™ COMMAND [3]	CONDITIONS / NOTES	ACCURACY (RATED RANGE)	FUNCTIONAL REPORTING RANGE	DEFAULT VALUE
Input / Output Overvoltage Protection Limit	(55h) VIN_OV_FAULT_LIMIT	V_{IN_OVLO-} is automatically 3% lower than this set point	± 5% (LL - HL)	130 V to 435 V	100%
Input / Output Overvoltage Warning Limit	(57h) VIN_OV_WARN_LIMIT		± 5% (LL - HL)	130 V to 435 V	100%
Input / Output Undervoltage Protection Limit	(D7h) DISABLE_FAULTS	Can only be disabled to a preset default value	± 5% (LL - HL)	130 V or 260 V	100%
Input Overcurrent Protection Limit	(5Bh) IIN_OC_FAULT_LIMIT		± 5% (10 - 133% of FL)	0 to 5.625 A	100%
Input Overcurrent Warning Limit	(5Dh) IIN_OC_WARN_LIMIT		± 5% (10 - 133% of FL)	0 to 5.625 A	100%
Overtemperature Protection Limit	(4Fh) OT_FAULT_LIMIT	Internal Temperature	± 7°C (Full Range)	0 to 125°C	100%
Overtemperature Warning Limit	(51h) OT_WARN_LIMIT	Internal Temperature	± 7°C (Full Range)	0 to 125°C	100%
Turn on Delay	(60h) TON_DELAY	Additional time delay to the Undervoltage Startup Delay	± 50 µs	0 to 100 ms	0 ms

[3] Refer to internal µC datasheet for complete list of supported commands.

Signal Characteristics

Specifications apply over all line and load conditions, unless otherwise noted; **Boldface** specifications apply over the temperature range of -40°C ≤ T_{CASE} ≤ 100°C (T-Grade); All other specifications are at T_{CASE} = 20°C unless otherwise noted

EXT. BIAS (VDDB) Pin

- Unregulated supply power input, required to power the circuitry internal to the VIA BCM adapter for communication signals such as SCL, SDA, ADDR etc
- Apply precise 5 V to this pin.

SIGNAL TYPE	STATE	ATTRIBUTE	SYMBOL	CONDITIONS / NOTES	MIN	TYP	MAX	UNIT
POWER INPUT	Regular Operation	VDDB Voltage	V_{VDDB}		4.5	5	9	V
		VDDB Current consumption	I_{VDDB}				50	mA
	Startup	Inrush Current Peak	I_{VDDB_INR}	V_{VDDB} Slew Rate = 1 V/µs		3.5		A
		Turn on time	t_{VDDB_ON}	From V_{VDDB_MIN} to PMBus active		1.5		ms

SGND Pin

- This pin is power supply return pin for Ext. Bias (VDDB) pin.
- All input and output signals (SCL, SDA, ADDR) are referenced to SGND pin.

Address (ADDR) Pin

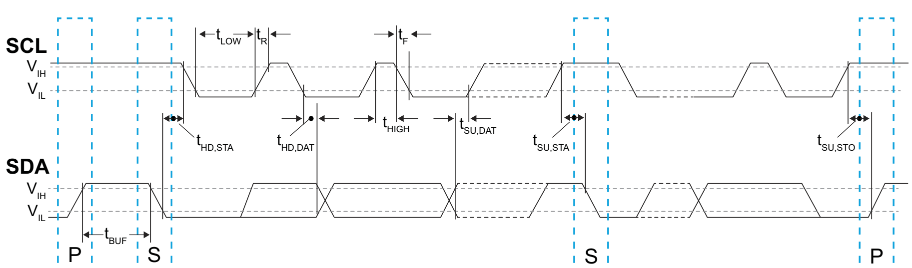
- This pin programs only a Fixed and Persistent slave address for VIA BCM Adapter.
- This pin programs the address using a resistor between ADDR pin and signal ground.
- The address is sampled during startup and is used until power is reset.
- This pin has 10 kΩ pullup resistor internally between ADDR pin and internal VDD.
- 16 addresses are available. Relative to nominal value of internal VDD (V_{VDD_NOM} = 3.3 V), a 206.25 mV range per address.

SIGNAL TYPE	STATE	ATTRIBUTE	SYMBOL	CONDITIONS / NOTES	MIN	TYP	MAX	UNIT
MULTI–LEVEL INPUT	Regular Operation	ADDR Input Voltage	V_{SADDR}	See address section	0		3.3	V
		ADDR leakage current	I_{SADDR}	Leakage current			1	µA
	Startup	ADDR registration time	t_{SADDR}	From $V_{VDD\_IN\_MIN}$		1		ms

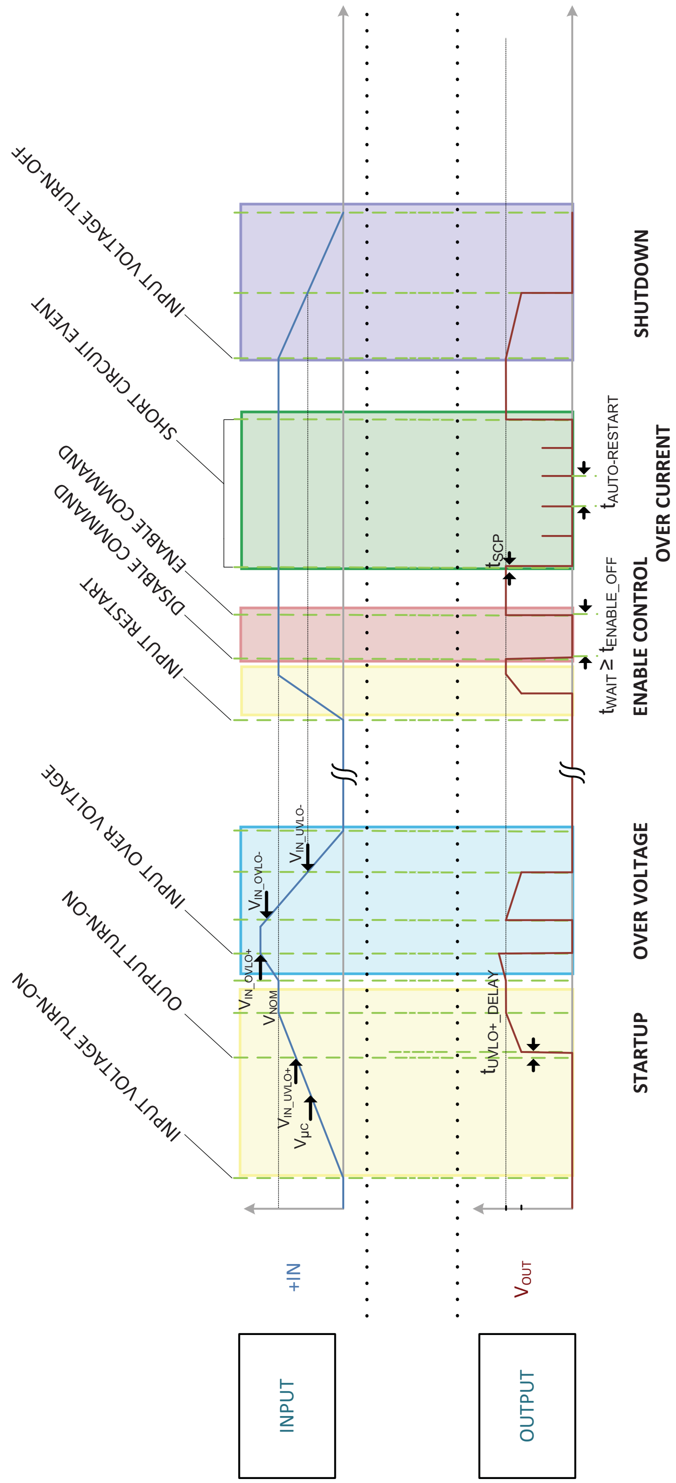
Serial Clock input (SCL) AND Serial Data (SDA) Pins

- High–power SMBus specification and SMBus physical layer compatible. Note that optional SMBALERT# is signal not supported.
- PMBus™ command compatible.
- The internal µC requires the use of a flip–flop to drive SSTOP. See system diagram section for more details.

SIGNAL TYPE	STATE	ATTRIBUTE	SYMBOL	CONDITIONS / NOTES	MIN	TYP	MAX	UNIT
DIGITAL INPUT/OUTPUT	Regular Operation	**Electrical Parameters**						
		Input Voltage Threshold	V_{IH}	V_{VDD_IN} = 3.3 V	2.1			V
			V_{IL}	V_{VDD_IN} = 3.3 V			0.8	V
		Output Voltage Threshold	V_{OH}	V_{VDD_IN} = 3.3 V	3			V
			V_{OL}	V_{VDD_IN} = 3.3 V			0.4	V
		Leakage current	$I_{LEAK-PIN}$	Unpowered device			10	µA
		Signal Sink Current	I_{LOAD}	V_{OL} = 0.4 V	4			mA
		Signal Capacitive Load	C_I	Total capacitive load of one device pin			10	pF
		Signal Noise Immunity	V_{NOISE_PP}	10 MHz to 100 MHz	300			mV
		Timing Parameters						
		Operating Frequency	F_{SMB}	Idle state = 0 Hz	10		400	KHz
		Free time between Stop and Start Condition	t_{BUF}		1.3			µs
		Hold time after Start or Repeated Start condition	$t_{HD:STA}$	First clock is generated after this hold time	0.6			µs
		Repeat Start Condition Setup time	$t_{SU:STA}$		0.6			µs
		Stop Condition setup time	$t_{SU:STO}$		0.6			µs
		Data Hold time	$t_{HD:DAT}$		300			ns
		Data Setup time	$t_{SU:DAT}$		100			ns
		Clock low time out	$t_{TIMEOUT}$		25		35	ms
		Clock low period	t_{LOW}		1.3			µs
		Clock high period	t_{HIGH}		0.6		50	µs
		Cumulative clock low extend time	$t_{LOW:SEXT}$				25	ms
		Clock or Data Fall time	t_F	Measured from (V_{IL_MAX} − 0.15) to (V_{IH_MIN} + 0.15)	20		300	ns
		Clock or Data Rise time	t_R	0.9 • $V_{VDD\_IN\_MAX}$ to (V_{IL_MAX} − 0.15)	20		300	ns



VIA BCM Bus Converter Timing diagram



Application Characteristics

Product is mounted and temperature controlled VIA top side cold plate, unless otherwise noted. See associated figures for general trend data.

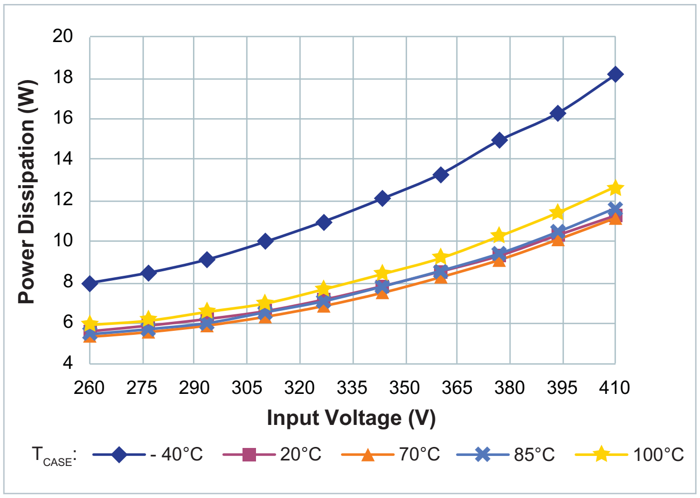


Figure 4 — *No load power dissipation vs. V_{IN}*

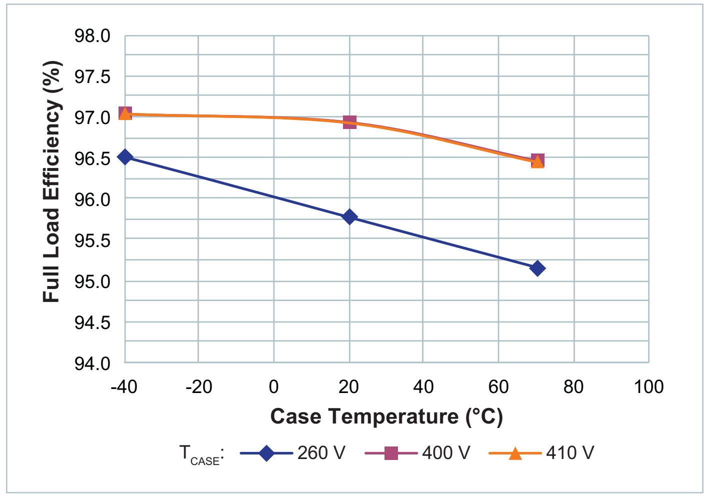


Figure 5 — *Full load efficiency vs. temperature; V_{IN}*

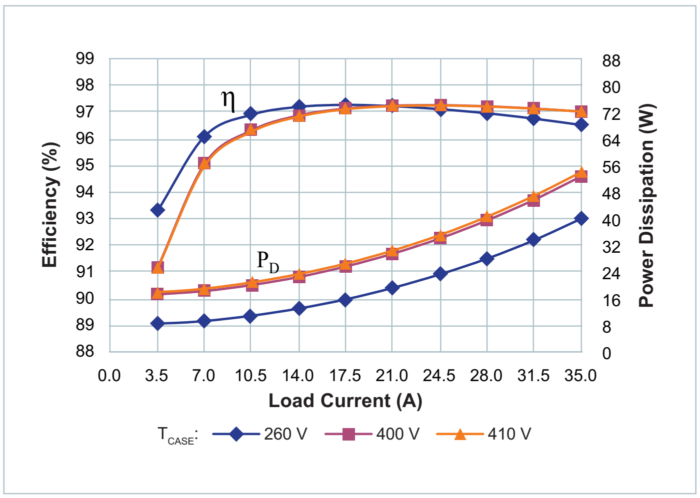


Figure 6 — *Efficiency and power dissipation at T_{CASE} = -40°C*

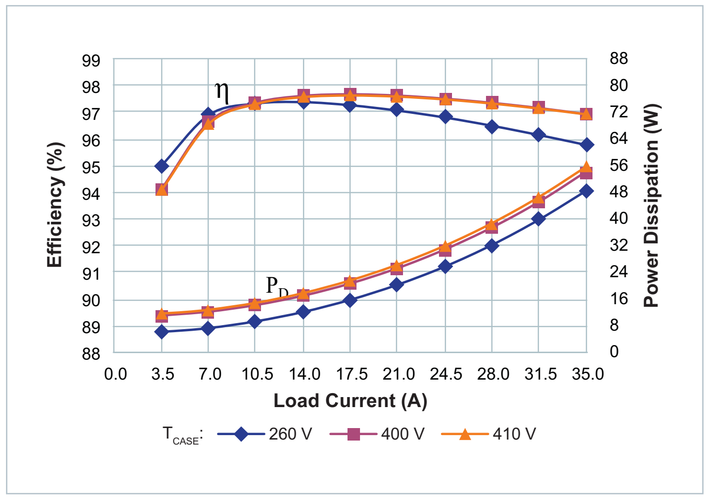


Figure 7 — *Efficiency and power dissipation at T_{CASE} = 20°C*

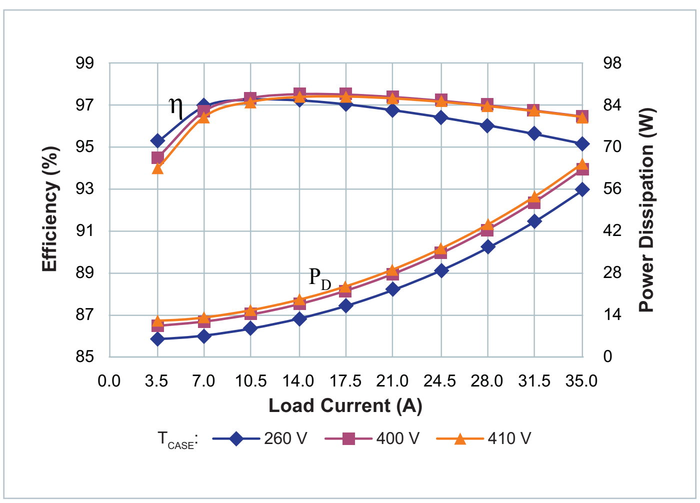


Figure 8 — *Efficiency and power dissipation at T_{CASE} = 70°C*

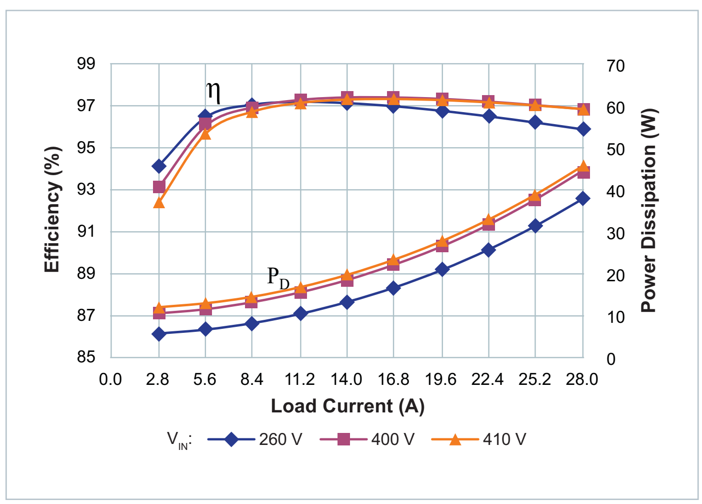


Figure 9 — *Efficiency and power dissipation at T_{CASE} = 85°C*

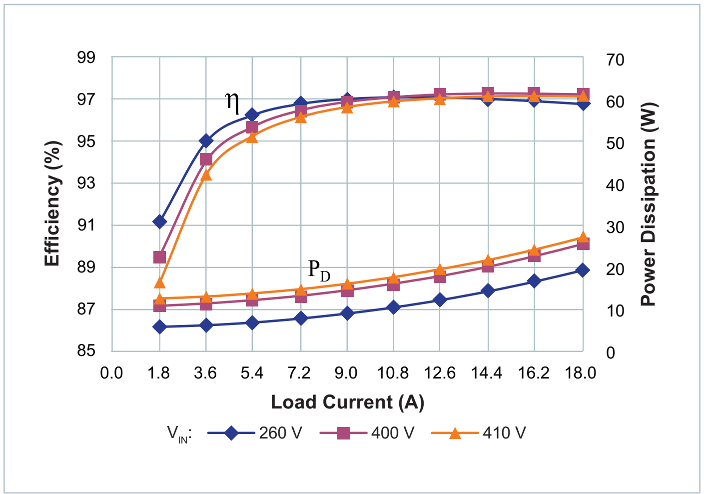


Figure 10 — *Efficiency and power dissipation at T_{CASE} = 100°C*

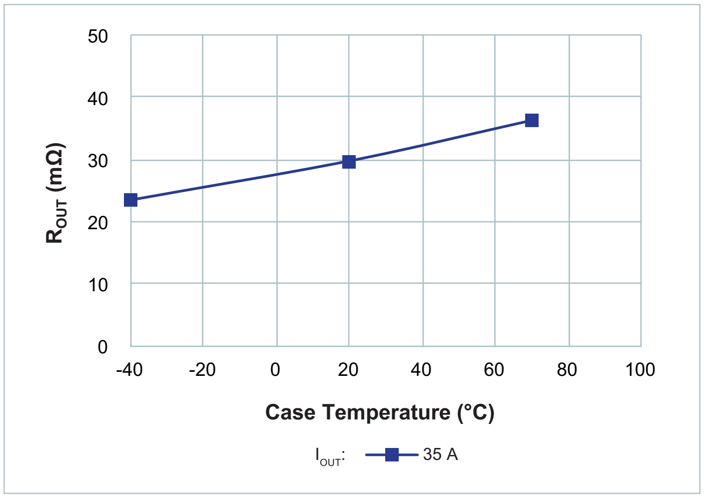


Figure 11 — *R_{OUT} vs. temperature; Nominal V_{IN}*

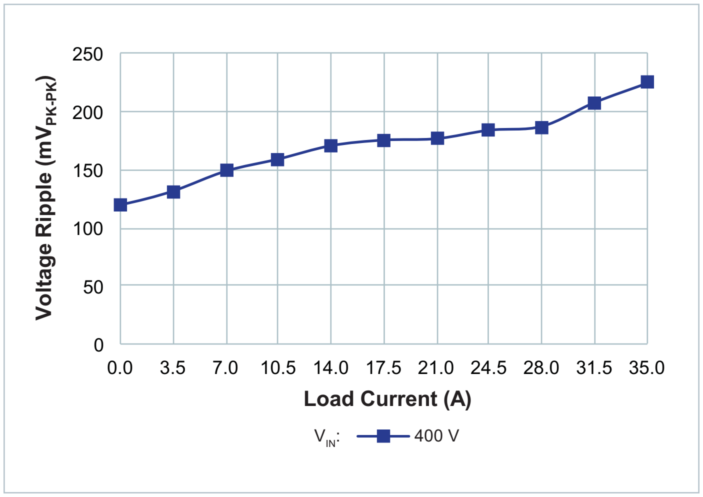


Figure 12 — *V_{RIPPLE} vs. I_{OUT} ; No external C_{OUT}. Board mounted module, scope setting : 20 MHz analog BW*

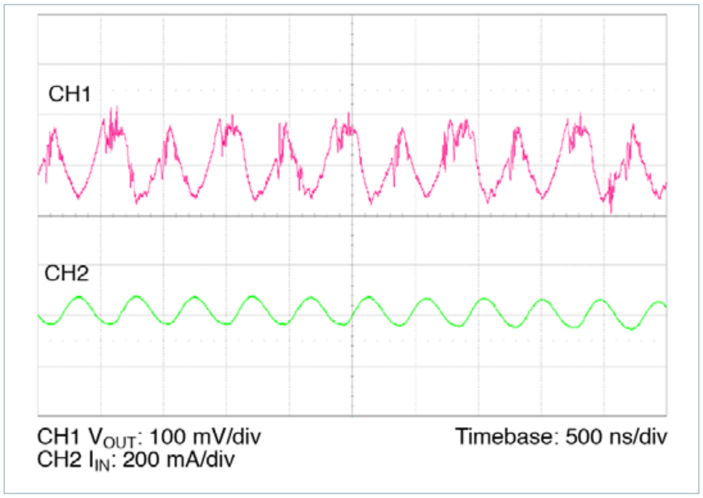


Figure 13 — *Full load ripple, 10 µF C_{IN}; No external C_{OUT}. Board mounted module, scope setting : 20 MHz analog BW*

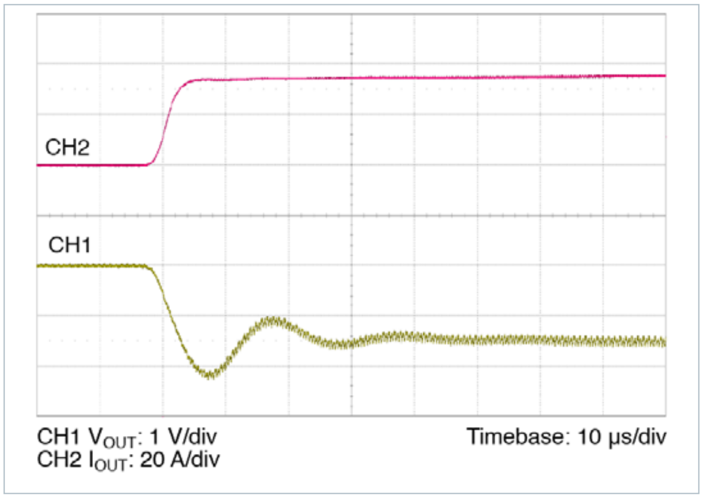


Figure 14 — *0 A– 35 A transient response: C_{IN} = 10 µF, no external C_{OUT}*

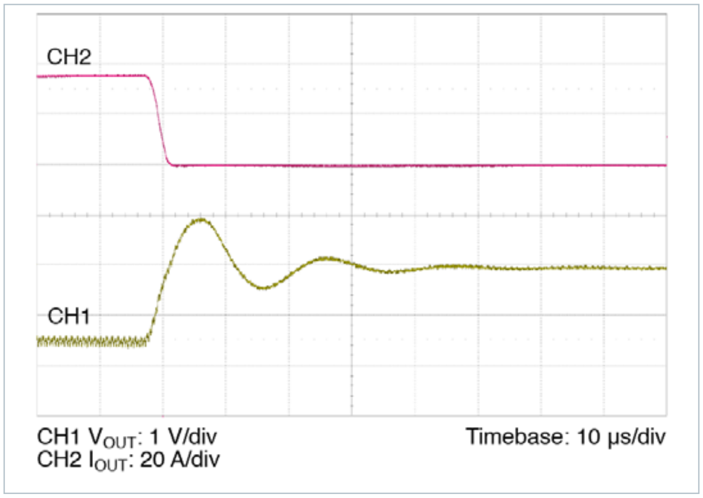


Figure 15 — *35 A – 0 A transient response: C_{IN} = 10 µF, no external C_{OUT}*

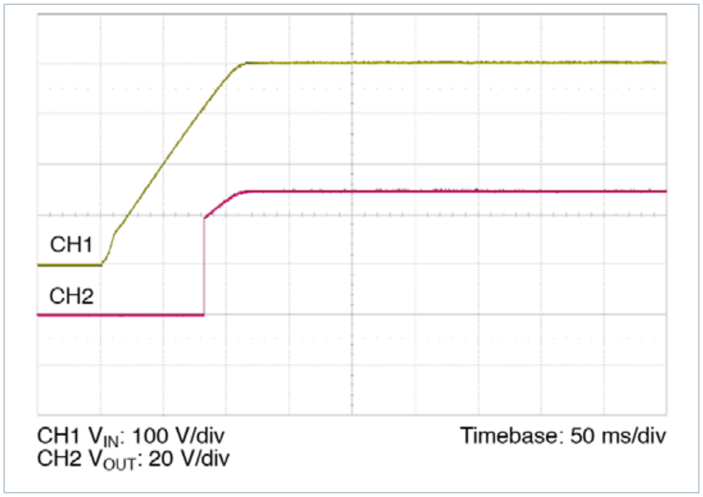


Figure 16 — *Start up from application of V_{IN} = 400 V, 50% I_{OUT}, 100% C_{OUT}*

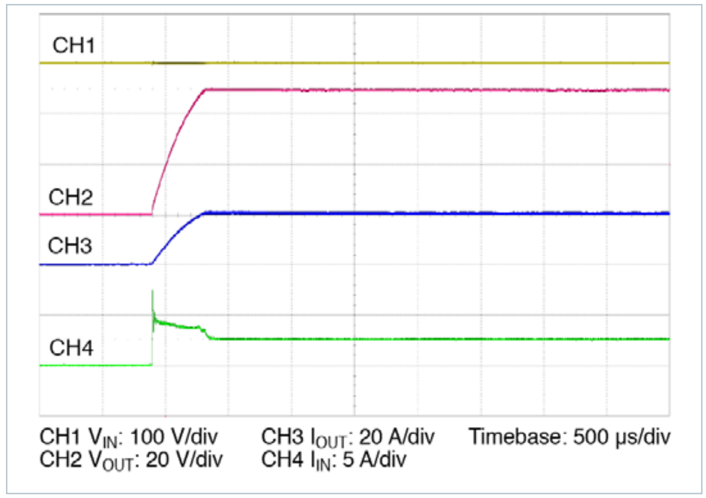


Figure 17 — *Start up from application of EN with pre-applied V_{IN} = 400 V, 50% I_{OUT}, 100% C_{OUT}*

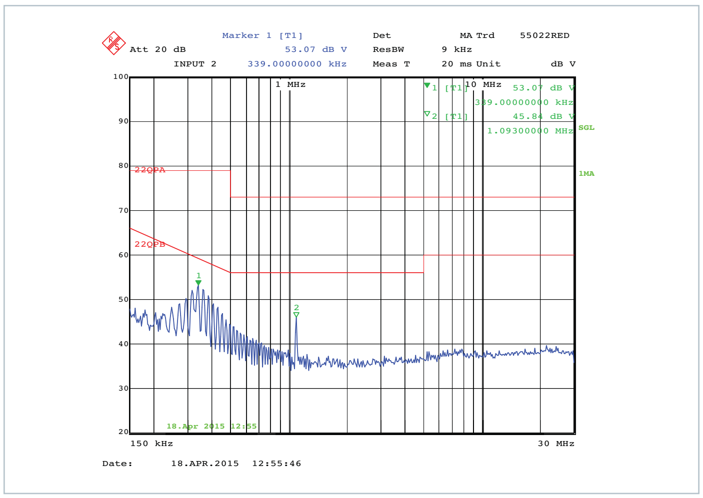


Figure 18 — *Typical EMI spectrum, Peak Scan, 10% load, Nominal Input, Test circuit - See Filtering Section*

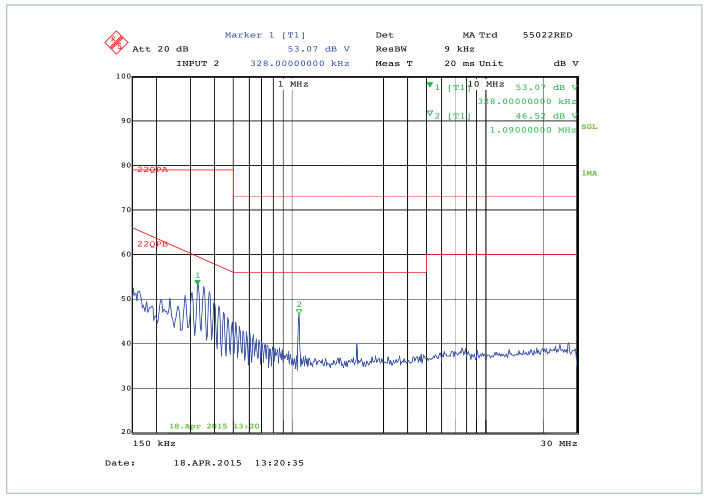


Figure 19 — *Typical EMI spectrum, Peak Scan, 50% load, Nominal Input, Test circuit - See Filtering Section*

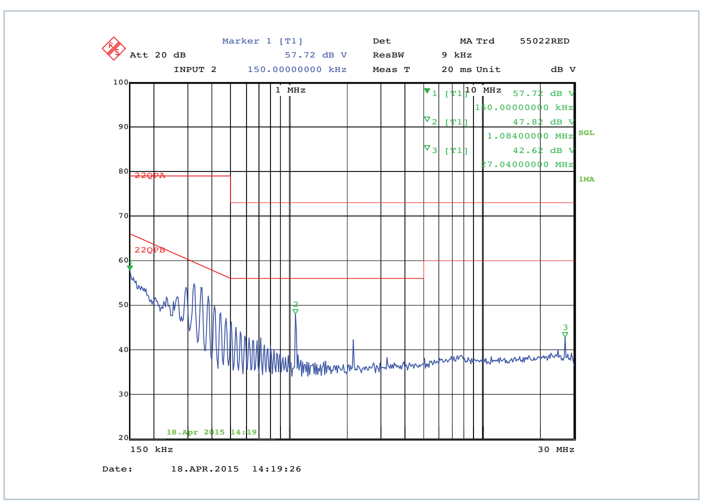


Figure 20 — *Typical EMI spectrum, Peak Scan, 90% load, Nominal Input, Test circuit - See Filtering Section*

General Characteristics

Specifications apply over all line, load conditions, unless otherwise noted; **Boldface** specifications apply over the temperature range of -40°C ≤ T_{CASE} ≤ 100°C (T-Grade); All other specifications are at T_{CASE} = 20ºC unless otherwise noted.

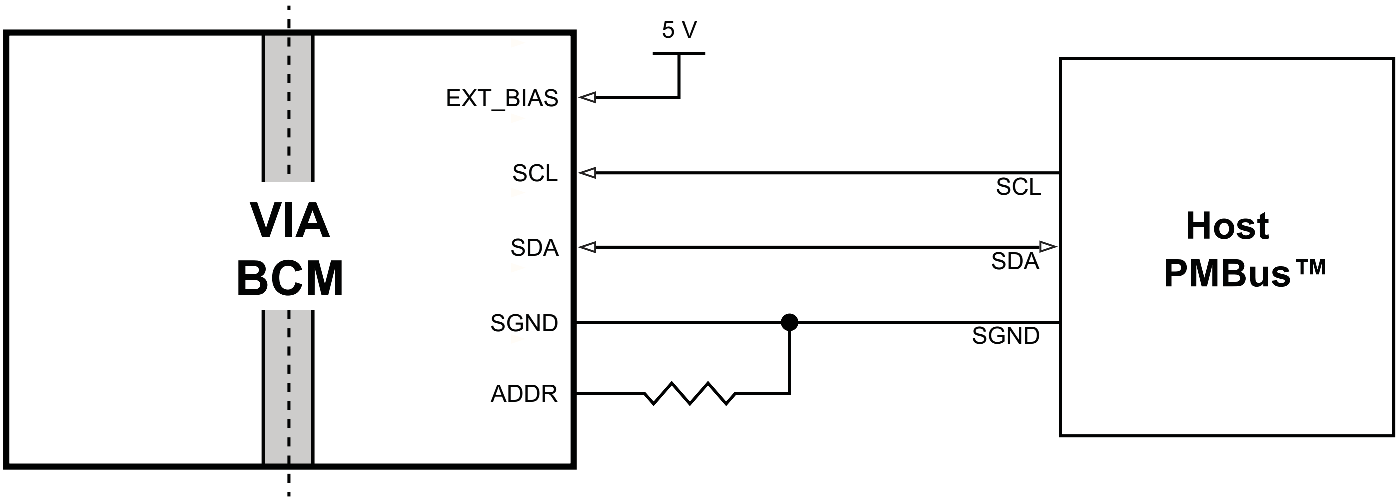
Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Mechanical						
Length	L	Lug Mount	124.52 / [4.90]	124.77 / [4.91]	125.02 / [4.92]	mm / [in]
Length	L	PCB Mount	126.73 / [4.99]	126.98 / [5.00]	127.23 / [5.01]	mm / [in]
Width	W		35.29 / [1.39]	35.54 / [1.40]	35.79 / [1.41]	mm / [in]
Height	H		9.05 / [0.36]	9.30 / [0.37]	9.55 / [0.38]	mm / [in]
Volume	Vol	Without heatsink		41.24 / [2.52]		cm^3/ [in^3]
Weight	W			156 / [5.5]		g / [oz]
Pin Material		C145 copper, 1/2 hard				
Underplate		Low stress ductile Nickel	50		100	µin
Pin Finish		Palladium	0.8		6	µin
		Soft Gold	0.12		2	
Thermal						
Operating junction temperature	$T_{INTERNAL}$	BCM4914xD1E5135yzz (T-Grade)	-40		125	°C
		BCM4914xD1E5135yzz (C-Grade)	-20		125	
Operating case temperature	T_{CASE}	BCM4914VD1E5135T02 (T-Grade), derating applied, see safe thermal operating area	-40		100	
		BCM4914xD1E5135yzz (C-Grade), derating applied, see safe thermal operating area	-20		100	
Thermal resistance top side	R_{JC-TOP}	Estimated thermal resistance to maximum temperature internal component from isothermal top		1.52		°C/W
Thermal Resistance Coupling between top case and bottom case	R_{HOU}	Estimated thermal resistance of thermal coupling between the top and bottom case surfaces		0.26		°C/W
Thermal resistance bottom side	R_{JC-BOT}	Estimated thermal resistance to maximum temperature internal component from isothermal bottom		1.55		°C/W
Thermal capacity				32		Ws/°C
Assembly						
Storage Temperature	T_{ST}	BCM4914xD1E5135yzz (T-Grade)	-40		125	°C
		BCM4914xD1E5135yzz (C-Grade)	-40		125	°C
ESD Withstand	ESD_{HBM}	Human Body Model, "ESDA / JEDEC JDS-001-2012" Class I-C (1kV to < 2 kV)	1000			
	ESD_{CDM}	Charge Device Model, "JESD 22-C101-E" Class II (200V to < 500V)	200			

General Characteristics (Cont.)

Specifications apply over all line, load conditions, unless otherwise noted; **Boldface** specifications apply over the temperature range of -40°C ≤ T_{CASE} ≤ 125°C (T-Grade); All other specifications are at T_{CASE} = 20°C unless otherwise noted.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Safety						
Isolation capacitance	C_{IN_OUT}	Unpowered unit	**620**	**780**	**940**	pF
Isolation resistance	R_{IN_OUT}	At 500 Vdc	**10**			MΩ
MTBF		MIL-HDBK-217Plus Parts Count - 25°C Ground Benign, Stationary, Indoors / Computer		3.53		MHrs
		Telcordia Issue 2 - Method I Case III; 25°C Ground Benign, Controlled		3.90		MHrs
Agency approvals / standards		cTÜVus "EN 60950-1"				
		cURus "UL 60950-1"				
		CE Marked for Low Voltage Directive and RoHS Recast Directive, as applicable				
EMI/EMC Compliance						
FCC Part 15, EN55022, CISPR22:2006+A1:2007, Conducted Emissions		Class B Limits - with components connected as shown in Filtering Section				

System Diagram



The VIA BCM bus converter provides accurate telemetry monitoring and reporting, threshold and warning limits adjustment, in addition to corresponding status flags.

The VIA BCM internal µC is referenced to secondary ground.

The VIA BCM provides the host system µC with access to standalone VIA BCM. The standalone VIA BCM is constantly polled for status by the internal µC. Direct communication to VIA BCM is enabled by a page command. For example, the page (0x00) prior to a telemetry inquiry points to the internal µC data and pages (0x01) prior to a telemetry inquiry points to the VIA BCM connected data. The VIA BCM constantly polls it's data through the PMBus™.

The VIA BCM enables the PMBus compatible host interface with an operating bus speed of up to 400 kHz. The VIA BCM follows the PMBus command structure and specification.

PMBus™ Interface

Refer to "PMBus Power System Management Protocol SpecificationRevision 1.2, Part I and II" for complete PMBus specifications details visit http://pmbus.org.

Device Address

The PMBus address (ADDR Pin) should be set to one of a predetermined 16 possible addresses shown in the table below using a resistor between ADDR pin and SGND pin.

The VIA BCM accepts only a fixed and persistent address and does not support SMBus address resolution protocol. At initial power–up, the VIA BCM internal µC will sample the address pin voltage, and will hold this address until device power is removed.

ID	Slave Address	HEX	Recommended Resistor R_{ADDR} (Ω)
1	1010 000b	50h	487
2	1010 001b	51h	1050
3	1010 010b	52h	1870
4	1010 011b	53h	2800
5	1010 100b	54h	3920
6	1010 101b	55h	5230
7	1010 110b	56h	6810
8	1010 111b	57h	8870
9	1011 000b	58h	11300
10	1011 001b	59h	14700
11	1011 010b	5Ah	19100
12	1011 011b	5Bh	25500
13	1011 100b	5Ch	35700
14	1011 101b	5Dh	53600
15	1011 110b	5Eh	97600
16	1011 111b	5Fh	316000

Reported DATA Formats

The VIA BCM internal µC employs a direct data format where all reported internal µC measurements are in Volts, Amperes, Degrees Celsius, or Seconds. The host uses the following PMBus specification to interpret received values metric prefixes. Note that the Coefficients command is not supported:

$$X = \left(\frac{1}{m}\right) \cdot (Y \cdot 10^{-R} - b)$$

Where:

X, is a "real world" value in units (A, V, °C, s)
Y, is a two's complement integer received from the internal µC
m, b and R are two's complement integers defined as follows:

Command	Code	m	R	b
TON_DELAY	60h	1	3	0
READ_VIN	88h	1	1	0
READ_IIN	89h	1	3	0
READ_VOUT	8Bh	1	1	0
READ_IOUT	8Ch	1	2	0
READ_TEMPERATURE_1	8Dh	1	0	0
READ_POUT	96h	1	0	0
MFR_VIN_MIN	A0h	1	0	0
MFR_VIN_MAX	A1h	1	0	0
MFR_VOUT_MIN	A4h	1	0	0
MFR_VOUT_MAX	A5h	1	0	0
MFR_IOUT_MAX	A6h	1	0	0
MFR_POUT_MAX	A7h	1	0	0
READ_K_FACTOR	D1h	65536	0	0
READ_BCM_ROUT	D4h	1	2	0

[1] Default READ Output Voltage returned when VIA BCM unit is disabled = -300 V.
[2] Default READ Temperature returned when VIA BCM unit is disabled = -273°C.

No special formatting is required when lowering the supervisory limits and warnings.

Supported Command List

Command	Code	Function	Default Data Content	Data Bytes
PAGE	00h	Access VIA BCM stored information for all connected devices	00h	1
OPERATION	01h	Turn VIA BCMs on or off	80h	1
ON_OFF_CONFIG	02h	Defines startup when power is applied as well as immediate on/off control over the VIA BCMs	1Dh	1
CLEAR_FAULTS	03h	Clear all VIA BCM and all internal µC faults	N/A	None
CAPABILITY	19h	Internal µC PMBus^{TM} key capabilities set by factory	20h	1
OT_FAULT_LIMIT	4Fh[1]	VIA BCM over temperature protection	64h	2
OT_WARN_LIMIT	51h[1]	VIA BCM over temperature warning	64h	2
VIN_OV_FAULT_LIMIT	55h[1]	VIA BCM VIN overvoltage warning	64h	2
VIN_OV_WARN_LIMIT	57h[1]	VIA BCM VIN overvoltage protection	64h	2
IIN_OC_FAULT_LIMIT	5Bh[1]	VIA BCM IOUT overcurrent protection	64h	2
IIN_OC_WARN_LIMIT	5Dh[1]	VIA BCM IOUT overcurrent warning	64h	2
TON_DELAY	60h[1]	Startup delay additional to any VIA BCM fixed delays	00h	2
STATUS_BYTE	78h	Summary of VIA BCM faults	00h	1
STATUS_WORD	79h	Summary of VIA BCM fault conditions	00h	2
STATUS_IOUT	7Bh	VIA BCM overcurrent fault status	00h	1
STATUS_INPUT	7Ch	VIA BCM overvoltage and under voltage fault status	00h	1
STATUS_TEMPERATURE	7Dh	VIA BCM over temperature and under temperature fault status	00h	1
STATUS_CML	7Eh	Internal µC PMBus Communication fault	00h	1
STATUS_MFR_SPECIFIC	80h	Other VIA BCM status indicator	00h	1
READ_VIN	88h	VIA BCM input voltage	FFFFh	2
READ_IIN	89h	VIA BCM input current	FFFFh	2
READ_VOUT	8Bh	VIA BCM output voltage	FFFFh	2
READ_IOUT	8Ch	VIA BCM output current	FFFFh	2
READ_TEMPERATURE_1	8Dh	VIA BCM temperature	FFFFh	2
READ_POUT	96h	VIA BCM output power	FFFFh	2
PMBUS_REVISION	98h	Internal µC PMBus compatible revision	22h	1
MFR_ID	99h	Internal µC ID	"VI"	2
MFR_MODEL	9Ah	Internal µC or VIA BCM model	Part Number	18
MFR_REVISION	9Bh	Internal µC or VIA BCM revision	FW and HW revision	18
MFR_LOCATION	9Ch	Internal µC or VIA BCM factory location	“AP”	2
MFR_DATE	9Dh	Internal µC or VIA BCM manufacturing date	"YYWW"	4
MFR_SERIAL	9Eh	Internal µC or VIA BCM serial number	Serial Number	16
MFR_VIN_MIN	A0h	VIA BCM Minimum rated VIN	Varies per VIA BCM	2
MFR_VIN_MAX	A1h	VIA BCM Maximum rated VIN	Varies per VIA BCM	2
MFR_VOUT_MIN	A4h	VIA BCM Minimum rated VOUT	Varies per VIA BCM	2
MFR_VOUT_MAX	A5h	VIA BCM Maximum rated VOUT	Varies per VIA BCM	2
MFR_IOUT_MAX	A6h	VIA BCM Maximum rated IOUT	Varies per VIA BCM	2
MFR_POUT_MAX	A7h	VIA BCM Maximum rated POUT	Varies per VIA BCM	2
BCM_EN_POLARITY	D0h[1]	Set VIA BCM EN pin polarity	02h	1
READ_K_FACTOR	D1h	VIA BCM K factor	Varies per VIA BCM	2
READ_BCM_ROUT	D4h	VIA BCM Rout	Varies per VIA BCM	2
SET_ALL_THRESHOLDS	D5h[1]	Set VIA BCM supervisory warning and protection thresholds	646464646464h	6
DISABLE_FAULT	D7h[1]	Disable VIA BCM overvoltage, overcurrent or under voltage supervisory faults	00h	2

[1] The VIA BCM must be in a disabled state during a write message.

Command Structure Overview

Write Byte protocol:

The Host always initiates PMBus™ communication with a START bit. All messages are terminated by the Host with a STOP bit. In a write message, the master sends the slave device address followed by a write bit. Once the slave acknowledges, the master proceeds with the command code and then similarly the data byte.

1	7	1	1	8	1	8	1	1
S	Slave Address	Wr	A	Command Code	A	Data Byte	A	P
		x = 0	x = 0		x = 0		x = 0	

S Start Condition

Sr Repeated start Condition

Rd Read

Wr Write

X Indicated that field is required to have the value of x

A Acknowledge (bit may be 0 for an ACK or 1 for a NACK)

P Stop Condition

From Master to Slave

From Slave to Master

... Continued next line

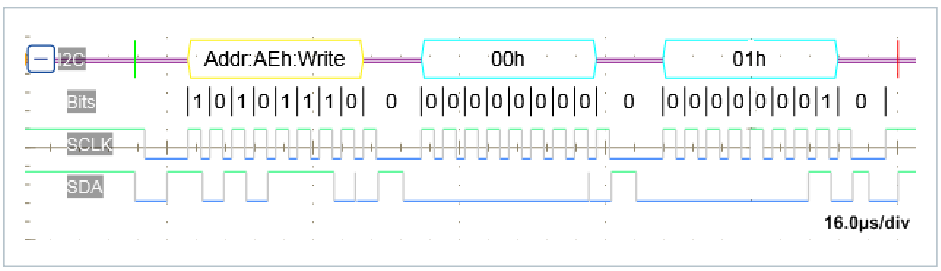


Figure 1 *— PAGE COMMAND (00h), WRITE BYTE PROTOCOL*

Read Byte protocol:

A Read message begins by first sending a Write Command, followed by a REPEATED START Bit and a slave Address. After receiving the READ bit, the internal µC begins transmission of the Data responding to the Command. Once the Host receives the requested Data, it terminates the message with a NACK preceding a stop condition signifying the end of a read transfer.

1	7	1	1	8	1	1	7	1	1	8	1	1
S	Slave Address	Wr	A	Command Code	A	Sr	Slave Address	Rd	A	Data Byte	A	P
		x = 0	x = 0		x = 0			x = 1	x = 0		x = 1	

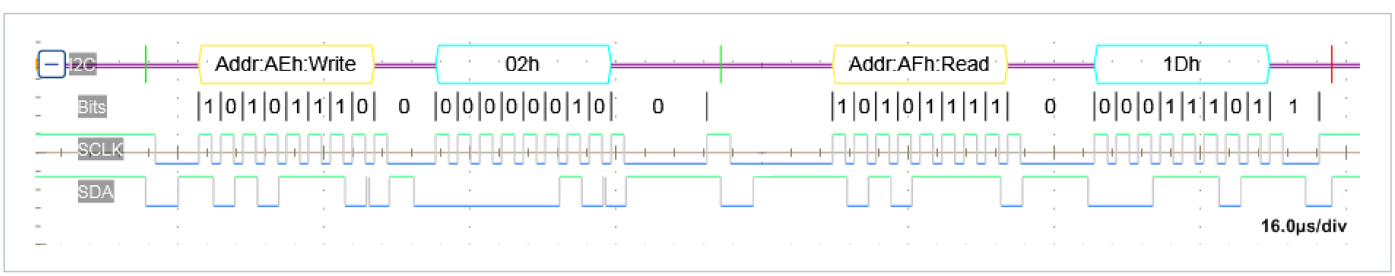


Figure 2 *— ON_OFF_CONFIG COMMAND (02h), READ BYTE PROTOCOL*

Write Word protocol:

When transmitting a word, the lowest order byte leads the highest order byte. Furthermore, when transmitting a Byte, the least significant bit (LSB) is sent last. Refer to System Management Bus (SMBus) specification version 2.0 for more details.
Note: Extended command and Packet Error Checking Protocols are not supported.

1	7	1	1	8	1	8	1	8	1	1
S	Slave Address	Wr	A	Command Code	A	Data Byte Low	A	Data Byte High	A	P
		x = 0	x = 0		x = 0		x = 0		x = 0	

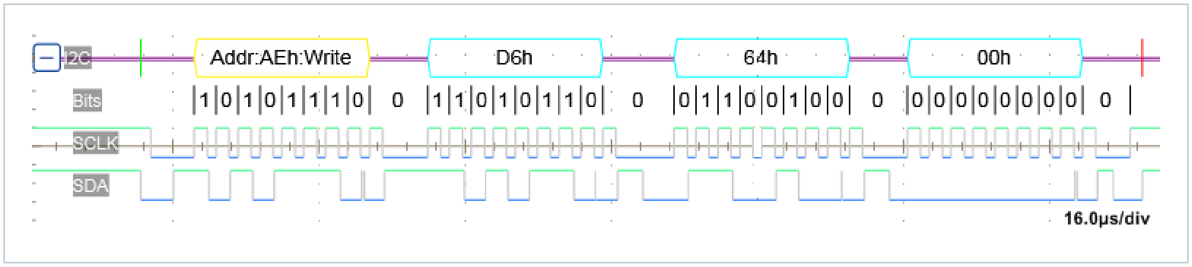


Figure 3 *— TON_DELAY COMMAND (60h)_WRITE WORD PROTOCOL*

Read Word protocol:

1	7	1	1	8	1	1	7	1	1	8	1	8	1	1
S	Slave Address	Wr	A	Command Code	A	Sr	Slave Address	Rd	A	Data Byte Low	A	Data Byte High	A	P
		x = 0	x = 0		x = 0			x = 1	x = 0		x = 0		x = 1	

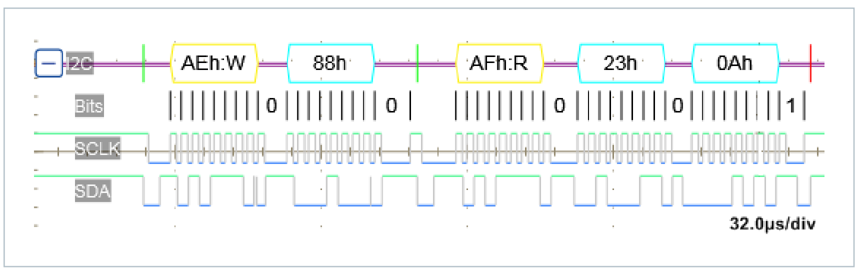


Figure 4 *— MFR_VIN_MIN COMMAND (A0h)_READ WORD PROTOCOL*

Write Block protocol:

1	7	1	1	8	1	8	1	8	1	
S	Slave Address	Wr	A	Command Code	A	Byte Count = N	A	Data Byte 1	A	...
		x = 0	x = 0		x = 0		x = 0		x = 0	

8	1	...	8	1	1
Data Byte 2	A	...	Data Byte N	A	P
	x = 0	...		x = 0	

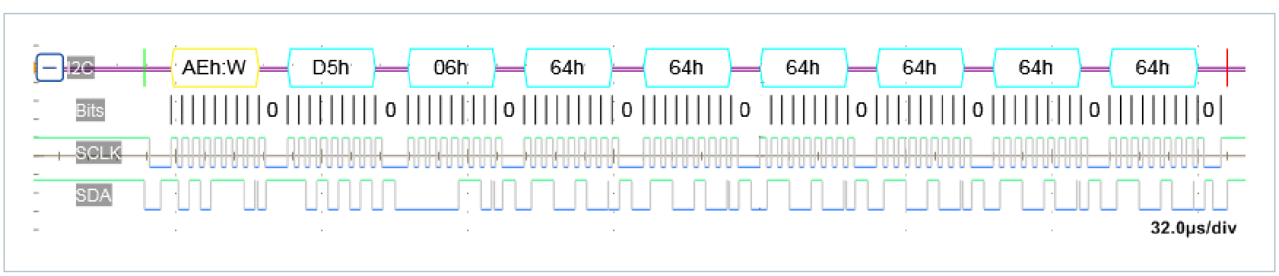


Figure 5 *— SET_ALL_THRESHOLDS COMMAND (D5h)_WRITE BLOCK PROTOCOL*

Read Block protocol:

1	7	1	1	8	1	1	7	1	1	8	1	
S	Slave Address	Wr	A	Command Code	A	Sr	Slave Address	Rd	A	Data Byte = N	A	...
		x = 0	x = 0		x = 0			x = 1	x = 0		x = 0	

8	1	8	1	...	8	1	1
Data Byte 1	A	Data Byte 2	A	...	Data Byte N	A	P
	x = 0		x = 0	...		x = 1	

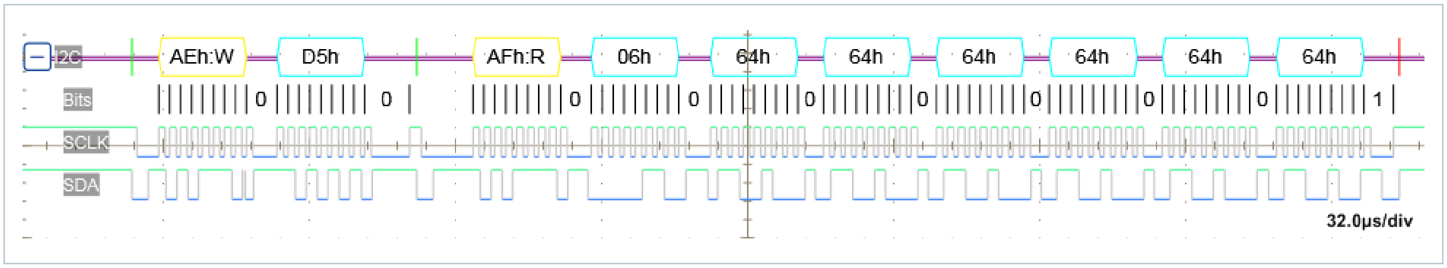


Figure 6 *— SET_ALL_THRESHOLDS COMMAND (D5h)_READ BLOCK PROTOCOL*

Write Group Command protocol:

Note that only one command per device is allowed in a group command.

1	7	1	1	8	1	8	1	8	1	
S	Slave Address	Wr	A	Command Code	A	Data Byte Low	A	Data Byte High	A	...
	First Device	x = 0	x = 0	First Command	x = 0		x = 0	One or more Data Bytes	x = 0	

1	7	1	1	8	1	8	1	8	1	
Sr	Slave Address	Wr	A	Command Code	A	Data Byte Low	A	Data Byte High	A	...
	Second Device	x = 0	x = 0	Second Command	x = 0		x = 0	One or more Data Bytes	x = 0	

1	7	1	1	8	1	8	1	8	1	
Sr	Slave Address	Wr	A	Command Code	A	Data Byte Low	A	Data Byte High	A	P
	Nth Device	x = 0	x = 0	Nth Command	x = 0		x = 0	One or more Data Bytes	x = 0	

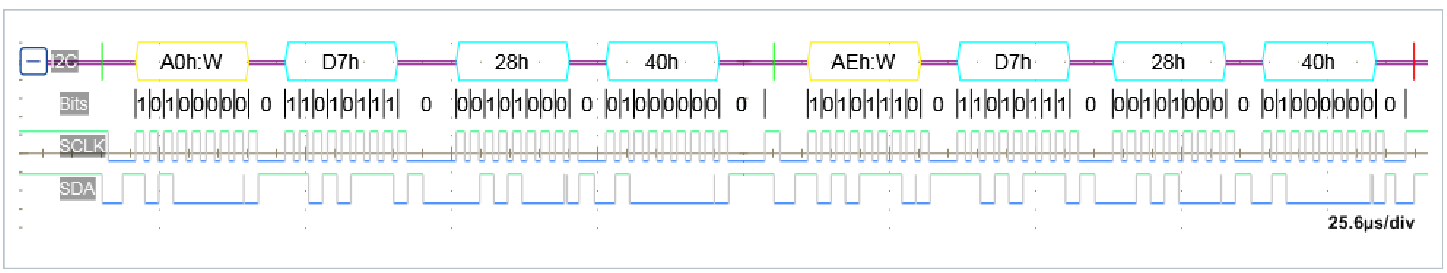


Figure 7 *— DISABLE_FAULT COMMAND (D7h)_WRITE*

Supported Commands Transaction type

A direct communication to the VIA BCM internal µC and a simulated communication to non-PMBus™ devices is enabled by a page command. Supported command access privileges with a pre-selected PAGE are defined in the following table. Deviation from this table generates a communication error in STATUS_CML register.

Command	Code	PAGE Data Byte Access Type	
		00h	01h
PAGE	00h	R/W	R/W
OPERATION	01h	R	R/W
ON_OFF_CONFIG	02h		R
CLEAR_FAULTS	03h	W	W
CAPABILITY	19h	R	
OT_FAULT_LIMIT	4Fh		R/W
OT_WARN_LIMIT	51h		R/W
VIN_OV_FAULT_LIMIT	55h		R/W
VIN_OV_WARN_LIMIT	57h		R/W
IIN_OC_FAULT_LIMIT	5Bh		R/W
IIN_OC_WARN_LIMIT	5Dh		R/W
TON_DELAY	60h		R/W
STATUS_BYTE	78h	R/W	R
STATUS_WORD	79h	R	R
STATUS_IOUT	7Bh	R	R/W
STATUS_INPUT	7Ch	R	R/W
STATUS_TEMPERATURE	7Dh	R	R/W
STATUS_CML	7Eh	R/W	
STATUS_MFR_SPECIFIC	80h	R	R/W
READ_VIN	88h		R
READ_IIN	89h	R	R
READ_VOUT	8Bh		R
READ_IOUT	8Ch	R	R
READ_TEMPERATURE_1	8Dh	R	R
READ_POUT	96h	R	R
PMBUS_REVISION	98h	R	
MFR_ID	99h	R	
MFR_MODEL	9Ah	R	R
MFR_REVISION	9Bh	R	R
MFR_LOCATION	9Ch	R	R
MFR_DATE	9Dh	R	R
MFR_SERIAL	9Eh	R	R
MFR_VIN_MIN	A0h	R	R
MFR_VIN_MAX	A1h	R	R
MFR_VOUT_MIN	A4h	R	R
MFR_VOUT_MAX	A5h	R	R
MFR_IOUT_MAX	A6h	R	R
MFR_POUT_MAX	A7h	R	R
VIA BCM_EN_POLARITY	D0h		R/W
READ_K_FACTOR	D1h		R
READ_VIA BCM_ROUT	D4h		R
SET_ALL_THRESHOLDS	D5h		R/W
DISABLE_FAULT	D7h		R/W

Page Command (00h)

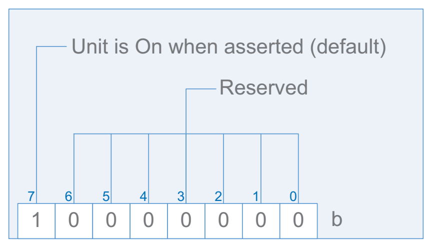
The page command data byte of 00h prior to a command call will address the internal µC specific data and a page data byte of FFh would broadcast to all of the connected VIA BCMs. The value of the Data Byte corresponds to the pin name trailing number with the exception of 00h and FFh.

Data Byte	Description
00h	µC
01h	VIA BCM

OPERATION Command (01h)

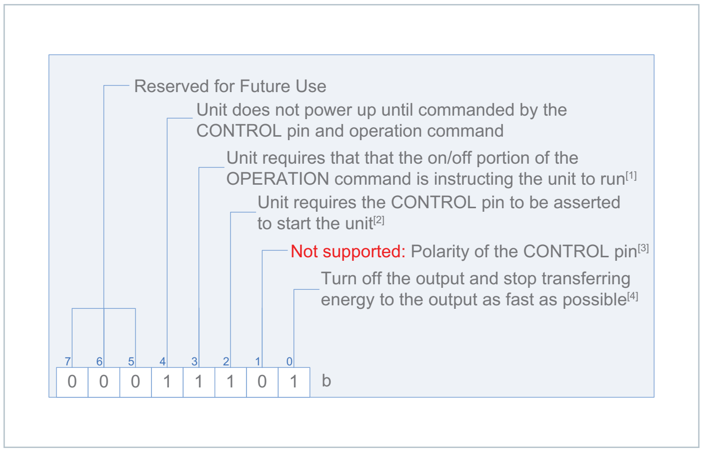
The Operation command can be used to turn on and off the connected VIA BCM. Note that the host OPERATION command will not enable the VIA BCM if the VIA BCM EN pin is disabled in hardware with respect to the pre-set pin polarity. Only with the EN pin active, will the OPERATION command provide ON/OFF control.

If synchronous startup is required in the system, it is recommended to use the command from host PMBus in order to achieve simultaneous array startup.



This command accepts only two data values: 00h and 80h. If any other value is sent the command will be rejected and a CML Data error will result.

ON_OFF_CONFIG Command (02h)



[1] The VIA BCM Enable pin is ALWAYS to be asserted for powerup. The BCM_EN_POLARITY command (D0h) bit[(1) defines the logic level required for the control pin (i.e VIA BCM Enable pin) to be asserted.

[2] With respect to the VIA BCM EN Control Pin if used in system

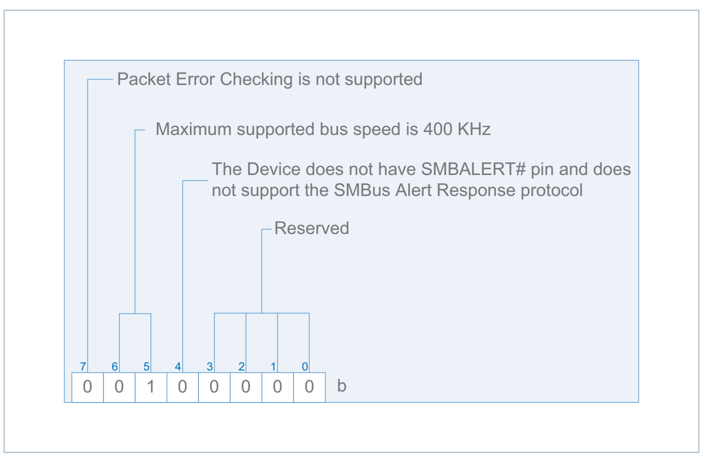
[3] See MFR_SPECIFIC_00 / VIA BCM_EN_POLARITY to change the Polarity of the VIA BCM Enable Pin

[4] The VIA BCM powertrain once disabled cannot sink current

CLEAR_FAULTS Command (03h)

This command clears all status bits that have been previously set. Persistent or active faults are re–asserted again once cleared. All faults are latched once asserted in the internal µC. Registered faults will not be cleared when shutting down the VIA BCM powertrain by recycling the VIA BCM input voltage, or toggling the VIA BCM EN pin, or sending the OPERATION command.

CAPABILITY Command (19h)



The internal µC returns a default value of 20h. This value indicates that the PMBus™ frequency supported is up to 400 KHz and that both Packet Error Checking (PEC) and SMBALERT# are not supported.

OT_FAULT_LIMIT Command (4Fh), OT_WARN_ LIMIT Command (51h), VIN_OV_FAULT_ LIMIT Command (55h), VIN_OV_WARN_ LIMIT Command (57h), IIN_OC_FAULT_ LIMIT Command (5Bh), IIN_OC_WARN_ LIMIT Command (5Dh)

The values of these registers are set in non–volatile memory and can only be written when the VIA BCMs are disabled.

The values of the above mentioned fault and warning are set by default to a 100% of the respective VIA BCM model supervisory limits. However these limits can be set to a lower value. For example: In order for a limit percentage to be set to 80% one would send a write command with a (50h) Data Word.

Any values outside the range of (00h – 64h) sent by a host will be rejected, will not override the currently stored value and will set the Unsupported Data bit in STATUS_CML.

The SET_ALL_THRESHOLDS COMMAND (D5h) combines in one block over temperature fault and warning limits, V_{IN} overvoltage fault and warning limits as well as I_{OUT} overcurrent fault and warning limits. A delay prior to a read command of up to 200 ms following a write of new value is required.

The VIN_UV_WARN_LIMIT (58h) and VIN_UV_FAULT_LIMIT (59h) are set by the factory and cannot be changed by the host. However, a host can disable the under voltage setting using the DISABLE_FAULT COMMAND (D7h).

All FAULT_RESPONSE commands are unsupported. The VIA BCM powertrain supervisory limits and powertrain protection will behave as described in the VIA BCM datasheet. In general, once a fault is detected, the VIA BCM powertrain will shut down and attempt to auto–restart after a predetermined delay.

TON_DELAY Command (60h)

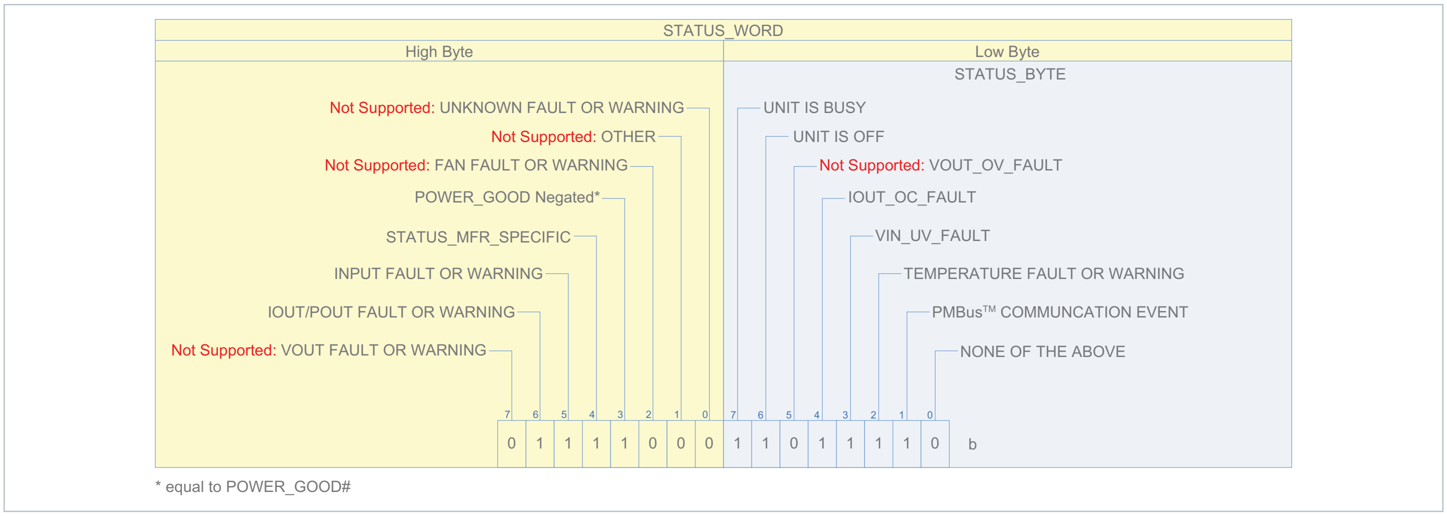
The value of this register word is set in non–volatile memory and can only be written when the VIA BCMs are disabled.

The maximum possible delay is 100ms. Default value is set to (00h). Follow this equation below to interpret the reported value.

$$TON\_DELAY_{ACTUAL} = t_{REPORTED} \cdot 10^{-3}(s)$$

Staggering startup in an array is possible with TON_DELAY Command. This delay will be in addition to any startup delay inherent in the VIA BCM module. For example: startup delay from application of V_{IN} is typically 20 ms whereas startup with EN pin is typically 250 us. When TON_DELAY is greater than zero, the set delay will be added to both.

STATUS_BYTE (78h) and STATUS_WORD (79h)



All fault or warning flags, if set, will remain asserted until cleared by the host or once the internal µC power is removed. This includes under voltage fault, overvoltage fault, overvoltage warning, overcurrent warning, over temperature fault, over temperature warning, under temperature fault, reverse operation, communication faults and analog controller shutdown fault.

Asserted status bits in all status registers, with the exception of STATUS_WORD and STATUS_BYTE, can be individually cleared. This is done by sending a data byte with one in the bit position corresponding to the intended warning or fault to be cleared. Refer to the PMBus™ Power System Management Protocol Specification – Part II – Revision 1.2 for details.

The POWER_GOOD# bit reflects the state of the device and does not reflect the state of the POWER_GOOD# signal limits. The POWER_GOOD_ON COMMAND (5Eh) and POWER_GOOD_OFF COMMAND (5Fh) are not supported. The POWER_GOOD# bit is set anytime the VIA BCM is not in the enabled state, to indicate that the powertrain is inactive and not switching. The POWER_GOOD# bit is cleared when the VIA BCM completes the enabling state, 5 ms after the powertrain is activated allowing for soft–start to elapse. POWER_GOOD# and OFF bits cannot be cleared as they always reflect the current state of the device.

When Page (00h) is used the POWER_GOOD# bit reflects the OR-ing of all active VIA BCMs' POWER_GOOD# bits. When Page (01h – 04h) is used POWER_GOOD# is clear only when the VIA BCM is active.

When Page (00h) is used UNIT IS OFF is SET when all VIA BCMs are not active. When Page (01h – 04h) is used UNIT IS OFF is clear only when the VIA BCM is active.

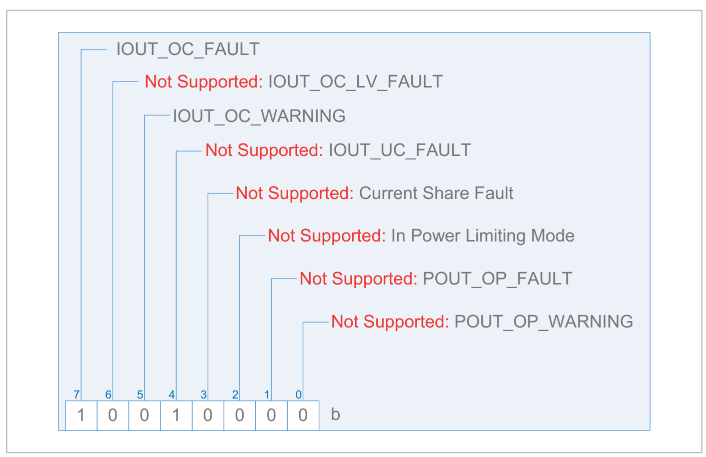
The Busy bit can be cleared using CLEAR_ALL Command (03h) or by writing either data value (40h, 80h) to PAGE (00h) using the STATUS_BYTE (78h).

Fault reporting, such as SMBALERT# signal output, and host notification by temporarily acquiring bus master status is not supported.

If the internal µC is still powered, it will retain the last status it received from the VIA BCM and this information will be available to the user via a PMBus Status request. This is in agreement with the PMBus standard which requires that status bits remain set until specifically cleared. Note that in this case where the VIA BCM V_{IN} is lost, the status will always indicate an under voltage fault, in addition to any other fault that occurred.

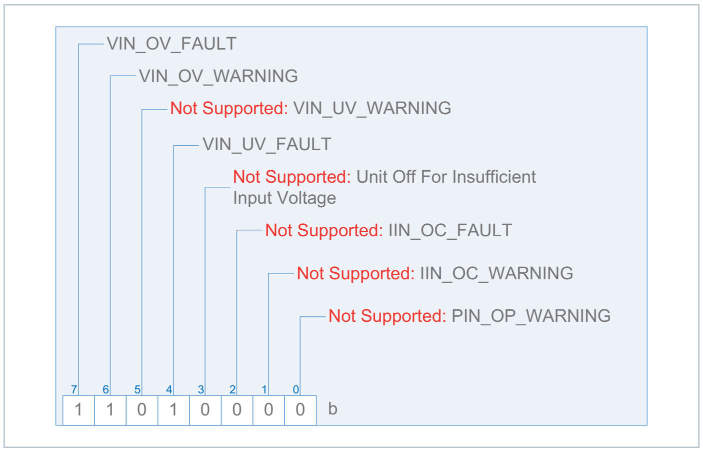
NONE OF THE ABOVE bit will be asserted if either the STATUS_MFR_SPECIFIC (80h) or the High Byte of the STATUS WORD is set.

STATUS_IOUT (7Bh)



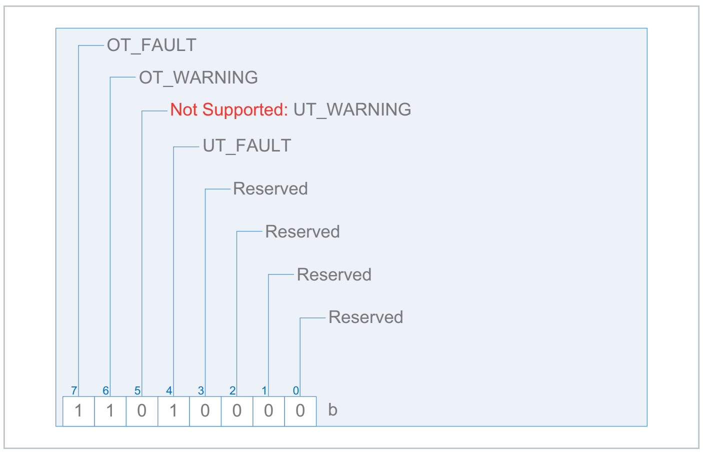
Unsupported bits are indicated above. A one indicates a fault.

STATUS_INPUT (7Ch)



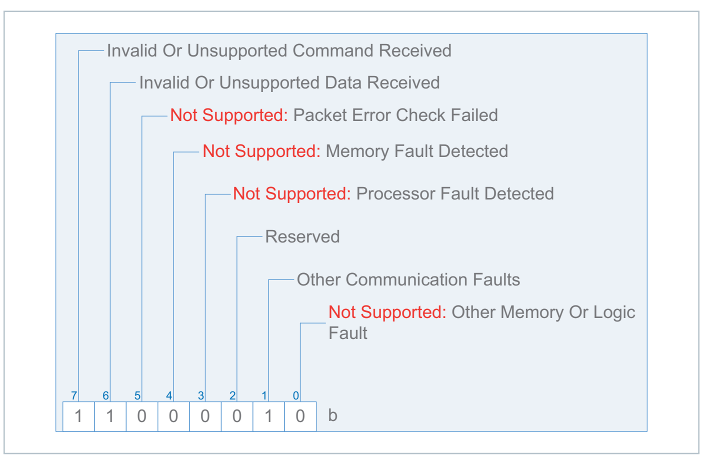
Unsupported bits are indicated above. A one indicates a fault.

STATUS_TEMPERATURE (7Dh)



Unsupported bits are indicated above. A one indicates a fault.

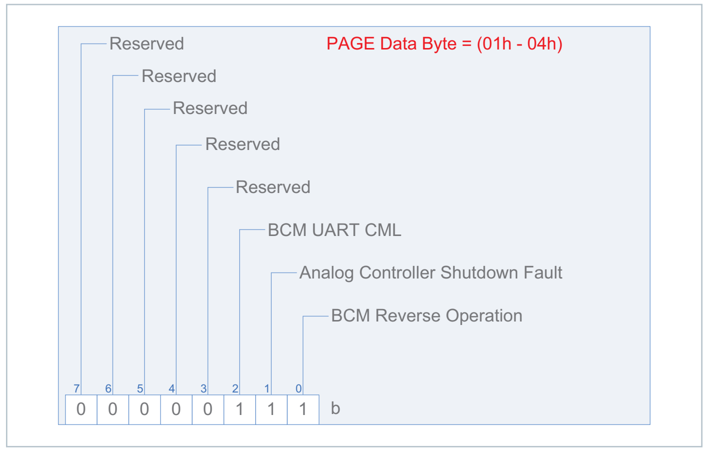
STATUS_CML (7Eh)



Unsupported bits are indicated above. A one indicates a fault.

The STATUS_CML data byte will be asserted when an unsupported PMBus™ command or data or other communication fault occured.

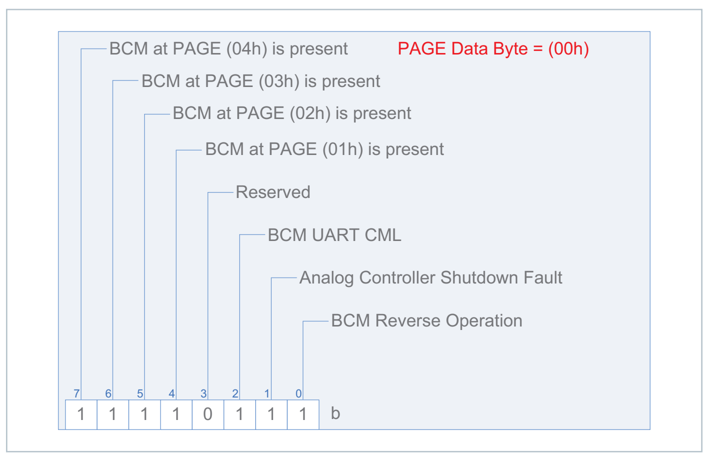
STATUS_MFR_SPECIFIC (80h)



The reverse operation bit, if asserted, indicates that the VIA BCM is processing current in reverse. Reverse current reported value is not supported.

The VIA BCM has analog protections and internal µC protections. The analog controller provides an additional layer of protection and has the fastest response time. The analog controller shutdown fault, when asserted, indicates that at least one of the powertrain protection faults is triggered. This fault will also be asserted if a disabled fault event occurs after asserting any bit using the DISABLE_FAULTS COMMAND.

The VIA BCM UART is designed to operate with the internal µC UART. If the VIA BCM UART CML is asserted, it may indicate a hardware or connection issue between both devices.



When PAGE COMMAND (00h) data byte is equal to (00h), the the BCM Reverse operation, Analog Controller Shutdown Fault, and BCM UART CML bit will return OR-ing result of active BCMs. The BCM UART CML will also be asserted if any of the active BCMs stops responding. The BCM must communicate at least once to the internal µC in order to trigger this FAULT. The BCM UART CML can be cleared from the culprit BCM once the internal µC is able to communicate with it once again or can be cleared using PAGE (00h) CLEAR_FAULTS (03h) Command.

READ_VIN Command (88h)

If PAGE data byte is equal to (01h - 04h) command will return a reported individual VIA BCM's input voltage in the following format:

$$V_{VIN\_ACTUAL} = V_{VIN\_REPORTED} \bullet 10^{-1}(V)$$

READ_IIN Command (89h)

If PAGE data byte is equal to (01h - 04h) command will return a reported individual VIA BCM's input current in the following format:

$$I_{IIN\_ACTUAL} = I_{IIN\_REPORTED} \bullet 10^{-3}(A)$$

If PAGE data byte is equal (00h) command will return the sum of active VIA BCMs' input current.

READ_VOUT Command (8Bh)

If PAGE data byte is equal to (01h - 04h) command will return a reported individual VIA BCM's output voltage in the following format:

$$V_{VOUT\_ACTUAL} = V_{VOUT\_REPORTED} \bullet 10^{-1}(V)$$

READ_IOUT Command (8Ch)

If PAGE data byte is equal to (01h - 04h) command will return a reported individual VIA BCM's output current in the following format:

$$I_{IOUT\_ACTUAL} = I_{IOUT\_REPORTED} \bullet 10^{-2}(A)$$

If PAGE data byte is equal (00h) command will return the sum of active VIA BCMs' output current.

READ_TEMPERATURE_1 Command (8Dh)

If PAGE data byte is equal to (01h - 04h) command will return a reported individual VIA BCM's temperature in the following format:

$$T_{ACTUAL} = \pm T_{REPORTED}\ (°C)$$

If PAGE data byte is equal (00h) command will return the maximum temperature of active VIA BCMs.

READ_POUT Command (96h)

If PAGE data byte is equal to (01h - 04h) command will return a reported individual VIA BCM's output power in the following format:

$$POUT_{ACTUAL} = POUT_{REPORTED}\ (W)$$

If PAGE data byte is equal to (00h) command will return the sum of active VIA BCMs' ouput power.

MFR_VIN_MIN Command (A0h), MFR_VIN_MAX Command (A1h), MFR_VOUT_MIN Command (A4h), MFR_VOUT_MAX Command (A5h), MFR_IOUT_MAX Command (A6h), MFR_POUT_MAX Command (A7h)

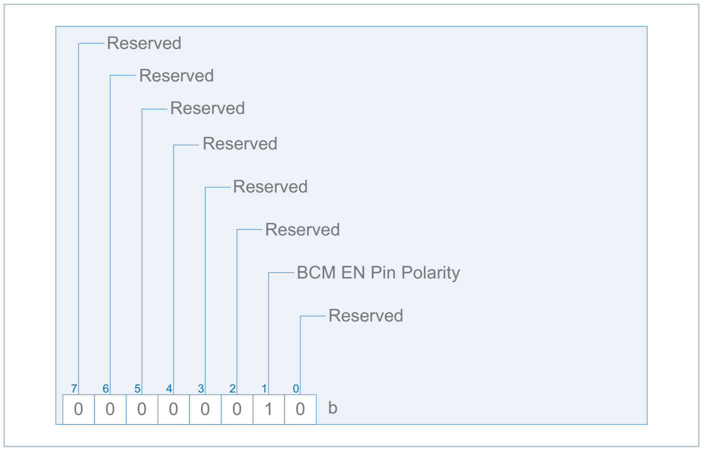
These values are set by the factory and indicate the device input output voltage and output current range and output power capacity.

The internal µC will report rated VIA BCM input voltage minimum and maximum in Volts, output voltage minimum and maximum in Volts, output current maximum in Amperes and output power maximum in Watts.

If PAGE data byte is equal to (00h) then:

- MFR_VIN_MIN COMMAND (A0h) will return the highest MFR_VIN_MIN of all active VIA BCMs
- MFR_VIN_MAX COMMAND (A1h) will return the lowest MFR_VIN_MAX of all active VIA BCMs
- MFR_VOUT_MIN COMMAND (A4h) will return the highest MFR_VOUT_MIN of all active VIA BCMs
- MFR_VOUT_MAX COMMAND (A5h) will return the lowest MFR_VOUT_MAX of all active VIA BCMs
- MFR_IOUT_MAX COMMAND (A6h) will return the SUM of MFR_IOUT_MAX of all active VIA BCMs
- MFR_POUT_MAX COMMAND (A7h) will return the SUM of MFR_POUT_MAX of all active VIA BCMs

BCM_EN_POLARITY Command (D0h)



The value of this register is set in non–volatile memory and can only be written when the BCMs are disabled.

When PAGE COMMAND (00h) data byte is equal to (01h – 04h), this command defines the polarity of the EN pin. If BCM_EN_POLARITY is set, the BCM will startup once VIN is greater than the under voltage threshold.

The BCM EN PIN is internally pulled-up to 3.3V. If the BCM_EN_POLARITY is cleared, an external pull-down is then required. Applying VIN greater than the under voltage threshold will not suffice to start the BCM.

READ_K_FACTOR Command (D1h)

If PAGE data byte is equal to (01h - 04h) command will return a reported individual BCM's K factor in the following format:

$$K\_FACTOR_{ACTUAL} = K\_FACTOR_{REPORTED} \bullet 2^{-16}(V/V)$$

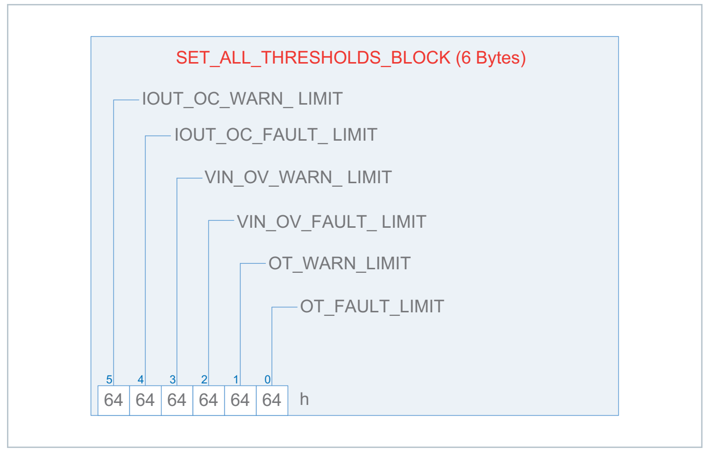
The K factor is defined in a BCM to represent the ratio of the transformer winding and hence is equal to V_{OUT} / V_{IN}.

READ_BCM_ROUT Command (D4h)

If PAGE data byte is equal to (01h - 04h) command will return a reported individual BCM's output resistance in the following format:

$$BCM\_ROUT_{ACTUAL} = BCM\_ROUT_{REPORTED} \bullet 10^{-5}(\Omega)$$

SET_ALL_THRESHOLDS Command (D5h)



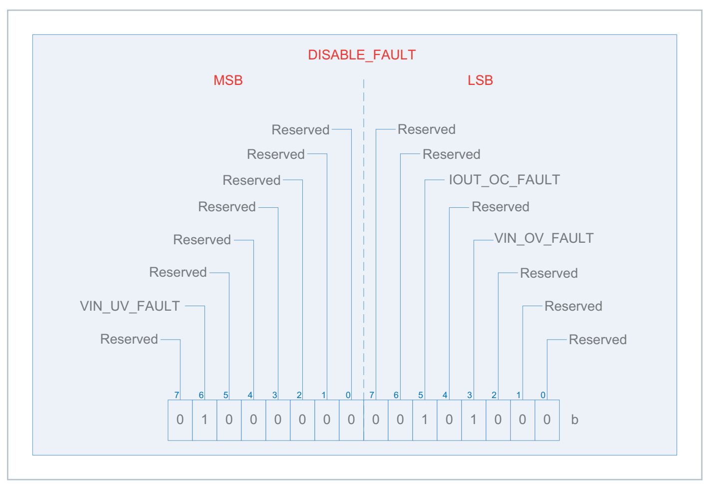
Values of this register block is set in non–volatile memory and can only be written when the BCMs are disabled.

This command provides a convenient way to configure all the limits, or any combination of limits described previously using one command.

Vin Overvoltage, Overcurrent and over–Temperature values are all set to 100% of the BCM datasheet supervisory limits by default and can only be set to a lower percentage.

To leave a particular threshold unchanged, set the corresponding threshold data byte to a value greater than (64h).

DISABLE_FAULT Command (D7h)



Unsupported bits are indicated above. A one indicates that the supervisory fault associated with the asserted bit is disabled.

The value of these registers is set in non–volatile memory and can only be written when the BCMs are disabled.

This command allows the host to disable the supervisory faults and respective statuses. It does not disable the powertrain analog protections or warnings with respect to the set limits in the SET_ALL_THRESHOLDS Command.

The input under–voltage can only be disabled to a pre–set low limit as shown in the functional reporting range in the BCM data sheet.

The internal µC Implementation vs. PMBus™ Specification Rev 1.2

The internal µC is an I²C compliant, SMBus™ compatible device and PMBus command compliant device. This section denotes some deviation, perceived as differences from the PMBus Part I and Part II specification Rev 1.2.

1. The internal µC meets all Part I and II PMBus specification requirements with the following differences to the transport requirement.

Unmet DC parameter Implementation vs SMBus™ spec						
Symbol	Parameter	D44TL1A0		SMBus™ Rev 2.0		Units
		Min	Max	Min	Max	
V_{IL}[a]	Input Low Voltage	-	0.99	-	0.8	V
V_{IH}[a]	Input High Voltage	2.31	-	2.1	V_{VDD_IN}	V
I_{LEAK_PIN}[b]	Input Leakage per Pin	10	22	-	±5	µA

[a] V_{VDD_IN} = 3.3 V
[b] V_{BUS} = 5 V

2. The internal µC accepts 38 PMBus command codes. Implemented commands execute functions as described in the PMBus specification.

- Deviations from the PMBus specification:
  - **a.** Section 15, fault related commands
    - The limits and Warnings unit implemented is percentage (%) a range from decimal (0-100) of the factory set limits.

3. The internal µC unsupported PMBus command code response as described in the Fault Management and Reporting:

- Deviations from the PMBus specification:
  - **a.** PMBus section 10.2.5.3, exceptions
    - The busy bit of the STATUS_BYTE as implemented can be cleared (80h). In order to maintain compatibility with the specification (40h) can also be used.
- Manufacturer Implementation of the PMBus Spec
  - **a.** PMBus section 10.5, setting the response to a detected fault condition
    - All powertrain responses are pre-set and cannot be changed. Refer to the BCM datasheet for details.
  - **b.** PMBus section 10.6, reporting faults and warnings to the Host
    - SMBALERT# signal and Direct PMBus Device to Host Communication are not supported. However, the Digital Supervisor will set the corresponding fault status bits and will wait for the host to poll.
  - **c.** PMBus section 10.7, clearing a shutdown due to a fault
    - There is no RESET pin or EN pin in the internal µC. Cycling power to the internal µC will not clear a BCM Shutdown. The BCM will clear itself once the fault condition is removed. Refer to the BCM datasheet for details.
  - **d.** PMBus Section 10.8.1, corrupted data transmission faults:
    - Packet error checking is not supported.

Data Transmission Faults Implementation

This section describes data transmission faults as implemented in the internal µC.

Section	Description	Response to Host		STATUS_BYTE	STATUS_CML		Notes
		NAK	FFh	CML	Other Fault	Unsupported Data	
10.8.1	Corrupted data						No response; PEC not supported
10.8.2	Sending too few bits			X	X		
10.8.3	Reading too few bits			X	X		
10.8.4	Host sends or reads too few bytes			X	X		
10.8.5	Host sends too many bytes	X		X		X	
10.8.6	Reading too many bytes		X	X	X		
10.8.7	Device busy	X	X				Device will ACK own address BUSY bit in STATUS_BYTE even if STATUS_WORD is set

Data Content Faults Implementation

This section describes data content fault as implemented in the internal μC.

Section	Description	Response to Host	STATUS_BYTE	STATUS_CML			Notes
		NAK	CML	Other Fault	Unsupported Command	Unsupported Data	
10.9.1	Improperly Set Read Bit In The Address Byte	X	X	X			
10.9.2	Unsupported Command Code	X	X		X		
10.9.3	Invalid or Unsupported Data		X			X	
10.9.4	Data Out of Range		X			X	
10.9.5	Reserved Bits						No response; not a fault

VIA BCM Sine Amplitude Converter™

The Sine Amplitude Converter (VIA BCM SAC™) uses a high frequency resonant tank to move energy from input to output. (The resonant tank is formed by Cr and Lr in the power transformer windings as shown in the BCM module Block Diagram). The resonant LC tank, operated at high frequency, is amplitude modulated as a function of input voltage and output current. A small amount of capacitance embedded in the input and output stages of the module is sufficient for full functionality and is key to achieving high
power density.

The BCM4914xD1E5135yzz VIA BCM SAC can be simplified into the preceeding model.

At no load:

$$V_{OUT} = V_{IN} \bullet K \qquad (1)$$

K represents the “turns ratio” of the VIA BCM SAC.
Rearranging Equation (1):

$$K = \frac{V_{OUT}}{V_{IN}} \qquad (2)$$

In the presence of load, V_{OUT} is represented by:

$$V_{OUT} = V_{IN} \bullet K - I_{OUT} \bullet R_{OUT} \qquad (3)$$

and I_{OUT} is represented by:

$$I_{OUT} = \frac{I_{IN} - I_Q}{K} \qquad (4)$$

R_{OUT} represents the impedance of the VIA BCM SAC, and is a function of the R_{DSON} of the input and output MOSFETs, input and output pc board resistance and the winding resistance of the power transformer. I_Q represents the quiescent current of the VIA BCM SAC control, gate drive circuitry, and core losses.

The use of DC voltage transformation provides additional interesting attributes. Assuming that $R_{OUT} = 0\ \Omega$ and $I_Q = 0$ A, Equation (3) now becomes Equation (1) and is essentially load independent, resistor R is now placed in series with V_{IN}.

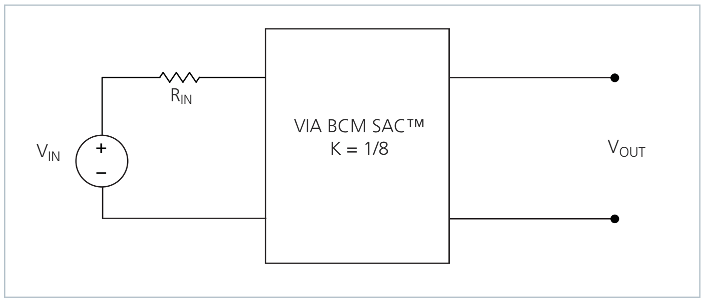


Figure 21 *— K = 1/8 Sine Amplitude Converter with series input resistor*

The relationship between V_{IN} and V_{OUT} becomes:

$$V_{OUT} = (V_{IN} - I_{IN} \bullet R_{IN}) \bullet K \qquad (5)$$

Substituting the simplified version of Equation (4)
(I_Q is assumed = 0 A) into Equation (5) yields:

$$V_{OUT} = V_{IN} \bullet K - I_{OUT} \bullet R_{IN} \bullet K^2 \qquad (6)$$

This is similar in form to Equation (3), where R_{OUT} is used to represent the characteristic impedance of the VIA BCM SAC™. However, in this case a real R on the input side of the VIA BCM SAC is effectively scaled by K^2 with respect to the output.

Assuming that R = 1 Ω, the effective R as seen from the secondary side is 15.6 mΩ, with K = 1/8 .

A similar exercise should be performed with the addition of a capacitor or shunt impedance at the input to the VIA BCM SAC. A switch in series with V_{IN} is added to the circuit. This is depicted in Figure 22.

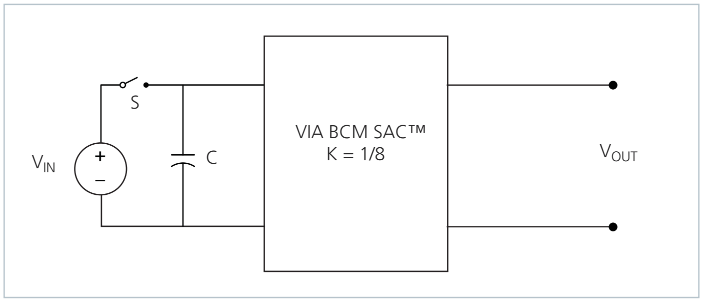


Figure 22 — *Sine Amplitude Converter with input capacitor*

A change in V_{IN} with the switch closed would result in a change in capacitor current according to the following equation:

$$I_C(t) = C\frac{dV_{IN}}{dt} \tag{7}$$

Assume that with the capacitor charged to V_{IN}, the switch is opened and the capacitor is discharged through the idealized VIA BCM SAC. In this case,

$$I_C = I_{OUT} \bullet K \tag{8}$$

substituting Equation (1) and (8) into Equation (7) reveals:

$$I_{OUT} = \frac{C}{K^2} \bullet \frac{dV_{OUT}}{dt} \tag{9}$$

The equation in terms of the output has yielded a K^2 scaling factor for C, specified in the denominator of the equation.

A K factor less than unity results in an effectively larger capacitance on the output when converted from the input. With a K = 1/8 as shown in Figure 22, C=1 µF would appear as C=64 µF when viewed from the output.

Low impedance is a key requirement for powering a high-current, low-voltage load efficiently. A switching regulation stage should have minimal impedance while simultaneously providing appropriate filtering for any switched current. The use of a VIA BCM SAC between the regulation stage and the point of load provides a dual benefit of scaling down series impedance leading back to the source and scaling up shunt capacitance or energy storage as a function of its K factor squared. However, the benefits are not useful if the series impedance of the VIA BCM SAC is too high. The impedance of the VIA BCM SAC must be low, i.e. well beyond the crossover frequency of the system.

A solution for keeping the impedance of the VIA BCM SAC low involves switching at a high frequency. This enables small magnetic components because magnetizing currents remain low. Small magnetics mean small path lengths for turns. Use of low loss core material at high frequencies also reduces core losses.

The two main terms of power loss in the VIA BCM module are:

- No load power dissipation (P_{NL}): defined as the power used to power up the module with an enabled powertrain at no load.
- Resistive loss (R_{OUT}): refers to the power loss across the VIA BCM module modeled as pure resistive impedance.

$$P_{DISSIPATED} = P_{NL} + P_{R_{OUT}} \tag{10}$$

Therefore,

$$P_{OUT} = P_{IN} - P_{DISSIPATED} = P_{IN} - P_{NL} - P_{R_{OUT}} \tag{11}$$

The above relations can be combined to calculate the overall VIA module efficiency:

$$\eta = \frac{P_{OUT}}{P_{IN}} = \frac{P_{IN} - P_{NL} - P_{R_{OUT}}}{P_{IN}} \tag{12}$$

$$= \frac{V_{IN} \bullet I_{IN} - P_{NL} - (I_{OUT})^2 \bullet R_{OUT}}{V_{IN} \bullet I_{IN}}$$

$$= 1 - \left(\frac{P_{NL} + (I_{OUT})^2 \bullet R_{OUT}}{V_{IN} \bullet I_{IN}}\right)$$

Input and Output Filtering

The VIA BCM adapter has built-in EMI filtering with hot-swap circuitry input side. EMI filtering helps to provide EN class B or class A for conducted emission. VIA BCM does not require external EMI filtering. Typical EMI spectrum is shown in figures 18, 19, and 20 for test setup as shown in Figure 23. Hot-swap circuitry provides inrush current limiting through the MOSFET.

Further, along with internal ceramic input and output capacitance, it reduces the input and output voltage ripple. External output filtering can be added as needed. Ceramic capacitance can be used as an output bypass for this purpose. Moreover, along with hot-swap circuitry, it protects the adapter from overvoltage transients imposed by a system that would exceed maximum ratings and induce stresses. Adapter input and output voltage ranges shall not be exceeded. An internal overvoltage function prevents operation outside of the normal operating input range. Even when disabled, the adapter is exposed to the applied voltage and adapter must withstand it.

Given the wide bandwidth of the adapter, the source response is generally the limiting factor in the overall system response. Anomalies in the response of the source will appear at the output of the module multiplied by its K factor.

Total load capacitance at the output of the adapter shall not exceed the specified maximum for correct operation of it in startup and steady state conditions. Owing to the wide bandwidth and low output impedance of the adapter, low frequency bypass capacitance and significant energy storage may be more densely and efficiently provided by adding capacitance at the input of the adapter. At frequencies less than 500 KHz, the adapter appears as an impedance of R_{OUT} between the source and load.

Within this frequency range, capacitance at the input appears as effective capacitance on the output per the relationship defined in equatiion (13).

$$C_{OUT} = \frac{C_{IN}}{K^2} \qquad (13)$$

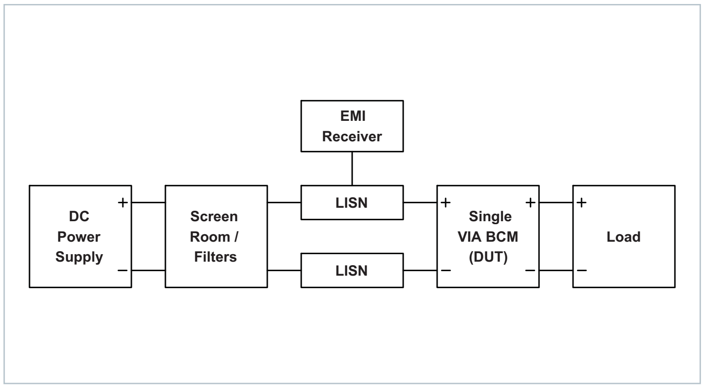


***Figure 23 –** Typical test set-up block diagram for Conducted Emissions*

Note: The measurement were evaluated against the class A and class B limits of EN55022. Testing was performed with -OUT terminal of VIA BCM connected to Chassis and Chassis was grounded.

Thermal Considerations

The VIA™ package provides effective conduction cooling from either of the two module surfaces. Heat may be removed from the top surface, the bottom surface or both. The extent to which these two surfaces are cooled is a key component for determining the maximum power that can be processed by a VIA, as can be seen from specified thermal operating area in Figure 1. Since the VIA has a maximum internal temperature rating, it is necessary to estimate this internal temperature based on a system-level thermal solution. To this purpose, it is helpful to simplify the thermal solution into a roughly equivalent circuit where power dissipation is modeled as a current source, isothermal surface temperatures are represented as voltage sources and the thermal resistances are represented as resistors. Figure 24 shows the "thermal circuit" for the VIA module.

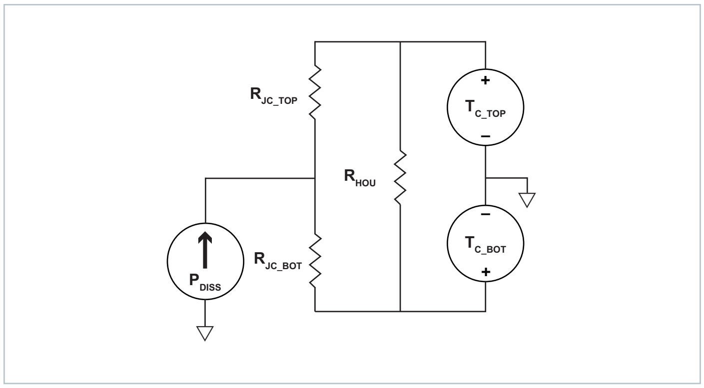


***Figure 24 –** Double sided cooling VIA thermal model*

In this case, the internal power dissipation is P_{DISS}, R_{JC_TOP} and R_{JC_BOT} are thermal resistance characteristics of the VIA module and the top and bottom surface temperatures are represented as T_{C_TOP}, and T_{C_BOT}. It interesting to notice that the package itself provides a high degree of thermal coupling between the top and bottom case surfaces (represented in the model by the resistor R_{HOU}). This feature enables two main options regarding thermal designs:

- Single side cooling: the model of Figure 24 can be simplified by calculating the parallel resistor network and using one simple thermal resistance number and the internal power dissipation curves; an example for bottom side cooling only is shown in Figure 25.

In this case, R_{JC} can be derived as following:

$$R_{JC} = \frac{(R_{JC\_TOP} + R_{HOU}) \bullet R_{JC\_BOT}}{R_{JC\_TOP} + R_{HOU} + R_{JC\_BOT}} \qquad (14)$$

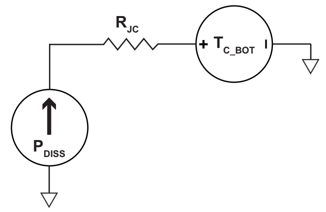


***Figure 25** – Single-sided cooling VIA thermal model*

- Double side cooling: while this option might bring limited advantage to the module internal components (given the surface-to-surface coupling provided), it might be appealing in cases where the external thermal system requires allocating power to two different elements, like for example heatsinks with independent airflows or a combination of chassis/air cooling.

Current Sharing

The performance of the VIA BCM SAC™ topology is based on efficient transfer of energy through a transformer without the need of closed loop control. For this reason, the transfer characteristic can be approximated by an ideal transformer with a positive temperature coefficient series resistance.

This type of characteristic is close to the impedance characteristic of a DC power distribution system both in dynamic (AC) behavior and for steady state (DC) operation.

When multiple VIA BCM modules of a given part number are connected in an array they will inherently share the load current according to the equivalent impedance divider that the system implements from the power source to the point of load.

Some general recommendations to achieve matched array impedances include:

- Dedicate common copper planes/wires within the PCB/Chassis to deliver and return the current to the VIA modules.
- Provide as symmetric a PCB/Wiring layout as possible among VIA™ modules

For further details see AN:016 Using BCM Bus Converters in High Power Arrays.

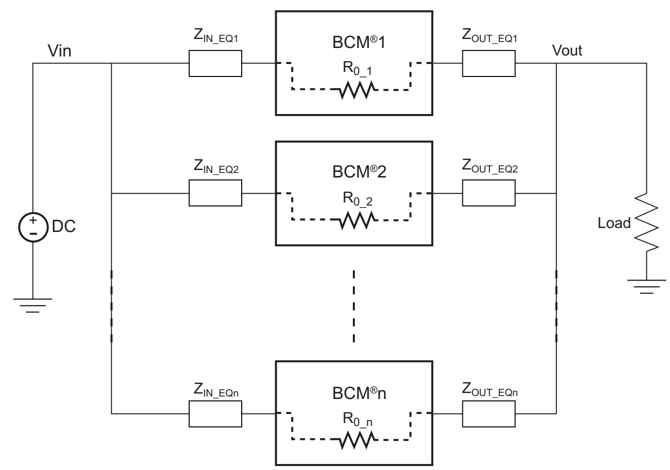


***Figure 26** — VIA BCM module array*

Fuse Selection

In order to provide flexibility in configuring power systems Adapter modules are not internally fused. Input line fusing of Adapter products is recommended at system level to provide thermal protection in case of catastrophic failure.

The fuse shall be selected by closely matching system requirements with the following characteristics:

- Current rating
  (usually greater than maximum current of VIA BCM module)
- Maximum voltage rating
  (usually greater than the maximum possible input voltage)
- Ambient temperature
- Nominal melting I^2t
- Recommend fuse: 10 A Littelfuse 505 Series or 10 A Littelfuse 487 Series.

Reverse Operation

VIA BCM modules are capable of reverse power operation. Once the unit is started, energy will be transferred from secondary back to the primary whenever the secondary voltage exceeds V_{IN} • K. The module will continue operation in this fashion for as long as no faults occur.

The BCM4914xD1E5135yzz has not been qualified for continuous operation in a reverse power condition. Furthermore fault protections which help protect the module in forward operation will not fully protect the module in reverse operation.

Transient operation in reverse is expected in cases where there is significant energy storage on the output and transient voltages appear on the input. Transient reverse power operation of less than 10 ms, 10% duty cycle is permitted and has been qualified to cover these cases.

Dielectric Withstand

The chassis of the VIA BCM is required to be connected to Protective Earth when installed in the end application and must satisfy the requirements of IEC 60950-1 for Class I products.

The VIA BCM contains an internal safety approved isolating component (VI ChiP) that provides the Reinforced Insulation from Input to Output. The isolating component is individually tested for Reinforced Insulation from Input to Output at 3000 Vac or 4242 Vdc prior to the final assembly of the VIA™.

When the VIA™ assembly is complete the Reinforced Insulation can only be tested at Basic Insulation values as specified in the electric strength Test Procedure noted in clause 5.2.2 of IEC 60950-1.

Test Procedure Note from IEC 60950-1

"For equipment incorporating both REINFORCED INSULATION and lower grades of insulation, care is taken that the voltage applied to the REINFORCED INSULATION does not overstress BASIC INSULATION or SUPPLEMENTARY INSULATION."

Summary

The final VIA assembly contains basic insulation from input to case, reinforced insulation from input to output, and functional insulation from output to case.Both sides of the housing are required to be connected to Protective Earth to satisfy safety and EMI requirements. Protective earthing can be accomplished through dedicated wiring harness (example: ring terminal clamped by mounting screw) or surface contact (example: pressure contact on bare conductive chassis or PCB copper layer with no solder mask).

The output of the VIA complies with the requirements of SELV circuits so only functional insulation is required from the output (SELV) to case (PE) because the case is required to be connected to protective earth in the final installation. The construction of the VIA can be summarized by describing it as a "Class II" component installed in a "Class I" subassembly. The reinforced insulation from input to output can only be tested at basic insulation values on the completely assembled VIA product.

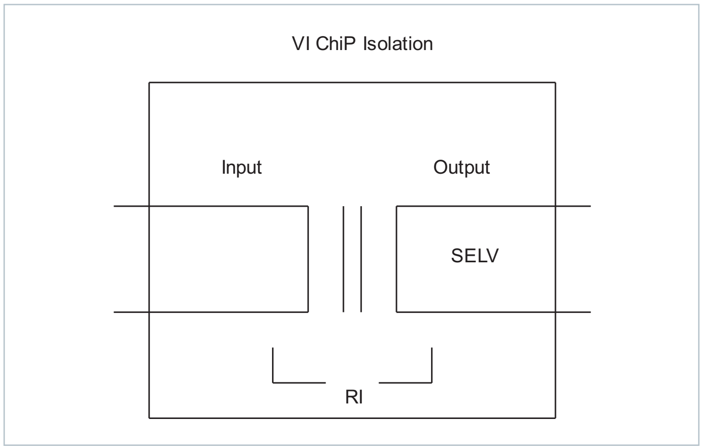


Figure 27 – *VI Chip before final assembly in the VIA*

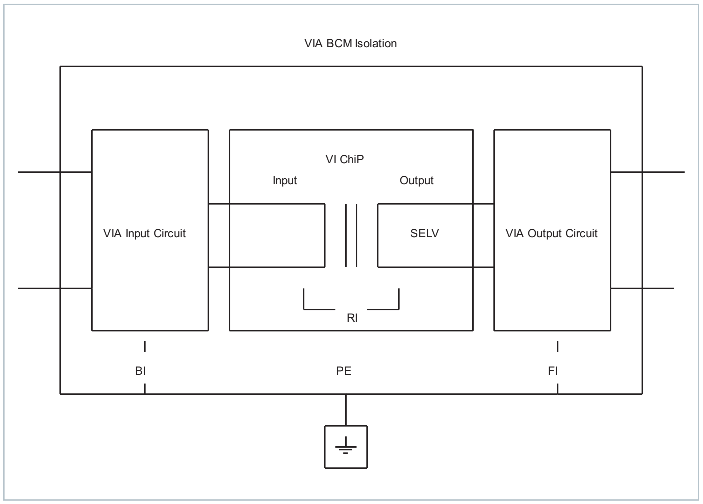


Figure 28 – *BCM VIA after final assembly*

Hot Swap

Many applications use a power architecture based on a 380 Vdc distribution bus. This supply level is emerging as a new standard and efficient means for distributing power through boards, racks and chassis mounted Telecom and Datacom system. The interconnect between the different modules is accomplished with a backplane and motherboard. Power is commonly provided to the various module slots via a 380 Vdc distribution bus.

Removing the faulty module from the rack is relatively easy, provided the remaining power modules can support the step increase in load. Plugging in the replacement module has more potential for problems, as it will present an uncharged capacitor load and draw a large inrush current. This could cause a momentary, but unacceptable interruption or sag to the backplane power bus if not limited. The problem can also arise if ordinary power module connectors are used, since the connector pins will engage and disengage in a random and unpredictable sequence during insertion and removal.

Hot swap or hot plug is the highly desirable feature in many applications, but it also creates several issues that must be addressed in the system design. A number of related phenomena occur with a live insertion and removal event, including bouncing, arcing between input connector pins, larger voltage and current transients. Hot swap circuitry in the converter modules protects the module and the rest of the system from the problem associated with live insertion.

To meet the maintenance, reconfiguration, redundancy and system upgrade, this new VIA BCM module is being designed to address the function of hot-swapping at the 380 Vdc distribution bus. This new module provides a high level of integration for DC to DC converters in 380 Vdc distributions, saving the system designer design time and critical board space. Hot swap circuitry as shown in Figure 29 uses an active MOSFET switching device in the input line. During insertion, the MOSFET is driven into a resistive state to limit the inrush current, and then when the inserted module's input capacitor has charged, the MOSFET becomes fully conductive to avoid the voltage drop losses. Performance verification is further illustrated through scope plots of circuit's response to various live insertion events.

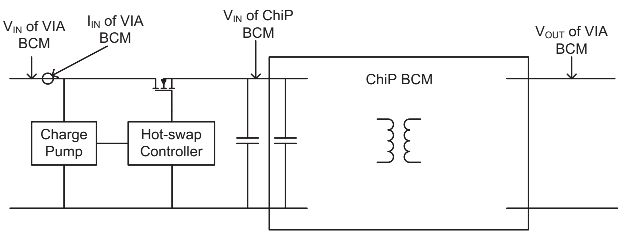


***Figure 29** – High-Level Diagram for 384 Vdc Hot Swap with ChiP BCM DC-DC converter*

Overall, the objective is always remains the same in hot swap applications; to give system designer the opportunity to build hot swap capability into redundant power module arrays. This allows telecoms and other mission critical applications to continue without interruption even through failure and replacement of one or possibly more of their power modules.

Hot Swap Test – Test circuit and Procedure

- Two VIA BCMs in parallel with mercury relay#1 open
- Close mercury relay#1 and measure inrush current going into #2 VIA BCM

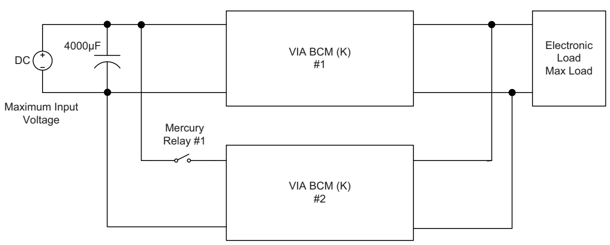


***Figure 30** – Test Circuit*

Hot Swap Test – Scope Pictures

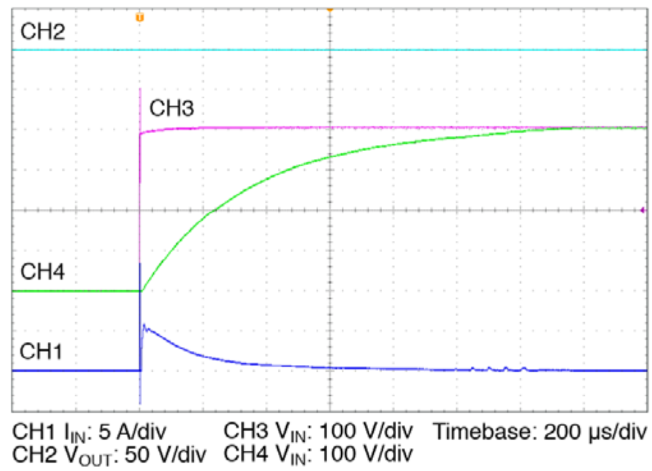


***Figure 31** – Hot swap start-up*

Ch1: I_{IN} of VIA BCM#2
Ch2: V_{OUT} of VIA BCM#2
Ch3: V_{IN} of VIA BCM#2 shows the fast input voltage transient at the input terminal of VIA BCM#2
Ch4: V_{IN} of ChiP BCM#2 shows the soft start charging the input capacitor as shown, time constant depends upon the gate signal.

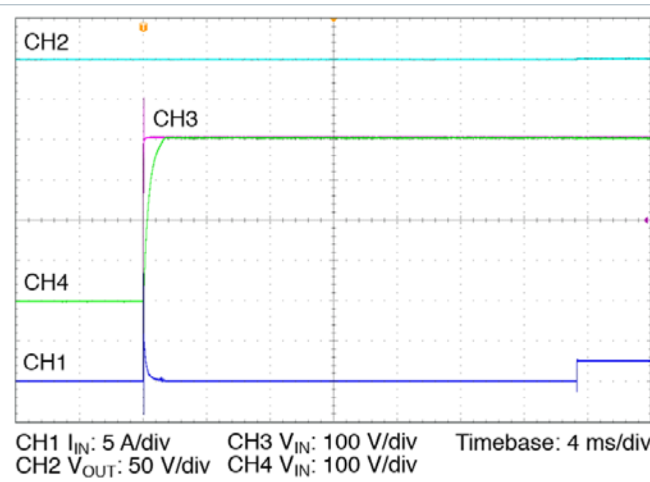
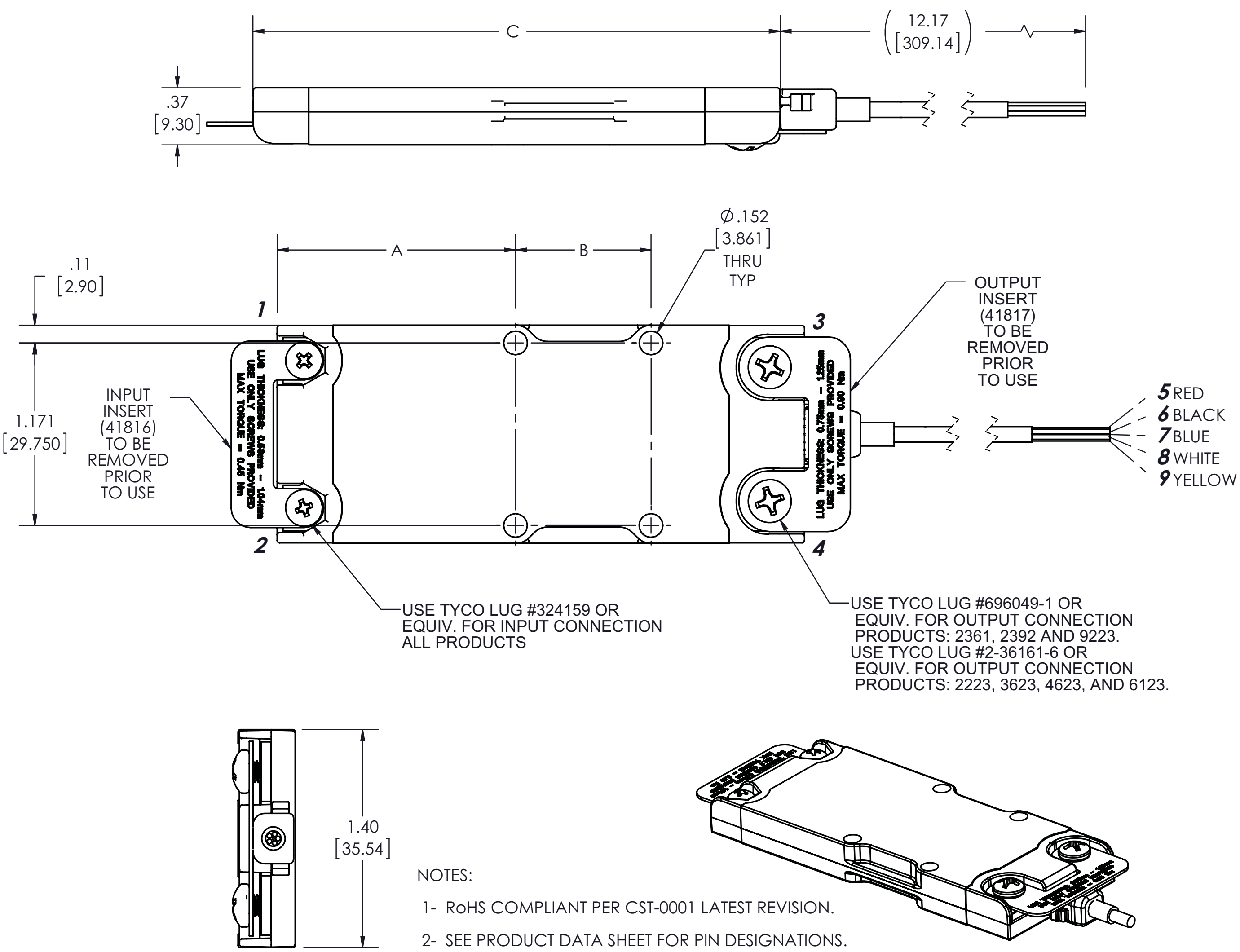


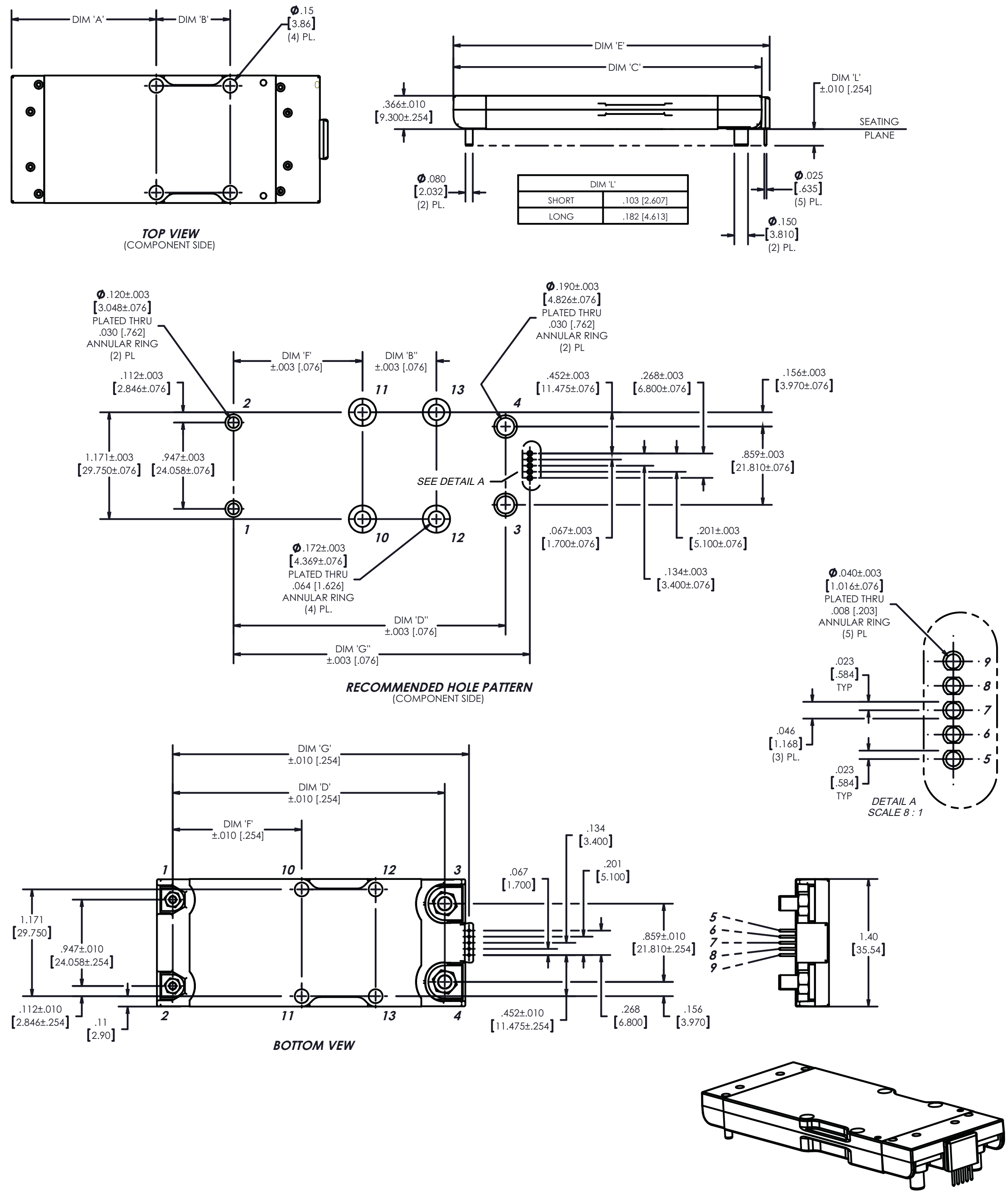
***Figure 32** – Same as figure 31 but at a bigger time scale shows the appearance of the VIA BCM#2 output*

VIA BCM Bus Converter Lug Mount, Cable, Adapter, Mechanical Drawing and Recommended Hole Pattern



PRODUCT	DIM 'A'	DIM 'B'	DIM 'C'
4914 VIA BCM	2.17 [55.15]	1.757 [44.625]	4.91 [124.77]

VIA BCM Bus Converter PCB Mount, Connector, Adapter, Mechanical Drawing and Recommended Hole Pattern



NOTES:

1- RoHS COMPLIANT PER CST-0001 LATEST REVISION.

2- SEE PRODUCT DATA SHEET FOR PIN DESIGNATIONS.

PRODUCT	DIM 'A'	DIM 'B'	DIM 'C'	DIM 'D'	DIM 'E'	DIM 'F'	DIM 'G'
4914 VIA BCM	2.17 [55.15]	1.757 [44.625]	4.91 [124.77]	4.517 [114.741]	5.00 [126.98]	1.999 [50.777]	4.781 [121.430]

Revision History

Revision	Date	Description	Page Number(s)
1.0	05/15/15	Initial release	n/a
1.1	06/10/15	Recommended Resistor (ID 1) Summary note added Updated Pin Information	18 34 37
1.2	07/07/15	Reassigned figures and figure numbers	12-14 30-35

Vicor's comprehensive line of power solutions includes high density AC-DC and DC-DC modules and accessory components, fully configurable AC-DC and DC-DC power supplies, and complete custom power systems.

Information furnished by Vicor is believed to be accurate and reliable. However, no responsibility is assumed by Vicor for its use. Vicor makes no representations or warranties with respect to the accuracy or completeness of the contents of this publication. Vicor reserves the right to make changes to any products, specifications, and product descriptions at any time without notice. Information published by Vicor has been checked and is believed to be accurate at the time it was printed; however, Vicor assumes no responsibility for inaccuracies. Testing and other quality controls are used to the extent Vicor deems necessary to support Vicor's product warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

Specifications are subject to change without notice.

Vicor's Standard Terms and Conditions

All sales are subject to Vicor's Standard Terms and Conditions of Sale, which are available on Vicor's webpage or upon request.

Product Warranty

In Vicor's standard terms and conditions of sale, Vicor warrants that its products are free from non-conformity to its Standard Specifications (the "Express Limited Warranty"). This warranty is extended only to the original Buyer for the period expiring two (2) years after the date of shipment and is not transferable.

UNLESS OTHERWISE EXPRESSLY STATED IN A WRITTEN SALES AGREEMENT SIGNED BY A DULY AUTHORIZED VICOR SIGNATORY, VICOR DISCLAIMS ALL REPRESENTATIONS, LIABILITIES, AND WARRANTIES OF ANY KIND (WHETHER ARISING BY IMPLICATION OR BY OPERATION OF LAW) WITH RESPECT TO THE PRODUCTS, INCLUDING, WITHOUT LIMITATION, ANY WARRANTIES OR REPRESENTATIONS AS TO MERCHANTABILITY, FITNESS FOR PARTICULAR PURPOSE, INFRINGEMENT OF ANY PATENT, COPYRIGHT, OR OTHER INTELLECTUAL PROPERTY RIGHT, OR ANY OTHER MATTER.

This warranty does not extend to products subjected to misuse, accident, or improper application, maintenance, or storage. Vicor shall not be liable for collateral or consequential damage. Vicor disclaims any and all liability arising out of the application or use of any product or circuit and assumes no liability for applications assistance or buyer product design. Buyers are responsible for their products and applications using Vicor products and components. Prior to using or distributing any products that include Vicor components, buyers should provide adequate design, testing and operating safeguards.

Vicor will repair or replace defective products in accordance with its own best judgment. For service under this warranty, the buyer must contact Vicor to obtain a Return Material Authorization (RMA) number and shipping instructions. Products returned without prior authorization will be returned to the buyer. The buyer will pay all charges incurred in returning the product to the factory. Vicor will pay all reshipment charges if the product was defective within the terms of this warranty.

Life Support Policy

VICOR'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS PRIOR WRITTEN APPROVAL OF THE CHIEF EXECUTIVE OFFICER AND GENERAL COUNSEL OF VICOR CORPORATION. As used herein, life support devices or systems are devices which (a) are intended for surgical implant into the body, or (b) support or sustain life and whose failure to perform when properly used in accordance with instructions for use provided in the labeling can be reasonably expected to result in a significant injury to the user. A critical component is any component in a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system or to affect its safety or effectiveness. Per Vicor Terms and Conditions of Sale, the user of Vicor products and components in life support applications assumes all risks of such use and indemnifies Vicor against all liability and damages.

Intellectual Property Notice

Vicor and its subsidiaries own Intellectual Property (including issued U.S. and Foreign Patents and pending patent applications) relating to the products described in this data sheet. No license, whether express, implied, or arising by estoppel or otherwise, to any intellectual property rights is granted by this document. Interested parties should contact Vicor's Intellectual Property Department.

The products described on this data sheet are protected by the following U.S. Patents Pending

Vicor Corporation
25 Frontage Road
Andover, MA, USA 01810
Tel: 800-735-6200
Fax: 978-475-6715

email
Customer Service: custserv@vicorpower.com
Technical Support: apps@vicorpower.com