

4M × 4 Bit CMOS Dynamic RAM with Static Column Mode

FEATURES

• Performance range:

	trAC	tcAC	trc
KM44C4002A/AL/ALL/ASL-5	50ns	13ns	90ns
KM44C4002A/AL/ALL/ASL-6	60ns	15ns	110ns
KM44C4002A/AL/ALL/ASL-7	70ns	20ns	130ns
KM44C4002A/AL/ALL/ASL-8	80ns	20ns	150ns

- Static Column Mode operation
- Self Refresh Operation (LL-ver, only)
- CS-before-RAS refresh capability
- RAS-only and Hidden Refresh capability
- Fast parallel test mode Capability
- TTL compatible inputs and outputs
- Early write or output enable controlled write
- Single+5.0V ± 10% power supply
- 4096 cycles/64ms refresh (Normal)
- 4096 cycles/128ms refresh (Low power & Self Ref.)
- 4096 cycles/256ms refresh (Super Low power)
- JEDEC standard pinout
- Available in plastic SOJ and TSOP(II)

GENERAL DESCRIPTION

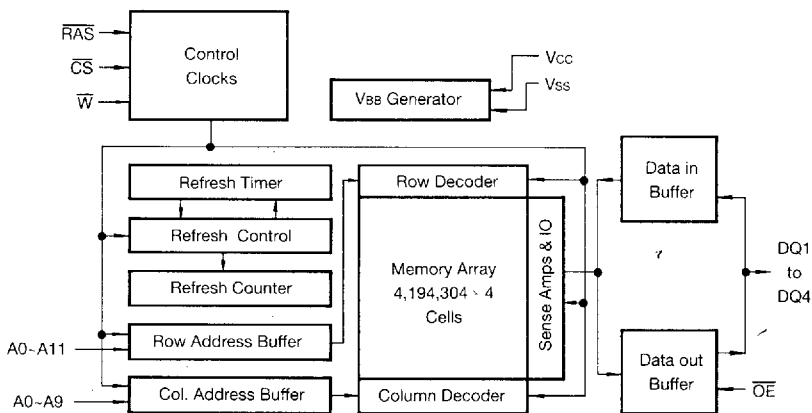
The Samsung KM44C4002A/AL/ALL/ASL is a high speed CMOS 4,194,304 bit × 4 Dynamic Random Access Memory. Its design is optimized for high performance applications such as mainframes, mini computers, graphics and high performance portable computers.

The KM44C4002A/AL/ALL/ASL features Static Column Mode operation which allows high speed random access of memory cells within the same row.

$\overline{CS}$ -before- $\overline{RAS}$  refresh capability provides on-chip auto refresh as an alternative to  $\overline{RAS}$ -only refresh. All inputs and outputs are fully TTL compatible.

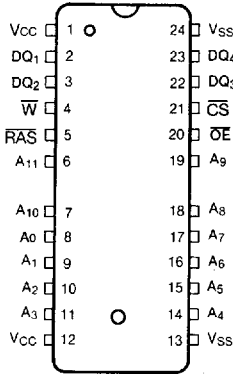
The KM44C4002A/AL/ALL/ASL is fabricated using Samsung's advanced CMOS process.

FUNCTIONAL BLOCK DIAGRAM



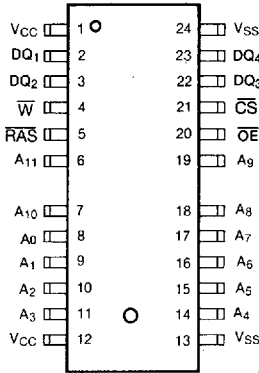
PIN CONFIGURATION (Top Views)

• KM44C4002 AJ/ALJ/ALLJ/ASLJ  
AK/ALK/ALLK/ASLK



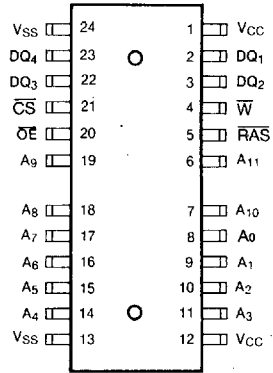
J : 400MIL  
K : 300MIL

• KM44C4002 AT/ALT/ALLT/ASLT  
AS/ALS/ALLS/ASLS



T : 400MIL(Forward)  
S : 300MIL(Forward)

• KM44C4002 ATR/ALTR/ALLTR/ASLTR  
ASR/ALSR/ALLSR/ASLSR



TR : 400MIL(Reverse)  
SR : 300MIL(Reverse)

Pin Name	Pin Function
A0-A11	Address Inputs
DQ1-4	Data In/Out
Vss	Ground
RAS	Row Address Strobe
CS	Chip Select input
W	Read/Write Input
OE	Data Output Enable
Vcc	Power(+5.0V)
N.C	No Connection

**ABSOLUTE MAXIMUM RATINGS**

Parameter	Symbol	Rating	Units
Voltage on Any Pin Relative to V <sub>SS</sub>	V <sub>IN</sub> , V <sub>OUT</sub>	-1 to + 7.0	V
Voltage on V <sub>CC</sub> Supply Relative to V <sub>SS</sub>	V <sub>CC</sub>	-1 to + 7.0	V
Storage Temperature	T <sub>stg</sub>	-55 to + 150	°C
Power Dissipation	P <sub>D</sub>	1	W
Short Circuit Output Current	I <sub>OS</sub>	50	mA

\* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**RECOMMENDED OPERATING CONDITIONS** (Voltage referenced to V<sub>SS</sub>, T<sub>A</sub>=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V <sub>CC</sub>	4.5	5.0	5.5	V
Ground	V <sub>SS</sub>	0	0	0	V
Input High Voltage	V <sub>IH</sub>	2.4	—	V <sub>CC</sub> + 1	V
Input Low Voltage	V <sub>IL</sub>	-1.0	—	0.8	V

**DC AND OPERATING CHARACTERISTICS** (Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Units
Operating Current* (R <sub>AS</sub> and C <sub>S</sub> Cycling @ t <sub>RC</sub> =min.)	KM44C4002A/AL/ALL/ASL-5	I <sub>CC1</sub>	-	90	mA
	KM44C4002A/AL/ALL/ASL-6			80	mA
	KM44C4002A/AL/ALL/ASL-7			70	mA
	KM44C4002A/AL/ALL/ASL-8			60	mA
Standby Current (R <sub>AS</sub> =C <sub>S</sub> =W=V <sub>IH</sub> )	KM44C4002A	I <sub>CC2</sub>	-	2	mA
	KM44C4002AL			1	mA
	KM44C4002ALL			1	mA
	KM44C4002ASL			1	mA
R <sub>AS</sub> -Only Refresh Current* (C <sub>S</sub> =V <sub>IH</sub> , R <sub>AS</sub> Cycling @ t <sub>RC</sub> =min.)	KM44C4002A/AL/ALL/ASL-5	I <sub>CC3</sub>	-	90	mA
	KM44C4002A/AL/ALL/ASL-6			80	mA
	KM44C4002A/AL/ALL/ASL-7			70	mA
	KM44C4002A/AL/ALL/ASL-8			60	mA
Fast Page Mode Current* (R <sub>AS</sub> =V <sub>IL</sub> , C <sub>S</sub> , Address Cycling @ t <sub>PC</sub> =min.)	KM44C4002A/AL/ALL/ASL-5	I <sub>CC4</sub>	-	80	mA
	KM44C4002A/AL/ALL/ASL-6			70	mA
	KM44C4002A/AL/ALL/ASL-7			60	mA
	KM44C4002A/AL/ALL/ASL-8			50	mA
Standby Current (R <sub>AS</sub> =C <sub>S</sub> =W=V <sub>CC</sub> -0.2V)	KM44C4002A	I <sub>CC5</sub>	-	1	mA
	KM44C4002AL			300	μA
	KM44C4002ALL			200	μA
	KM44C4002ASL			200	μA
C <sub>S</sub> -Before-R <sub>AS</sub> Refresh Current* (R <sub>AS</sub> and C <sub>S</sub> Cycling @ t <sub>RC</sub> =min.)	KM44C4002A/AL/ALL/ASL-5	I <sub>CC6</sub>	-	90	mA
	KM44C4002A/AL/ALL/ASL-6			80	mA
	KM44C4002A/AL/ALL/ASL-7			70	mA
	KM44C4002A/AL/ALL/ASL-8			60	mA
Battery Back Up Current Average Power Supply Current, Battery Back Up Mode, Input High Voltage(V <sub>IH</sub> )=V <sub>CC</sub> -0.2V Input Low Voltage(V <sub>IL</sub> )=0.2V C <sub>S</sub> =C <sub>S</sub> -Before-R <sub>AS</sub> Cycling or 0.2V DQ1-DQ4=Don't Care t <sub>RC</sub> =31.25μs(L-Ver.) 62.5μs(SL-Ver.), t <sub>RAS</sub> =t <sub>RAS</sub> min-300ns	KM44C4002AL	I <sub>CC7</sub>	-	450	μA
	KM44C4002ASL			350	μA

## DC AND OPERATING CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Units
Self Refresh Current RAS=CS=0.2V W=OE=A0-A11=Vcc-0.2V or 0.2V DQ1-DQ4=Vcc-0.2V, 0.2V or Open	ICC5	-	300	μA
Input Leakage Current (Any input $0 \leq V_{IN} \leq V_{CC} + 0.5V$ , all other pins not under test=0 volts.)	IIL	-10	10	μA
Output Leakage Current (Data out is disabled, $0V \leq V_{OUT} \leq V_{CC}$ )	IOL	-10	10	μA
Output High Voltage Level (IOH=5mA)	VOH	2.4	-	V
Output Low Voltage Level (IOL=4.2mA)	VOL	-	0.4	V

\*NOTE: ICC1, ICC3, ICC4 and ICC6 are dependent on output loading and cycle rates. Specified values are obtained with the output open. ICC is specified as an average current. In ICC1 and ICC3, Address can be changed maximum two times while RAS=VIL. In ICC4, Address can be changed maximum once within one Static Column cycle.

## CAPACITANCE (TA=25°C, VCC=5V, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input Capacitance (A0-A11)	CIN1	-	5	pF
Input Capacitance (RAS, CS, W, OE)	CIN2	-	7	pF
Input Capacitance (DQ1-DQ4)	CdQ	-	7	pF

## AC CHARACTERISTICS (0°C ≤ Ta ≤ 70°C, VCC=5.0V ± 10%, See notes 1,2)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	trc	90		110		130		150		ns	
Read-modify-write cycle time	trwc	133		155		185		205		ns	
Access time from RAS	trac		50		60		70		80	ns	3,4,11
Access time from CS	tcac		13		15		20		20	ns	3,4,5
Access time from column address	tAA		25		30		35		40	ns	3,11
CS to output in Low-Z	tCLZ	0		0		0		0		ns	3
Output buffer turn-off delay	tOFF	0	15	0	15	0	20	0	20	ns	7
Transition time (rise and fall)	tT	3	50	3	50	3	50	3	50	ns	2
RAS precharge time	trp	30		40		50		60		ns	
RAS pulse width	trAS	50	10,000	60	10,000	70	10,000	80	10,000	ns	
RAS hold time	trSH	13		15		20		20		ns	
CS hold time	tCSH	50		60		70		80		ns	
CS pulse width	tCS	13	10,000	15	10,000	20	10,000	20	10,000	ns	
RAS to CS delay time	trCD	20	37	20	45	20	50	20	60	ns	4
RAS to column address delay time	trAD	15	25	15	30	15	35	15	40	ns	11
CS to RAS precharge time	tCRP	5		5		5		5		ns	
Row address set-up time	tASR	0		0		0		0		ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Row address hold time	trAH	10		10		10		10		ns	
Column address set-up time	tASC	0		0		0		0		ns	
Column address hold time	tCAH	10		10		15		15		ns	
Column address hold time referenced to $\overline{\text{RAS}}$	tAR	40		50		55		60		ns	6
Column address to $\overline{\text{RAS}}$ lead time	trAL	25		30		35		40		ns	
Read command set-up time	trCS	0		0		0		0		ns	
Read command hold time referenced to $\overline{\text{CS}}$	trCH	0		0		0		0		ns	9
Read command hold time referenced to $\overline{\text{RAS}}$	trRH	0		0		0		0		ns	
Write command hold time	twCH	10		10		15		15		ns	
Write command hold time referenced to $\overline{\text{RAS}}$	twCR	40		45		55		60		ns	6
Write command pulse width	tWP	10		10		15		15		ns	
Write command to $\overline{\text{RAS}}$ lead time	trWL	15		15		20		20		ns	
Write command to $\overline{\text{CS}}$ lead time	tcWL	13		15		20		20		ns	
Data set-up time	tDS	0		0		0		0		ns	10
Data hold time	tDH	10		10		15		15		ns	10
Data hold time referenced to $\overline{\text{RAS}}$	tDHR	40		50		55		60		ns	6
Refresh period (Normal)	tREF		64		64		64		64	ms	
Refresh period (Low power & Self Ref.)	tREF		128		128		128		128	ms	
Refresh period (Super Low power)	tREF		256		256		256		256	ms	
Write command set-up time	twCS	0		0		0		0		ns	8
$\overline{\text{CS}}$ to $\overline{\text{W}}$ delay time	tcWD	36		40		50		50		ns	8
$\overline{\text{RAS}}$ to $\overline{\text{W}}$ delay time	trWD	73		85		100		110		ns	8
Column address to $\overline{\text{W}}$ delay time	tAWD	48		55		65		70		ns	8
$\overline{\text{CS}}$ set-up time ( $\overline{\text{CS}}$ -before- $\overline{\text{RAS}}$ refresh)	tCSR	10		10		10		10		ns	
$\overline{\text{CS}}$ hold time ( $\overline{\text{CS}}$ -before- $\overline{\text{RAS}}$ refresh)	tCHR	10		10		15		15		ns	
$\overline{\text{RAS}}$ to $\overline{\text{CS}}$ precharge time	trPC	5		5		5		5		ns	
$\overline{\text{CS}}$ precharge time ( $\overline{\text{C}}$ -B- $\overline{\text{R}}$ counter test cycle)	tcPT	20		20		30		30		ns	
Static column mode cycle time	tSC	30		35		40		45		ns	3
Static column mode read-write cycle time	tSRWC	80		85		100		110		ns	
Access time from last write	tALW		50		55		65		75	ns	3, 12
Output data hold time from column address	tAOH	5		5		5		5		ns	
Output data enable time from $\overline{\text{W}}$	tOW		35		40		45		55	ns	
$\overline{\text{RAS}}$ pulse width (Static column mode)	trASC	50	200000	60	200000	70	200000	80	200000	ns	
$\overline{\text{CS}}$ pulse width (Static column mode)	tcSC	13	200000	15	200000	20	200000	20	200000	ns	
$\overline{\text{CS}}$ precharge time (Static column mode)	tcp	10		10		10		10		ns	
Column address hold time referenced to $\overline{\text{RAS}}$ rising	tAH	5		5		5		5		ns	
Last write to column address delay time	tlWAD	20	25	20	25	25	30	25	35	ns	
Last write to column address hold time	tAHLW	50		55		65		75		ns	

5



AC CHARACTERISTICS (Continued)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Write command inactive time	t <sub>WI</sub>	10		10		10		10		ns	
$\overline{RAS}$ hold time referenced to $\overline{OE}$	t <sub>ROH</sub>	13		15		20		20		ns	
Write address hold time referenced to $\overline{RAS}$	t <sub>AWR</sub>	40		45		55		60		ns	6
$\overline{OE}$ access time	t <sub>OEA</sub>		13		15		20		20	ns	
$\overline{OE}$ to data delay	t <sub>OED</sub>	13		15		20		20		ns	
Output buffer turn off delay time from $\overline{OE}$	t <sub>OEZ</sub>	0	13	0	15	0	20	0	20	ns	
$\overline{OE}$ command hold time	t <sub>OEH</sub>	13		15		20		20		ns	
Write command set-up time (Test mode in)	t <sub>WTS</sub>	10		10		10		10		ns	
Write command hold time (Test mode in)	t <sub>WTH</sub>	10		10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ precharge time ( $\overline{C}$ - $\overline{B}$ - $\overline{R}$ refresh)	t <sub>WRP</sub>	10		10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time ( $\overline{C}$ - $\overline{B}$ - $\overline{R}$ refresh)	t <sub>WRH</sub>	10		10		10		10		ns	
$\overline{RAS}$ pulse width ( $\overline{C}$ - $\overline{B}$ - $\overline{R}$ self refresh)	t <sub>RASS</sub>	100		100		100		100		$\mu$ s	15
$\overline{RAS}$ precharge time ( $\overline{C}$ - $\overline{B}$ - $\overline{R}$ self refresh)	t <sub>RPS</sub>	90		110		130		150		ns	15
$\overline{CS}$ hold time ( $\overline{C}$ - $\overline{B}$ - $\overline{R}$ self refresh)	t <sub>CHS</sub>	-50		-50		-50		-50		ns	15

TEST MODE CYCLE

(Note.12)

Parameter	Symbol	-5		-6		-7		-8		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t <sub>RC</sub>	95		115		135		155		ns	
Read-modify-write cycle time	t <sub>RWC</sub>	140		160		190		210		ns	
Access time from $\overline{RAS}$	t <sub>RAC</sub>		55		65		75		85	ns	3,4,11
Access time from $\overline{CS}$	t <sub>CAC</sub>		18		20		25		25	ns	3,4,5
Access time from column address	t <sub>AAC</sub>		30		35		40		45	ns	3,11
$\overline{RAS}$ pulse width	t <sub>RAS</sub>	55	10,000	65	10,000	75	10,000	85	10,000	ns	
$\overline{CS}$ pulse width	t <sub>CS</sub>	18	10,000	20	10,000	25	10,000	25	10,000	ns	
$\overline{RAS}$ hold time	t <sub>RSH</sub>	20		20		25		25		ns	
$\overline{CS}$ hold time	t <sub>CSH</sub>	55		65		75		85		ns	
Column address to $\overline{RAS}$ lead time	t <sub>RAL</sub>	30		35		40		45		ns	
$\overline{CS}$ to $\overline{W}$ delay time	t <sub>CWD</sub>	45		45		55		55		ns	8
$\overline{RAS}$ to $\overline{W}$ delay time	t <sub>RWD</sub>	80		90		105		115		ns	8
Column address to $\overline{W}$ delay time	t <sub>AWD</sub>	55		60		70		75		ns	8
Static column mode cycle time	t <sub>SC</sub>	35		40		45		50		ns	
Static column mode read-write cycle time	t <sub>SRWC</sub>	85		90		105		110		ns	
$\overline{RAS}$ pulse width (Static column mode)	t <sub>RASC</sub>	55	200,000	65	200,000	75	200,000	85	200,000	ns	
Access time from last write	t <sub>ALW</sub>		55		60		70		80	ns	3,12
$\overline{OE}$ access time	t <sub>OEA</sub>		18		20		25		25	ns	
$\overline{OE}$ to data delay	t <sub>OED</sub>	18		20		25		25		ns	
$\overline{OE}$ command hold time	t <sub>OEH</sub>	18		20		25		25		ns	

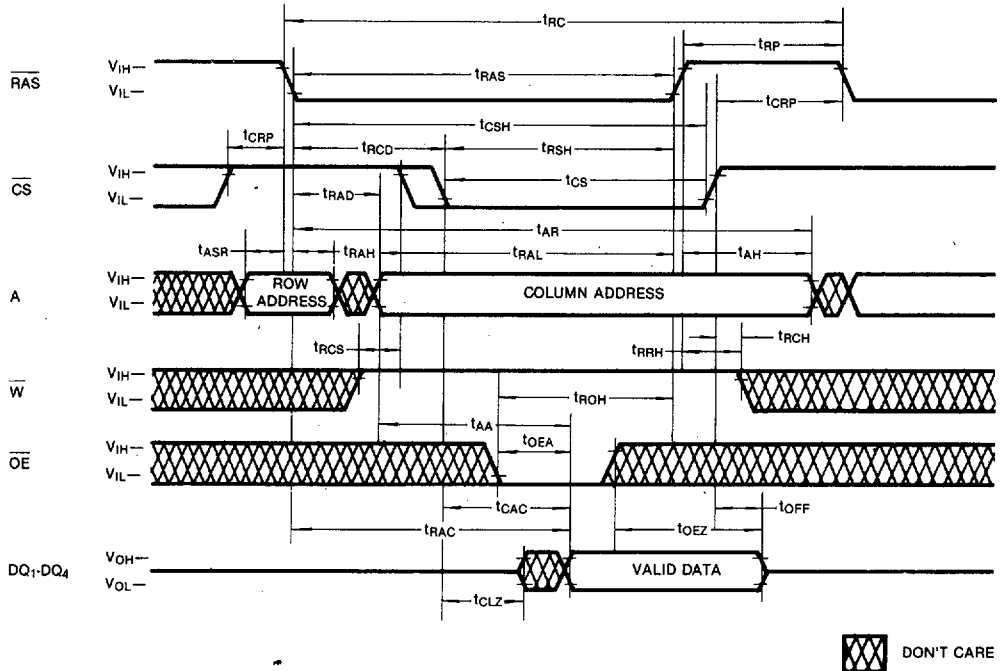


## NOTES

1. An initial pause of 200 $\mu$ s is required after power-up followed by any 8 CBR or ROR cycles before proper device operation is achieved.
2.  $V_{IH}(\min)$  and  $V_{IL}(\max)$  are reference levels for measuring timing of input signals. Transition times are measured between  $V_{IH}(\min)$  and  $V_{IL}(\max)$  are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the  $t_{RC}(\max)$  limit insures that  $t_{RAC}(\max)$  can be met.  $t_{RC}(\max)$  is specified as a reference point only. If  $t_{RC}$  is greater than the specified  $t_{RC}(\max)$  limit, then access time is controlled exclusively by  $t_{CAC}$ .
5. Assumes that  $t_{RC} \geq t_{RC}(\max)$ .
6.  $t_{AR}$ ,  $t_{WCR}$ ,  $t_{DHR}$  are referenced to  $t_{RAD}(\max)$ .
7. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to  $V_{OH}$  or  $V_{OL}$ .
8.  $t_{WCS}$ ,  $t_{RWD}$ ,  $t_{CWD}$  and  $t_{AWD}$  are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If  $t_{WCS} \geq t_{WCS}(\min)$  the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If  $t_{CWD} \geq t_{CWD}(\min)$ ,  $t_{RWD} \geq t_{RWD}(\min)$  and  $t_{AWD} \geq t_{AWD}(\min)$ , then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions are satisfied, the condition of the data output is indeterminate.
9. Either  $t_{RCH}$  or  $t_{RRH}$  must be satisfied for a read cycle.
10. These parameters are referenced to the  $\overline{CS}$  leading edge in early write cycles and to the  $\overline{W}$  leading edge in read-write cycles.
11. Operation within the  $t_{RAD}(\max)$  limit insures that  $t_{RAC}(\max)$  can be met.  $t_{RAD}(\max)$  is specified as a reference point only. If  $t_{RAD}$  is greater than the specified  $t_{RAD}(\max)$  limit, then access time is controlled by  $t_{AA}$ .
12. These specifications are applied in the test mode.
13. In test mode read cycle, the value of  $t_{RAC}$ ,  $t_{AA}$ ,  $t_{CAC}$  is delayed by 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
14.  $t_{OFF}(\max)$  and  $t_{OEZ}(\max)$  define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
15. 4096 cycle of burst refresh must be executed within 16ms before and after self refresh, in order to meet refresh specification.

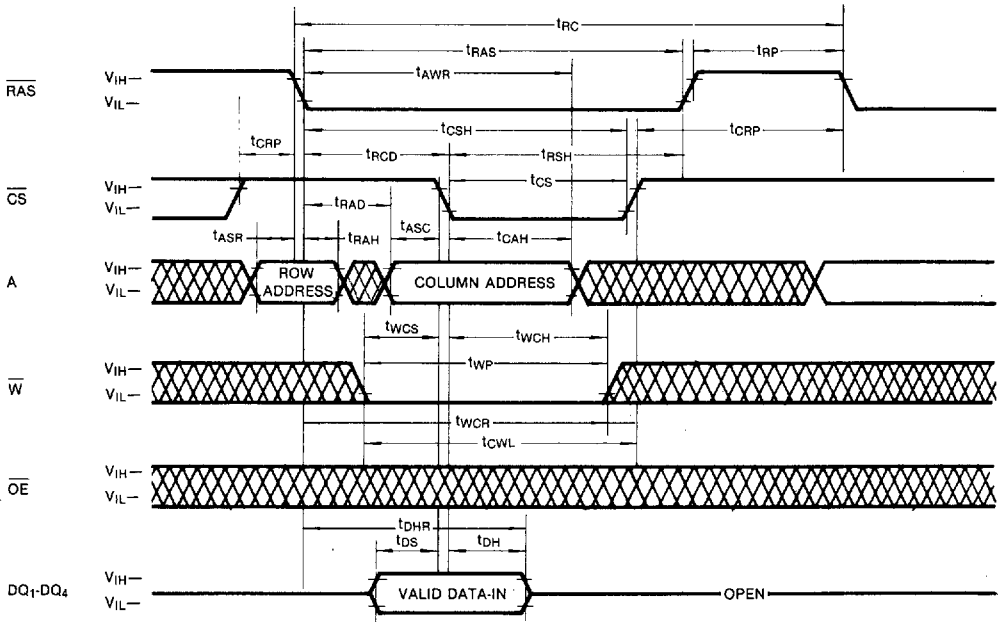
TIMING DIAGRAMS

READ CYCLE

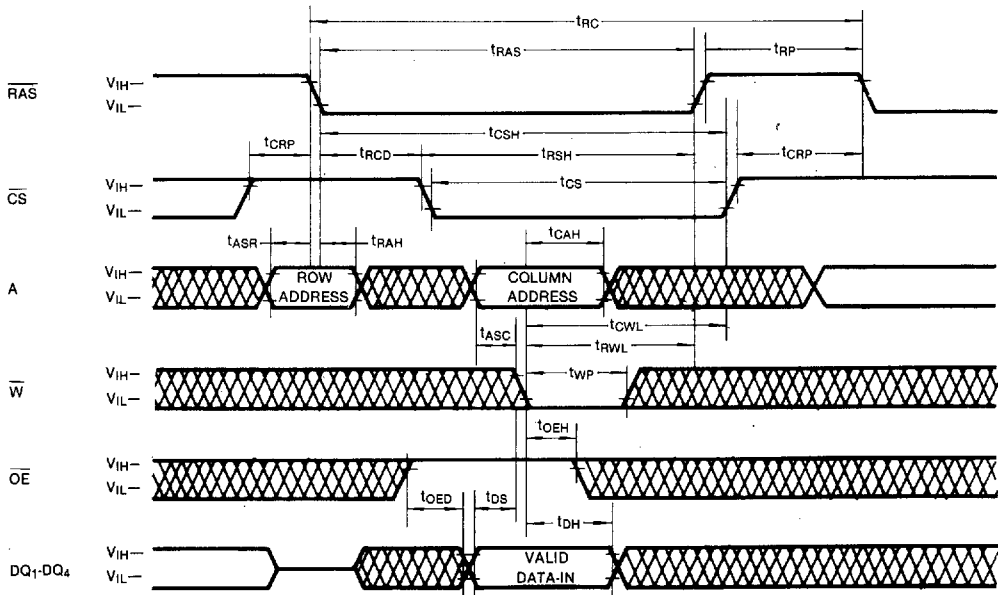


**TIMING DIAGRAMS** (Continued)

**WRITE CYCLE (EARLY WRITE)**



**WRITE CYCLE ( $\overline{OE}$  CONTROLLED WRITE)**



 DON'T CARE

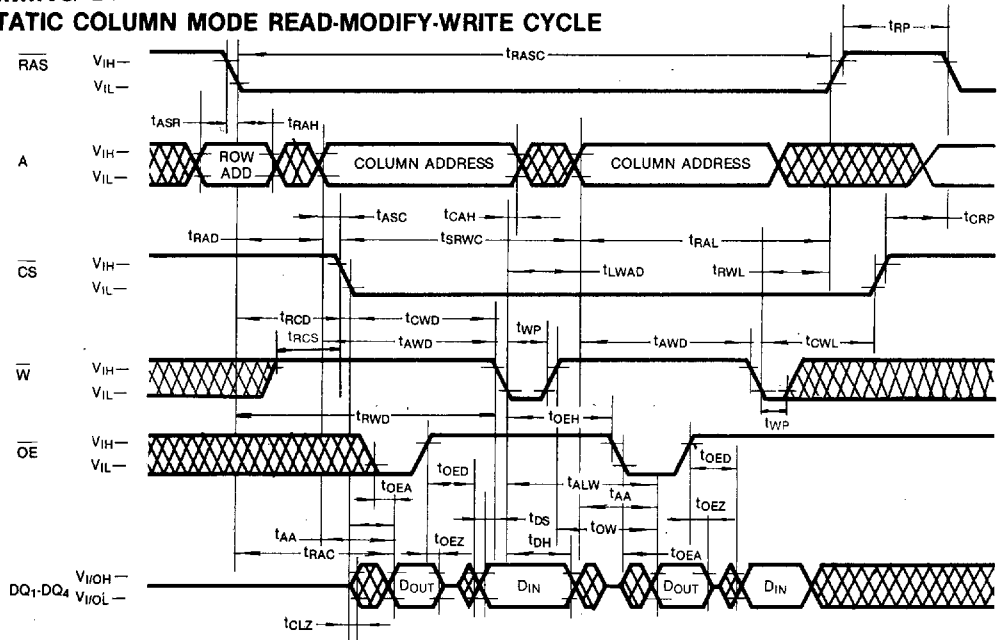
5



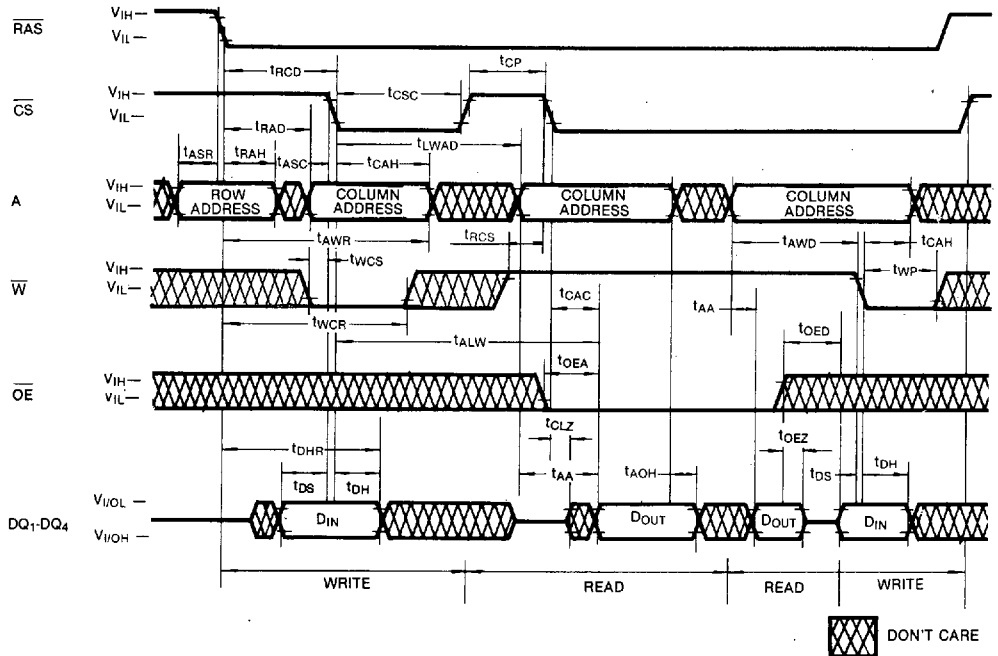


TIMING DIAGRAMS (Continued)

STATIC COLUMN MODE READ-MODIFY-WRITE CYCLE



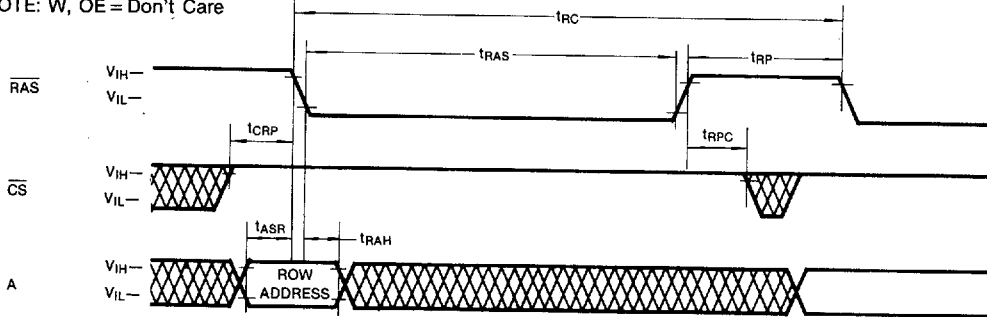
STATIC COLUMN MODE MIXED CYCLE



**TIMING DIAGRAMS** (Continued)

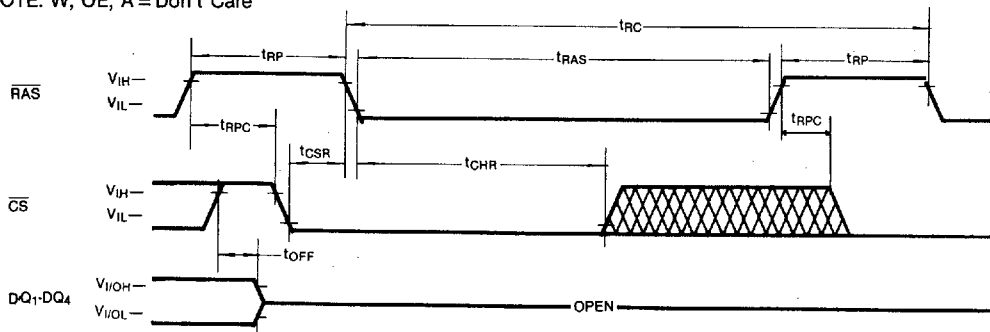
**RAS-ONLY REFRESH CYCLE**

NOTE:  $\bar{W}$ ,  $\bar{OE}$  = Don't Care



**$\bar{CS}$ -BEFORE- $\bar{RAS}$  REFRESH CYCLE**

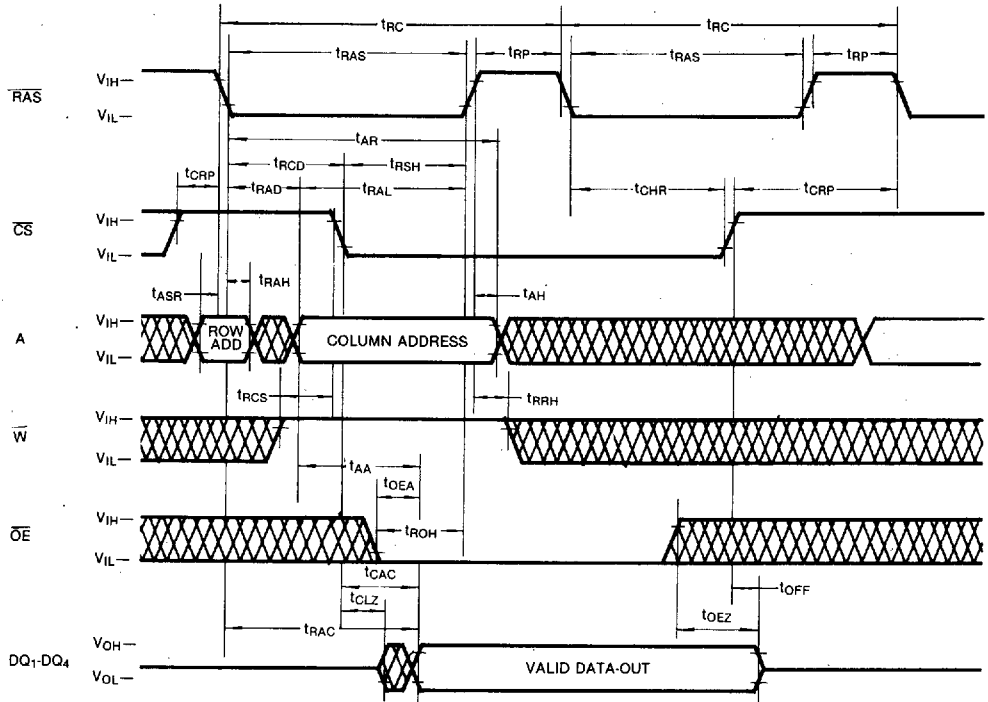
NOTE:  $\bar{W}$ ,  $\bar{OE}$ , A = Don't Care



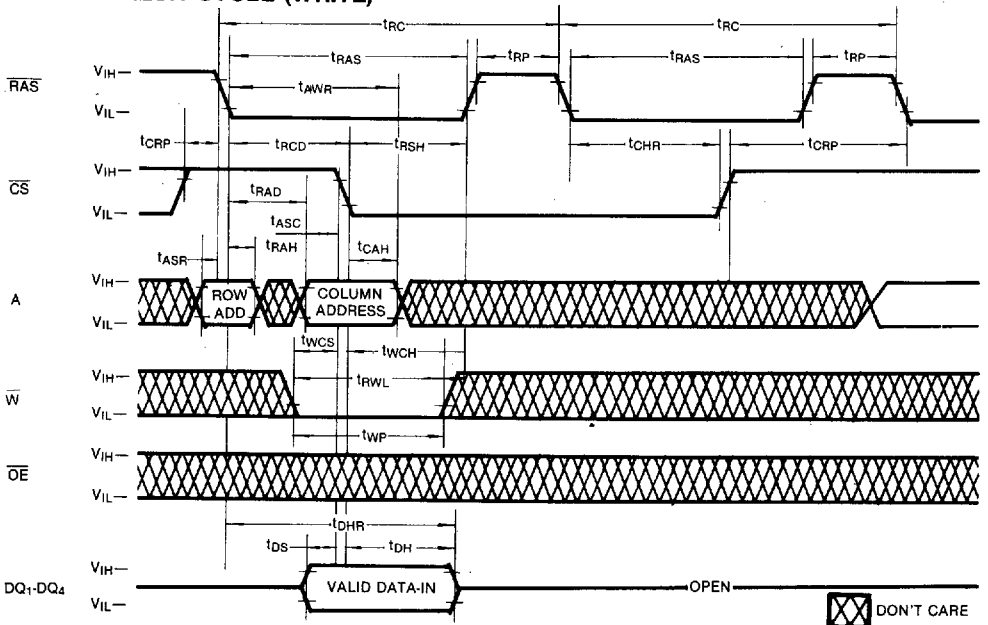
 DON'T CARE

5

**TIMING DIAGRAMS** (Continued)  
**HIDDEN REFRESH CYCLE (READ)**



**HIDDEN REFRESH CYCLE (WRITE)**

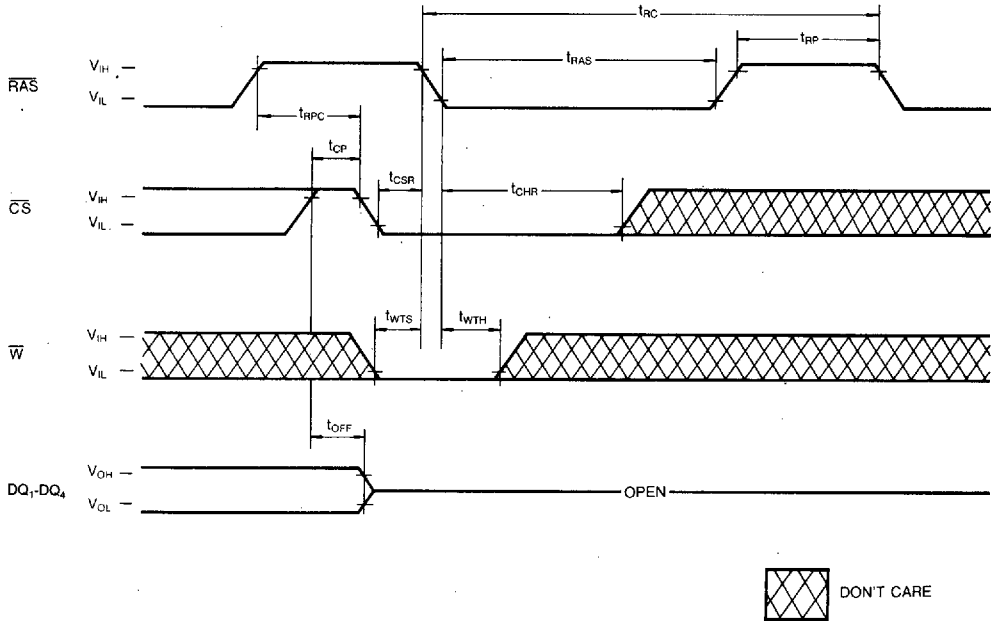




**TIMING DIAGRAMS** (Continued)

**TEST MODE IN CYCLE**

Note:  $\overline{OE}$ , Address: Don't Care



**TEST MODE DESCRIPTION**

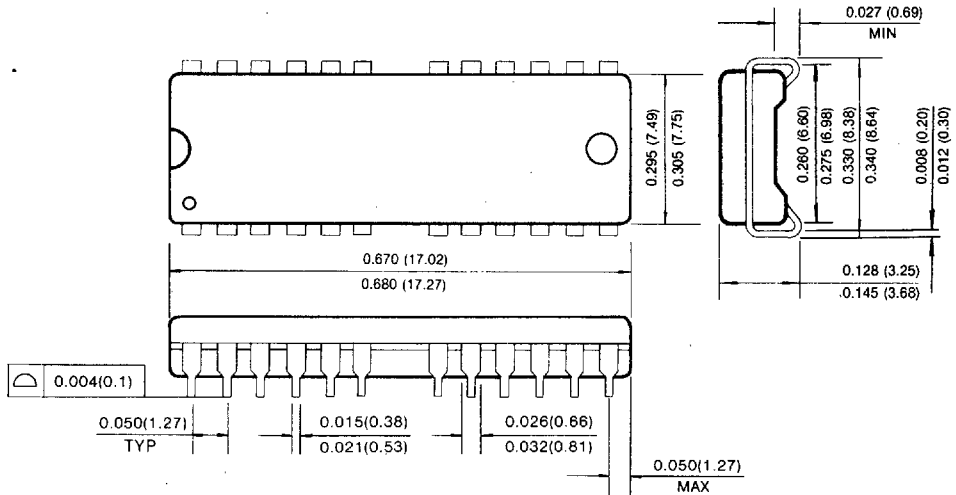
The KM44C4002 is the RAM organized 4,194,304 words by 4 bit, it is internally organized 1,048,576 words by 16 bits. In "Test Mode", data are written into 16 sectors in parallel and retrieved the same way. Column address bit  $A_0, A_1$ , are not used. If, upon reading, 16 bits are equal (all "1" or "0"s) the Q pin indicates a "1". If they were not equal, the Q pin would indicate a "0".

In "Test Mode", the 16M DRAM can be tested as if it were a  $1M \times 4$  DRAM.  $\overline{W}, \overline{CS}$ -BEFORE- $\overline{RAS}$  Cycle (Test Mode in Cycle) puts the device into "Test Mode". And  $\overline{CS}$ -BEFORE- $\overline{RAS}$  REFRESH CYCLE "or"  $\overline{RAS}$ -only Refresh Cycle" puts it back into "Normal Mode". The "Test Mode" function reduces test time (1/4 in cases of N test pattern).

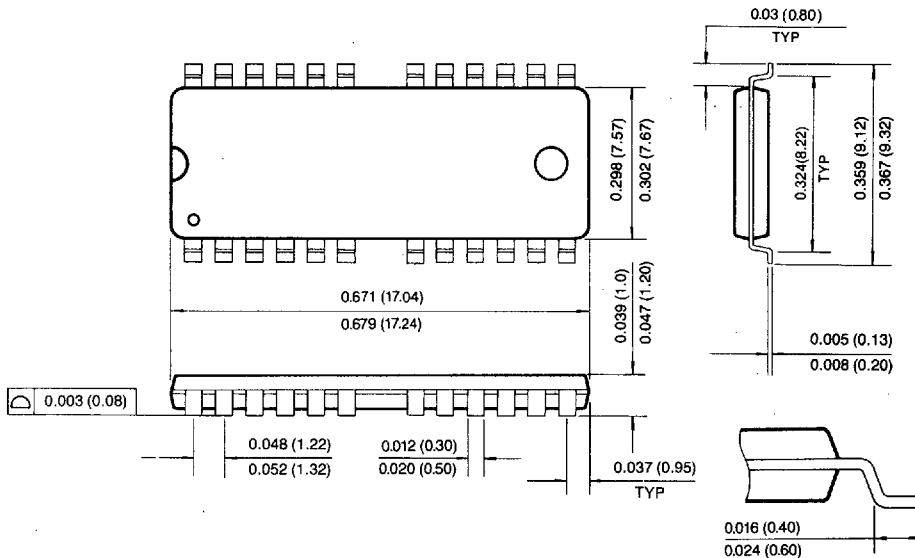
PACKAGE DIMENSIONS

24-LEAD PLASTIC SMALL OUT-LINE J-LEAD (300MIL)

Units: Inches (millimeters)



24-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE(II) (300MIL, Forward and Reverse Type)

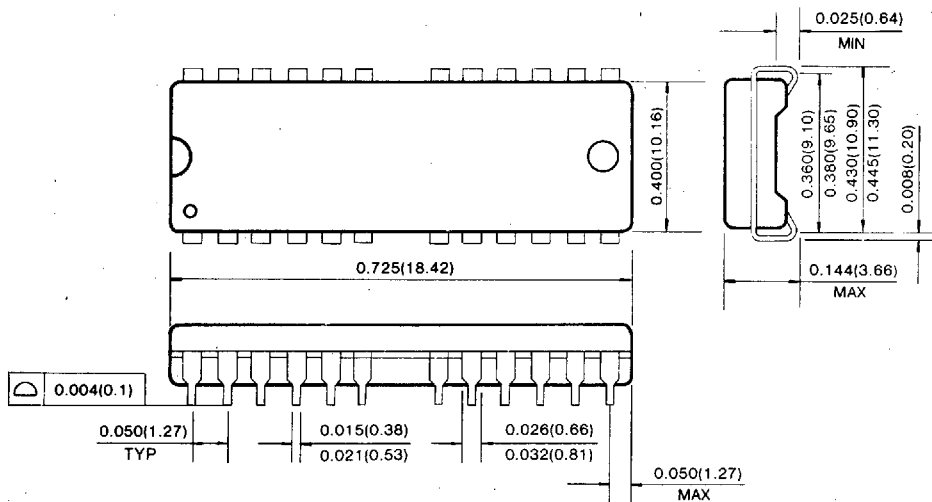


5

PACKAGE DIMENSIONS

24-LEAD PLASTIC SMALL OUT-LINE J-LEAD (400MIL)

Units: Inches (millimeters)



24-LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE (400MIL, Forward and Reverse Type)

