JUNE 1992

- **Free-Running CLKA and CLKB May Be Asynchronous or Coincident**
- **Two Independent 512 × 36 Clocked FIFOs Buffering Data in Opposite Directions**
- **Mailbox Bypass Register for Each FIFO**
- **Programmable Almost Full and Almost Empty Flags**
- **Microprocessor Interface Control Logic**
- **IRA, ORA, $\overline{AEA}$, and $\overline{AFA}$ Flags Synchronized by CLKA**
- **IRB, ORB, $\overline{AEB}$, and $\overline{AFB}$ Flags Synchronized by CLKB**
- **Low-Power 0.8-Micron Advanced CMOS Technology**
- **Supports Clock Frequencies up to 67 MHz**
- **Fast Access Times of 12 ns**
- **Available in 132-Pin Quad Flatpack (PQ) or Space-Saving 120-Pin Shrink Quad Flatpack (PCB)**

description

The SN74ACT7822 is a high-speed, low-power CMOS bidirectional clocked FIFO memory. It supports clock frequencies up to 67 MHz and has read access times as fast as 12 ns. Two independent 512 × 36 dual-port SRAM FIFOs on board the chip buffer data in opposite directions. Each FIFO has flags to indicate empty and full conditions and two programmable flags (almost full and almost empty) to indicate when a selected number of words is stored in memory. Communication between each port may bypass the FIFOs via two 36-bit mailbox registers. Each mailbox register has a flag to signal when new mail has been stored. Two or more devices may be used in parallel to create wider data paths.

The SN74ACT7822 is a clocked FIFO, which means each port employs a synchronous interface. All data transfers through a port are gated to the low-to-high transition of a continuous (free-running) port clock by enable signals. The continuous clocks for each port are independent of one another and can be asynchronous or coincident. The enables for each port are arranged to provide a simple bidirectional interface between microprocessors and/or buses with synchronous control.

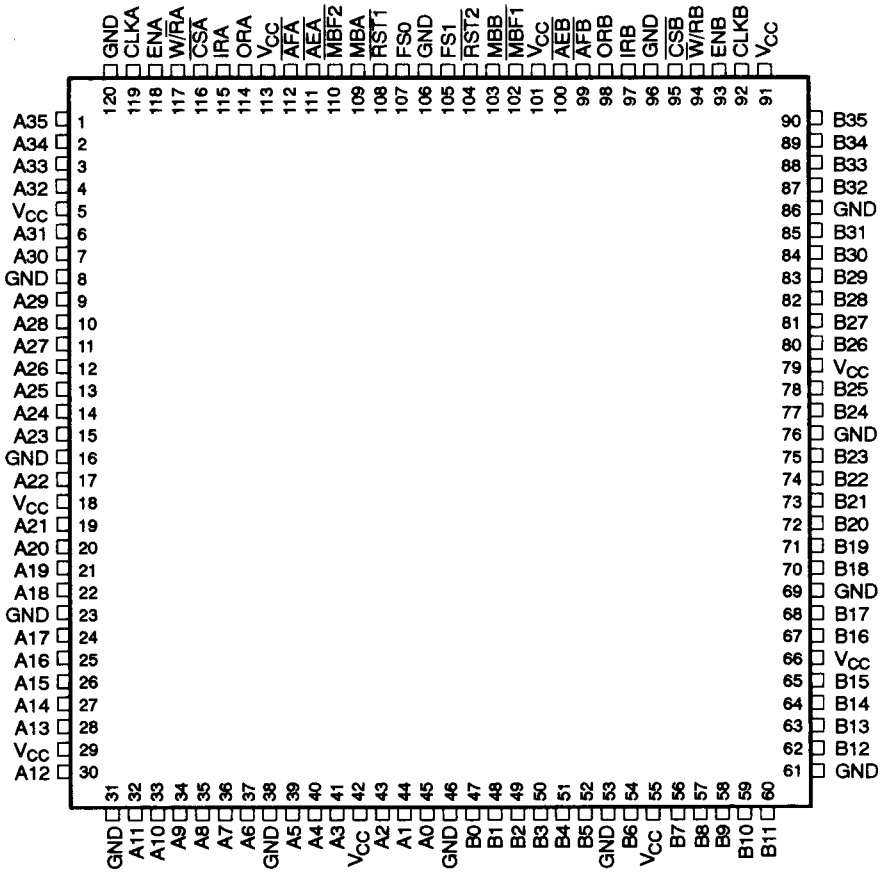
The input ready flag and almost full flag of a FIFO are two-stage synchronized to the port clock that writes data to its array. The output ready flag and almost empty flag of a FIFO are two-stage synchronized to the port clock that reads data from its array. Offsets for the almost full and almost empty flags of both FIFOs can be programmed from port A.

PRODUCT PREVIEW

JUNE 1992

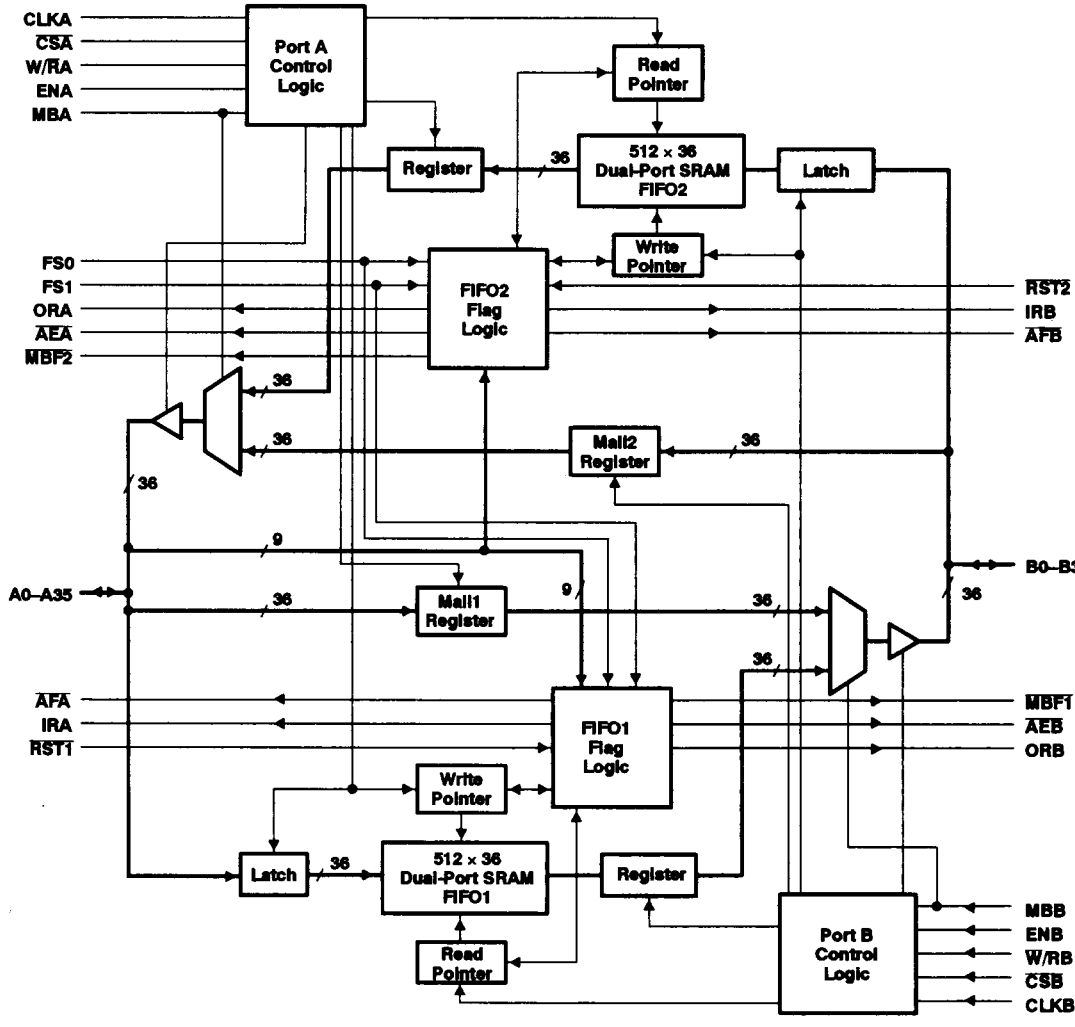
PRODUCT PREVIEW

PCB PACKAGE
(TOP VIEW)



TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

functional block diagram



PRODUCT PREVIEW

PRODUCT PREVIEW

Terminal Functions

PIN NAME	I/O	DESCRIPTION
A0–A35	I/O	Port A data. 36-bit bidirectional data port for side A.
$\overline{AEA}$	O	FIFO2 almost empty flag. Programmable flag synchronized to CLKA. It is low when the number of words in FIFO2 is less than or equal to the selected value.
$\overline{AEB}$	O	FIFO1 almost empty flag. Programmable flag synchronized to CLKB. It is low when the number of words in FIFO1 is less than or equal to the selected value.
$\overline{AFA}$	O	FIFO1 almost full flag. Programmable flag synchronized to CLKA. It is low when the number of empty locations in FIFO1 is less than or equal to the selected value.
$\overline{AFB}$	O	FIFO2 almost full flag. Programmable flag synchronized to CLKB. It is low when the number of empty locations in FIFO2 is less than or equal to the selected value.
B0–B35	I/O	Port B data. 36-bit bidirectional data port for side B.
CLKA	I	Port A clock. CLKA is a continuous clock that synchronizes all data transfers through port A and may be asynchronous or coincident to CLKB. IRA, ORA, $\overline{AFA}$, and $\overline{AEA}$ are all synchronous to the low-to-high transition of CLKA.
CLKB	I	Port B clock. CLKB is a continuous clock that synchronizes all data transfers through port B and may be asynchronous or coincident to CLKA. IRB, ORB, $\overline{AFB}$, and $\overline{AEB}$ are synchronous to the low-to-high transition of CLKB.
$\overline{CSA}$	I	Port A chip select. $\overline{CSA}$ must be low to enable a low-to-high transition of CLKA to read or write data on port A. The A0–A35 outputs are in the high-impedance state when $\overline{CSA}$ is high.
$\overline{CSB}$	I	Port B chip select. $\overline{CSB}$ must be low to enable a low-to-high transition of CLKB to read or write data on port B. The B0–B35 outputs are in the high-impedance state when $\overline{CSB}$ is high.
ENA	I	Port A master enable. ENA must be high to enable a low-to-high transition of CLKA to read or write data on port A.
ENB	I	Port B master enable. ENB must be high to enable a low-to-high transition of CLKB to read or write data on port B.
FS1, FS0	I	Flag offset selects. The low-to-high transition of a FIFO's reset input latches the values of FS0 and FS1. If either FS0 or FS1 is high when a reset input goes high, one of three preset values is selected as the offset for the FIFO's almost full and almost empty flags. If both FIFOs are reset simultaneously and both FS0 and FS1 are low when $\overline{RST1}$ and $\overline{RST2}$ go high, the first four writes to FIFO1 program the almost full and almost empty offsets for both FIFOs.
IRA	O	FIFO1 input ready flag. IRA is synchronized to the low-to-high transition of CLKA. When IRA is low, FIFO1 is full, and writes to its array are disabled. IRA is set low when FIFO1 is reset and is set high on the second low-to-high transition of CLKA after reset.
IRB	O	FIFO2 input ready flag. IRB is synchronized to the low-to-high transition of CLKB. When IRB is low, FIFO2 is full, and writes to its array are disabled. IRB is set low when FIFO2 is reset and is set high on the second low-to-high transition of CLKB after reset.
MBA	I	Port A mailbox select. A high level chooses a mailbox register for a port A read or write operation. When the A0–A35 outputs are active, a high level on MBA selects data from the mail2 register for output, and a low level selects FIFO2 data for output.
MBB	I	Port B mailbox select. A high level chooses a mailbox register for a port B read or write operation. When the B0–B35 outputs are active, a high level on MBB selects data from the mail1 register for output, and a low level selects FIFO1 data for output.
$\overline{MBF1}$	O	Mail1 register flag. $\overline{MBF1}$ is set low by the low-to-high transition of CLKA that writes data to the mail1 register. $\overline{MBF1}$ is set high by a low-to-high transition of CLKB when a port B read is selected and MBB is high. $\overline{MBF1}$ is also set high when FIFO1 is reset.
$\overline{MBF2}$	O	Mail2 register flag. $\overline{MBF2}$ is set low by the low-to-high transition of CLKB that writes data to the mail2 register. $\overline{MBF2}$ is set high by a low-to-high transition of CLKA when a port A read is selected and MBA is high. $\overline{MBF2}$ is also set high when FIFO2 is reset.
ORA	O	FIFO2 output ready flag. ORA is synchronized to the low-to-high transition of CLKA. When ORA is low, FIFO2 is empty, and reads are disabled. Ready data is present on the output register of FIFO2 when ORA is high. ORA is forced low when FIFO2 is reset and goes high on the third low-to-high transition of CLKA after a word is loaded to empty memory.

Terminal Functions (continued)

PIN NAME	I/O	DESCRIPTION
ORB	O	FIFO1 output ready flag. ORB is synchronized to the low-to-high transition of CLKB. When ORB is low, FIFO1 is empty, and reads are disabled. Ready data is present on the output register of FIFO1 when ORB is high. ORB is forced low when FIFO1 is reset and goes high on the third low-to-high transition of CLKB after a word is loaded to empty memory.
$\overline{RST1}$	I	FIFO1 reset. To reset FIFO1, four low-to-high transitions of CLKA and four low-to-high transitions of CLKB must occur while $\overline{RST1}$ is low. The low-to-high transition of $\overline{RST1}$ latches the status of FS0 and FS1 for $\overline{AFA}$ and $\overline{AEB}$ offset selection.
$\overline{RST2}$	I	FIFO2 reset. To reset FIFO2, four low-to-high transitions of CLKA and four low-to-high transitions of CLKB must occur while $\overline{RST2}$ is low. The low-to-high transition of $\overline{RST2}$ latches the status of FS0 and FS1 for $\overline{AFB}$ and $\overline{AEA}$ offset selection.
W/$\overline{RA}$	I	Port A write/$\overline{read}$ select. A high selects a write operation and a low selects a read operation on port A for a low-to-high transition of CLKA. The A0–A35 outputs are in the high-impedance state when W/$\overline{RA}$ is high.
$\overline{W}$/RB	I	Port B $\overline{write}$/read select. A low selects a write operation and a high selects a read operation on port B for a low-to-high transition of CLKB. The B0–B35 outputs are in the high-impedance state when $\overline{W}$/RB is low.

FIFO function

The state of the A0–A35 outputs is controlled by $\overline{CSA}$ and W/$\overline{RA}$. When both $\overline{CSA}$ and W/$\overline{RA}$ are low, the outputs are active. The outputs are in the high-impedance state when either $\overline{CSA}$ or W/$\overline{RA}$ is high. Data is written to FIFO1 from port A on the low-to-high transition of CLKA when $\overline{CSA}$ is low, W/$\overline{RA}$ is high, MBA is low, ENA is high, and the IRA flag is high. Data is read from FIFO2 to the A0–A35 outputs on the low-to-high transition of CLKA when $\overline{CSA}$ is low, W/$\overline{RA}$ is low, MBA is low, ENA is high, and the ORB flag is high.

The state of the B0–B35 outputs is controlled by $\overline{CSB}$ and $\overline{W}$/RB. When $\overline{CSB}$ is low and $\overline{W}$/RB is high, the outputs are active. The outputs are in the high-impedance state when either $\overline{CSB}$ is high or $\overline{W}$/RB is low. Data is written to FIFO2 from port B on the low-to-high transition of CLKB when $\overline{CSB}$ is low, $\overline{W}$/RB is low, MBB is low, ENB is high, and the IRB flag is high. Data is read from FIFO1 to the B0–B35 outputs on the low-to-high transition of CLKB when $\overline{CSB}$ is low, $\overline{W}$/RB is high, MBB is low, ENB is high, and the ORB flag is high.

The setup and hold time constraints to the port clocks for the chip selects ($\overline{CSA}$, $\overline{CSB}$) and write/read selects (W/$\overline{RA}$, $\overline{W}$/RB) are for enabling write and read operations and are not related to high-impedance control of the data outputs. If the master enable signal for a port (ENA or ENB) is set low during a clock cycle, the chip select and write/read select may switch at any time during the cycle to change the state of the data outputs.

Each FIFO flag is two-stage synchronized to a port clock for use as a reliable synchronous control signal. CLKA synchronizes the status of the output ready flag (ORA) and almost empty flag ($\overline{AEA}$) of FIFO2 and the input ready flag (IRA) and almost full flag ($\overline{AFA}$) of FIFO1. CLKB synchronizes the status of the output ready flag (ORB) and almost empty flag ($\overline{AEB}$) of FIFO1 and the input ready flag (IRB) and almost full flag ($\overline{AFB}$) of FIFO2.

When the input ready flag (IRA, IRB) of a port is low, the FIFO receiving input from the port is full, and writes are disabled to its array. When the output ready flag (ORA, ORB) of a port is low, the FIFO that outputs data to the port is empty, and reads from its memory are disabled. The first word loaded to an empty memory is sent to the FIFO's output register when the port's output ready flag is asserted (high). When the memory is read empty and the output ready flag is forced low, the last valid data remains on the FIFO outputs until the output ready flag is asserted (high) again. In this way, a high on the output ready flag indicates that new data is present on the FIFO outputs.

mailbox registers

A 36-bit word may be exchanged between ports and circumvent the normal FIFO path. The mailbox select inputs (MBA, MBB) choose between a mail register and a FIFO for a port data transfer operation. A0–A35 data is written to the mail1 register on a low-to-high transition of CLKA when $\overline{CSA}$ is low, W/$\overline{R}$A is high, ENA is high, and MBA is high. B0–B35 data is written to the mail2 register on a low-to-high transition of CLKB when $\overline{CSB}$ is low, $\overline{W}$/RB is low, ENB is high, and MBB is high.

When data is written to a mail register, its mailbox flag ($\overline{MBF1}$, $\overline{MBF2}$) is set low. The $\overline{MBF1}$ flag is set high on a low-to-high transition of CLKB when a read is selected for port B and the MBB input is high. The $\overline{MBF2}$ flag is set high on a low-to-high transition of CLKA when a read is selected for port A and the MBA input is high. The data in a mailbox register remains intact after it is read and changes only when new data is written to the register. When a port's data output registers are active, a high on the mailbox enable (MBA or MBB) selects mail data to be output on the port, and a low selects FIFO data for output.

reset

The FIFO memories of the SN74ACT7822 are reset separately by taking their reset inputs ($\overline{RST1}$ or $\overline{RST2}$) low for at least four CLKA and four CLKB low-to-high transitions. The reset inputs may be asynchronous with respect to either clock. This resets the internal read and write pointers to their initial locations and forces the FIFOs' $\overline{AF}$ flags high and IR, OR, and $\overline{AE}$ flags low. Resetting a FIFO also forces the flag of its parallel mailbox register high. Data outputs of the FIFO and mailbox register are not reset to any specific logic level. Both FIFOs must be reset upon power up.

almost full and almost empty flags

Three preset values are available for the offsets of the almost full and almost empty flags of a FIFO, or values can be programmed for each flag from port A. The flag select inputs (FS0, FS1) are sampled for each FIFO by the low-to-high transition of its reset input. If the values of FS0 and FS1 select a flag default value at the time of the rising edge of $\overline{RST1}$ or $\overline{RST2}$, the default value is set as the offset for the almost full and almost empty flags of the FIFO.

To program the almost full and almost empty flags of FIFO1 and FIFO2, both FIFOs should be reset simultaneously with FS0 and FS1 low during the low-to-high transition of the reset signals. After this reset cycle, IRA is forced high on the second low-to-high transition of CLKA, but IRB remains low until the programming is complete. The first four writes to FIFO1 program offsets for flags in the order of $\overline{AEA}$, $\overline{AEB}$, $\overline{AFA}$ and $\overline{AFB}$. The offsets may be programmed from 1 to 508. The IRB flag is asserted high by the second CLKB low-to-high transition after the $\overline{AFB}$ offset is programmed. The fifth write to FIFO1 stores the first word in its memory array.

An almost empty flag is low when the number of 36-bit words stored in its FIFO is less than or equal to the flag's offset value. An almost full flag is low when the number of empty locations left in its FIFO is less than or equal to the flag's offset value. Data in the output register of a FIFO has been read from memory, and its previous location is free.

FLAG PROGRAMMING TABLE

FS1	FS0	$\overline{RST1}$	$\overline{RST2}$	FIFO1 OFFSET	FIFO2 OFFSET
H	H	↑	X	64	X
H	H	X	↑	X	64
H	L	↑	X	16	X
H	L	X	↑	X	16
L	H	↑	X	8	X
L	H	X	↑	X	8
L	L	↑	↑	Programmed from port A	Programmed from port A

PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} ..... −0.5 V to 7 V
Input voltage, V_I ..... 7 V
Voltage applied to a disabled 3-state output ..... 5.5 V
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
I_{OH}	High-level output current		−4	mA
I_{OL}	Low-level output current		8	mA
T_A	Operating free-air temperature	0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP‡	MAX	UNIT
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −4 mA		2.4			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 8 mA				0.5	V
I_I	V_{CC} = 5.5 V,	$V_I = V_{CC}$ or 0				±5	μA
I_{OZ}	V_{CC} = 5.5 V,	$V_O = V_{CC}$ or 0				±5	μA
I_{CC}	V_{CC} = 5.5 V,	$V_I = V_{CC}$ − 0.2 V or 0				400	μA
ΔI_{CC}§	V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			1	mA
C_i	V_I = 0,	f = 1 MHz			4		pF
C_o	V_O = 0,	f = 1 MHz			8		pF

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ This is the supply current for each input that is at one of the specified TTL voltage levels rather 0 V or V_{CC}.

PRODUCT PREVIEW

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 30 pF (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	'ACT7822-15		'ACT7822-20		'ACT7822-25		'ACT7822-40		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}	CLKA or CLKB		67		50		40		25		MHz
t_{pd}	CLKA↑	A0–A35		12		13		15		17	ns
	CLKB↑	B0–B35		12		13		15		17	
	CLKA↑	IRA		12		13		15		17	
	CLKB↑	IRB		12		13		15		17	
	CLKA↑	ORA		12		13		15		17	
	CLKB↑	ORB		12		13		15		17	
	CLKA↑	$\overline{AFA}$		12		13		15		17	
	CLKB↑	$\overline{AFB}$		12		13		15		17	
	CLKA↑	$\overline{AEA}$		12		13		15		17	
	CLKB↑	$\overline{AEB}$		12		13		15		17	
t_{PHL}	CLKA↑	$\overline{MBF1}$		11		12		14		16	ns
t_{PLH}	CLKB↑			11		12		14		16	
t_{PHL}	CLKB↑	$\overline{MBF2}$		11		12		14		16	ns
t_{PLH}	CLKA↑			11		12		14		16	
t_{pd}	MBA	A0–A35		11		12		14		16	ns
	MBB	B0–B35		11		12		14		16	
t_{PHL}	$\overline{RST1}$	$\overline{AEB}$									ns
	$\overline{RST2}$	$\overline{AEA}$									
t_{PLH}	$\overline{RST1}$	$\overline{AFA}$									ns
	$\overline{RST2}$	$\overline{AFB}$									
t_{PLH}	$\overline{RST1}$	$\overline{MBF1}$									ns
	$\overline{RST2}$	$\overline{MBF2}$									
t_{en}	$\overline{CSA}$, W/$\overline{RA}$	A0–A35									ns
	$\overline{CSB}$, W/$\overline{RB}$	B0–B35									
t_{dis}	$\overline{CSA}$, W/$\overline{RA}$	A0–A35									ns
	$\overline{CSB}$, W/$\overline{RB}$	B0–B35									

PRODUCT PREVIEW