

74S280

Parity Generator/Checker

9-Bit Odd/Even Parity Generator/Checker
Product Specification

Logic Products

FEATURES

- Buffered inputs — one normalized load
- Word-length easily expanded by cascading
- Similar pin configuration to '180 for easy system up-grading

DESCRIPTION

The '280 is a 9-bit parity generator or checker commonly used to detect errors in high-speed data transmission or data retrieval systems. Both Even and Odd parity outputs are available for generating or checking even or odd parity on up to 9 bits.

The Even parity output (Σ_E) is HIGH when an even number of Data inputs ($I_0 - I_8$) are HIGH. The Odd parity output (Σ_O) is HIGH when an odd number of data inputs are HIGH.

Expansion to larger word sizes is accomplished by tying the Even outputs (Σ_E)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74S280	9.9ns	67mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N74S280N

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74S
$I_0 - I_8$	Data inputs	1Sul
Σ_E, Σ_O	Parity outputs	10Sul

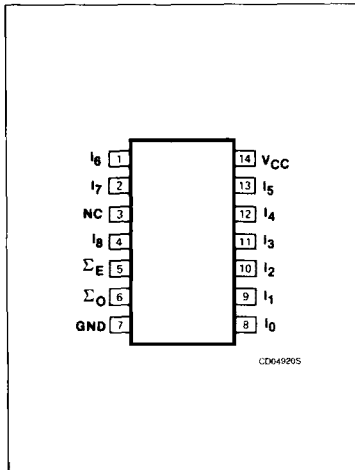
NOTE:

A 74S unit load (Sul) is $50\mu A$ I_{IH} and $-2.0mA$ I_{IL} .

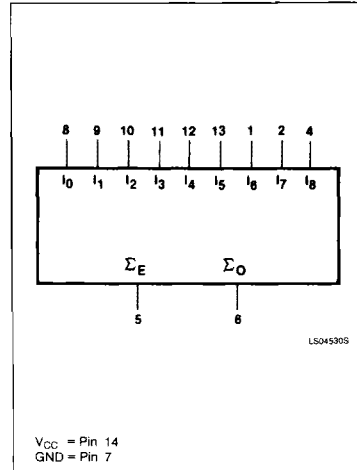
of up to nine parallel devices to the Data inputs of the final stage. This expansion scheme allows an 81-bit data word to be checked in less than 40ns with the 'S280.

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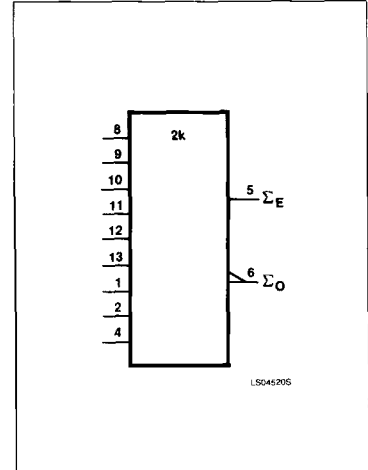
PIN CONFIGURATION



LOGIC SYMBOL



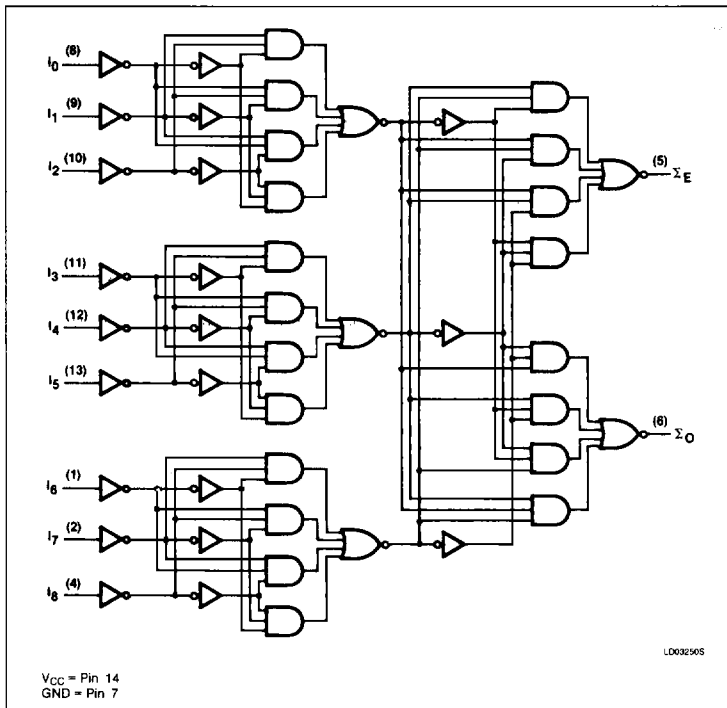
LOGIC SYMBOL (IEEE/IEC)



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LOGIC DIAGRAM



FUNCTION TABLE

INPUTS	OUTPUTS	
	Σ_E	Σ_O
Number of HIGH data inputs ($I_0 - I_9$)		
Even	H	L
Odd	L	H

H = HIGH voltage level
L = LOW voltage level

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	74S	UNIT
V _{CC} Supply voltage	7.0	V
V _{IN} Input voltage	-0.5 to +5.5	V
I _{IN} Input current	-30 to +5	mA
V _{OUT} Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	V
T _A Operating free-air temperature range	0 to 70	°C

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RECOMMENDED OPERATING CONDITIONS

PARAMETER		74S			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage	2.0			V
V_{IL}	LOW-level input voltage			+0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	HIGH-level output current			-1000	μ A
I_{OL}	LOW-level output current			20	mA
T_A	Operating free-air temperature	0		70	$^{\circ}$ C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS ¹	74S280			UNIT
			Min	Typ ²	Max	
V_{OH}	HIGH-level output voltage	$V_{CC} = \text{MIN}, V_{IL} = \text{MAX}, I_{OH} = \text{MAX}, V_{IH} = \text{MIN}$	2.7	3.4		V
V_{OL}	LOW-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = \text{MIN}, I_{OL} = \text{MAX}, V_{IL} = \text{MAX}$			0.5	V
V_{IK}	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = I_{IK}$			-1.2	V
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5\text{V}$			1.0	mA
I_{IH}	HIGH-level input current	$V_{CC} = \text{MAX}, V_I = 2.7\text{V}$			50	μ A
I_{IL}	LOW-level input current	$V_{CC} = \text{MAX}, V_I = 0.5\text{V}$			-2	mA
I_{OS}	Short-circuit output current ³	$V_{CC} = \text{MAX}$	-40		-100	mA
I_{CC}	Supply current ⁴ (total)	$V_{CC} = \text{MAX}$		67	105	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at $V_{CC} = 5\text{V}, T_A = 25^{\circ}\text{C}$.
- I_{OS} is tested with $V_{OUT} = +0.5\text{V}$ and $V_{CC} = V_{CC} \text{ MAX} + 0.5\text{V}$. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- I_{CC} is measured with all inputs grounded and all outputs open.

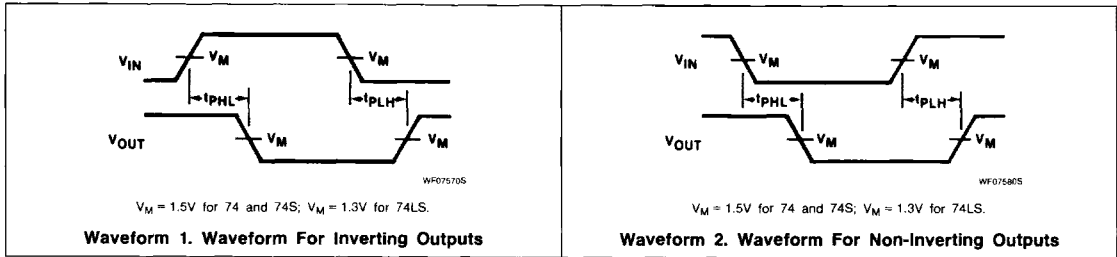
AC ELECTRICAL CHARACTERISTICS $T_A = 25^{\circ}\text{C}, V_{CC} = 5.0\text{V}$

PARAMETER		TEST CONDITIONS	74S280		UNIT
			$C_L = 15\text{pF}, R_L = 280\Omega$		
			Min	Max	
t_{PLH}	Propagation delay	Waveforms 1 & 2	10	21	ns
t_{PHL}	Data to even output		11	18	
t_{PLH}	Propagation delay	Waveforms 1 & 2	9.6	21	ns
t_{PHL}	Data to odd output		9.3	18	

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AC WAVEFORMS



TEST CIRCUITS AND WAVEFORMS

