8/16-bit Data Bus Flash Memory Card

MF8257-GBDATXX
MF8513-GBDATXX
MF81M1-GBDATXX
MF82M1-GBDATXX

Connector Type

Two-piece 68-pin

DESCRIPTION

The MF8XXX-GBDATXX is a flash memory card which uses one-megabit flash electrically erasable and programmable read only memory IC's.

APPLICATIONS

- Notebook computers
- Printers
- Industrial machines

FEATURES

- 68 pin JEIDA/PCMCIA
- 8/16 controllable data bus width
- Buffered interface
- TTL interface level
- Program/erase operation by software command control
- Program/erase voltage 12V
- 10,000 program/erase cycles
- Write protect switch

PRODUCT LIST

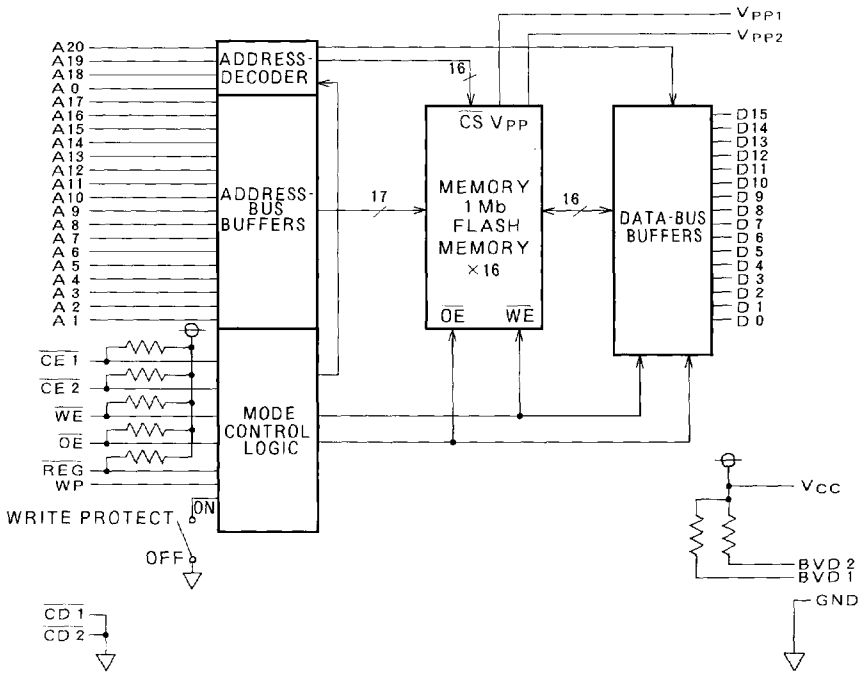
Item / Type name	Memory capacity	Data bus width (bits)	Access time (ns)	Connector type	Number of pins	Outline drawing
MF8257-GBDATXX	256KB	8/16	200	Two-piece	68	68P-002
MF8513-GBDATXX	512KB					
MF81M1-GBDATXX	1MB					
MF82M1-GBDATXX	2MB					

MITSUBISHI ELECTRIC

PIN ASSIGNMENT

Pin No.	Symbol	Function	Pin No.	Symbol	Function
1	GND	Ground	35	GND	Ground
2	D3	Data I/O	36	$\overline{CD1}$	Card detect 1
3	D4		37	D11	Data I/O
4	D5		38	D12	
5	D6		39	D13	
6	D7		40	D14	
7	$\overline{CE1}$	Card enable 1	41	D15	
8	A10	Address input	42	$\overline{CE2}$	Card enable 2
9	$\overline{OE}$	Output enable	43	NC	No connection
10	A11	Address input	44	NC	
11	A9		45	NC	
12	A8		46	A17	Address input
13	A13		47	A18	A18 (NC for ≤256KB types)
14	A14		48	A19	A19 (NC for ≤512KB types)
15	$\overline{WE}$	Write enable	49	A20	A20 (NC for ≤1MB types)
16	NC	No connection	50	NC	No connection
17	V_{CC}	Power supply voltage	51	V_{CC}	Power supply voltage
18	$V_{PP}1$	Programming supply voltage 1	52	$V_{PP}2$	Programming supply voltage 2
19	A16	Address input	53	NC	No connection
20	A15		54	NC	
21	A12		55	NC	
22	A7		56	NC	
23	A6		57	NC	
24	A5		58	NC	
25	A4		59	NC	
26	A3		60	NC	
27	A2		61	$\overline{REG}$	Attribute memory select
28	A1		62	BVD2	Battery voltage detect 2
29	A0		63	BVD1	Battery voltage detect 1
30	D0	Data I/O	64	D8	Data I/O
31	D1		65	D9	
32	D2		66	D10	
33	WP	Write protect	67	$\overline{CD2}$	Card detect 2
34	GND	Ground	68	GND	Ground

BLOCK DIAGRAM (MF82M1-GBDATXX)



FUNCTIONAL DESCRIPTION

The operating mode of the card is determined by five active low control signals ($\overline{REG}$, $\overline{CE1}$, $\overline{CE2}$, $\overline{OE}$, $\overline{WE}$), three supply voltages (V_{CC}, V_{PP1}, V_{PP2}) and control registers located in each memory IC.

Common memory function

When the $\overline{REG}$ signal is set to a high level common memory is selected.

Read only mode

When the voltages applied to both V_{PP1} and V_{PP2} are less than the voltage applied to V_{CC} (i.e. V_{PP} = 0V to V_{CC}), the control registers of each memory IC are set to read only mode.

Operation of the card then depends on the four possible combinations of $\overline{CE1}$ and $\overline{CE2}$ (note $\overline{WE}$ should be set to a high level when the device is in read only mode except during combination (4) where it's condition is unimportant) :

(1) If $\overline{CE1}$ is set to a low level and $\overline{CE2}$ is set to a high level, the card will work as an eight bit data bus width card. Data can be accessed via the lower half of the data bus (D0 to D7).

(2) If both $\overline{CE1}$ and $\overline{CE2}$ are set to a low level, data will be accessible via the full sixteen bit data bus width of the card. In this mode LSB of address bus (A0) is ignored.

(3) If $\overline{CE1}$ is set to a high level and $\overline{CE2}$ is set to a low level the odd bytes (only) can be accessed through upper half of the data bus (D8 to D15). This mode is useful when handling the odd (upper) bytes in a sixteen bit interface system. Note that A0 is also ignored in this operating condition.

(4) If $\overline{CE1}$ and $\overline{CE2}$ are set to a high level, the card will be in standby mode where it consumes low power. The data bus is kept high impedance.

When $\overline{OE}$ is set to a low level data can be read from the card, depending on the address applied and the setting of $\overline{CE1}$ and $\overline{CE2}$ as mentioned above, except under combination (4).

When $\overline{OE}$ is set to a high level and $\overline{WE}$ is set to a high level the card is in an output disable mode and the data bus will be in a high impedance state regardless of the condition of $\overline{CE1}$ and $\overline{CE2}$.

Read/write mode

When a programming voltage ($V_{PP}H$) is applied to either or both of $V_{PP}1$ and $V_{PP}2$, read/write mode is enabled for the corresponding banks of memory IC's inside the card. $V_{PP}1$ enables the Even Byte bank and $V_{PP}2$ enables the Odd Byte bank.

By using the 4 combinations of $\overline{CE1}$ and $\overline{CE2}$ as described under Read only mode above the appropriate Data Out and Command/Data In bus selection can be made.

If $\overline{OE}$ is set to a high level and $\overline{WE}$ set to a low level, the control register will latch command data applied at the rising edge of the $\overline{WE}$ signal. Note that more than one bus cycle may be required to latch the command and/or the related data – please refer to the Command Definition table.

If $\overline{OE}$ is set to a low level and $\overline{WE}$ is set to a high level the card data can be read from the card depending on the condition of the control register.

After latching the command data, the card will go into programming, erasure or other operation mode. For details please refer to the Command Definition table, each individual command's definition and the programming and erasure algorithms.

Attribute memory

When $\overline{REG}$ is set to a low level attribute memory is selected.

The card then outputs FFh on the lower half of the data bus (D0 to D7) when the following conditions are applied :

(1) $\overline{CE1}$: low level, $\overline{CE2}$: high level, $\overline{OE}$: low level, $\overline{WE}$: high level, A0 : low level
(2) $\overline{CE1}$: low level, $\overline{CE2}$: low level, $\overline{OE}$: low level, $\overline{WE}$: high level.

Write protect mode

The card has a write protect switch on the opposite edge to the connector edge. When it is switched on, the card will be placed into a write protect mode, where data can be read from the card but it cannot be written to it. The WP output pin is set to a high level when the card is in write protect mode and V_{CC} is applied. When the card is not in write protect mode the WP output pin is set to a low level when V_{CC} is applied. By reading the state of the WP output the host system can easily check whether the card is in write protect mode or not.

FUNCTION TABLE (COMMON MEMORY) READ ONLY MODE

Mode	$\overline{REG}$	$\overline{CE2}$	$\overline{CE1}$	$\overline{OE}$	$\overline{WE}$	A0	V_{PP2}	V_{PP1}	I/O (D15-D8)	I/O (D7-D0)
Standby	H	H	H	X	X	X	V_{PPL}	V_{PPL}	High-Z	High-Z
Read A (16-bit)	H	L	L	L	H	X	V_{PPL}	V_{PPL}	Odd byte data out	Even byte data out
Read B (8-bit)	H	H	L	L	H	L	V_{PPL}	V_{PPL}	High-Z	Even byte data out
	H	H	L	L	H	H	V_{PPL}	V_{PPL}	High-Z	Odd byte data out
Read C (8-bit)	H	L	H	L	H	X	V_{PPL}	V_{PPL}	Odd byte data out	High-Z
Output disable	H	X	X	H	H	X	V_{PPL}	V_{PPL}	High-Z	High-Z

Note 1 : H = V_{IH}, L = V_{IL}, X = V_{IH} or V_{IL}

FUNCTION TABLE (COMMON MEMORY) READ/WRITE MODE

Mode	$\overline{REG}$	$\overline{CE2}$	$\overline{CE1}$	$\overline{OE}$	$\overline{WE}$	A0	V_{PP2}	V_{PP1}	I/O (D15-D8)	I/O (D7-D0)
Standby	H	H	H	X	X	X	V_{PPX}	V_{PPH}	High-Z	High-Z
	H	H	H	X	X	X	V_{PPH}	V_{PPX}	High-Z	High-Z
Read A (16-bit)	H	L	L	L	H	X	V_{PPH}	V_{PPH}	Odd byte data out	Even byte data out
Read B (8-bit)	H	H	L	L	H	L	V_{PPX}	V_{PPH}	High-Z	Even byte data out
	H	H	L	L	H	H	V_{PPH}	V_{PPX}	High-Z	Odd byte data out
Read C (8-bit)	H	L	H	L	H	X	V_{PPH}	V_{PPX}	Odd byte data out	High-Z
Write A (16-bit)	H	L	L	H	L	X	V_{PPH}	V_{PPH}	Command or odd byte data in	Command or even byte data in
Write B (8-bit)	H	H	L	H	L	L	V_{PPX}	V_{PPH}	High-Z	Command or even byte data in
	H	H	L	H	L	H	V_{PPH}	V_{PPX}	High-Z	Command or odd byte data in
Write C (8-bit)	H	L	H	H	L	X	V_{PPH}	V_{PPX}	Command or odd byte data in	High-Z
Output disable	H	X	X	H	H	X	V_{PPH}	V_{PPX}	High-Z	High-Z
	H	X	X	H	H	X	V_{PPX}	V_{PPH}	High-Z	High-Z

Note 2 : H = V_{IH}, L = V_{IL}, X = V_{IH} or V_{IL}, V_{PPX} = V_{PPL} or V_{PPH}
To operate refer to the command definition, algorithms.

FUNCTION TABLE (ATTRIBUTE MEMORY)

Mode	$\overline{REG}$	$\overline{CE2}$	$\overline{CE1}$	$\overline{OE}$	$\overline{WE}$	A0	V_{PP2}	V_{PP1}	I/O (D15-D8)	I/O (D7-D0)
Standby	L	H	H	X	X	X	V_{CC}	V_{CC}	High-Z	High-Z
Read A (16-bit)	L	L	L	L	H	X	V_{CC}	V_{CC}	Data out (not valid)	Data out (FFh)
Read B (8-bit)	L	H	L	L	H	L	V_{CC}	V_{CC}	High-Z	Data out (FFh)
	L	H	L	L	H	H	V_{CC}	V_{CC}	High-Z	Data out (not valid)
Read C (8-bit)	L	L	H	L	H	X	V_{CC}	V_{CC}	Data out (not valid)	High-Z
Output disable	L	X	X	H	H	X	V_{CC}	V_{CC}	High-Z	High-Z

COMMAND DEFINITION

8 bit mode

Command	Bus Cycles Required	First Bus Cycle			Second Bus Cycle			
		Mode	Address	Data in	Mode	Address	Data in	Data out
Read memory	1	Write	BA	00h	–	–	–	–
Setup program/program	2	Write	PA	40h	Write	PA	PD	–
Program verify	2	Write	PA	C0h	Read	PA	–	PVD
Setup erase/erase	2	Write	BA	20h	Write	BA	20h	–
Erase verify	2	Write	EVA	A0h	Read	EVA	–	EVD
Reset	2	Write	BA	FFh	Write	BA	FFh	–
Read device identifier code	2	Write	BA	90h	Read	DIA	–	DID

16 bit mode

Command	Bus Cycles Required	First Bus Cycle			Second Bus Cycle			
		Mode	Address	Data in	Mode	Address	Data in	Data out
Read memory	1	Write	BA	0000h	–	–	–	–
Setup program/program	2	Write	PA	4040h	Write	PA	PD	–
Program verify	2	Write	PA	C0C0h	Read	PA	–	PVD
Setup erase/erase	2	Write	BA	2020h	Write	BA	2020h	–
Erase verify	2	Write	EVA	A0A0h	Read	EVA	–	EVD
Reset	2	Write	BA	FFFFh	Write	BA	FFFFh	–
Read device identifier code	2	Write	BA	9090h	Read	DIA	–	DID

Note3 : These tables show the basic functions of commands. Please refer to the individual programming and erase algorithms for exact operating details. Signal and bus status are defined in the function table.

BA : Memory block address (any address within the selected block)
PA : Programming address
PD : Programming data
PVD : Program verify data
EVA : Erase verifying address
EVD : Erase verify data
DIA : Device identifier address :
000000h for manufacturer code
000002h for device code
DID : Device identifier data
Manufacturer Code 1Ch (1C1Ch)
Device Code D0h (D0D0h)

COMMAND DEFINITIONS

Read

The memory in the card is switched to read mode by writing 00h (0000h for 16 bit operation) into the control register. This mode is maintained until the contents of the register are changed. When V_{PP} is switched to $V_{PP}H$ the card enters this mode. This mode needs to be written to every memory block to which access is required.

Setup program/program

The setup program command sets up the card for programming. It is applied when 40h (4040h for 16 bit operation) is written to the control register. Programming will take place after latching the address and data which are applied at the rising edge of $\overline{WE}$. The programming operation will finish 10 μs or less after that.

The operation should be repeated for a specified number of times if the program verify which follows is not successful (For details please refer to the algorithm).

Program verify

It is necessary to verify the programmed data after the execution of the program command. The program verify command is applied by writing C0h (C0C0h for 16 bit operation) into the control register. The address to be verified is not latched when writing this command

(For details please refer to the algorithm).

Setup erase/erase

The setup erase command sets up a memory block (selected by the applied block address) for erasure. It is applied when 20h (2020h for 16 bit operation) is written to the command register. It should be followed by writing the erase command which is also 20h (2020h for 16 bit operation) and this will initiate a erasure operation. This operation will finish in 9.5ms or less after the rising edge of $\overline{WE}$ this being controlled by an internal timer. The setup erase and erase commands should be repeated a specified number of times if the erase verify sequence which follows is not successful and should only be executed after confirming that the data programmed to all of the area to be erased is 00h (0000h for 16 bit operation). (For details please refer to the algorithm)

These commands will not erase all the data in a memory card and should be repeated for each of the memory blocks where erasure is required. When in eight bit access mode it should be noted that the erasure of a memory block will result in eiher odd byte or even byte erasure.

Erase verify

After finishing an erase operation the data in the corresponding memory block should be verified.

A0h (A0A0h at 16 bit operation) is the command for erase verify. When writing the command the address to be verified is latched at the rising edge of WE. The erase verify operation should be repeated for each address within the selected memory block until either unerased data is read or the data read from all the addresses of the block has been verified as correctly erased.

(For details please refer to the algorithm)

Reset

The reset command exists to allow erasure or programming operations to be safely aborted. It is applied by writing FFh (FFFFh for 16 bit operation) twice after the erase setup command or program setup command. It will reset operation for the corresponding memory block and set it to a read mode without changing data.

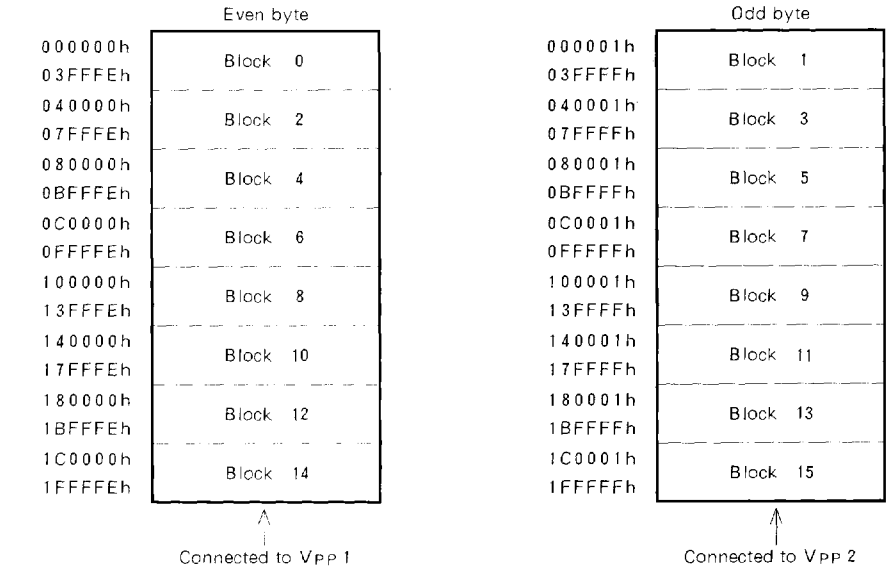
Read device identifier codes

The read device identifier codes command is implemented by writing 90h (9090h at 16 bit access) to the command register. After writing the command, the device manufacturer code can be read at address 000000h of the block and the device code can be read at address 000002h of the block. Each card uses the same type of memory throughout and each memory block will respond with the same code.

(NOTE : Do not apply a high voltage (super voltage) to the A10 pin in order to try and read the device identifier codes as this will result in the card being destroyed.)

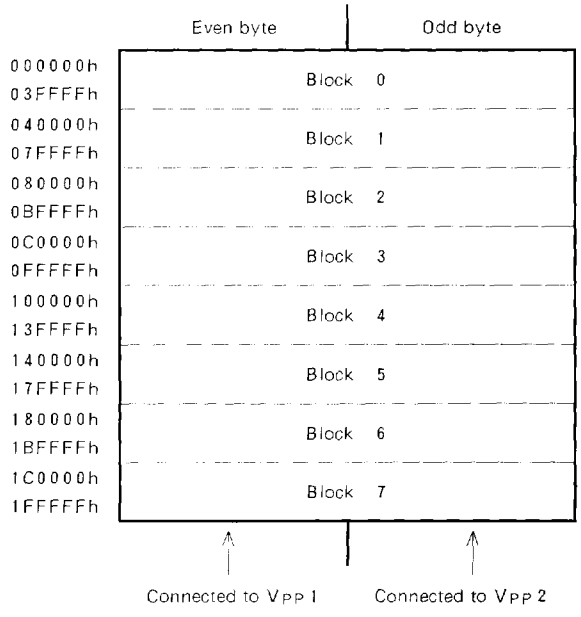
MEMORY BLOCK

8 bit mode



Block 2 to 15 do not exist in 256KB.
Block 4 to 15 do not exist in 512KB.
Block 8 to 15 do not exist in 1 MB.

16 bit mode



A 0 signal is ignored at 16 bit mode.

Block 1 to 7 do not exist in 256KB.
Block 2 to 7 do not exist in 512KB.
Block 4 to 7 do not exist in 1 MB.

PROGRAMMING ALGORITHM

8 bit Operation

First apply $V_{PP}H$ to $V_{PP}1$ and/or $V_{PP}2$. Then write the program setup command (40h) to the address to be programmed. The next write sequence will initiate a programming operation which will end in 10 μs or less this period being controlled by an internal timer and the data will then have been programmed. To verify that the data is programmed correctly write a program verify command (C0h) and then read the data (Reading should be not commence until 6 μs after the program verify command has been input). If the data is not programmed correctly repeat the above routine (program setup/write/program verify/read) up to a maximum of 25 times. If the data is programmed step to the next address to be programmed and program data according to the above sequence. The next address to be programmed should be within a memory block whose V_{PP} voltage is set to $V_{PP}H$. If it is not write the read command (00h) and then drop the V_{PP} voltage to $V_{PP}L$. Then apply V_{PP} for the desired memory block and proceed with programming.

(Note : In applications where $V_{PP}1$ and $V_{PP}2$ are shorted together all addresses can be programmed without there being any need for the programming algorithm to take account of the cards memory block architecture).

16 bit Operation

The algorithm for 16 bit programming is almost same as that for 8 bit programming. The difference between the two algorithms is that during 16 bit programming, when either the upper or lower 8 bits of data in a word has been programmed successfully, but programming of the other 8 bits has still to be completed, FFh is written to the half of the command word corresponding to the successfully programmed byte instead of the program setup command and data to be programmed. This operation can be achieved by masking the appropriate half of the data bus by carrying out a logical OR between it and FFh.

Also 00h should be used to replace the program verify command for the applicable half of the data.

(For further details please refer to the programming algorithm and the table describing the bus status during programming)

ERASE ALGORITHM

8 bit Operation

First apply $V_{PP}H$ to $V_{PP}1$ and/or $V_{PP}2$. Then confirm that the data at all the addresses within the memory block to be erased is 00h. If the data is not 00h program it to 00h following the programming algorithms. Then write the erase setup command (20h) and erase command (20h) for the applicable block address. An erasure operation will then commence which will be finished in 9.5ms or less this being automatically controlled by an internal timer. To verify the erasure start by applying the erase verify command (A0h) for the lowest address of the memory block. In 6 μs the verifying data can be read. If the data is not FFh repeat the erasure operation by again writing the erase setup and erase commands and then re - verify. If the data is FFh verify the data for the next address of the memory block and, again if this address fails to verify repeat the erasure process. However, If the next address does verify again step forward one address and repeat the process. These operations should be repeated until the whole of the block is verified as erased or the allowed maximum of 3,000 erase cycles per erase operation per block has been reached. Note that once an address has been verified as erased it need not be re-verified even if further erase cycles to its block have taken place following the non-verification of another address. Also note that the erase verify operation should be restricted to the memory block currently being erased. After erasure has been completed write the read command (00h) to the command register, set $V_{PP}1$ and/or $V_{PP}2$ to $V_{PP}L$ as applicable and proceed with the erase operation for the next memory block.

Please note that when the card is being used in 8bit mode, due to the organisation of the memory blocks, erasure of a memory block result in an erasure of a block of only odd or even addresses (not a block of continuous addresses.)

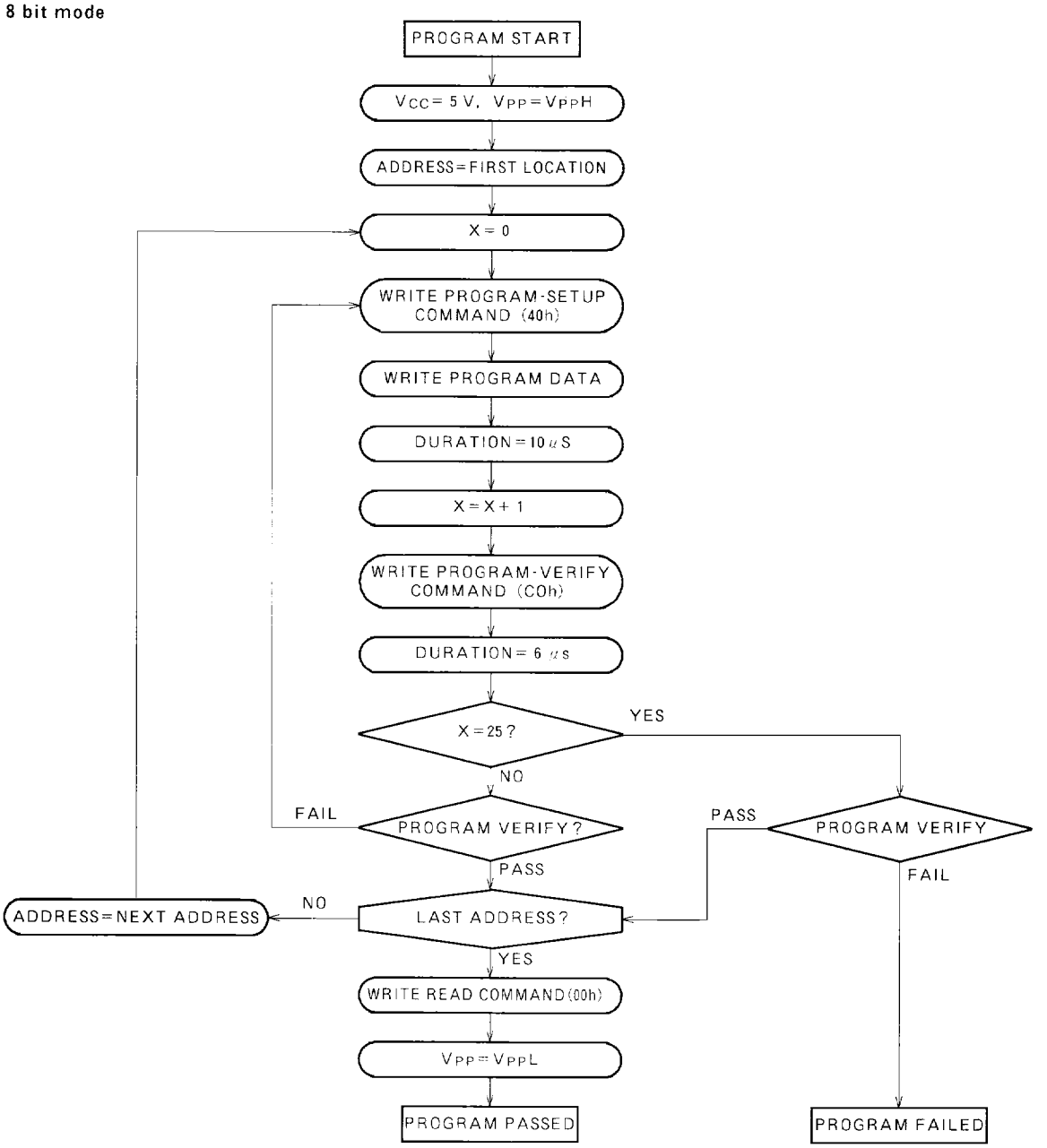
16 bit Operation

The algorithm for 16 bit erasure is almost the same as the one for 8bit erasure. The difference between the two modes is that when either the upper byte or the lower byte has been successfully erased but erasure has still to be completed for the other byte the half of the command word corresponding to the erased byte should be FFh instead of the erase setup command and erase command. Also the corresponding half of the erase verify command word has to be changed to a read command (00h) until the other byte has been successfully erased.

(For further details please refer to the erase algorithms and the table showing the status of the bus during erasure.)

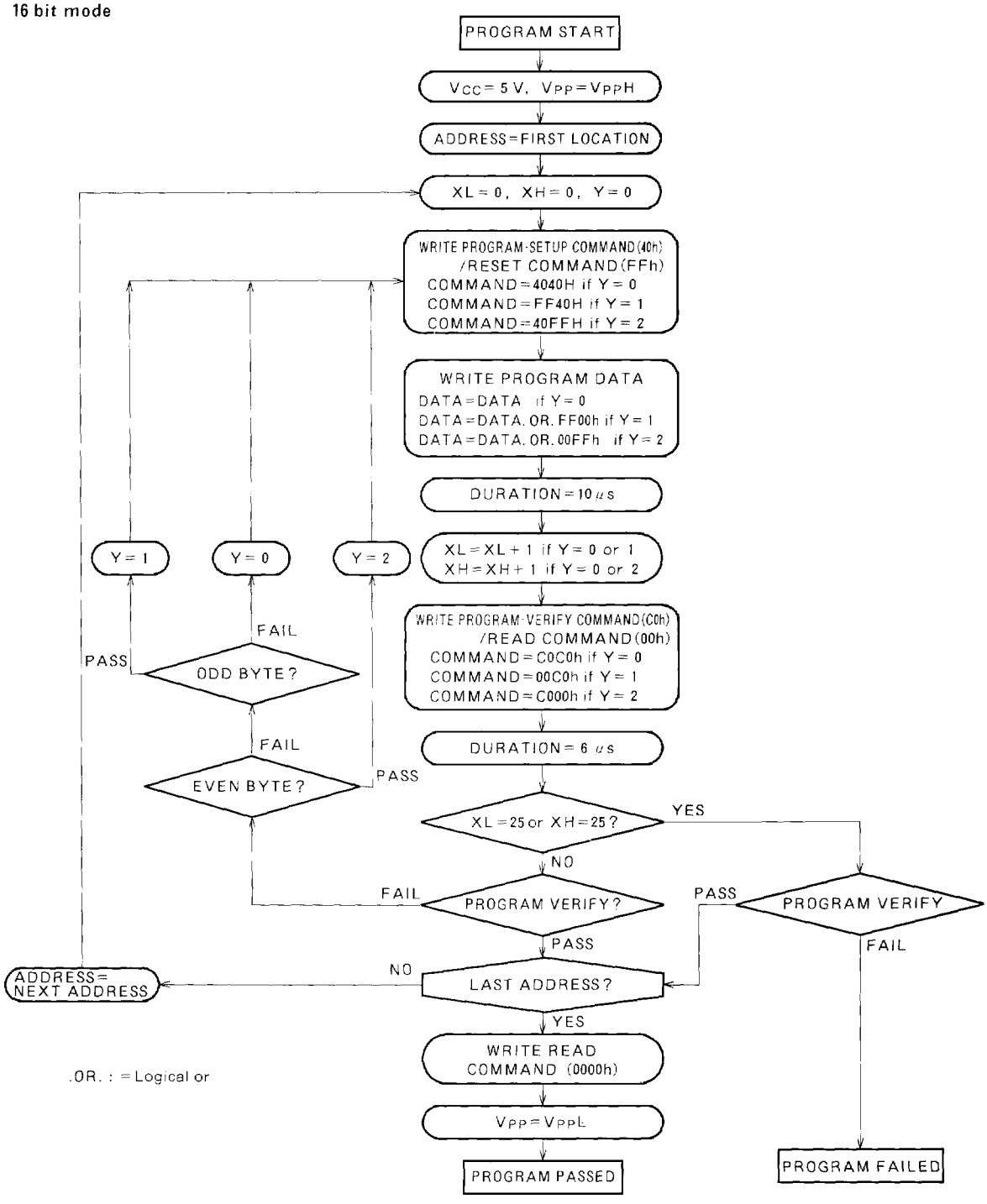
PROGRAM ALGORITHM

8 bit mode



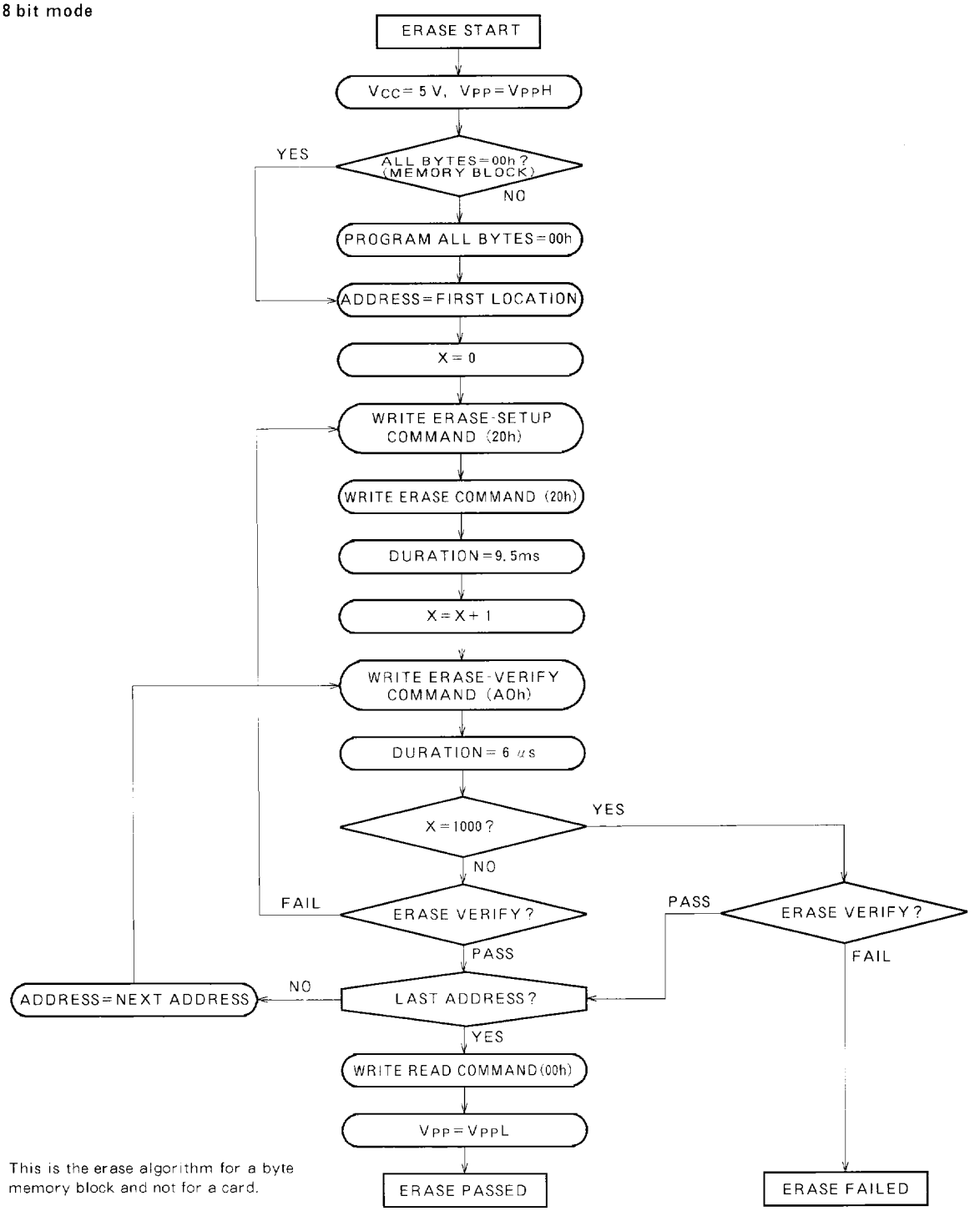
PROGRAM ALGORITHM

16 bit mode



ERASE ALGORITHM

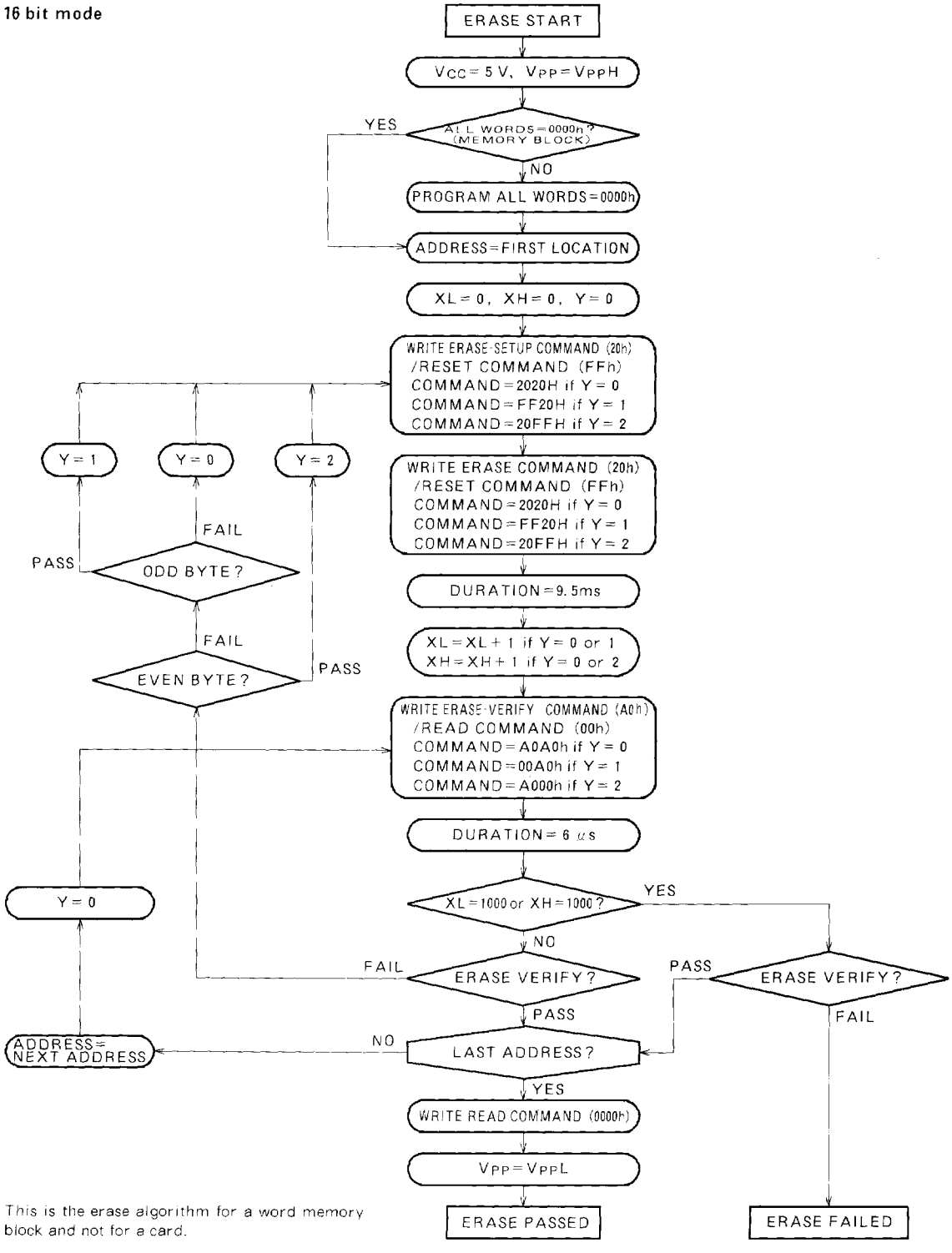
8 bit mode



This is the erase algorithm for a byte memory block and not for a card.

ERASE ALGORITHM

16 bit mode



This is the erase algorithm for a word memory block and not for a card.

BUS STATUS AT PROGRAMMING

8 bit mode

Mode	Address	Data in	Data out	Notes
Write program setup command	PA	40h	—	PA = Programming address
Program	PA	PD	—	PD = Programming data
Write program verify command	PA	C0h	—	
Read program verified data	PA	—	PVD	PVD = Program verified data

16 bit mode

Mode		Address	Data in		Data out		Notes
D15~D8	D7~D0		D15~D8	D7~D0	D15~D8	D7~D0	
Write program setup command		PA	40h	40h	—	—	
Program		PA	PDH	PDL	—	—	PDH = Programming data PDL = Programming data
Write program verify command		PA	C0h	C0h	—	—	
Read program verified data		PA	—	—	PVDH	PVDL	PVDH = Program verified data PVDL = Program verified data
Write program setup command	Write reset command	PA	40h	FFh	—	—	When programming of even byte has completed
Program	Write reset command	PA	PDH	FFh	—	—	
Write program verify command	Write read command	PA	C0h	00h	—	—	
Read program verified data	Read data	PA	—	—	PVDH	PDL	
Write reset command	Write program setup command	PA	FFh	40h	—	—	When programming of odd byte has completed
Write reset command	Program	PA	FFh	PDL	—	—	
Write read command	Write program verify command	PA	00h	C0h	—	—	
Read data	Read program verified data	PA	—	—	PDH	PVDL	

BUS STATUS AT ERASURE

8 bit mode

Mode	Address	Data in	Data out	Notes
Write erase setup command	BA	20h	—	BA = Block address
Write erase command	BA	20h	—	
Write erase verify command	EVA	A0h	—	EVA = Erase verifying address
Read erase verified data	EVA	—	EVD	EVD = Erase verified data

16 bit mode

Mode		Address	Data in		Data out		Notes
D15~D8	D7~D0		D15~D8	D7~D0	D15~D8	D7~D0	
Write erase setup command		BA	20h	20h	—	—	
Write erase command		BA	20h	20h	—	—	
Write erase verify command		EVA	A0h	A0h	—	—	
Read erase verified data		EVA	—	—	EVDH	EVDL	EVDH = Erase verified data EVDL = Erase verified data
Write erase setup command	Write reset command	BA	20h	FFh	—	—	When erasure of even byte has completed
Write erase command	Write reset command	BA	20h	FFh	—	—	
Write erase verify command	Write read command	EVA	A0h	00h	—	—	
Read erase verified data	Read data	EVA	—	—	EVDH	FFh	
Write reset command	Write erase setup command	BA	FFh	20h	—	—	When erasure of odd byte has completed
Write reset command	Write erase command	BA	FFh	20h	—	—	
Write read command	Write erase verify command	EVA	00h	A0h	—	—	
Read data	Read erase verified data	EVA	—	—	FFh	EVDL	

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	V_{CC} supply voltage	With respect to GND	−0.5~6.0	V
V_{PP}	V_{PP} supply voltage		−0.5~14.0	V
V_I	Input voltage		−0.3~V_{CC}+0.3	V
V_O	Output voltage		0~V_{CC}	V
T_{opr}	Operating temperature	Read/Write operation	0~70	℃
T_{stg}	Storage temperature		−40~80	℃

RECOMMENDED OPERATING CONDITIONS (T_a = 0 ~ 55℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
V_{CC}	V_{CC} supply voltage	4.75	5.0	5.25	V
V_{PPL}	V_{PP} supply voltage during READ only mode	0	V_{CC}	V_{CC}+1.0	V
V_{PPH}	V_{PP} supply voltage during READ WRITE mode	11.4	12.0	12.6	V
V_{IH}	High input voltage	2.4		V_{CC}	V
V_{IL}	Low input voltage	0		0.8	V
NACT	Number of simultaneous activated memory blocks			1	Block

ELECTRICAL CHARACTERISTICS (T_a = 0 ~ 55℃, V_{CC} = 5 V ± 5 %, V_{PP}=V_{PPL} or V_{PPH}, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min.	Typ.	Max.	
V_{OH}	High output voltage	I_{OH} = −0.1mA, BVDn		2.4			V
		I_{OH} = −1.0mA, Other outputs		2.4			
V_{OL}	Low output voltage	I_{OL} = 2mA				0.4	V
I_{IH}	High input current	V_I = V_{CC} V				10	μA
I_{IL}	Low input current	V_I = 0 V	$\overline{CE1}$, $\overline{CE2}$, $\overline{WE}$, $\overline{OE}$, $\overline{REG}$	−10		−70	μA
			Other inputs			−10	
I_{OZH}	High output current in off state	$\overline{CE1}$ = $\overline{CE2}$ = V_{IH} or $\overline{OE}$ = V_{IH}, V_O = V_{CC}				10	μA
I_{OZL}	Low output current in off state	$\overline{CE1}$ = $\overline{CE2}$ = V_{IH} or $\overline{OE}$ = V_{IH}, V_O = 0 V				−10	μA
$I_{CC1 \cdot 1}$	Active supply current 1	$\overline{CE1}$ = $\overline{CE2}$ = V_{IL}, Other inputs = V_{IH} or V_{IL}, Outputs = open				200	mA
$I_{CC1 \cdot 2}$	Active supply current 2	$\overline{CE1}$ = $\overline{CE2}$ ≤ 0.2V, Other inputs ≤ 0.2V or ≥ V_{CC} − 0.2V, Outputs = open				180	mA
$I_{CC2 \cdot 1}$	Standby supply current	$\overline{CE1}$ = $\overline{CE2}$ = V_{IH}, Other inputs = V_{IH} or V_{IL}				10	mA
$I_{CC2 \cdot 2}$	Standby supply current	$\overline{CE1}$ = $\overline{CE2}$ ≥ V_{CC} − 0.2V, Other inputs ≤ 0.2V or ≥ V_{CC} − 0.2V	256KB			0.5	mA
			512KB			0.7	
			1 MB			1.1	
			2 MB			2.0	
I_{PP1}	V_{PP} supply current (each V_{PP} pin)	V_{PP} = V_{PPL} ≦ V_{CC}	256KB			20	μA
			512KB			30	
			1 MB			50	
			2 MB			100	
I_{PP2}	V_{PP} supply current (each V_{PP} pin)	V_{PP} = V_{PPH} (standby, read)	256KB			0.3	mA
			512KB			0.5	
			1 MB			0.9	
			2 MB			1.7	
I_{PP3}	V_{PP} supply current (each V_{PP} pin)	V_{PP} = V_{PPH} (program/erase/verify)				35	mA

Note 4 : Currents flowing into the card are taken as positive.

5 : Typical values are measured at V_{CC} = 5 V, V_{PPL} = 5 V, V_{PPH} = 12V, T_a = 25℃.

6 : Card consumes active current at programming, erasure and verification.

CAPACITANCE

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
C_I	Input capacitance	V_I=GND, v_i=25mVrms, f=1 MHz, T_a=25℃			45	pF
C_O	Output capacitance	V_O=GND, v_o=25mVrms, f=1 MHz, T_a=25℃			45	pF

Note 7 : These parameters are not 100% tested.

SWITCHING CHARACTERISTICS (COMMON MEMORY)

Read Cycle (T_a=0~55℃, V_{CC}=5 V±5%, V_{PP}=V_{PPL} or V_{PPH}, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t_{RC}	Read cycle time	200			ns
$t_{a(A)}$	Address access time			200	ns
$t_{a(CE)}$	Card enable access time			200	ns
$t_{a(OE)}$	Output enable access time			100	ns
$t_{dis(CE)}$	Output disable time (from $\overline{CE}$)			90	ns
$t_{dis(OE)}$	Output disable time (from $\overline{OE}$)			90	ns
$t_{en(CE)}$	Output enable time (from $\overline{CE}$)	5			ns
$t_{en(OE)}$	Output enable time (from $\overline{OE}$)	5			ns
$t_{V(A)}$	Data valid time after address change	0			ns
t_{WRR}	Write recovery time before read	6			μs

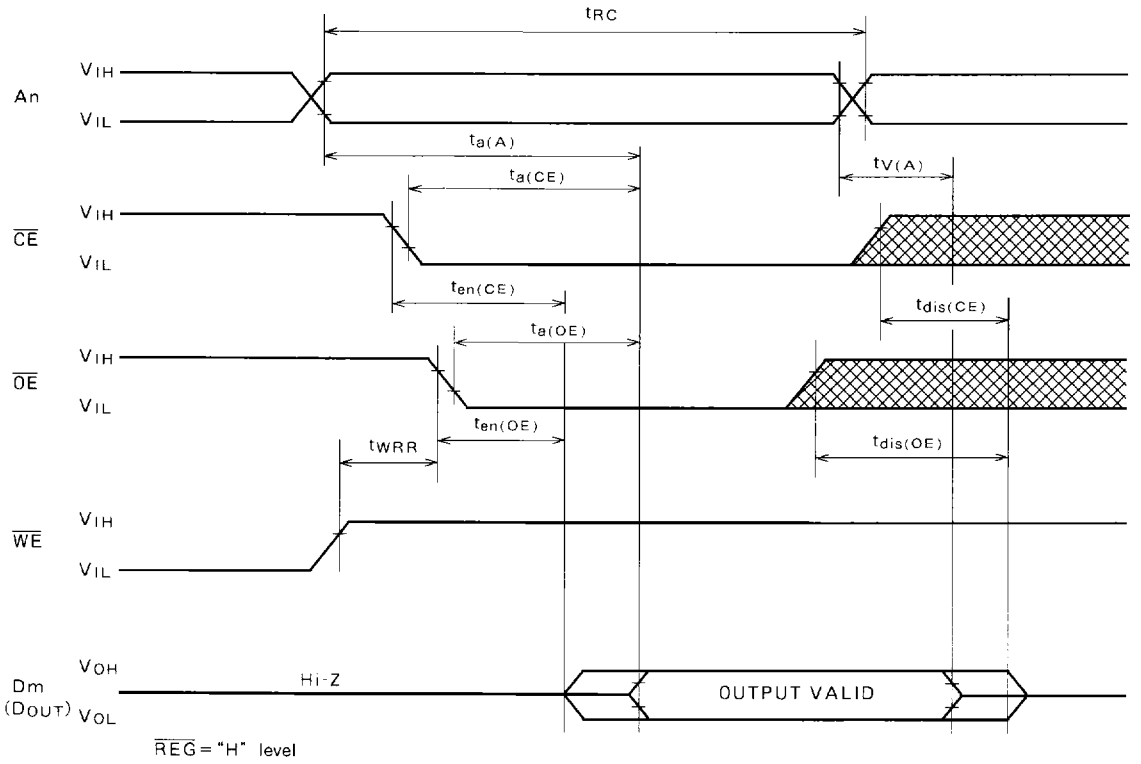
TIMING REQUIREMENTS (COMMON MEMORY)

Write Cycle (T_a=0~55℃, V_{CC}=5 V±5%, V_{PP}=V_{PPH}, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t_{WC}	Write cycle time	200			ns
t_{AS}	Address setup time	20			ns
t_{AH}	Address hold time	30			ns
t_{DS}	Data setup time	60			ns
t_{DH}	Data hold time	30			ns
t_{WRR}	Write recovery time before read	6			μs
t_{RRW}	Read recovery time before write	10			ns
t_{CS}	Card enable setup time before write	20			ns
t_{CH}	Card enable hold time	30			ns
t_{WP}	Write pulse width	120			ns
t_{WPH}	Write pulse width high	40			ns
t_{DP}	Duration of programming operation	10			μs
t_{DE}	Duration of erase operation	9.5			ms
t_{VSC}	V_{PP} setup time to card enable low	1			μs

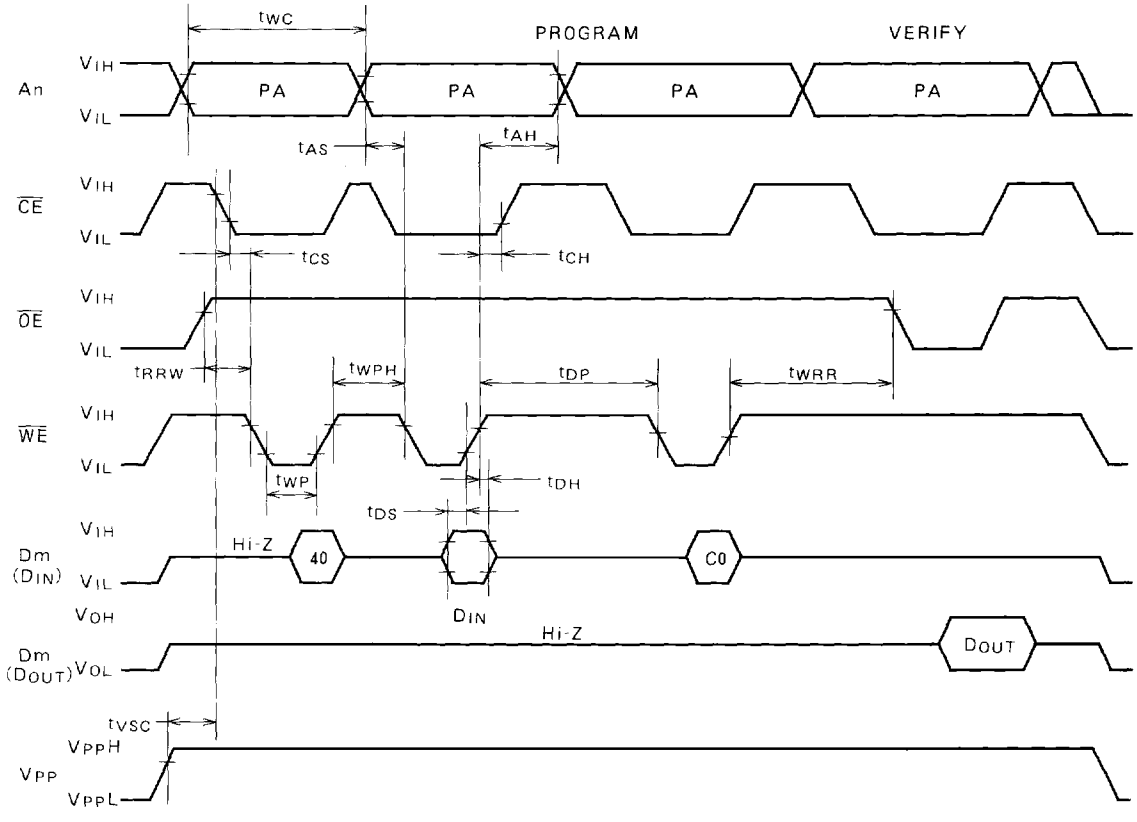
Note 8 : Refer to switching characteritics for read parameters

TIMING DIAGRAM
Common Memory Read



Note 9 : Indicates the don't care input.

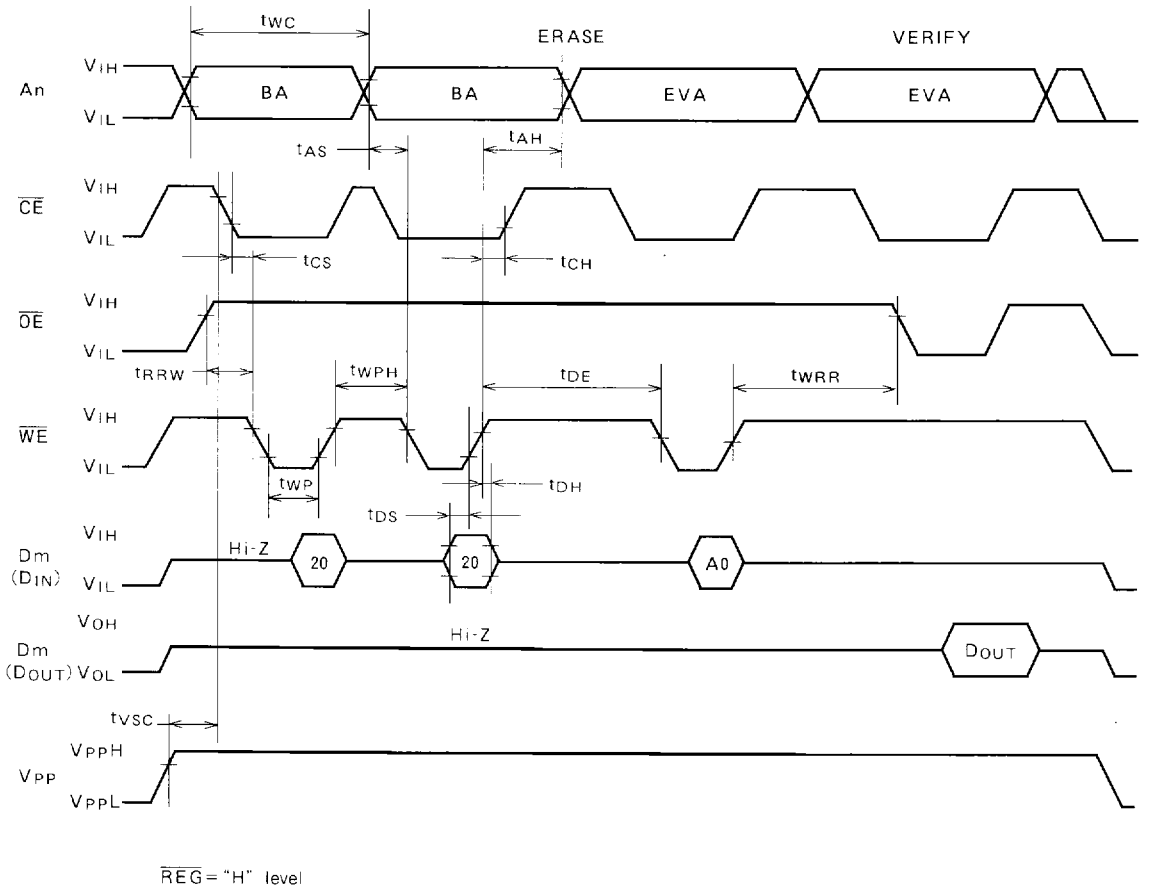
Common Memory Program



$\overline{REG}$ = "H" level

TIMING DIAGRAM

Common Memory Erase



$\overline{REG}$ = "H" level

SWITCHING CHARACTERISTICS (Attribute Memory)

Read Cycle (T_a = 0 ~ 55℃, V_{CC} = 5 V ± 5 %, V_{PP} = V_{CC}, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t_{RCR}	Read cycle time	300			ns
$t_{a(A)R}$	Address access time			300	ns
$t_{a(CE)R}$	Card enable access time			300	ns
$t_{a(OE)R}$	Output enable access time			150	ns
$t_{dis(CE)R}$	Output disable time (from $\overline{CE}$)			100	ns
$t_{dis(OE)R}$	Output disable time (from $\overline{OE}$)			100	ns
$t_{en(CE)R}$	Output enable time (from $\overline{CE}$)	5			ns
$t_{en(OE)R}$	Output enable time (from $\overline{OE}$)	5			ns
$t_{V(A)R}$	Data valid time after address change	0			ns

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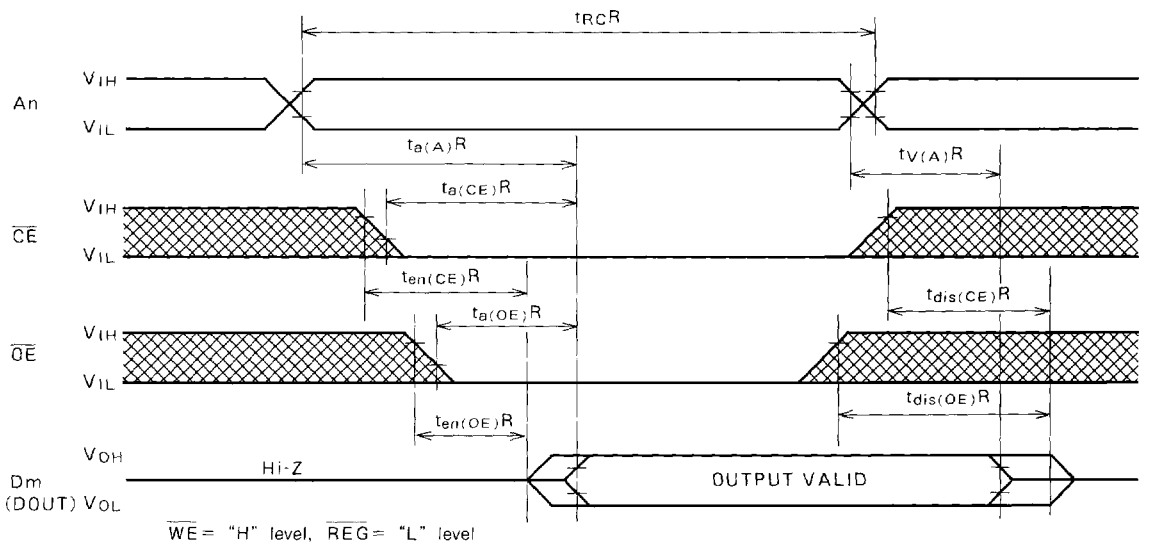
TIMING DIAGRAM (Attribute Memory)

Read



Note 10 : AC Test Conditions
Input pulse levels ; V_{IL} = 0.4V, V_{IH} = 2.8V
Input pulse rise, fall time ; $t_r = t_f$ = 10ns
Reference voltage
Input : V_{IL} = 0.8V, V_{IH} = 2.4V
Output : V_{OL} = 0.8V, V_{OH} = 2.0V
(t_{en} and t_{dis} are measured when output voltage is ±500mV from steady state.)
Load : 100pF + 1 TTL gate
5 pF + 1 TTL gate (at t_{en} and t_{dis} measuring)

11 : The data write is performed during the interval when both $\overline{CE}$ and $\overline{WE}$ are low "L" level.

12 : Do not apply inverted phase signal externally when Dm pin is in output mode.

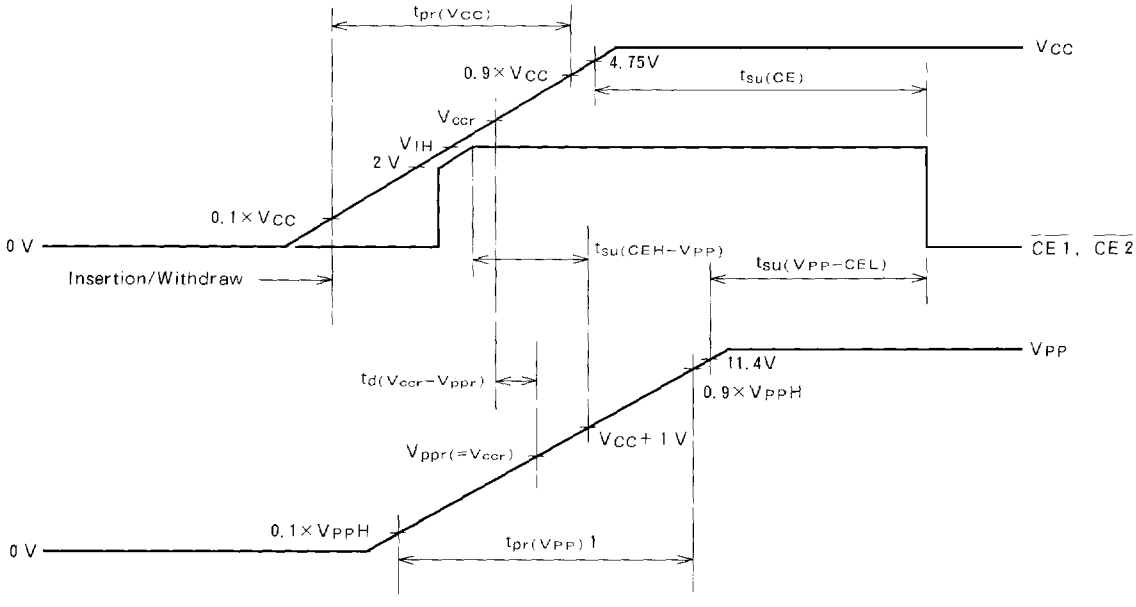
13 : $\overline{CE}$ is indicated as follows ;
Read A/Write A : $\overline{CE} = \overline{CE1} = \overline{CE2}$
Read B/Write B : $\overline{CE} = \overline{CE1}$, $\overline{CE2}$ = "H" level
Read C/Write C : $\overline{CE} = \overline{CE2}$, $\overline{CE1}$ = "H" level

RECOMMENDED POWER UP/DOWN CONDITIONS (T_a = 0 ~55℃, unless otherwise noted)

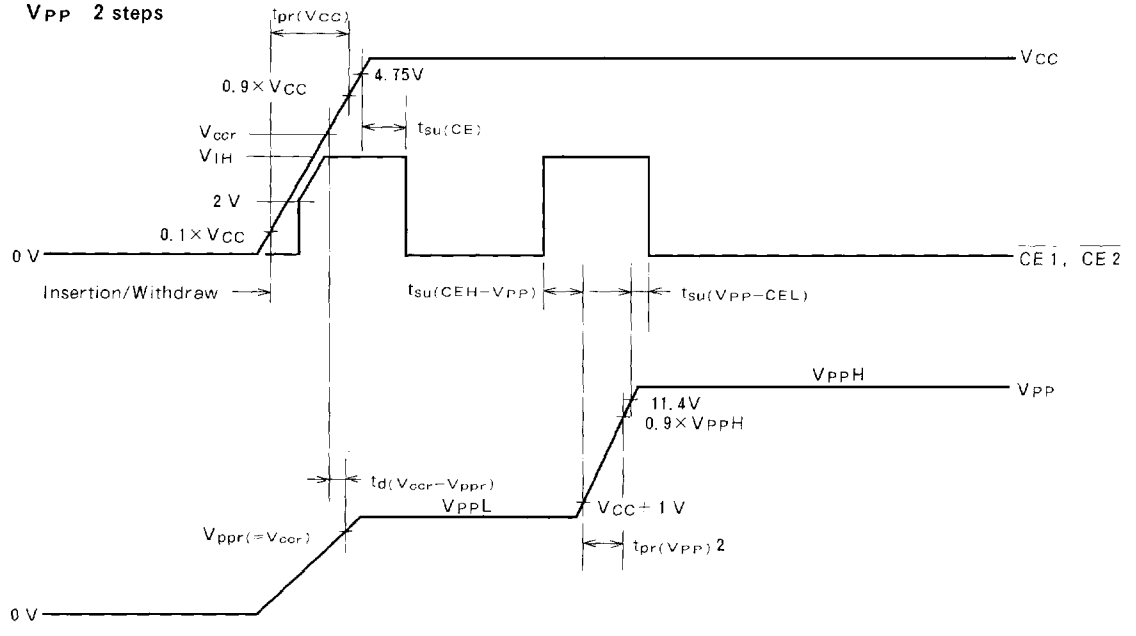
Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Vi (CE)	$\overline{CE}$ input voltage	0 V≦V_{CC}< 2 V	0		V_{CC}	V
		2 V≦V_{CC}<2.4V	V_{CC}-0.1	V_{CC}	V_{CC}+0.1	V
		2.4V≦V_{CC}	2.4		V_{CC}+0.1	V
$t_{su(CE)}$	$\overline{CE}$ setup time		1			ms
$t_{rec(CE)}$	$\overline{CE}$ recovery time		1			μs
$t_{pr(VCC)}$	V_{CC} rise time		0.1		300	ms
$t_{pf(VCC)}$	V_{CC} fall time		3		300	ms
$t_{su(CEH-VPP)}$	Setup time before V_{PP} rise		0.15			μs
$t_{su(VPP-CEL)}$	Setup time after V_{PP} rise		1			μs
$t_{rec(CEH-VPP)}$	Recovery time before V_{PP} fall		0.15			μs
$t_{rec(VPP-CEL)}$	Recovery time after V_{PP} fall		1			μs
$t_{pr(VPP)1}$	V_{PP} rise time 1		0.24		300	ms
$t_{pf(VPP)1}$	V_{PP} fall time 1		7.2		300	ms
$t_{pr(VPP)2}$	V_{PP} rise time 2		0.1		300	ms
$t_{pf(VPP)2}$	V_{PP} fall time 2		3		300	ms
$t_{d(VCCr-VPPr)}$	V_{PPr} delay time after V_{CCr}	0 V≦V_{CC}≦4.75V	0			μs
$t_{d(VPPf-VCCf)}$	V_{CCf} delay time after V_{PPf}	0 V≦V_{CC}≦4.75V	0			μs

POWER UP TIMING DIAGRAM

V_{PP} 1 step



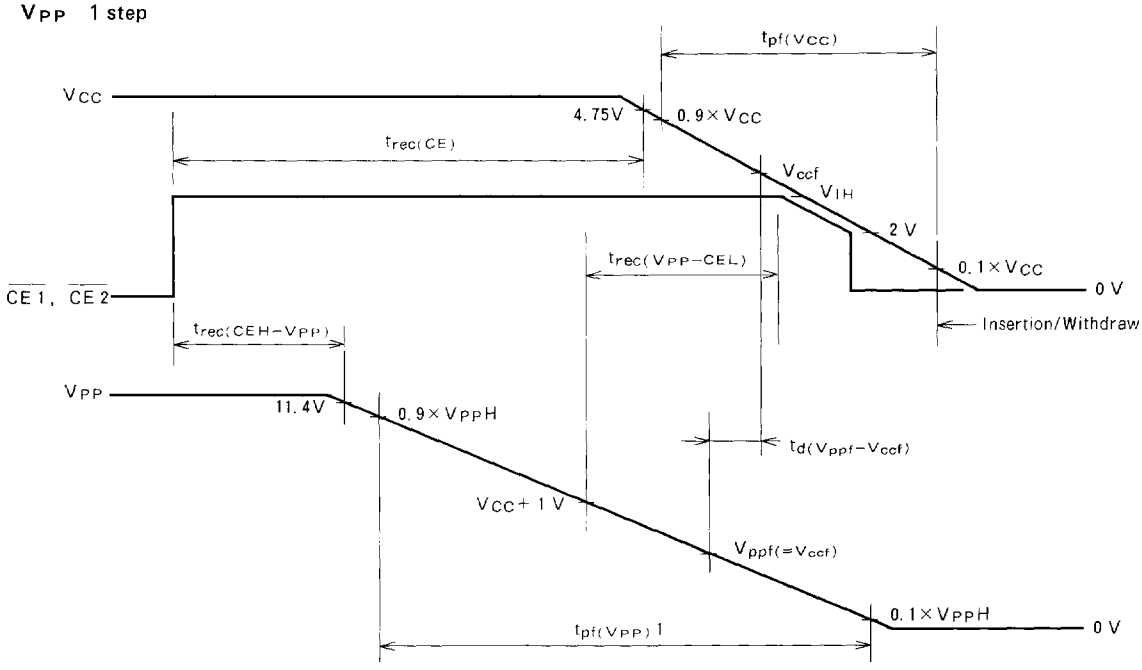
V_{PP} 2 steps



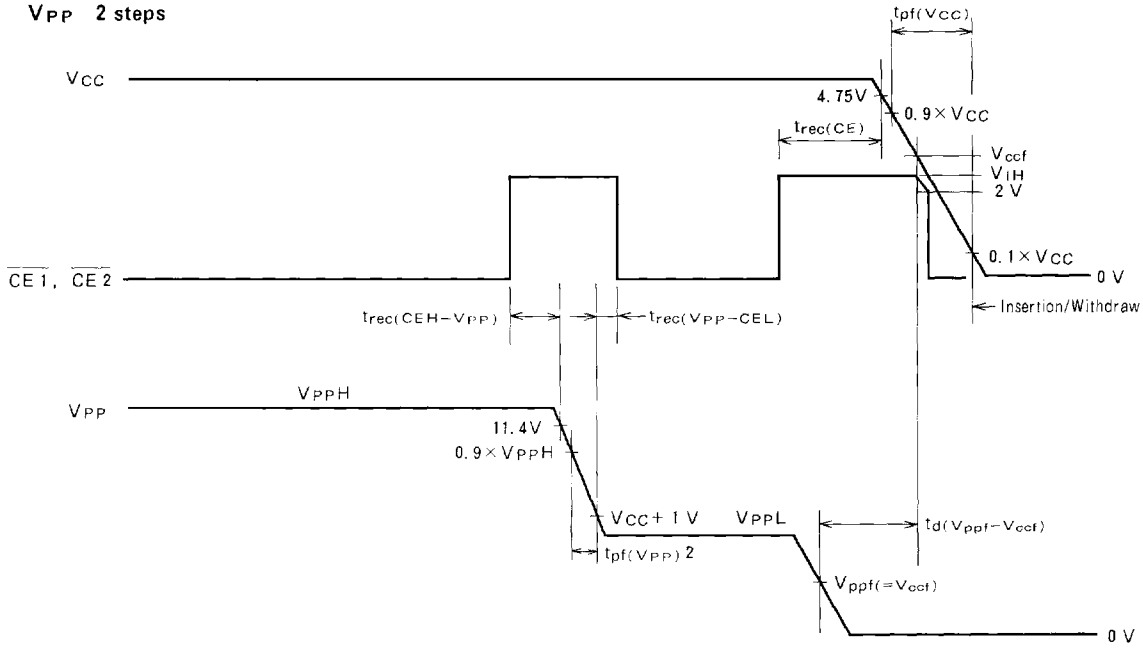
Note 14 : V_{ccr} and V_{ppr} (= V_{ccr}) indicates any voltage when V_{CC} voltage is in the range of 0 V to 4.75V

POWER DOWN TIMING DIAGRAM

V_{PP} 1 step



V_{PP} 2 steps



Note 15 : V_{ccr} and V_{ppr} ($=V_{ccr}$) indicates any voltage when V_{CC} voltage is in the range of 0 V to 4.75V