QUALITY SEMICONDUCTOR, INC.

Low Skew Clock Driver/ Buffer for Mobile PC with 4 SO-DIMMS

QS5810

ADVANCE INFORMATION

FEATURES/BENEFITS

- 1 to 10 output buffer/driver
- Tri-state pin for testing
- I^2C programming capability
- Power Supply Voltage 3.3V ±5%
- Low Skew outputs (<250ps)
- Up to 100MHz operation
- Multiple V_{DD} and GND for noise reduction
- 28 pin SSOP package

DESCRIPTION

The QS5810 is a high speed, low noise and 1 - 10 non-inverting buffer designed for SDRAM clock buffer applications. Out of the 10 outputs 8 of them could be used to drive up to four SDRAM SO-DIMMs, and the remaining can be used for external feedback to a PLL stage for synchronization to a master clock. The device is intended for use at 3.3V and the outputs can run up to 100MHz. The QS5810 also includes an I^2C interface, which can enable or disable each output clock driver. Turning unused outputs off reduces EMI.

Figure 1. Functional Block Diagram

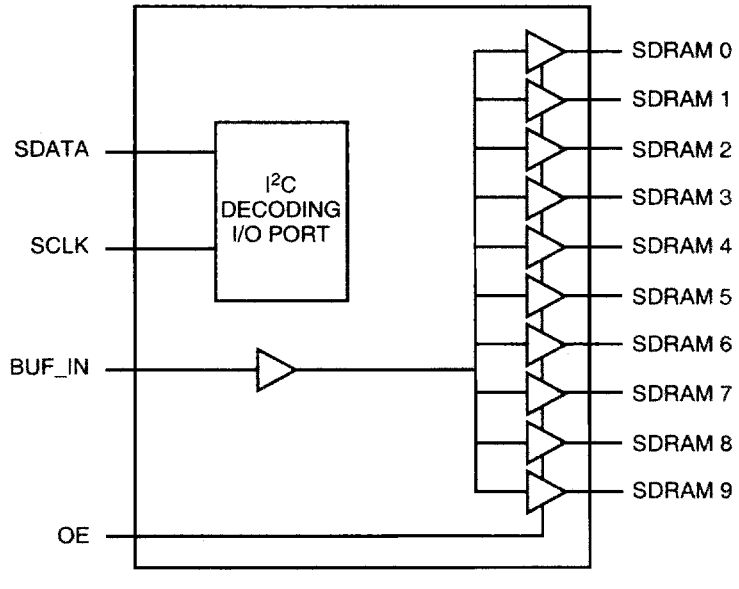


Figure 2. Pin Configuration
(All Pins Top View)

SSOP

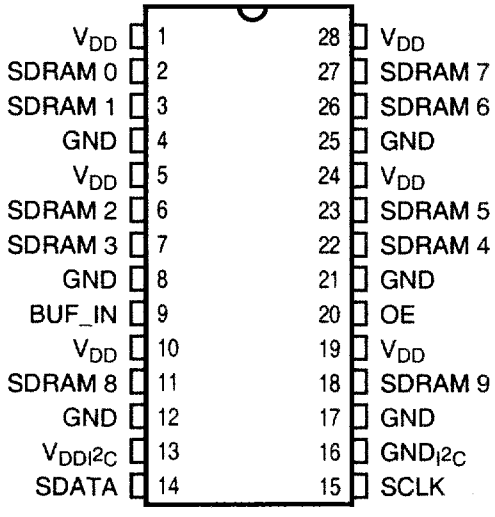


Table 1. Pin Description

Pin Name	Pin Number	Type	Functional Description
SDRAM (0:3)	2,3,6,7	Out	SDRAM Byte 0 Clock outputs.
SDRAM (4:7)	22,23,26,27	Out	SDRAM Byte 1 Clock outputs.
SDRAM (8:9)	11,18	Out	SDRAM Byte 2 Clock outputs.
BUF_IN	9	IN	Input for buffers.
SDATA	14	I/O	I^2C Data input. It has 100kΩ internal pull up to V_{DD}.
SCLK	15	I/O	I^2C Clock input. It has 100kΩ internal pull up to V_{DD}.
OE	20	IN	Tri-state output enable. When asserted HIGH, clock outputs are high impedance. It has 100kΩ internal pull up to V_{DD}.
V_{DD}	1,5,10,19,24,28	PWR	3.3V power supply for output buffers.
GND	4,8,12,17,21,25	PWR	Ground for output buffers
GND_{I2C}	16	PWR	Ground for I^2C circuitry.
V_{DDI2C}	13	PWR	3.3V power supply for I^2C circuitry.

Table 2. Absolute Maximum Ratings

Supply Voltage to Ground	–0.5V to 4.6V
DC Output Voltage V_{OUT}	–0.5V to 4.6V
DC Input Voltage V_{IN}	–0.5V to 4.6V
DC Input Diode Current with $V_I < 0$	–20mA
Maximum Power Dissipation at $T_A = 85°C$,	600mW
T_{STG} Storage Temperature	–65° to 150°C

Note: Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to QSI devices that result in functional or reliability type failures.

Table 3. Recommended Operating Conditions

Symbol	Description	Min	Typ	Max	Unit
V_{DD}	Power Supply Voltage	3.135	3.3	3.465	V
T_A	Operating Temperature	–40	25	85	°C
C_L	Load Capacitance	—	—	30	pF
C_{IN}	Input Capacitance(1)	—	—	7	pF

Table 4. DC Electrical Characteristics Over Operating Range

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{IH}	Input High Voltage	For all inputs	2.0	—	—	V
V_{IL}	Input Low Voltage	For all inputs except I^2C inputs	—	—	0.8	V
		I^2C inputs (SDATA and SCLK)	—	—	0.7	
I_{IH}	Input High Input Current	$V_{IN} = V_{DD}$	–5	—	5	µA
I_{IL}	Input Low Current	V_{IN} = 0V; BUF_IN	–5		5	µA
		V_{IN} = 0V; OE, SDATA, SCLK	–100		0	
I_{DD}	Supply Current	C_L = 0pF; f_{IN} @ 66.66MHz(1)	—		150	mA
		C_L = 0pF; f_{IN} @ 100MHz(1)	—		200	
		C_L = 30pF; f_{IN} @ 66.66MHz(1)	—		230	
		C_L = 30pF; f_{IN} @ 100MHz(1)	—		360	
		BUF_IN = GND or V_{DD}, all other inputs to V_{DD}	—		500	µA
V_{OH}	Output High Voltage	SDRAM (0:9) I_{OH} = –36mA	2.4		—	V
V_{OL}	Output Low Voltage	SDRAM (0:9) I_{OL} = 25mA	—		0.4	V
V_{OLI2C}	Output Low Voltage	SDATA I_{OLI2C} = 3mA	—	—	0.4	V

Table 5. AC Electrical Characteristics Over Operating Range

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
T_R	Rise Time(1)	0.4V to 2.4V; C_L = 30pF	—		2.2	ns
T_F	Fall Time(1)	2.4V to 0.4V; C_L = 30pF	—		2.2	ns
D_t	Duty Cycle(1)	V_T = 1.5V; C_L = 30pF; With 50% Input Clock	45	50	55	%
T_{SK}	Skew (output – output)(1)	V_T = 1.5V; C_L = 30pF for all outputs; see Figure 3	—		200	ps
T_{PHL} or T_{PLH}	Propagation Delay	V_T = 1.5V	—		6.0	ns
T_{PZL} or T_{PZH}	Enable Delay	V_T = 1.5V; see Figure 4	—		8.0	ns
T_{PLZ} or T_{PHZ}	DisableDelay	V_T = 1.5V: see Figure 4	—		8.0	ns
F_{IN}	Input Frequency	All the outputs loaded	—		100	MHz

Note:
1. Applies to SDRAM (0:9) outputs. Guaranteed by design, not subject to 100% production testing.

I²C Serial Interface Control

The I²C interface permits individual enable/disable of each clock output: any unused outputs may be disabled to reduce the EMI. The QS5810 is a slave receiver device. It can read back the data stored in the latches for verification.

The data transfer rate supported by the I²C interface is 100k bits/sec. Data is transferred in bytes (with the addition of start, stop, acknowledge bits) in sequential order from lowest to highest byte with the ability to stop after any complete byte has been transferred. The first two bytes transferred must be a Command Code followed by a Byte Count. Both of these bytes are ignored by the device.

The I²C address of the QS5810 is:

A7	A6	A5	A4	A3	A2	A1
1	1	0	1	0	0	1

Address A0 is the read/write bit and is set to 0 for writes and 1 for reads.

During read back, the first byte read is a Byte Count representing the number of bytes following (fixed at 3).

Table 6. Serial Configuration Command Bitmaps

Byte 0: SDRAM Active/Inactive Register
(1 = Enable, 0 = Disable), Default = Enable

Bit	Pin #	Description
Bit 7	—	Initialize to 0
Bit 6	—	Initialize to 0
Bit 5	—	Initialize to 0
Bit 4	—	Initialize to 0
Bit 3	7	SDRAM 3 (Active/Inactive)
Bit 2	6	SDRAM 2 (Active/Inactive)
Bit 1	3	SDRAM 1 (Active/Inactive)
Bit 0	2	SDRAM 0 (Active/Inactive)

Byte 1: SDRAM Active/Inactive Register
(1 = Enable, 0 = Disable), Default = Enable

Bit	Pin #	Description
Bit 7	27	SDRAM 7 (Active/Inactive)
Bit 6	26	SDRAM 6 (Active/Inactive)
Bit 5	23	SDRAM 5 (Active/Inactive)
Bit 4	22	SDRAM 4 (Active/Inactive)
Bit 3	—	Initialize to 0
Bit 2	—	Initialize to 0
Bit 1	—	Initialize to 0
Bit 0	—	Initialize to 0

Byte 2: SDRAM Active/Inactive Register
(1 = Enable, 0 = Disable), Default = Enable

Bit	Pin #	Description
Bit 7	18	SDRAM 9 (Active/Inactive)
Bit 6	11	SDRAM 8 (Active/Inactive)
Bit 5	—	Reserved, 1 at power up, set to 0
Bit 4	—	Reserved, 1 at power up, set to 0
Bit 3	—	Reserved, 1 at power up, set to 0
Bit 2	—	Reserved, 1 at power up, set to 0
Bit 1	—	Reserved, 1 at power up, set to 0
Bit 0	—	Reserved, 1 at power up, set to 0

Figure 3. Test Loads

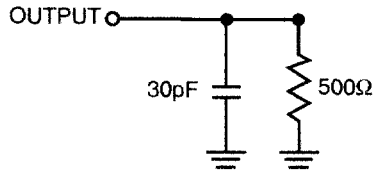
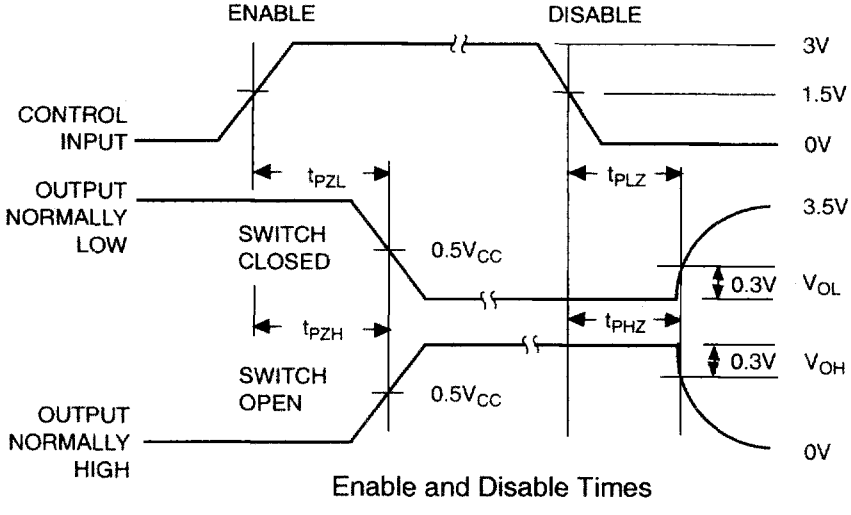


Figure 4. AC Timing Diagram



Enable and Disable Times

Figure 5. Ordering Information

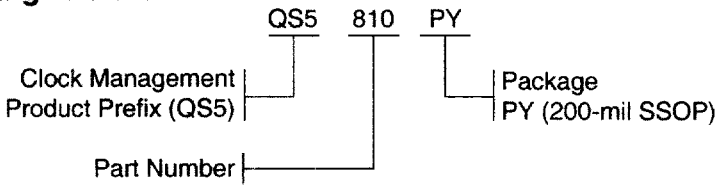
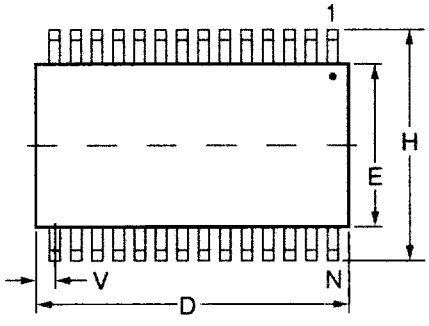
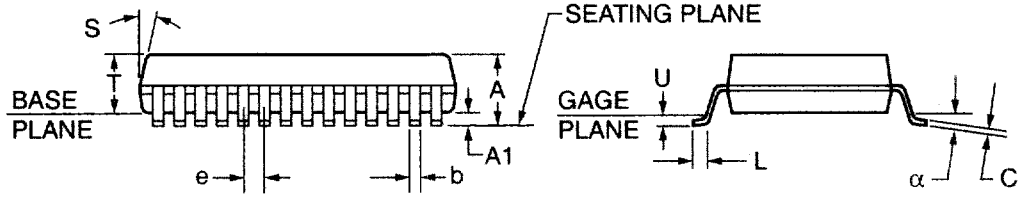


Figure 6. Packaging Information
200-mil SSOP - Package Code PY

Shrink Small Outline Package



Note:
1. Refer to applicable symbol list.
2. All dimensions are in inches.
3. N is the number of lead positions.
4. "D" and "E" are referance datums on the molded body and do not include mold flash/protrusions. Mold flash/protrusions at "D" shall not exceed .006in. per side. Inter-lead flash / protrusions at "E" shall not exceed .008in. per side.



JEDEC#	MO-150-AH		
DWG#			
Symbol	**Min**	**Nom**	**Max**
A	0.079		
A1	0.002		0.008
b	0.010		0.015
C	0.004		0.008
D	0.394		0.409
E	0.205		0.212
e	0.0256 BSC		
H	0.295		0.319
L	0.025		0.040
N		28	
α	0°		8°
S		14°	
T	.065		.071
U		.010	
V		.035	