

# Synchronous-Rectified Buck MOSFET Driver

## General Description

The RT9612A/B is a high frequency, synchronous rectified, single phase dual MOSFET driver designed to adapt from normal MOSFET driving applications to high performance CPU VR driving capabilities.

The RT9612A/B can be utilized under both  $V_{CC} = 5V$  or  $V_{CC} = 12V$  applications. The RT9612A/B also builds in an internal power switch to replace external boot strap diode. The RT9612A/B can support switching frequency efficiently up to 500kHz. The RT9612A/B has the UGATE driving circuit and the LGATE driving circuit for synchronous rectified DC/DC converter applications. The driving rise/fall time capability is designed within 30ns and the shoot through protection mechanism is designed to prevent shoot through of high side and low side power MOSFETs. The RT9612A/B has PWM tri-state shut down function which can force driver output into high impedance.

The difference of the RT9612A and the RT9612B is the propagation delay,  $t_{UGATEpdh}$ . The RT9612B has comparatively large  $t_{UGATEpdh}$  than RT9612A. Hence, the RT9612A is usually recommended to be utilized in performance oriented applications, such as high power density CPU VR or GPU VR. The RT9612A/B comes in a small footprint with SOP-8, SOP-8 (Exposed Pad), WDFN-8EL 3x3 and WDFN-8L 2x2 packages.

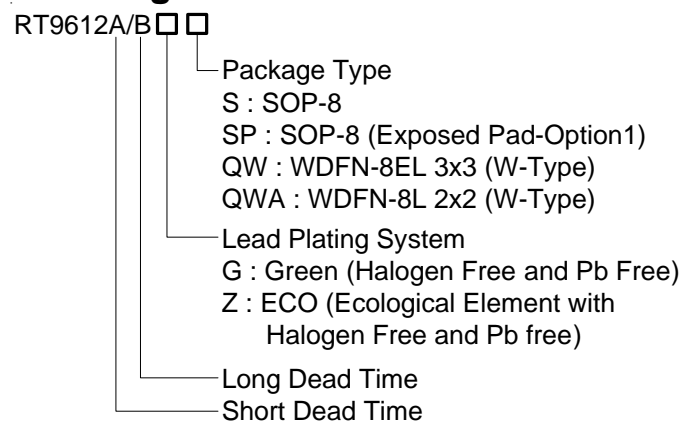
## Features

- Drive Two N-MOSFETs
- Adaptive Shoot Through Protection
- Embedded Bootstrap Diode
- Support High Switching Frequency
- Fast Output Rise Time
- Tri-State Input for Bridge Shutdown
- Small SOP-8, SOP-8 (Exposed Pad) and 8-Lead WDFN Packages
- RoHS Compliant and Halogen Free

## Applications

- Core Voltage Supplies for Desktop, Motherboard CPU
- High Frequency Low Profile DC/DC Converters
- High Current Low Voltage DC/DC Converters

## Ordering Information



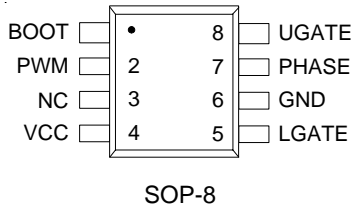
Note :

Richtek products are :

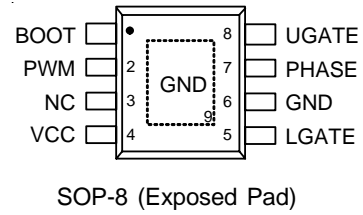
- ▶ RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- ▶ Suitable for use in SnPb or Pb-free soldering processes.

## Pin Configurations

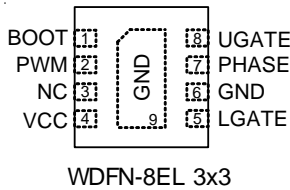
(TOP VIEW)



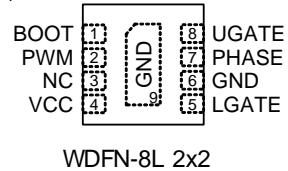
SOP-8



SOP-8 (Exposed Pad)



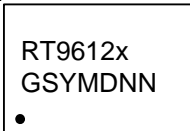
WDFN-8EL 3x3



WDFN-8L 2x2

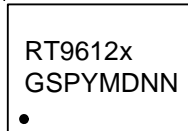
## Marking Information

RT9612xGS



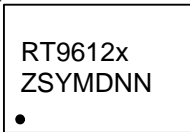
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x : A or B  
YMDNN : Date Code

RT9612xGSP



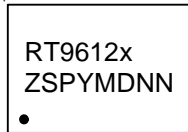
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RT9612xZS



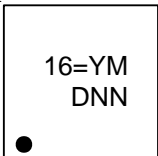
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RT9612xZSP



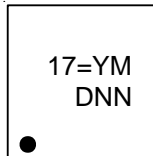
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RT9612AGQW



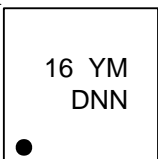
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RT9612BGQW



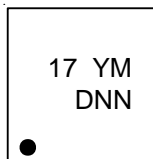
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RT9612AZQW



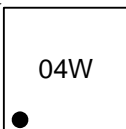
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RT9612BZQW



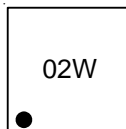
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RT9612AGQWA



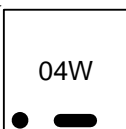
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RT9612BGQWA



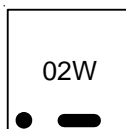
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RT9612AZQWA



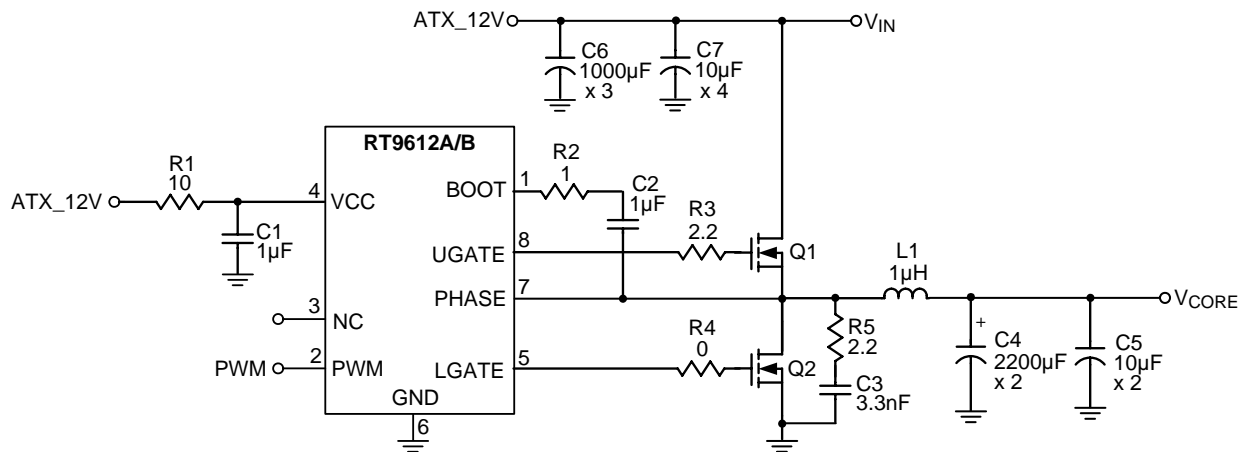
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RT9612BZQWA

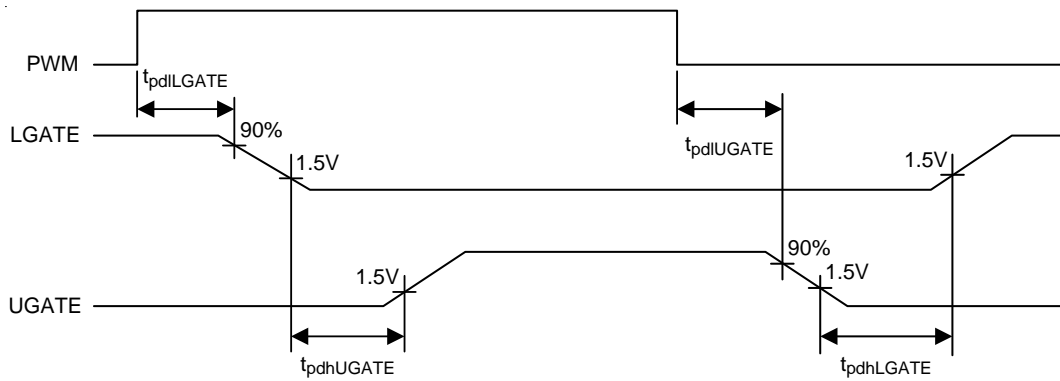


02 : Product Code  
W : Date Code

**Typical Application Circuit**



**Timing Diagram**





**Absolute Maximum Ratings** (Note 1)

- Supply Voltage,  $V_{CC}$  ----- -0.3V to 15V
- BOOT to PHASE ----- -0.3V to 15V
- PHASE to GND
  - DC ----- -5V to 15V
  - < 200ns ----- -10V to 30V
- LGATE
  - DC ----- (GND - 0.3V) to ( $V_{CC} + 0.3V$ )
  - < 200ns ----- -2V to ( $V_{CC} + 0.3V$ )
- UGATE ----- ( $V_{PHASE} - 0.3V$ ) to ( $V_{BOOT} + 0.3V$ )
  - < 200ns ----- ( $V_{PHASE} - 2V$ ) to ( $V_{BOOT} + 0.3V$ )
- PWM Input Voltage ----- (GND - 0.3V) to 7V
- Power Dissipation,  $P_D$  @  $T_A = 25^\circ C$ 
  - SOP-8 ----- 0.833W
  - SOP-8 (Exposed Pad) ----- 1.333W
  - WDFN-8EL 3x3 ----- 1.429W
  - WDFN-8L 2x2 ----- 0.833W
- Package Thermal Resistance (Note 2)
  - SOP-8,  $\theta_{JA}$  ----- 120°C/W
  - SOP-8 (Exposed Pad),  $\theta_{JA}$  ----- 75°C/W
  - SOP-8 (Exposed Pad),  $\theta_{JC}$  ----- 15°C/W
  - WDFN-8EL 3x3,  $\theta_{JA}$  ----- 70°C/W
  - WDFN-8EL 3x3,  $\theta_{JC}$  ----- 8.2°C/W
  - WDFN-8L 2x2,  $\theta_{JA}$  ----- 120°C/W
  - WDFN-8L 2x2,  $\theta_{JC}$  ----- 8.2°C/W
- Lead Temperature (Soldering, 10 sec.) ----- 260°C
- Junction Temperature ----- 150°C
- Storage Temperature Range ----- -65°C to 150°C
- ESD Susceptibility (Note 3)
  - HBM ----- 2kV
  - MM ----- 200V

**Recommended Operating Conditions** (Note 4)

- Supply Voltage,  $V_{CC}$  ----- 12V  $\pm$  10%
- Junction Temperature Range ----- -40°C to 125°C
- Ambient Temperature Range ----- -40°C to 85°C

## Electrical Characteristics

(V<sub>CC</sub> = 12V, T<sub>A</sub> = 25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit		
Power Supply Voltage	V <sub>CC</sub>		4.5	--	13.5	V		
Power Supply Current	I <sub>VCC</sub>	V <sub>BOOT</sub> = 12V, PWM = 0V	--	1.2	--	mA		
<b>Power On Reset</b>								
POR Threshold	V <sub>POR</sub>	V <sub>CC</sub> Rising	3	4	4.4	V		
Hysteresis	V <sub>CCh_ys</sub>		--	0.5	--	V		
<b>PWM Input</b>								
Maximum Input Current	I <sub>PWM</sub>	PWM = 0V or 5V	--	300	--	μA		
PWM Floating Voltage	V <sub>PWM_fl</sub>	V <sub>CC</sub> = 12V	1.6	1.8	2	V		
PWM Rising Threshold	V <sub>PWM_rth</sub>		2.8	--	--	V		
PWM Falling Threshold	V <sub>PWM_fth</sub>		--	--	0.8	V		
<b>Timing</b>								
UGATE Rise Time	t <sub>UGATEr</sub>	V <sub>CC</sub> = 12V, 3nF Load	--	25	--	ns		
UGATE Fall Time	t <sub>UGATEf</sub>	V <sub>CC</sub> = 12V, 3nF Load	--	12	--	ns		
LGATE Rise Time	t <sub>LGATEr</sub>	V <sub>CC</sub> = 12V, 3nF Load	--	24	--	ns		
LGATE Fall Time	t <sub>LGATEf</sub>	V <sub>CC</sub> = 12V, 3nF Load	--	10	--	ns		
Propagation Delay	RT9612A	t <sub>UGATEpdh</sub>	V <sub>BOOT</sub> – V <sub>PHASE</sub> = 12V See Timing Diagram	--	22	--	ns	
	RT9612B			--	60	--		
	RT9612A/B	t <sub>UGATEpdl</sub>		--	22	--		
		t <sub>LGATEpdh</sub>		See Timing Diagram	--	20		--
		t <sub>LGATEpdl</sub>			--	8		--
<b>Output</b>								
UGATE Drive Source	I <sub>UGATE_sr</sub>	V <sub>BOOT</sub> – V <sub>PHASE</sub> = 12V V <sub>UGATE</sub> – V <sub>PHASE</sub> = 12V	--	2	--	A		
UGATE Drive Sink	R <sub>UGATE_sk</sub>	V <sub>BOOT</sub> – V <sub>PHASE</sub> = 12V	--	1.4	--	Ω		
LGATE Drive Source	I <sub>LGATE_sr</sub>	V <sub>CC</sub> = 12V, V <sub>LGATE</sub> = 2V	--	2.2	--	A		
LGATE Drive Sink	R <sub>LGATE_sk</sub>	V <sub>CC</sub> = 12V	--	1.1	--	Ω		

**Note 1.** Stresses listed as the above “Absolute Maximum Ratings” may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

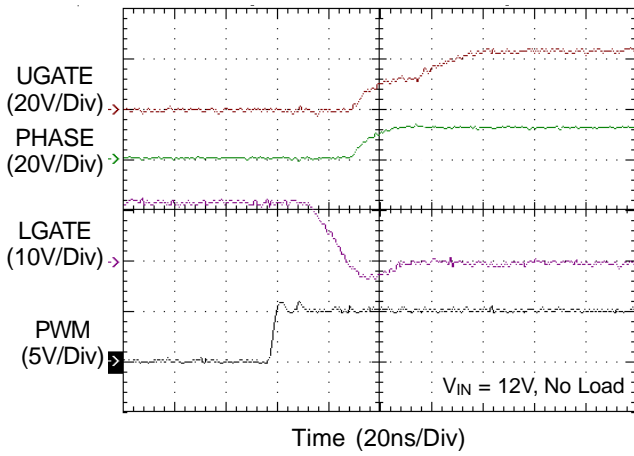
**Note 2.** θ<sub>JA</sub> is measured in natural convection at T<sub>A</sub> = 25°C on a high effective thermal conductivity test board of JEDEC 51-7 thermal measurement standard. The measurement case position of θ<sub>JC</sub> is on the exposed pad of the packages.

**Note 3.** Devices are ESD sensitive. Handling precaution is recommended.

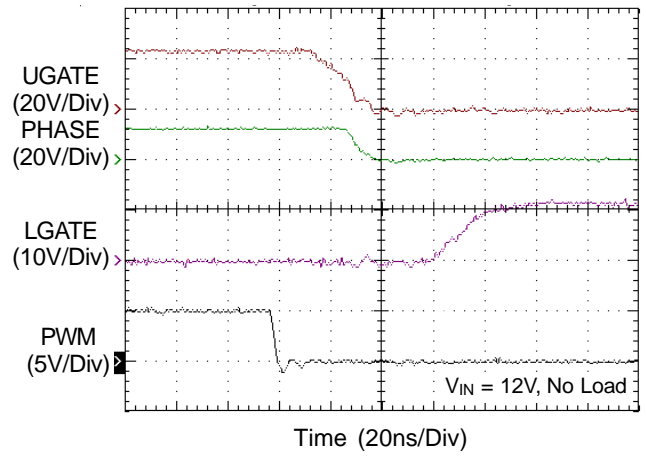
**Note 4.** The device is not guaranteed to function outside its operating conditions.

**Typical Operating Characteristics**

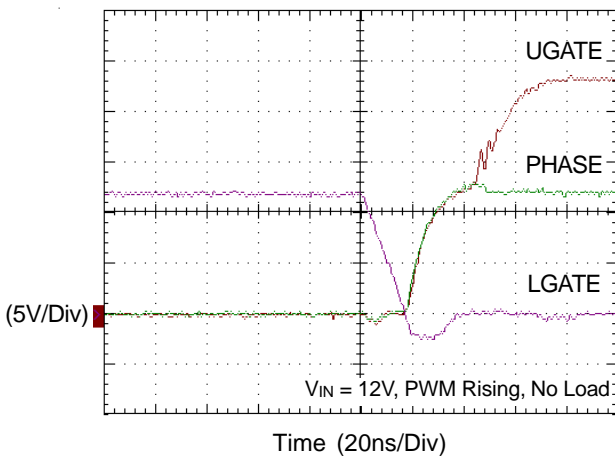
**PWM Rising Edge**



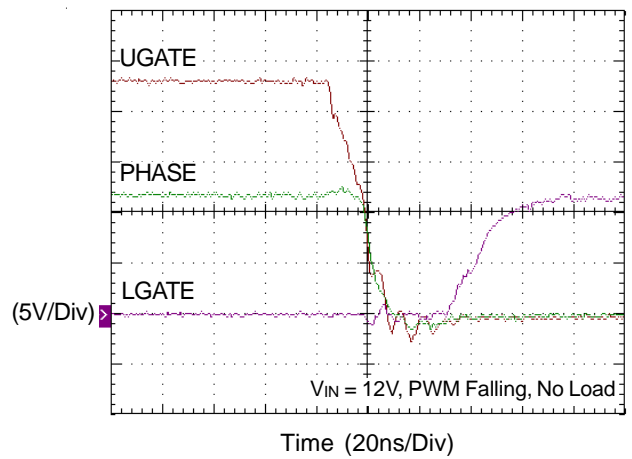
**PWM Falling Edge**



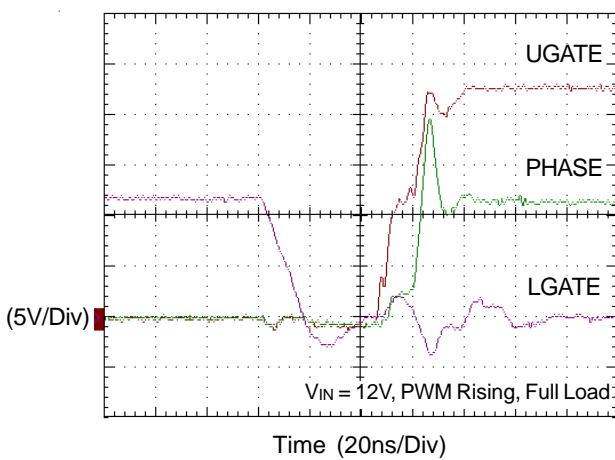
**Dead Time**



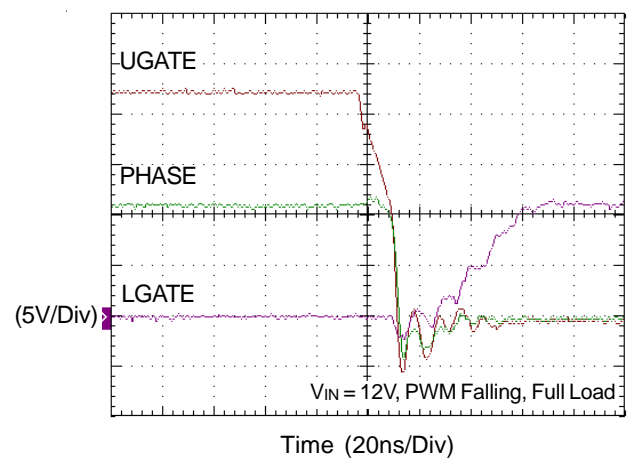
**Dead Time**



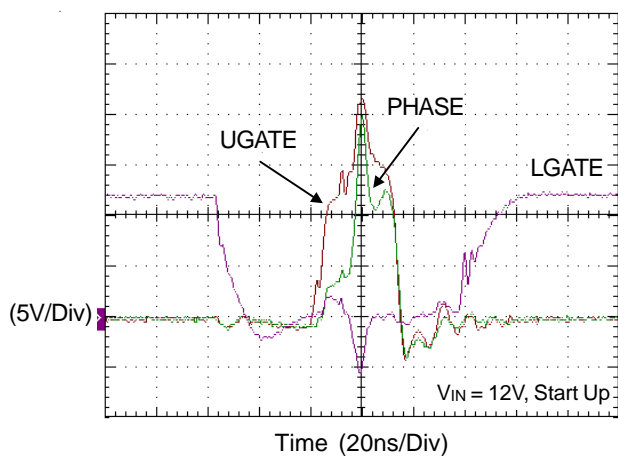
**Dead Time**



**Dead Time**



Short Pulse



## Application Information

The RT9612A/B is a High frequency, synchronous rectified, single phase dual MOSFET driver containing Richtek's advanced MOSFET driver technologies. The RT9612A/B is designed to be able to adapt from normal MOSFET driving applications to high performance CPU VR driving capabilities. The RT9612A/B can be utilized under both  $V_{CC} = 5V$  or  $V_{CC} = 12V$  applications which may happen in different fields of electronics application circuits. In the efficiency point of view, higher  $V_{CC}$  equals higher driving voltage of UG/LG which may result in higher switching loss and lower conduction loss of power MOSFETs. The choice of  $V_{CC} = 12V$  or  $V_{CC} = 5V$  can be a tradeoff to optimize system efficiency.

The RT9612A/B are designed to drive both high side and low side N-MOSFET through external input PWM control signal. It has power on protection function which held UGATE and LGATE low before the VCC voltage rises to higher than rising threshold voltage. After the initialization, the PWM signal takes the control. The rising PWM signal first forces the LGATE signal turns low then UGATE signal is allowed to go high just after a non-overlapping time to avoid shoot through current. The falling of PWM signal first forces UGATE to go low. When UGATE and PHASE signal reach a predetermined low level, LGATE signal is allowed to turn high.

The PWM signal is acted as “High” if the signal is above the rising threshold and acted as “Low” if the signal is below the falling threshold. Any signal level enters and remains within the shutdown window is considered as “tri-state”, the output drivers are disabled and both MOSFET gates are pulled and held low. If the PWM signal is left floating, the pin will be kept around 1.8V by the internal divider and provide the PWM controller with a recognizable level.

The RT9612A/B builds in an internal bootstrap power switch to replace external bootstrap diode, and this can facilitate PCB design and reduce total BOM cost of the system. Hence, no external bootstrap diode is required in real applications.

The difference of the RT9612A and the RT9612B is the propagation delay,  $t_{UGATEpdh}$ . The RT9612B has

comparatively large  $t_{UGATEpdh}$  to further prevent from shoot through when high side power MOSFETs are going to be turned on. The long propagation delay of the RT9612B sacrifices efficiency for compromise of system safety. Hence, the RT9612A is usually recommended to be utilized in performance oriented applications, such as high power density CPU VR or GPU VR.

### Non-overlap Control

To prevent the overlap of the gate drives during the UGATE pull low and the LGATE pull high, the non-overlap circuit monitors the voltages at the PHASE node and high side gate drive (UGATE-PHASE). When the PWM input signal goes low, UGATE begins to pull low (after propagation delay). Before LGATE can pull high, the non-overlap protection circuit ensures that the monitored voltages have gone below 1.1V. Once the monitored voltages fall below 1.1V, LGATE begins to turn high. For short pulse condition, if the PHASE pin had not gone high after LGATE pulls low, the LGATE has to wait for 200ns before pull high. By waiting for the voltages of the PHASE pin and high side gate drive to fall below 1.1V, the non-overlap protection circuit ensures that UGATE is low before LGATE pulls high.

Also to prevent the overlap of the gate drives during LGATE pull low and UGATE pull high, the non-overlap circuit monitors the LGATE voltage. When LGATE go below 1.1V, UGATE is allowed to go high.

### Driving Power MOSFETs

The DC input impedance of the power MOSFET is extremely high. When  $V_{gs1}$  or  $V_{gs2}$  is at 12V or 5V, the gate draws the current only for few nano-amperes. Thus once the gate has been driven up to “ON” level, the current could be negligible.

However, the capacitance at the gate to source terminal should be considered. It requires relatively large currents to drive the gate up and down 12V (or 5V) rapidly. It is also required to switch drain current on and off with the required speed. The required gate drive currents are calculated as follows.

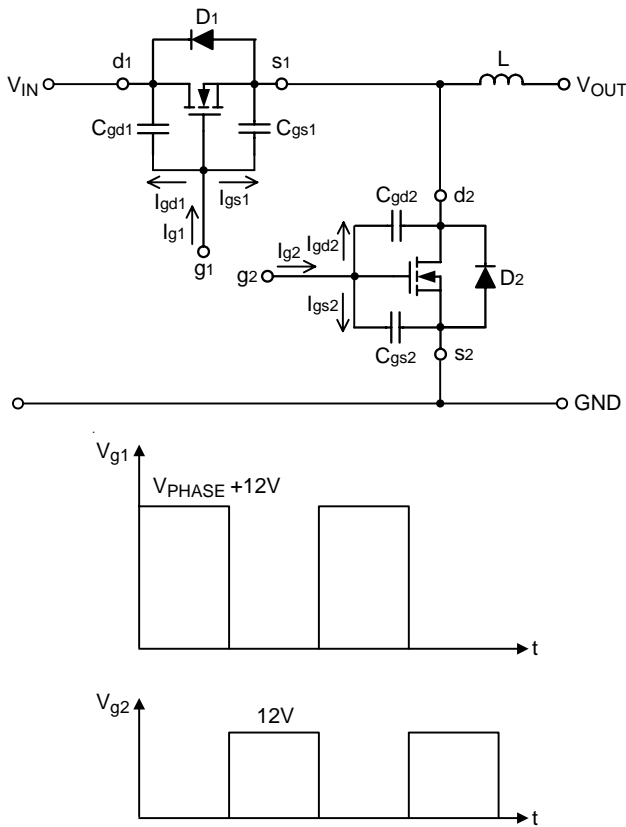


Figure 1. Equivalent Circuit and Associated Waveforms

In Figure 1, the current  $I_{g1}$  and  $I_{g2}$  are required to move the gate up to 12V. The operation consists of charging  $C_{gd1}$ ,  $C_{gd2}$ ,  $C_{gs1}$  and  $C_{gs2}$ .  $C_{gs1}$  and  $C_{gs2}$  are the capacitors from gate to source of the high side and the low side power MOSFETs, respectively. In general data sheets, the  $C_{gs1}$  and  $C_{gs2}$  are referred as “ $C_{iss}$ ” which are the input capacitors.  $C_{gd1}$  and  $C_{gd2}$  are the capacitors from gate to drain of the high side and the low side power MOSFETs, respectively and referred to the data sheets as “ $C_{r_{ss}}$ ” the reverse transfer capacitance. For example,  $t_{r1}$  and  $t_{r2}$  are the rising time of the high side and the low side power MOSFETs respectively, the required current  $I_{gs1}$  and  $I_{gs2}$ , are shown as below :

$$I_{gs1} = C_{gs1} \frac{dV_{g1}}{dt} = \frac{C_{gs1} \times 12}{t_{r1}} \quad (1)$$

$$I_{gs2} = C_{gs2} \frac{dV_{g2}}{dt} = \frac{C_{gs2} \times 12}{t_{r2}} \quad (2)$$

Before driving the gate of the high side MOSFET up to 12V (or 5V), the low side MOSFET has to be off; and the high side MOSFET will be turned off before the

low side is turned on. From Figure 1, the body diode “ $D_2$ ” will be turned on before high side MOSFETs turn on.

$$I_{gd1} = C_{gd1} \frac{dV}{dt} = C_{gd1} \frac{12}{t_{r1}} \quad (3)$$

Before the low side MOSFET is turned on, the  $C_{gd2}$  have been charged to  $V_{IN}$ . Thus, as  $C_{gd2}$  reverses its polarity and  $g_2$  is charged up to 12V, the required current is

$$I_{gd2} = C_{gd2} \frac{dV}{dt} = C_{gd2} \frac{V_i + 12}{t_{r2}} \quad (4)$$

It is helpful to calculate these currents in a typical case. Assume a synchronous rectified buck converter, input voltage  $V_{IN} = 12V$ ,  $V_{g1} = V_{g2} = 12V$ . The high side MOSFET is PHB83N03LT whose  $C_{iss} = 1660pF$ ,  $C_{r_{ss}} = 380pF$ , and  $t_r = 14ns$ . The low side MOSFET is PHB95N03LT whose  $C_{iss} = 2200pF$ ,  $C_{r_{ss}} = 500pF$  and  $t_r = 30ns$ , from the equation (1) and (2) we can obtain

$$I_{gs1} = \frac{1660 \times 10^{-12} \times 12}{14 \times 10^{-9}} = 1.428 \quad (A) \quad (5)$$

$$I_{gs2} = \frac{2200 \times 10^{-12} \times 12}{30 \times 10^{-9}} = 0.88 \quad (A) \quad (6)$$

from equation. (3) and (4)

$$I_{gd1} = \frac{380 \times 10^{-12} \times 12}{14 \times 10^{-9}} = 0.326 \quad (A) \quad (7)$$

$$I_{gd2} = \frac{500 \times 10^{-12} \times (12+12)}{30 \times 10^{-9}} = 0.4 \quad (A) \quad (8)$$

the total current required from the gate driving source can be calculated as following equations.

$$I_{g1} = I_{gs1} + I_{gd1} = (1.428 + 0.326) = 1.754 \quad (A) \quad (9)$$

$$I_{g2} = I_{gs2} + I_{gd2} = (0.88 + 0.4) = 1.28 \quad (A) \quad (10)$$

By a similar calculation, we can also get the sink current required from the turned off MOSFET.

### Select the Bootstrap Capacitor

Figure 2 shows part of the bootstrap circuit of the RT9612A/B. The  $V_{CB}$  (the voltage difference between BOOT and PHASE on RT9612A/B) provides a voltage to the gate of the high side power MOSFET. This supply needs to be ensured that the MOSFET can be driven. For this, the capacitance  $C_B$  has to be selected properly. It is determined by following constraints.

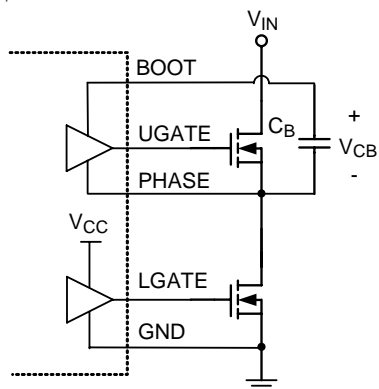


Figure 2. Part of Bootstrap Circuit of RT9612A/B

In practice, a low value capacitor  $C_B$  will lead to the over charging that could damage the IC. Therefore, to minimize the risk of overcharging and to reduce the ripple on  $V_{CB}$ , the bootstrap capacitor should not be smaller than  $0.1\mu\text{F}$ , and the larger the better. In general design, using  $1\mu\text{F}$  can provide better performance. At least one low-ESR capacitor should be used to provide good local de-coupling. It is recommended to adopt a ceramic or tantalum capacitor.

**Power Dissipation**

To prevent driving the IC beyond the maximum recommended operating junction temperature of  $125^\circ\text{C}$ , it is necessary to calculate the power dissipation appropriately. This dissipation is a function of switching frequency and total gate charge of the selected MOSFET.

Figure 3 shows the power dissipation test circuit.  $C_L$  and  $C_U$  are the UGATE and LGATE load capacitors, respectively. The bootstrap capacitor value is  $1\mu\text{F}$ .

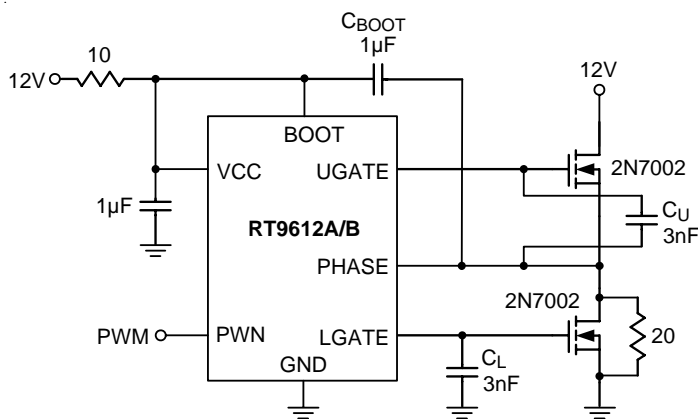


Figure 3. Test Circuit

Figure 4 shows the power dissipation of the RT9612A/B as a function of frequency and load capacitance. The value of  $C_U$  and  $C_L$  are the same and the frequency is varied from 100kHz to 1MHz.

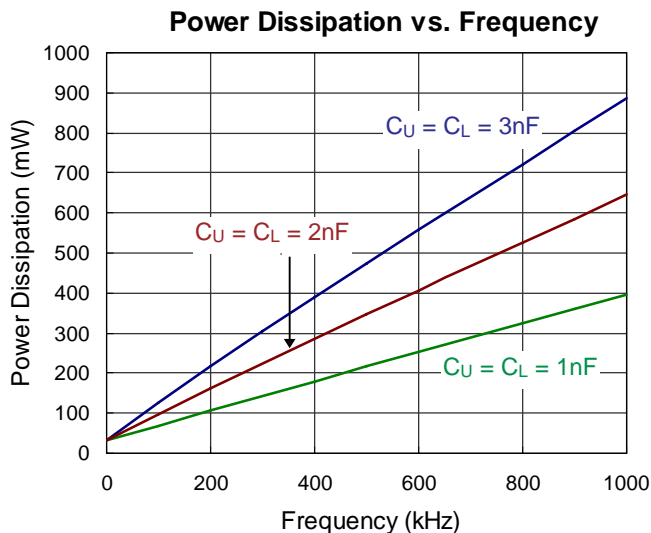


Figure 4. Power Dissipation vs. Frequency

The operating junction temperature can be calculated from the power dissipation curves (Figure 4). Assume

$V_{CC} = 12\text{V}$ , operating frequency is 200kHz and  $C_U = C_L = 1\text{nF}$  which emulate the input capacitances of the high side and low side power MOSFETs. From Figure 4, the power dissipation is 100mW. Thus, for example, with the SOP-8 package, the package thermal resistance  $\theta_{JA}$  is  $120^\circ\text{C}/\text{W}$ . The operating junction temperature is then calculated as :

$$T_J = (120^\circ\text{C}/\text{W} \times 100\text{mW}) + 25^\circ\text{C} = 37^\circ\text{C} \quad (11)$$

where the ambient temperature is  $25^\circ\text{C}$ .

**Thermal Considerations**

For recommended operating condition specifications of the RT9612A/B, the maximum junction temperature is  $125^\circ\text{C}$  and  $T_A$  is the ambient temperature. The junction to ambient thermal resistance,  $\theta_{JA}$ , is layout dependent. For SOP-8 packages, the thermal resistance,  $\theta_{JA}$ , is  $120^\circ\text{C}/\text{W}$  on a standard JEDEC 51-7 four-layer thermal test board. For WDFN-8L 2x2 packages, the thermal resistance,  $\theta_{JA}$ , is  $120^\circ\text{C}/\text{W}$  on a standard JEDEC 51-7 four-layer thermal test board. For SOP-8 (Exposed Pad) packages, the thermal resistance,  $\theta_{JA}$ , is  $75^\circ\text{C}/\text{W}$  on a standard JEDEC 51-7 four-layer thermal test board. For WDFN-8EL 3x3 packages, the thermal resistance,  $\theta_{JA}$ , is

70°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at  $T_A = 25^\circ\text{C}$  can be calculated by the following formulas :

$$P_{D(\text{MAX})} = (125^\circ\text{C} - 25^\circ\text{C}) / (120^\circ\text{C/W}) = 0.833\text{W for SOP-8 package}$$

$$P_{D(\text{MAX})} = (125^\circ\text{C} - 25^\circ\text{C}) / (75^\circ\text{C/W}) = 1.333\text{W for SOP-8 (Exposed Pad) package}$$

$$P_{D(\text{MAX})} = (125^\circ\text{C} - 25^\circ\text{C}) / (70^\circ\text{C/W}) = 1.429\text{W for WDFN-8EL 3x3 package}$$

$$P_{D(\text{MAX})} = (125^\circ\text{C} - 25^\circ\text{C}) / (120^\circ\text{C/W}) = 0.833\text{W for WDFN-8L 2x2 package}$$

The maximum power dissipation depends on the operating ambient temperature for fixed  $T_{J(\text{MAX})}$  and thermal resistance,  $\theta_{JA}$ . For the RT9612A/B packages, the derating curves in Figure 5 allow the designer to see the effect of rising ambient temperature on the maximum power dissipation.

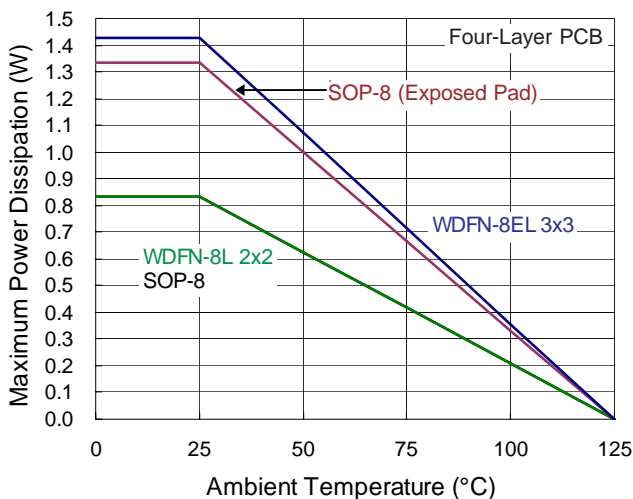


Figure 5. Derating Curves for the RT9612A/B Packages

### Layout Consideration

Figure 6 shows the schematic circuit of a synchronous buck converter to implement the RT9612A/B. The converter operates from 5V to 12V of input Voltage.

When layout the PCB, it should be very careful. The power circuit section is the most critical one. If not configured properly, it will generate a large amount of EMI. The junction of Q1, Q2, L2 should be very close.

Next, the trace from UGATE, and LGATE should also be short to decrease the noise of the driver output signals. PHASE signals from the junction of the power MOSFET, carrying the large gate drive current pulses, should be as heavy as the gate drive trace. The bypass capacitor C4 should be connected to GND directly. Furthermore, the bootstrap capacitors ( $C_B$ ) should always be placed as close to the pins of the IC as possible.

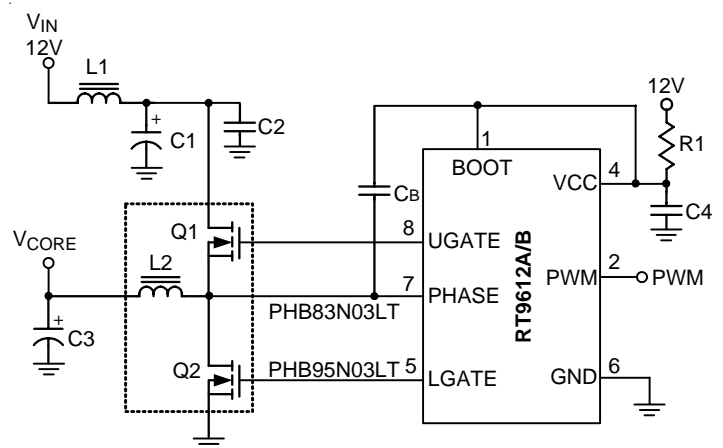
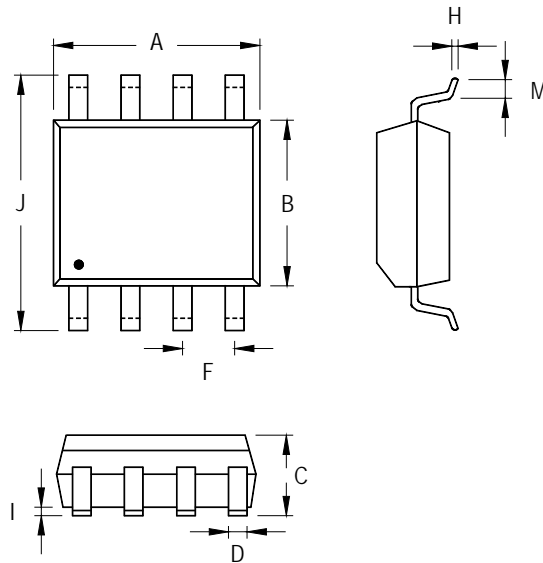


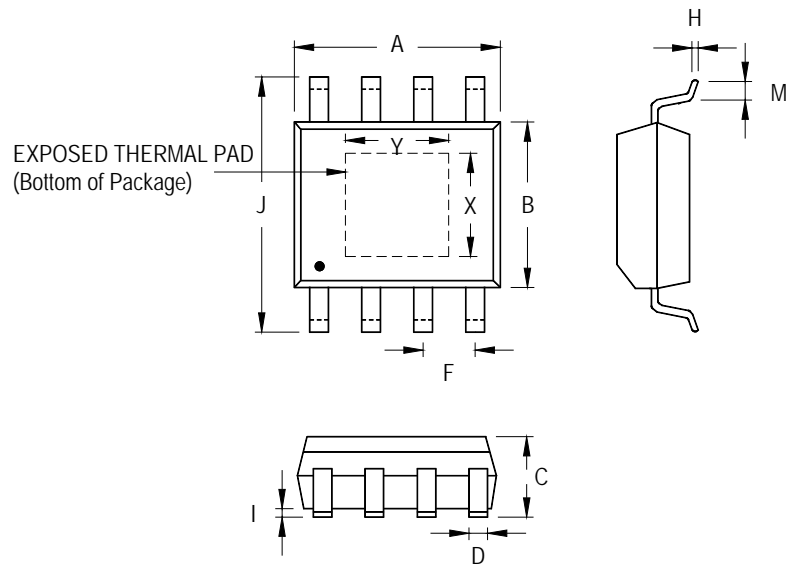
Figure 6. Synchronous Buck Converter Circuit

**Outline Dimension**



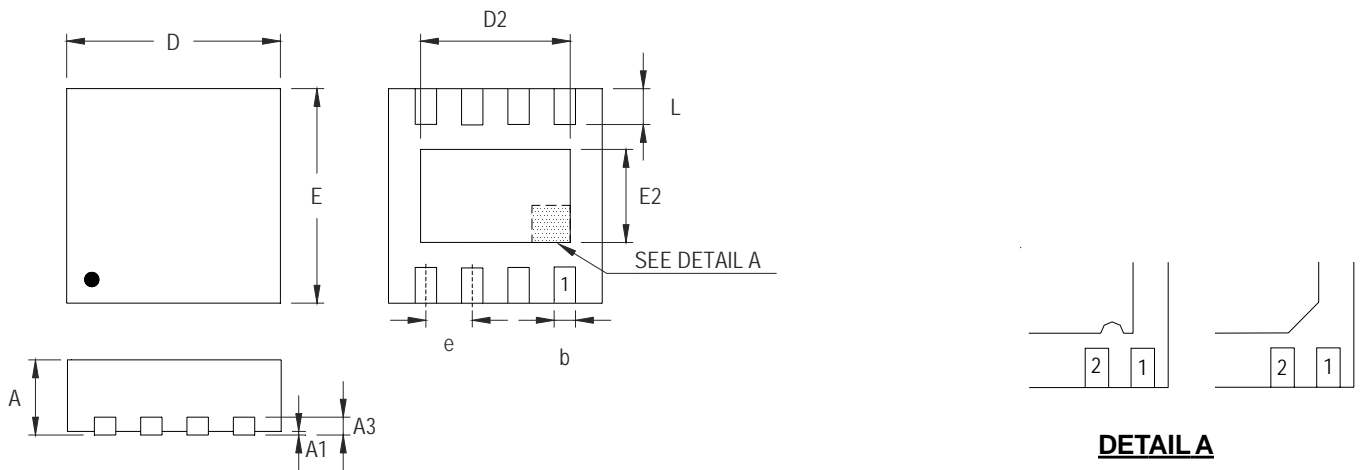
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	4.801	5.004	0.189	0.197
B	3.810	3.988	0.150	0.157
C	1.346	1.753	0.053	0.069
D	0.330	0.508	0.013	0.020
F	1.194	1.346	0.047	0.053
H	0.170	0.254	0.007	0.010
I	0.050	0.254	0.002	0.010
J	5.791	6.200	0.228	0.244
M	0.400	1.270	0.016	0.050

**8-Lead SOP Plastic Package**



Symbol	Dimensions In Millimeters		Dimensions In Inches		
	Min	Max	Min	Max	
A	4.801	5.004	0.189	0.197	
B	3.810	4.000	0.150	0.157	
C	1.346	1.753	0.053	0.069	
D	0.330	0.510	0.013	0.020	
F	1.194	1.346	0.047	0.053	
H	0.170	0.254	0.007	0.010	
I	0.000	0.152	0.000	0.006	
J	5.791	6.200	0.228	0.244	
M	0.406	1.270	0.016	0.050	
Option 1	X	2.000	2.300	0.079	0.091
	Y	2.000	2.300	0.079	0.091
Option 2	X	2.100	2.500	0.083	0.098
	Y	3.000	3.500	0.118	0.138

8-Lead SOP (Exposed Pad) Plastic Package

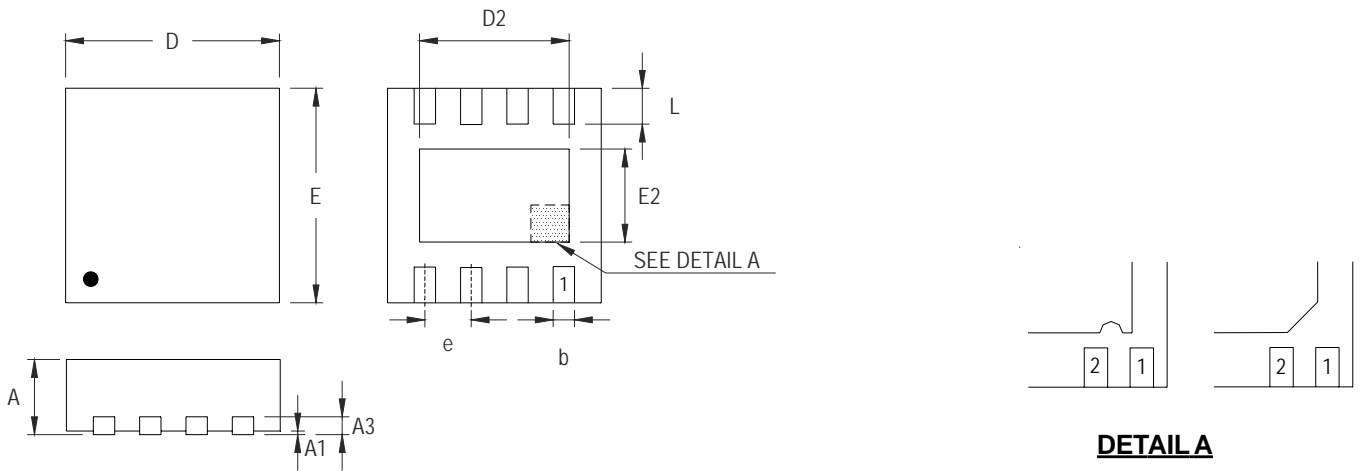


**DETAIL A**  
Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	2.950	3.050	0.116	0.120
D2	2.200	2.700	0.087	0.106
E	2.950	3.050	0.116	0.120
E2	1.450	1.750	0.057	0.069
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

**W-Type 8EL DFN 3x3 Package (0.5mm Lead Pitch)**



**DETAIL A**  
Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.200	0.300	0.008	0.012
D	1.950	2.050	0.077	0.081
D2	1.000	1.250	0.039	0.049
E	1.950	2.050	0.077	0.081
E2	0.400	0.650	0.016	0.026
e	0.500		0.020	
L	0.300	0.400	0.012	0.016

**W-Type 8L DFN 2x2 Package**

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