PM5317

SPECTRA_9953

SONET/SDH Payload Extractor/Aligner for 9953 Mbit/s

Data Sheet

Proprietary and Confidential

Released

Issue No. 6: January, 2007

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Revision History

Issue No.	Issue Date	Details of Change
Issue 6	January 2007	Amended Table 43 Ordering Information. Added Figure 59 1152-Pin 35x35mm FCBGA (HDBU Substrate).
Issue 5	June 2002	Created from Eng Doc issue 5. - Clarify operation of Ring control port - Remove OIF_RES/OIF_RESK (M7/N8) pins from document (the resistor is now located on-package for Production devices). These pins are now NC, but there will be no problem if there is a resistor across them. - Document ROHI_RESET bits, ROHI_RST_OOF_EN bit - Clarify operation of SHPI, RHPP registers - Clarify alarm propagation when SHPI is bypassed (HPT Mode) - Reveal DLL status bit registers (04CH – 04FH) - Clock activity monitor clarification - Add power supply requirements detail - Add power supply sequencing section
Issue 4	March 2002	Created from Eng Doc issue 4. -Miscellaneous corrections
Issue 3	June 2001	Created from Eng Doc issue 3. -Updated Functional timings -Updated AC timings -Updated Ball Mapping -Registers update -Operation section update -Mechanical Drawing -Implementation section update Edited document for grammar/style. Applied new template. Revised registers 00A0H, 00B0H, 20A0H, 20B0H to include the PATH[3:0] bits.
Issue 2	Oct 2000	Created from Eng Doc issue 2. Changes to that document are: Updated registers Updated operation section AC timings Implementation description Layout Information Fixed document after plan review
Issue 1	February 2000	Document created

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1 Definitions

The following table defines the abbreviations used in this document.

Table 1 Definitions

SRLI_192	SONET/SDH Receive Line Interface for STS-192/STM-64
RRMP	Receive Regenerator Multiplexer Processor
RHPP	Receive High order Path Processor
RTTP	Received Trail trace Processor
STLI_192	SONET/SDH Transmit Line Interface for STS-192/STM-64
TRMP	Transmit Regenerator Multiplexer Processor
THPP	Transmit High order Path Processor
TTTP	Transmit Trail trace Processor
SVCA	SONET/SDH Virtual Container Aligner
SSI	SONET/SDH Space Slot Interchange
SARC_48	SONET/SDH Alarm Reporting Controller for STS-48/STM-16
SHPI	Sonet/SDH High Order Pointer Interpreter
SBER	SONET/SDH Bit Error Rate
R8TD	Receive 8B/10B Telecom Decoder
T8TE	Transmit 8B/10B Telecom Encoder
DRU	Data Recovery Unit
CSU	Clock Synthesis Unit
TXLV	LVDS Transmitter
RXLV	LVDS Receiver
DLL	Delay Lock Loop
PISO	Parallel to Serial Converter
SIPO	Serial to Parallel Converter

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2 Features

2.1 General

The PM5317 SPECTRA-9953 is a single channel STS-192/STM-64 or four channels STS-48/STM-16 monolithic SONET/SDH Payload Extractor and Aligner for use with single STS-192c (STM-64/AU4-64c), single STS-192 (STM-64/AU4-16c/AU4-4c/AU4/AU3), quad STS-48c (STM-16/AU4-16c), or quad STS-48 (STM-16/AU4-4c/AU4/AU3) interface applications operating at serial interface speeds of up to 9953 Mbit/s.

- In single STS-192/STM-64 mode, supports a duplex 16-bit 622 MHz LVDS line side interface for direct connection to external clock recovery, clock synthesis, and serializer-deserializer (SERDES) components. The interface is compatible with OIF-99 SFI-4 specifications.
- In quad STS-48/STM-16 mode, supports four duplex 4-bit 622 MHz LVDS line side interfaces to directly connect to external clock recovery, clock synthesis, and SERDES components. Supports direct interface to the PM5395 CRSU-4x2488 4xOC48 serializer
- Provides termination for SONET Section, Line and Path overhead or SDH Regenerator Section, Multiplexer Section, and High Order Path overhead.
- In single STS-192/STM-64 mode, provides a 16-bit 777.7 MHz LVDS Add and Drop Serial TelecomBus with extended 8B/10B-based encoding.
- In quad STS-48/STM-16 mode, provides four 4-bit 777.7 MHz LVDS Add and Drop Serial TelecomBus interfaces with extended 8B/10B-based encoding.
- Maps SONET/SDH payloads to system timing, accommodating plesiochronous timing offsets between the line and system timing references, through pointer processing.
- Supports Space Slot Interchange (SSI) functions at the Drop and Add TelecomBuses for switching any legal mix of STS-12/STM-4 SONET/SDH streams.
- Supports line loopback from the line side receive stream to the transmit stream and diagnostic loopback from an Add TelecomBus interface to a Drop TelecomBus interface.
- Provides a standard 5 signal IEEE 1149.1 JTAG test port for boundary scan board test purposes.
- Provides a generic 16-bit microprocessor bus interface for configuration, control, and status monitoring.
- Low power 1.8 V CMOS core logic with 3.3 V CMOS/TTL compatible digital inputs and digital outputs.
  - Wide temperature range (-40 °C to +105 °C).
  - 1152 pin Flip-Chip BGA (FCBGA) package.

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2.2 SONET Section and Line / SDH Regenerator and Multiplexer Section

- Frames to the SONET/SDH receive stream and inserts the framing bytes (A1, A2) and the section trace byte (J0) into the transmit stream; descrambles the received stream and scrambles the transmit stream.

- Calculates and compares the bit interleaved parity (BIP) error detection codes (B1, B2) for the receive stream. Calculates and inserts B1 and B2 in the transmit stream. Accumulates near end errors (B1, B2) and far end errors (M1) and inserts line remote error indications (REI) into the M1 byte based on received B2 errors.

- Detects signal degrade (SD) and signal fail (SF) threshold crossing alarms based on received B2 errors.

- The entire SONET/SDH transport overhead (used and unused bytes) is extracted to and inserted from dedicated pins.

- Extracts and serializes on dedicated pins the data communication channels (D1-D3, D4-D12) and inserts the corresponding signals into the transmit stream.

- Extracts and filters the automatic protection switch (APS) channel (K1, K2) bytes into internal registers. Inserts the APS channel into the transmit stream.

- Extracts and filters the synchronization status message (S1) byte into an internal register for the receive stream. Inserts the synchronization status message (S1) byte into the transmit stream.

- Extracts a 64-byte (Telcordia-compatible) or 16-byte (ITU-compatible) section trace (J0) message using an internal register bank for the receive stream. Detects an unstable message or mismatch message with an expected message. Inserts a 64-byte or 16-byte section trace (J0) message using an internal register bank for the transmit stream. Provides access to the accepted message via the microprocessor port.

- Detects loss of signal (LOS), out of frame (OOF), loss of frame (LOF), line remote defect indication (RDI), line alarm indication signal (AIS), and protection switching byte failure alarms on the receive stream.

- Provides a transmit and receive ring control port, allowing alarm and maintenance signal control and status to be passed between mate SPECTRA-9953 devices for ring-based Add/ Drop multiplexer and line multiplexer applications.

- Configurable to force Line AIS in the transmit stream.

- Provides automatic transmit line RDI insertion following detection of various received alarms (LOS, LOF, LAIS, SD, SF, STIM, STIU). Registers are provided to individually enable/disable each alarm.

- Provides automatic Drop bus path AIS insertion following detection of various received alarms (LOS, LOF, LAIS, SD, SF, STIM, STIU). Registers are provided to individually enable/disable each alarm.

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2.3 SONET Path / SDH High Order Path

- Interprets any legal mix of STS (AU) pointer bytes (H1, H2, and H3), extracts the synchronous payload envelope(s) and processes the path overhead for the receive stream.
- Generates any legal mix of STS (AU) pointer bytes (H1, H2, and H3) and inserts the path overhead for the transmit stream.
- Detects loss of pointer (LOP), path alarm indication signal (PAIS) and path (normal and enhanced) remote defect indication (RDI) for the receive stream. Optionally inserts path alarm indication signal (PAIS) and path remote defect indication (RDI) in the transmit stream.
- Inserts the entire SONET/SDH path overhead. The path overhead bytes may be sourced from internal registers. Path overhead insertion may also be disabled.
- Extracts the received path payload label (C2) byte into an internal register and detects for payload label unstable (PLU), payload label mismatch (PLM), payload unequipped (UNEQ), and payload defect indication (PDI). Inserts the path payload label (C2) byte from an internal register for the transmit stream.
- Inserts 192 64-byte or 16-byte path trace (J1) messages using an internal register bank for the transmit stream.
- Extracts 192 64-byte or 16-byte path trace (J1) messages using an internal register bank for the receive stream. Detects an unstable message or mismatch message with an expected message. Provides access to the captured, accepted and expected message via the microprocessor port.
- Detects received path BIP-8 and counts received path BIP-8 errors for performance monitoring purposes. BIP-8 errors are selectable to be treated on a bit basis or block basis. Optionally calculates and inserts path BIP-8 error detection codes for the transmit stream.
- Counts received path remote error indications (REIs) for performance monitoring purposes. Optionally inserts the path REI count into the path status byte (G1) based on bit or block BIP-8 errors detected in the receive path. Reporting of BIP-8 errors is on a bit or block basis independent of the accumulation of BIP-8 errors.
- Ring control port provides communication of path REI and path RDI alarms to the transmit stream of a mate SPECTRA-9953 device in the returning direction.
- Provides automatic transmit path RDI and path Enhanced RDI insertion following detection of various received alarms (LAIS, LOP, LOPCON, PAIS, PAISCON, PTIM, PTIU, PLM, PLU, UNEQ, PDI). Registers are provided to individually enable/disable each alarm.
- Provides automatic receive path AIS insertion following detection of various received alarms (LAIS, LOP, LOPCON, PAIS, PAISCON, PTIM, PTIU, PLM, PLU, UNEQ, PDI). Registers are provided to individually enable/disable each alarm.

2.4 System Side Interfaces

- In single STS-192/STM-64 mode, provides a single 16-bit differential LVDS 777.7 MHz serial TelecomBus interface.

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- In quad STS-48/STM-16 mode, provides a four 4-bit differential LVDS 777.7 MHz serial TelecomBus interfaces.
- The serial TelecomBus accommodates phase and frequency differences between the receive/transmit streams and the Drop/Add busses via pointer adjustments.
- Supports a Space Slot Interchange (SSI) function at the Drop and Add TelecomBuses for switching any legal mix of STS-12/STM-4 SONET/SDH streams.
- Supports Ring Control Port to pass defect information between mate SPECTRA-9953 devices.
- Supports Add bus AIS Insertion through dedicated pins and internal registers.

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3 Applications

- SONET/SDH Add/Drop Multiplexers
- SONET/SDH Terminal Multiplexers
- SONET/SDH Line Multiplexers
- SONET/SDH Cross Connects
- SONET/SDH Test Equipment
- Switches and Hubs
- Routers

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5 Application Examples

The PM5317 SPECTRA-9953 device has been designed for use in SONET/SDH network elements including switches, terminal multiplexers, and Add/Drop multiplexers. In these applications, the line interface of the SPECTRA-9953 device is typically connected to an external CDR/SERDES device such as a PM5395 CRSU-4x2488 device. On its system side interface, the SPECTRA-9953 device is typically connected to a PM5307 TBS-9953, a PM5372 TSE or a PM7390 S/UNI-MACH48 device.

Figure 1 shows how the SPECTRA-9953 device is used to connect an STS-192/STM-64 line to a DS3 card. In this application, the SPECTRA-9953 performs SONET/SDH section, line and path termination and the S/UNI-MACH48 provides DS3 mapping. Figure 2 shows how the SPECTRA-9953 device is used to connect an STS-192/STM-64 line to a DS3 card with 1:1 protection. Figure 3 shows how the SPECTRA-9953 and the TSE devices are used in a scalable 160 Gbit/s cross connect fabric.

Figure 1 STS-192/STM-64 to DS3 Card

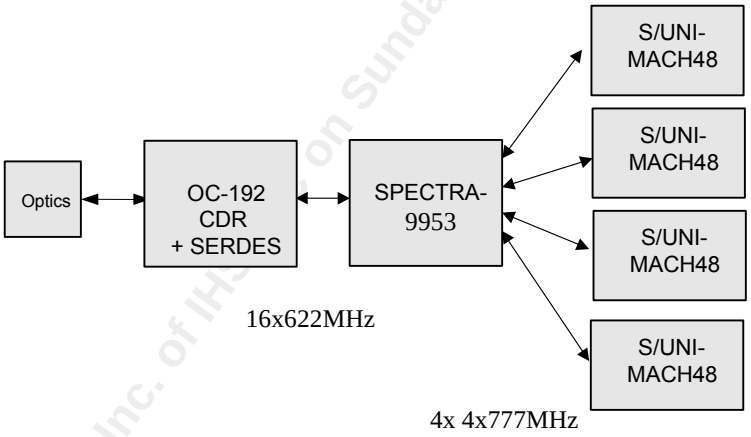

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Figure 2 STS-192/STM-64 to DS3 Card with 1:1 Protection

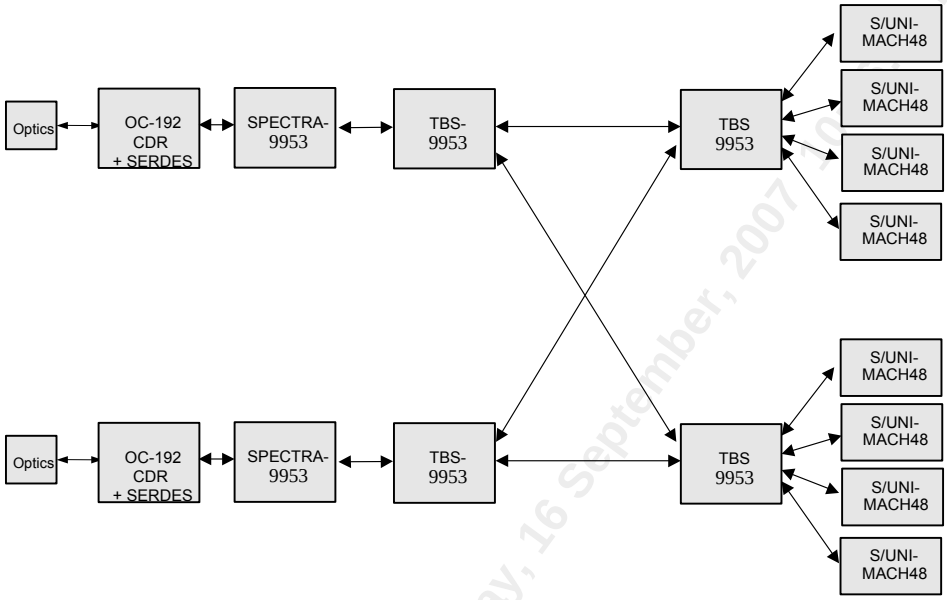

Figure 3 160 Gigabit STS-1 Cross-Connect

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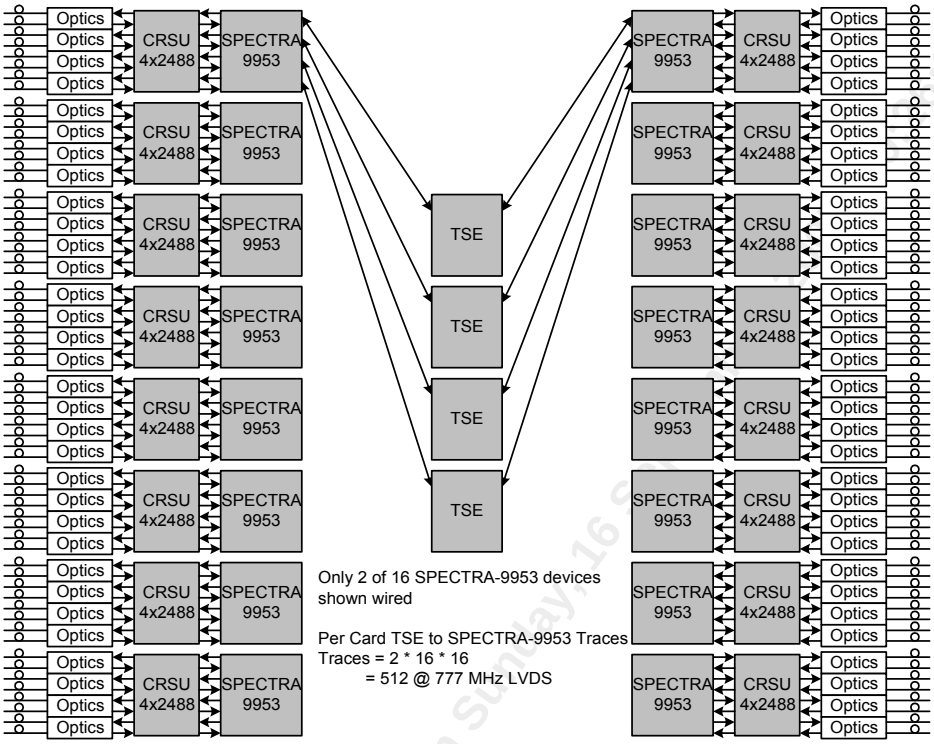

Total Devices

2.5G Optical Modules = 64
CRSU-4x2488 = 16
SPECTRA-9953 = 16
TSE = 4

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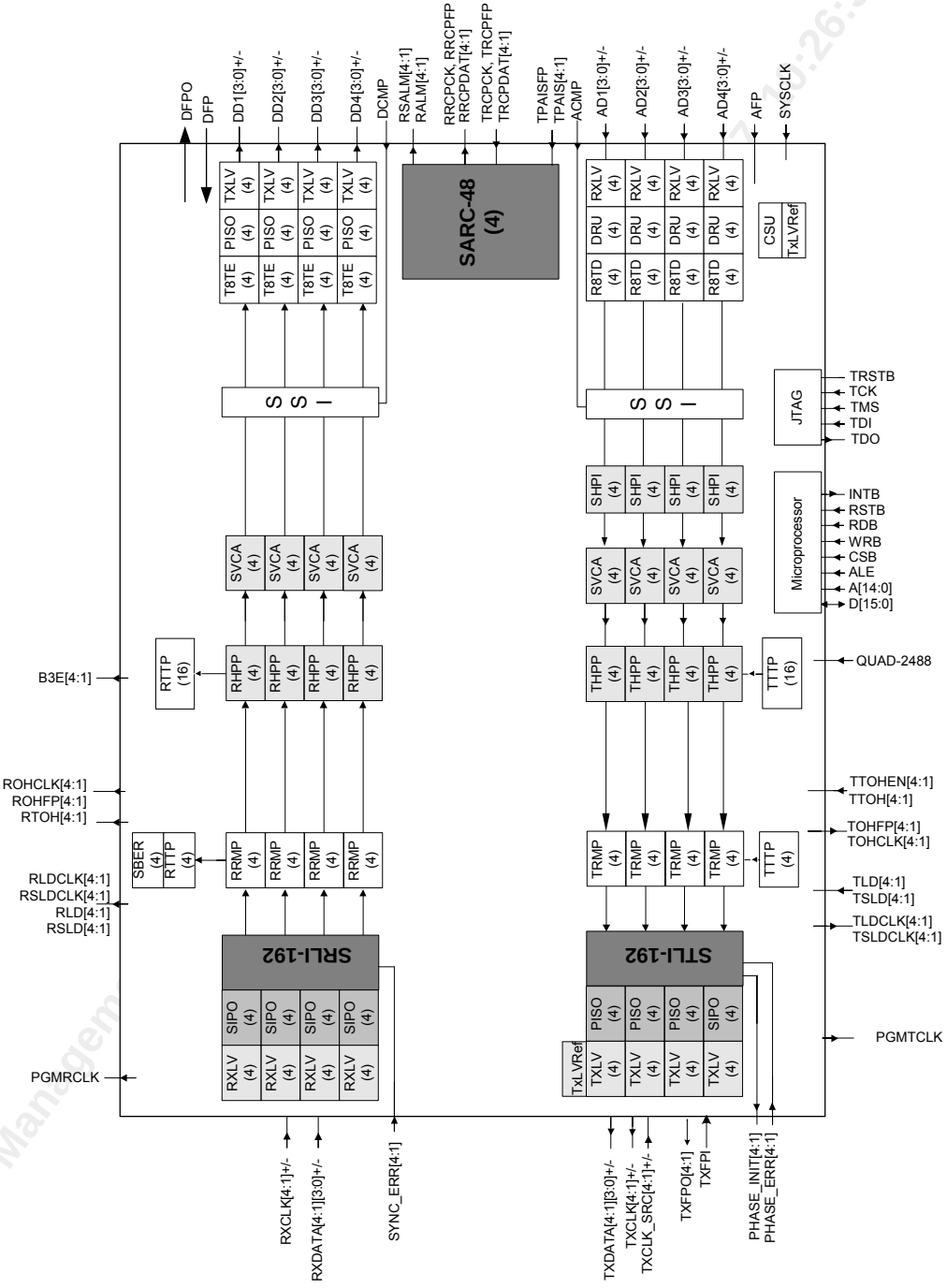
6 Block Diagram



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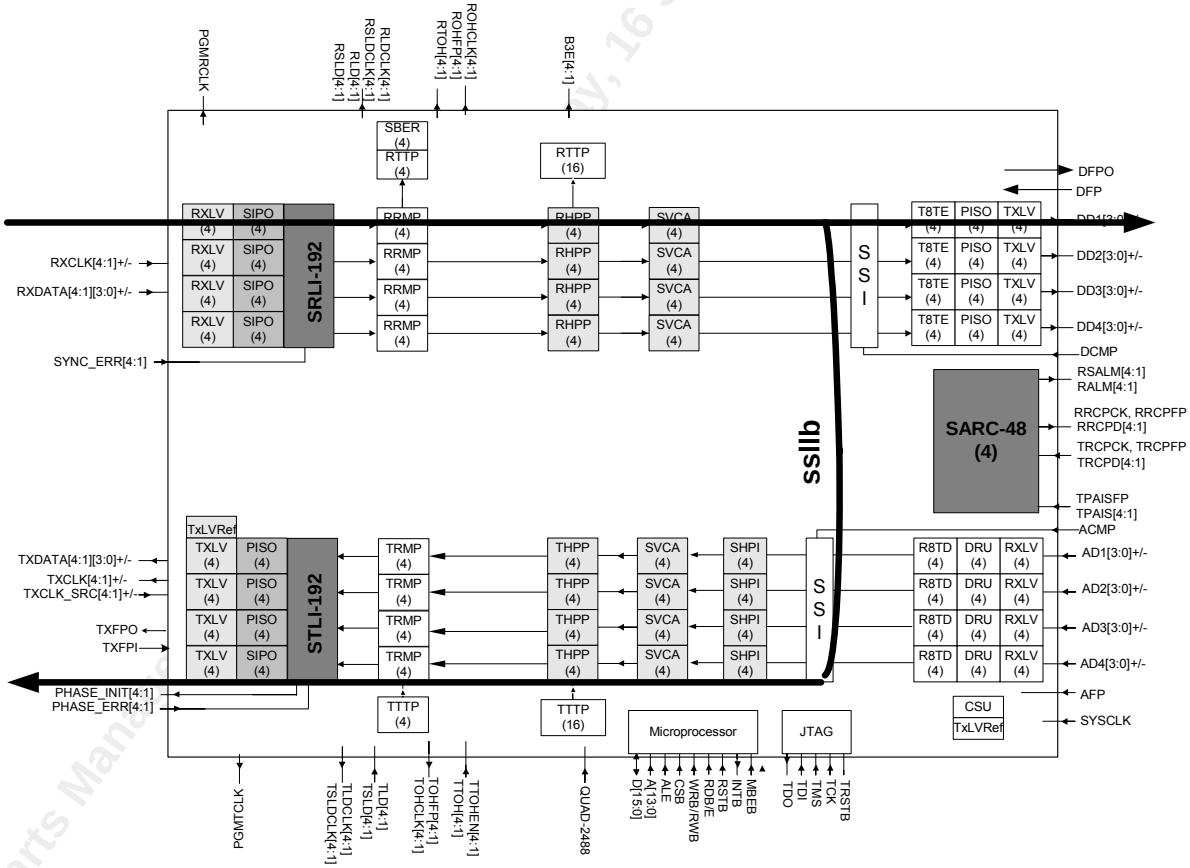
7 Loopback Modes

7.1 Line Loopback Modes

The SPECTRA-9953 device supports SONET STS-1/STM-0 terminal loopback (SSLLB). When enabled, the receive SVCA output is fed back to the Add bus SSI block input. The Drop bus data stream is still valid when this type of loopback is enabled.

The SPECTRA-9953 device does not support SONET facility loopback (line loopback before de-scrambling). This feature should be implemented within the external SERDES device.

Figure 4 Line Loopback Modes



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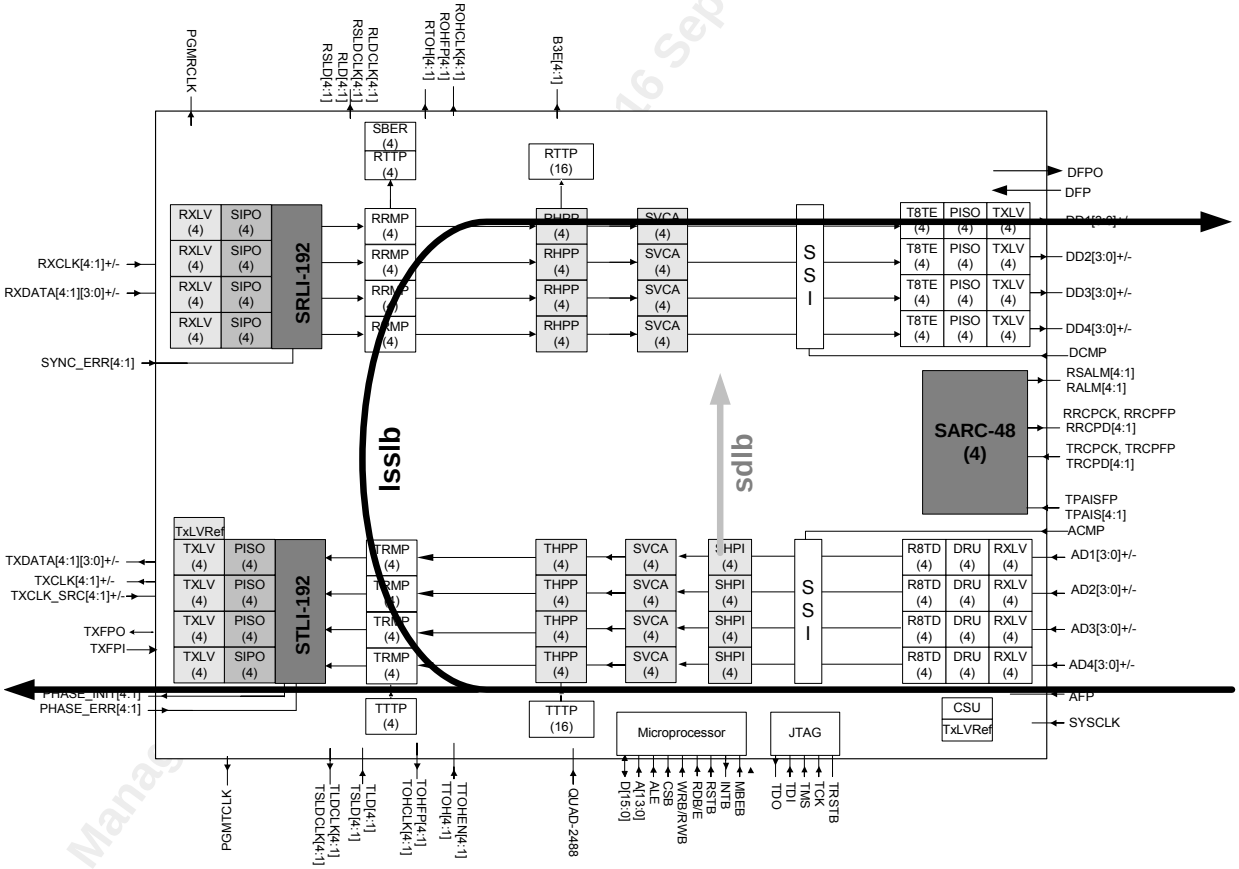
7.2 System Loopback

The SPECTRA-9953 device supports the section layer diagnostic line side system loopback (LSSLB). The TRMP output is fed-back to the RRMP input when LSSLB is enabled. The line transmit interface is still valid when such a section layer diagnostic loopback is enabled. However, the receive overhead ports (rld, rsld, rtoh, and b3e outputs) are not operational in this loopback.

Also implemented on the SPECTRA-9953 device, is a system-side diagnostic loopback before the aligners. The SHPI output is fed-back to the Drop bus SSI input.

Figure 5 System Loopback Modes



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8 Description

The PM5317 SONET/SDH Payload Extractor/Aligner (SPECTRA-9953) device terminates the transport and path overhead of a single STS-192 (STM-64/AU4-16c/AU4-4c/AU4/AU3) stream, a single STS-192c (STM-64/AU4-64c) stream, quad STS-48 (STM-16/AU4-4c/AU4/AU3) streams or quad STS-48c (STM-16-16c) data streams at 9953 Mbit/s. The SPECTRA-9953 device implements significant functions for a SONET/SDH-compliant line interface.

In single STS-192/STM-64 mode, the SPECTRA-9953 receives SONET/SDH frames via a 16-bit LVDS interface at 622.08 Mbit/s. In quad STS-48/STM-16 mode, the SPECTRA-9953 receives SONET/SDH frames via four 4-bit LVDS interfaces at 622.08 Mbit/s. The SPECTRA-9953 terminates the SONET section, line and path or the SDH regenerator section, multiplexer section and high order path overhead. It performs framing (A1, A2), descrambling, detects section and line alarm conditions, and monitors section and line bit interleaved parity (BIP) (B1, B2), accumulating error counts at each level for performance monitoring purposes. B2 errors are also monitored to detect signal fail and signal degrade threshold crossing alarms. Line remote error indications (M1) are also accumulated. A 16 or 64-byte section trace (J0) message may be buffered and compared against an expected message. In addition, the SPECTRA-9953 interprets the received payload pointers (H1, H2), detects path alarm conditions, detects and accumulates path BIPs (B3), monitors and accumulates path Remote Error Indications (REIs), accumulates and compares the 16 or 64-byte path trace (J1) message against an expected message, and extracts the synchronous payload envelope (SPE) (virtual container). All transport overhead bytes are extracted and serialized on lower rate interfaces, allowing additional external processing of overhead, if desired.

The extracted SPE (VC) is placed on a 16-bit LVDS, 8B/10B encoded, Serial Telecom Drop bus at 777.6 MHz. For TelecomBus applications, frequency offsets (e.g., due to plesiochronous network boundaries, or the loss of a primary reference timing source) and phase differences (due to normal network operation) between the received data stream and the Drop bus are accommodated by pointer adjustments in the Drop bus.

In STS-192/STM-64 mode, the SPECTRA-9953 device transmits SONET/SDH frames via a 16-bit LVDS interface at 622.08 Mbit/s. In quad STS-48/STM-4 mode, the SPECTRA-9953 device transmits SONET/SDH frames via four 4-bit LVDS interfaces at 622.08 Mbit/s. The SPECTRA-9953 device formats the SONET section, line and path or the SDH regenerator section, multiplexer section and high order path overhead. It performs framing pattern insertion (A1, A2), scrambling, section and line alarm insertion, and section and line BIPs (B1, B2) calculation as required to allow performance monitoring at the far end. Line remote error indications (M1) are optionally inserted. A 16 or 64-byte section trace (J0) message may be inserted. In addition, the SPECTRA-9953 generates the transmit payload pointers (H1, H2), creates and inserts the path BIPs (B3), optionally inserts a 16 or 64-byte path trace (J1) message, and optionally inserts the path status byte (G1). In addition to its basic processing of the transmit SONET/SDH overhead, the SPECTRA-9953 provides convenient access to all overhead bytes. The SPECTRA-9953 also allows a variety of diagnostic errors to be inserted into the transmit stream, such as framing pattern errors, pointer errors, and BIP errors. These are useful for system diagnostics and tester applications.

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The inserted SPE (VC) is sourced from a 16-bit LVDS, 8B/10B encoded, Serial Telecom Add bus at 777.6 MHz. For TelecomBus applications, frequency offsets (due to plesiochronous network boundaries, or the loss of a primary reference timing source) and phase differences (due to normal network operation) between the transmit data stream and the Add bus are accommodated by pointer adjustments in the transmit data stream.

The transmitter and receiver are independently configurable (on a payload mapping level) to allow for asymmetric interfaces. Ring control ports are provide to pass and control status information between mate transceivers.

The SPECTRA-9953 device is configured, controlled and monitored via a generic 16-bit microprocessor bus interface. The device is implemented in low power 1.8 Volt CMOS core logic with 3.3 Volt CMOS/TTL compatible digital inputs and digital outputs. It has LVDS inputs and outputs and is packaged in a 1152 pin Flip-Chip BGA (FCBGA) package.

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9 Pin Diagram

The SPECTRA-9953 device is packaged in a 1152-ball FCBGA. Table 2 shows the left side of the pin diagram. Table 3 shows the right side of the diagram.

Table 2 Pin Diagram Left Side (Bottom View)

	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18
A		VDDI	[A1]	A[6]	A[8]	A[9]	VSS	VDDO	RDB	NC9	ALE	TRSTB	VSS	VDDI	TDO	TDI	TTOHEN[2]
B	VDDI	VDDI	VSS	A[0]	A[5]	A[7]	A[13]	VDDO	VSS	WRB	CSB	INTB	RSTB	VDDI	VSS	TMS	TCK
C	D[15]	VSS	VSS	VDDO	NC8	A[4]	A[10]	A[12]	VSS	VDDO	VDDO	VDDI	VDDI	VSS	VSS	VDDI	VDDI
D	D[5]	D[14]	VDDO	VDDO	VSS	A[2]	A[3]	A[14]	A[11]	VDDO	VSS	VDDI	VSS	VSS	VDDI	VDDI	VSS
E	D[3]	D[4]	D[13]	VSS	VSS	VDDI	VDDI	VDDO	VDDO	VSS	VSS	VDDO	VSS	VDDI	VDDI	VSS	VSS
F	ACMP	D[2]	D[7]	D[12]	VDDI	VDDI	VSS	VDDO	VDDI	VSS	VDDO	VDDO	VSS	VDDI	VSS	VSS	VDDI
G	VSS	TPAISFP	TPAIS[2]	D[6]	D[11]	VSS	VSS	VDDI	VDDI	VDDO	VDDO	VSS	VSS	VDDO	VSS	VDDI	VDDI
H	VDDO	VDDO	AFP	TPAIS[1]	D[1]	D[10]	VDDI	VDDI	VSS	VSS	VDDI	VDDI	VDDI	VDDO	VSS	VDDI	VDDO
J	NC5	VSS	VSS	DFP	NC3	D[0]	D[9]	VSS	VSS	VDDI	VDDI	VDDI	VDDO	VDDO	VSS	VDDO	VDDO
K	TRCPDAT[2]	TRCPDAT[4]	VDDO	VDDO	SYSCLK	NC4	TPAIS[4]	D[8]	VDDI	VDDI	VSS	VDDI	VDDI	VDDO	VDDO	VDDO	VSS
L	RRCPDAT[4]	RRCPDAT[2]	TRCPDAT[1]	VSS	VSS	QUAD2488	DFPO	TPAIS[3]	VDDI	VSS	VSS	VDDI	VDDI	VDDI	VDDO	VDDO	VSS
M	AD1_N[1]	NC6	RRCPDAT[3]	RRCPDAT[1]	VDDO	VDDO	NC1	DCMP	VDDI	VDDI	VDDI	VDDI	VSS	VDDI	VDDI	VDDO	VDDO
N	VSS	AD1_P[1]	TRCPFP	NC7	SYS_OOL	VSS	VSS	TRCPDAT[3]	VDDO	VDDI	VDDI	VSS	VSS	VDDI	VDDI	VDDI	VDDO
P	VDDI	VDDI	AD1_N[0]	RRCPFP	RRCPCLK	NC2	VDDO	VDDO	VDDO	VDDO	VDDI	VDDI	VDDI	VDDI	VSS	VDDI	VDDI
R	DD1_P[0]	VSS	VSS	AD1_P[0]	RALM[3]	TRCPCLK	RALM[1]	VSS	VSS	VDDO	VDDO	VDDI	VDDI	VSS	VSS	VDDI	VSS
T	DD1_P[3]	DD1_N[0]	VDDI	VDDI	DD1_P[1]	RALM[4]	RSALM[3]	RALM[2]	VDDO	VDDO	VDDO	VDDO	VDDI	VDDI	VDDI	VDDI	VSS
U	AD2_N[2]	DD1_N[3]	AD2_N[1]	VSS	VSS	DD1_N[1]	AD1_N[2]	RSALM[4]	RSALM[1]	VSS	VSS	VDDO	VDDO	VDDI	VSS	VSS	VSS
V	AD2_P[2]	DD2_N[0]	AD2_P[1]	VSS	VSS	DD1_N[2]	AD1_P[2]	AD1_P[3]	RSALM[2]	VSS	VSS	VDDO	VDDO	VDDI	VSS	VSS	VSS
W	DD2_P[0]	DD2_N[1]	VDDI	VDDI	DD1_P[2]	AD2_P[3]	AD1_N[3]	AD2_P[0]	VDDO	VDDO	VDDO	VDDO	VDDI	VDDI	VDDI	VDDI	VSS
Y	DD2_P[1]	VSS	VSS	DD2_N[3]	AD2_N[3]	DD2_N[2]	AD2_N[0]	VSS	VSS	VDDO	VDDO	VDDI	VDDI	VSS	VSS	VDDI	VSS
AA	VDDI	VDDI	DD2_P[3]	AD3_P[0]	DD2_P[2]	AD3_P[1]	VDDO	VDDO	VDDO	VDDO	VDDI	VDDI	VDDI	VDDI	VSS	VDDI	VDDI
AB	VSS	AD3_P[2]	AD3_N[0]	AD3_P[3]	AD3_N[1]	VSS	VSS	DD3_N[1]	VDDO	VDDI	VDDI	VSS	VSS	VDDI	VDDI	VDDI	VDDO
AC	AD3_N[2]	DD3_N[3]	AD3_N[3]	DD3_N[0]	VDDO	VDDO	DD3_P[1]	AD4_P[0]	VDDI	VDDI	VDDI	VDDI	VSS	VDDI	VDDI	VDDO	VDDO
AD	DD3_P[3]	DD3_N[2]	DD3_P[0]	VSS	VSS	AD4_P[2]	AD4_N[0]	AVSL4	VDDI	VSS	VSS	VDDI	VDDI	VDDI	VDDO	VDDO	VSS
AE	DD3_P[2]	AD4_P[1]	VDDO	VDDO	AD4_N[2]	DD4_N[1]	AVSL1	AVDL4	VDDI	VDDI	VSS	VDDI	VDDI	VDDO	VDDO	VDDO	VSS
AF	AD4_N[1]	VSS	VSS	AD4_P[3]	DD4_P[1]	AVDL4	QAVS	VSS	VSS	VDDI	VSS	VSS	VDDI	VSS	VSS	VDDO	VDDI
AG	VDDO	VDDO	AD4_N[3]	DD4_N[2]	AVSL4	ATB0	VDDI	VDDI	VSS	VSS	VSS	VDDI	VDDI	VDDO	VSS	VDDO	VDDO
AH	VSS	DD4_N[0]	DD4_P[2]	ATB1	OSCB	VSS	VSS	VDDI	VSS	VSS	VDDI	VDDI	VSS	VDDO	VDDO	VDDO	VDDI
AJ	DD4_P[0]	DD4_N[3]	OSC	AVSH1	VDDI	VDDI	VSS	VDDI	VDDI	VDDO	VDDO	VDDO	VSS	VSS	VDDO	VDDI	VDDI
AK	DD4_P[3]	AVDL1	AVDL3	VSS	VSS	VDDI	VDDI	VDDI	VDDO	VDDO	VSS	VDDO	VSS	VSS	VDDI	VDDI	VSS
AL	AVSH1	AVSL3	VDDO	VDDO	VSS	VSS	VSS	VSS	VDDO	VDDO	VSS	VSS	VSS	VDDO	VDDI	VDDI	VSS
AM	QAVD	VSS	VSS	VDDO	VDDO	VSS	VSS	VSS	VSS	VDDO	VSS	VSS	VDDO	VDDO	VSS	VDDI	VSS
AN	VDDI	VDDI	VSS	VSS	AVSH1	AVDL2	AVSH2	VDDO	VSS	AVSL2	RESK	AVSL3	AVDH2	VDDI	VSS	VDDO	VDDO
AP		VDDI	VSS	AVSL2	AVSL2	AVDH1	VSS	VDDO	AVDL2	AVSL2	AVDL3	RES	VSS	VDDI	VDDO	VDDO	VDDI

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Table 3 Pin Diagram Right Side (Bottom View)

17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
TTOH[2]	TTOH[1]	TTOH[4]	VDDI	VSS	TOHCLK[2]	TOHCLK[4]	TLDCLK[2]	TLD[4]	VDDO	VSS	TSLD[2]	TSLD[4]	PGMTCLK		VDDI		A
TTOHEN[1]	TTOHEN[4]	VSS	VDDI	TOHFP[2]	TOHFP[4]	TLD[2]	TLD[3]	VSS	VDDO	TSLD[1]	TSLD[3]	TEST_TCLK	NC10	VSS	VDDI	VDDI	B
VDDI	VDDI	VSS	TTOH[3]	TOHCLK[1]	TOHCLK[3]	TLDCLK[1]	VDDO	VSS	TLDCLK[4]	TSLDCLK[2]	TSLDCLK[4]	VDDO	VDDO	VSS	VSS	TXFPO1	C
VSS	VDDI	TTOHEN[3]	TOHFP[1]	TOHFP[3]	TLD[1]	VSS	VDDO	TLDCLK[3]	TSLDCLK[1]	TSLDCLK[3]	VSS	VSS	VDDO	VDDO	TXFPI	PHASE_ER R4	D
VSS	VSS	VDDI	VDDI	VDDO	VDDO	VSS	VDDI	VDDI	VSS	VSS	VDDI	VSS	VSS	TXFPO3	PHASE_ER R3	TXDATA4_P [0]	E
VDDI	VSS	VSS	VDDI	VSS	VDDO	VSS	VSS	VDDI	VDDI	VSS	VDDI	VDDI	NC15	PHASE_INI T1	TXDATA4_ N[0]	TXCLK4_P	F
VDDI	VDDI	VSS	VDDO	VSS	VDDI	VDDI	VSS	VSS	VDDI	VSS	VSS	TXFPO2	PHASE_ER R1	TXDATA4_P [3]	TXCLK4_N	VSS	G
VDDO	VDDI	VSS	VDDO	VDDO	VDDO	VDDI	VDDI	VSS	VDDI	VDDI	LINE_OOL	PHASE_INI T4	TXDATA4_ N[3]	TXCLK_SR C4_N	VDDO	VDDO	H
VDDO	VDDO	VSS	VDDO	VDDO	VDDI	VDDI	VDDI	VSS	VSS	TXFPO4	PHASE_INI T3	TXDATA4_P [1]	TXCLK_SR C4_P	VSS	VSS	TXDATA3_P [1]	J
VSS	VDDO	VDDO	VDDO	VDDI	VDDI	VSS	VDDI	VDDI	NC14	PHASE_INI T2	TXDATA4_ N[1]	TXDATA4_P [2]	VDDO	VDDO	TXDATA3_ N[1]	TXDATA3_P [3]	K
VSS	VDDO	VDDO	VDDI	VDDI	VDDI	VSS	VSS	VDDI	PHASE_ER R2	AVDHVREF	TXDATA4_ N[2]	VSS	VSS	TXDATA3_P [2]	TXDATA3_ N[3]	TXDATA3_P [0]	L
VDDO	VDDO	VDDI	VDDI	VSS	VDDI	VDDI	VDDI	VDDI	VDDI	NC16	VDDO	VDDO	TXDATA3_ N[2]	TXCLK_SR C2_N	TXDATA3_ N[0]	TXCLK3_P	M
VDDO	VDDI	VDDI	VDDI	VSS	VSS	VDDI	VDDI	VDDO	NC17	VSS	VSS	TXCLK_SR C3_N	TXCLK_SR C2_P	TXDATA2_P [3]	TXCLK3_N	VSS	N
VDDI	VDDI	VSS	VDDI	VDDI	VDDI	VDDI	VDDO	VDDO	VDDO	VDDO	TXCLK_SR C3_P	TXCLK2_P	TXDATA2_ N[3]	TXDATA2_P [1]	VDDI	VDDI	P
VSS	VDDI	VSS	VSS	VDDI	VDDI	VDDO	VDDO	VSS	VSS	VSS	TXCLK2_N	TXDATA2_P [0]	TXDATA2_ N[1]	VSS	VSS	TXDATA2_P [2]	R
VSS	VDDI	VDDI	VDDI	VDDI	VDDO	VDDO	VDDO	VDDO	VSS	VDDI	TXDATA2_ N[0]	TXCLK1_P	VDDI	VDDI	TXDATA2_ N[2]	TXCLK_SR C1_N	T
VSS	VSS	VSS	VDDI	VDDO	VDDO	VSS	VSS	VDDO	VDDI	VDDI	TXCLK1_N	VSS	VSS	TXDATA1_ N[3]	TXCLK_SR C1_P	TXDATA1_ N[1]	U
VSS	VSS	VSS	VDDI	VDDO	VDDO	VSS	VSS	VDDI	VDDI	VSS	OIF_ATB1	VSS	VSS	TXDATA1_P [3]	TXDATA1_ N[2]	TXDATA1_P [1]	V
VSS	VDDI	VDDI	VDDI	VDDI	VDDO	VDDO	VDDO	VDDO	VSS	VSS	RXDATA4_ P[1]	OIF_ATB0	VDDI	VDDI	TXDATA1_ N[0]	TXDATA1_P [2]	W
VSS	VDDI	VSS	VSS	VDDI	VDDI	VDDO	VDDO	VSS	VSS	VDDO	RXDATA4_ P[3]	RXDATA4_ N[1]	RXDATA4_ P[0]	VSS	VSS	TXDATA1_P [0]	Y
VDDI	VDDI	VSS	VDDI	VDDI	VDDI	VDDI	VDDO	VDDO	VDDO	VDDO	RXCLK3_P	RXDATA4_ N[3]	RXDATA4_ P[2]	RXDATA4_ N[0]	VDDI	VDDI	AA
VDDO	VDDI	VDDI	VDDI	VSS	VSS	VDDI	VDDI	VDDO	VDDO	VSS	VSS	RXCLK3_N	RXDATA3_ P[1]	RXDATA4_ N[2]	RXCLK4_P	VSS	AB
VDDO	VDDO	VDDI	VDDI	VSS	VDDI	VDDI	VDDI	VDDI	VSS	VSS	VDDO	VDDO	RXCLK2_P	RXDATA3_ N[1]	RXDATA3_ P[3]	RXCLK4_N	AC
VSS	VDDO	VDDO	VDDI	VDDI	VDDI	VSS	VSS	VDDI	VSS	VDDO	RXDATA2_ P[3]	VSS	VSS	RXCLK2_N	RXDATA3_ P[2]	RXDATA3_ N[3]	AD
VSS	VDDO	VDDO	VDDO	VDDI	VDDI	VSS	VDDI	VDDI	VDDO	VDDO	RXDATA1_ P[1]	RXDATA2_ N[3]	VDDO	VDDO	RXDATA3_ P[0]	RXDATA3_ N[2]	AE
VSS	VDDO	VSS	VSS	VDDO	VDDO	VSS	VDDI	VSS	VSS	VDDI	RXDATA1_ P[2]	RXDATA1_ N[1]	RXDATA2_ P[0]	VSS	VSS	RXDATA3_ N[0]	AF
VDDO	VDDO	VSS	VDDO	VDDO	VSS	VSS	VDDO	VSS	VDDI	VDDI	VSS	RXDATA1_ N[2]	RXDATA2_ P[1]	RXDATA2_ N[0]	VDDO	VDDO	AG
VDDI	VDDI	VDDO	VDDO	VSS	VSS	VDDO	VDDO	VSS	VDDI	VSS	VSS	VDDI	RXDATA1_ P[0]	RXDATA2_ N[1]	RXDATA2_ P[2]	VSS	AH
VDDI	VDDO	VDDO	VSS	VSS	VDDO	VDDO	VSS	VSS	VDDO	VSS	VDDI	VDDI	RXDATA1_ P[3]	RXDATA1_ N[0]	RXCLK1_P	RXDATA2_ N[2]	AJ
VSS	VDDO	VSS	VSS	VDDO	VDDO	VSS	VSS	VDDO	VDDO	VDDI	VDDI	VSS	VSS	RXDATA1_ N[3]	SYNC_ERR 4	RXCLK1_N	AK
VSS	VDDI	B3E[1]	RTOH[3]	ROHFP[1]	ROHCLK[3]	VSS	VDDO	RLDCLK[1]	RLDCLK[4]	RSLDCLK[1]	NC13	VSS	VDDO	VDDO	SYNC_ERR 2	SYNC_ERR 3	AL
VDDI	VDDI	VSS	RTOH[1]	ROHFP[3]	ROHCLK[1]	RLD[3]	VDDO	VSS	RLDCLK[2]	RSLD[4]	RSLDCLK[2]	NC12	VDDO	VSS	VSS	SYNC_ERR 1	AM
B3E[4]	B3E[2]	VSS	VDDI	RTOH[4]	ROHFP[2]	ROHCLK[4]	RLD[1]	VSS	VDDO	RLDCLK[3]	RSLD[1]	RSLDCLK[3]	TEST_RCL K	VSS	VDDI	VDDI	AN
VDDI	B3E[3]	RTOH[2]	VDDI	VSS	ROHFP[4]	ROHCLK[2]	RLD[4]	RLD[2]	VDDO	VSS	RSLD[3]	RSLD[2]	RSLDCLK[4]	PGMRCLK	VDDI		AP

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10 Pin Description

This section describes the pins shown in Section 9.

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11 Configuration Pin Signals

Pin Name	Type	Pin No.	Function
QUAD_2488	Input	L29	The **quad 2488 Mbit/s mode select** (QUAD_2488) signal selects between the single STS-192/STM-64 mode or the quad STS-48/STM-16 mode. When QUAD is low, the device is in single STS-192/STM-64 mode. When QUAD is high, the device is in quad STS-48/STM-16 mode. QUAD_2488 is considered static. A software reset must be issued when toggling QUAD_2488 pin while the device is in operation.

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12 STS-192/STM-64 Line Side Interface Signals

Pin Name	Type	Pin No.	Function
RXCLK4_p RXCLK4_n RXCLK3_p RXCLK3_n RXCLK2_p RXCLK2_n RXCLK1_p RXCLK1_n	Analog LVDS Input	AB2 AC1 AA6 AB5 AC4 AD3 AJ2 AK1	The **differential receive clock** (RXCLK) inputs provides timing for the SPECTRA-9953 receive operation. RXCLK[N]_p/n is a 622.08 Mbit/s nominally 45-55% duty cycle clock. For quad STS-48/STM-16 mode, the rising edge of RXCLK[N]+/- is used to sample the respective RXDATA[N]_p/n[3:0] receive data bus (i.e. RXCLK1_p/n is used to sample RXDATA1[3:0]). For STS-192/STM-64 mode, the rising edge of RXCLK2_p/n is used to sample the four RXDATA[4:1][3:0] buses. RXCLK1_p/n, RXCLK3_p/n and RXCLK4_p/n are ignored.
RXDATA4_p[3] RXDATA4_n[3] RXDATA4_p[2] RXDATA4_n[2] RXDATA4_p[1] RXDATA4_n[1] RXDATA4_p[0] RXDATA4_n[0] RXDATA3_p[3] RXDATA3_n[3] RXDATA3_p[2] RXDATA3_n[2] RXDATA3_p[1] RXDATA3_n[1] RXDATA3_p[0] RXDATA3_n[0] RXDATA2_p[3] RXDATA2_n[3] RXDATA2_p[2] RXDATA2_n[2] RXDATA2_p[1] RXDATA2_n[1] RXDATA2_p[0] RXDATA2_n[0] RXDATA1_p[3] RXDATA1_n[3] RXDATA1_p[2] RXDATA1_n[2] RXDATA1_p[1] RXDATA1_n[1] RXDATA1_p[0] RXDATA1_n[0]	Analog LVDS Input	Y6 AA5 AA4 AB3 W6 Y5 Y4 AA3 AC2 AD1 AD2 AE1 AB4 AC3 AE2 AF1 AD6 AE5 AH2 AJ1 AG4 AH3 AF4 AG3 AJ4 AK3 AF6 AG5 AE6 AF5 AH4 AJ3	The **differential receive data** (RXDATA) inputs carries the byte-serial STS-48 (STM-16) or STS-192 (STM-64) streams. Each differential pair is a 622.08 Mbps stream. For quad STS-48/STM-16 mode, each of the four RXDATA[N]_p/n[3:0] buses represents a single STS-48c (STM-16c) stream. RXDATA[N]_p/n[3] is the most significant bit (corresponding to bit 1 of each serial word, the first bit received). RXDATA[N]_p/n[0] is the least significant bit (corresponding to bit 4 of each word, the last bit received). RXDATA[N]_p/n[3:0] is sampled on the rising edge of the corresponding RXCLK[N]_p/n. For STS-192/STM-64 mode, the four RXDATA[N]_p/n[3:0] buses represents a single STS-192c (STM-64c) stream. RXDATA4_p/n[3:0] represents the most significant nibble while RXDATA1_p/n[3:0] represents the least significant nibble of the received word. RXDATA4_p/n[3] is the most significant bit (corresponding to bit 1 of each serial word, the first bit received). RXDATA1_p/n[0] is the least significant bit (corresponding to bit 16 of each word, the last bit received). RXDATA[4:1]_p/n[3:0] is sampled on the rising edge of the RXCLK2_p/n.
SYNC_ERR4 SYNC_ERR3 SYNC_ERR2 SYNC_ERR1	LV-TTL Input	AK2 AL1 AL2 AM1	The **synchronization error** (SYNC_ERR) inputs indicates if the RXDATA[N]_p/n buses can be safely sampled. When SYNC_ERR[N] is high (optionally low), RXDATA[N]_p/n is not derived from the optical line and is suspect or might indicate a fiber loss of signal. When SYNC_ERR[N] is low

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Pin Name	Type	Pin No.	Function
			(optionally high), RXDATA[N]_p/n is recovered from the optical stream. The SYNC_ERR[N] signals are treated as asynchronous inputs. A change of SYNC_ERR value triggers an interruption, optionally zeros the received data and optionally leads to a Loss of Signal (LOS) interrupt. For quad STS-48/STM-16 mode, SYNC_ERR[N] indicates the validity of the RXDATA[N]_p/n[3:0] receive data bus (i.e. SYNC_ERR1 validates RXDATA1[3:0]). For STS-192/STM-64 mode, SYNC_ERR1 indicates the validity of the RXDATA[4:1]_p/n[3:0] receive data buses. SYNC_ERR2, SYNC_ERR3 and SYNC_ERR4 are ignored.
TXCLK_SRC4_p TXCLK_SRC4_n TXCLK_SRC3_p TXCLK_SRC3_n TXCLK_SRC2_p TXCLK_SRC2_n TXCLK_SRC1_p TXCLK_SRC1_n	Analog LVDS Input	J4 H3 P6 N5 N4 M3 U2 T1	The **differential transmit clock source** (TXCLK_SRC) inputs provides timing for the SPECTRA-9953 transmit operation. TXCLK_SRC[N]_p/n is a 622.08 Mbit/s nominally 45-55% duty cycle clock. For quad STS-48/STM-16 mode, the TXCLK_SRC[N]_p/n is used to clock the respective STS-48/STM-16 slice. TXCLK_SRC[N]_p/n is looped back internally as the corresponding TXCLK[N]_p/n output (i.e. TXCLK_SRC1_p/n is looped back as TXCLK1_p/n). For STS-192/STM-64 mode, TXCLK_SRC2_p/n is used to clock the transmit side. TXCLK_SRC2_p/n is looped back internally as the TXCLK2_p/n output. TXCLK1_p/n, TXCLK3_p/n and TXCLK4_p/n are ignored.
TXCLK4_p TXCLK4_n TXCLK3_p TXCLK3_n TXCLK2_p TXCLK2_n TXCLK1_p TXCLK1_n	Analog LVDS Output	F1 G2 M1 N2 P5 R6 T5 U6	The **differential transmit clock** (TXCLK) outputs provides a timing reference for the transmit TXDATA[N]_p/n[3:0] buses. TXCLK[N]_p/n is a 622.08 Mbit/s nominally 40%-60% duty cycle clock. For quad STS-48/STM-16 mode, the rising edge of TXCLK[N]_p/n is used to update the corresponding TXDATA[N]_p/n[3:0] bus. TXCLK[N]_p/n is an internally looped back version of the corresponding TXCLK_SRC[N]_p/n input (i.e. TXCLK_SRC1+/- is looped back as TXCLK1_p/n). For STS-192/STM-64 mode, the rising edge of TXCLK2_p/n is used to update the TXDATA[4:1]_p/n[3:0] bus. TXCLK1_p/n, TXCLK3_p/n and TXCLK4_p/n should not be used..
TXDATA4_p[3] TXDATA4_n[3] TXDATA4_p[2] TXDATA4_n[2] TXDATA4_p[1] TXDATA4_n[1] TXDATA4_p[0] TXDATA4_n[0] TXDATA3_p[3] TXDATA3_n[3] TXDATA3_p[2] TXDATA3_n[2]	Analog LVDS Output	G3 H4 K5 L6 J5 K6 E1 F2 K1 L2 L3 M4	The **differential transmit data** (TXDATA) outputs carries the byte-serial STS-48 (STM-16) or STS-192 (STM-64) streams. Each differential pair is a 622.08 Mbps stream. For quad STS-48/STM-16 mode, each of the four TXDATA[N]_p/n[3:0] buses represents a single STS-48 (STM-16) stream. TXDATA[N]_p/n[3] is the most significant bit (corresponding to bit 1 of each serial word, the first bit transmitted). TXDATA[N]_p/n[0] is the least significant bit (corresponding to bit 4 of each word, the last bit transmitted). TXDATA[N]_p/n[3:0] is updated on the rising edge of the corresponding TXCLK[N]_p/n. For STS-192/STM-64 mode, the four TXDATA[N]_p/n[3:0]

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Pin Name	Type	Pin No.	Function
TXDATA3_p[1] TXDATA3_n[1] TXDATA3_p[0] TXDATA3_n[0] TXDATA2_p[3] TXDATA2_n[3] TXDATA2_p[2] TXDATA2_n[2] TXDATA2_p[1] TXDATA2_n[1] TXDATA2_p[0] TXDATA2_n[0] TXDATA1_p[3] TXDATA1_n[3] TXDATA1_p[2] TXDATA1_n[2] TXDATA1_p[1] TXDATA1_n[1] TXDATA1_p[0] TXDATA1_n[0]		J1 K2 L1 M2 N3 P4 R1 T2 P3 R4 R5 T6 V3 U3 W1 V2 V1 U1 Y1 W2	buses represents a single STS-192 (STM-64) stream. TXDATA4_p/n[3:0] represents the most significant nibble while TXDATA1_p/n[3:0] represents the least significant nibble of the transmitted word. TXDATA4_p/n[3] is the most significant bit (corresponding to bit 1 of each serial word, the first bit transmitted). TXDATA1_p/n[0] is the least significant bit (corresponding to bit 16 of each word, the last bit transmitted). TXDATA[4:1]_p/n[3:0] is updated on the rising edge of the TXCLK2_p/n.
TXFPI[1]	Input	D2	The **transmit line frame pulse input** provides line timing on the serial interface. TXFPI rising edge is detected (with a 6 byte blind window) to force re-alignement of the internal line transmit timings. TXFPO is used to indicate a rought estimate of the first A1 bytes of the transmitted SONET/SDH frame. TXFPI can be disabled by setting to 1 the SPECTRA-9953 transmit configuration 1 TXFPI_DISABLE register bit. TXFPI is an asynchronous input.
TXFPO[4] TXFPO[3] TXFPO[2] TXFPO[1]	Output	J7 E3 G5 C1	The **transmit line frame pulse output** provide line timing on the serial interface. TXFPO is set high once every 9720 TXCLK_SRC/8 to roughly indicate that a 125us (first A1) frame boundary has been serialized on the line. For quad-2488 mode, TXFPO[N] is used to indicate rough alignment on STS-48/STM-16[N] SONET/SDH stream. For STS-192/STM-64 mode, only TXFPO1 is used to indicate rough alignment on STS-192/STM-64 data stream. TXFPO2_4 should be ignored. TXFPO is an asynchronous output.

[1] TXFPI and TXFPO are considered dirty frame pulse indicators. They do not indicate the exact frame boundary byte position. Instead an approximate A1 byte is indicated. This allows easy and quick external alignment and framing algorithms to be implemented.

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Pin Name	Type	Pin No.	Function
PHASE_ERR4 PHASE_ERR3 PHASE_ERR2 PHASE_ERR1	Input	D1 E2 L8 G4	The **phase error** (PHASE_ERR) inputs indicates when the TXCLK[N]_p/n output is not aligned with the corresponding TXDATA[N]_p/n bus. When asserted, the receiving device cannot use the source synchronous TXCLK[N]_p/n to sample the corresponding TXDATA[N]_p/n bus. PHASE_ERR[N] are treated as asynchronous signals and are used to trigger maskable interrupts. In addition, the associated PHASE_INIT[N] output should be asserted to reinitiate alignment under user control. For quad STS-48/STM-16 mode, PHASE_ERR[N] indicates a phase alignment error for the corresponding transmit TXCLK[N]_p/n clock and TXDATA[N]_p/n data bus. For STS-192/STM-64 mode, PHASE_ERR1 indicates a phase alignment error for the TXCLK2 clock (the OC-192 mode clock) and the TXDATA[4:1]_p/n[3:0] bus. PHASE_ERR2, PHASE_ERR3 and PHASE_ERR4 are ignored. PHASE_ERR[4:1] is a low speed asynchronous input.
PHASE_INIT4 PHASE_INIT3 PHASE_INIT2 PHASE_INIT1	Output	H5 J6 K7 F3	The **phase initiatilization** (PHASE_INIT) outputs indicates to the receiving device that the device should start the TXCLK[N]_p/n and TXDATA[N]_p/n alignment process. The PHASE_INIT[N] outputs are directly sourced from the SPECTRA-9953 STLI-192 Phase Alignment register. PHASE_INIT[4:1] is a low speed asynchronous output.

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13 Receive and Transmit Reference

Pin Name	Type	Pin No.	Function
PGMRCLK	Output	AP3	The **programmable receive clock** (PGMRCLK) signal provides timing reference for the receive line interface. In single STS-192 mode, PGMRCLK is a divided version of RXCLK2_p/n clock. Using SRLI_192 PGMRCLKSEL[1:0] register bits, PGMRCLK is a nominal 19.44 MHz, 50% duty cycle clock or a nominal 8 KHz, 50% duty cycle clock or a nominal 77.76MHz, 50% duty cycle. In quad STS-48 mode, PGMRCLK is a divided version of one of the RXCLK1-4_p/n clocks. The SRLI_192 PGMRCLKSRC[1:0] register is used to select which of the four clocks is muxed onto PRGMRCLK. Using PGMRCLKSEL register bits, PGMRCLK is a nominal 19.44 MHz, 50% duty cycle clock or a nominal 8 KHz, 50% duty cycle clock or a nominal 77.76MHz, 50% duty cycle. PGMRCLK output can be disabled and held low by programming the SRLI_192 PGMRCLKSEL[1:0] to 00.
PGMTCLK	Output	A4	The **programmable transmit clock** (PGMTCLK) signal provides timing reference for the transmit line interface. In single STS-192 mode, PGMTCLK is a divided version of TXCLK2_p/n clock. Using STLI_192 PGMTCLKSEL[1:0] register bits, PGMTCLK is a nominal 19.44 MHz, 50% duty cycle clock or a nominal 8 KHz, 50% duty cycle clock or a nominal 77.76MHz, 50% duty cycle. In quad STS-48 mode, PGMTCLK is a divided version of one of the TXCLK1-4_p/n clocks. The STLI_192 PGMTCLKSRC[1:0] register is used to select which of the four clocks is muxed onto PGMTCLK. Using PGMTCLKSEL register bits, PGMTCLK is a nominal 19.44 MHz, 50% duty cycle clock or a nominal 8 KHz, 50% duty cycle clock or a nominal 77.76MHz, 50% duty cycle. PGMTCLK output can be disabled and held low by programming the STLI_192 PGMTCLKSEL[1:0] to 00.

13.1 Receive Section/Line DCC Extraction Signals

Pin Name	Type	Pin No.	Function
RSLDCLK1 RSLDCLK2 RSLDCLK3 RSLDCLK4	Tristate Output	AL7 AM6 AN5 AP4	The **receive section or line data communication channel clock** (RSLDCLK1-4) signal is used to update the receive section or line DCC (RSLD1-4). In STS-192/STM-64 mode, only RSLDCLK1 is active. RSLDCLK2-4 is undefined.

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Pin Name	Type	Pin No.	Function
			When section DCC is selected, RSLDCLK1-4 is a nominal 192 kHz clock 50 % duty cycle. When line DCC is selected, RSLDCLK1-4 is a nominal 576 kHz clock with 50 % duty cycle. RSLD1-4 is updated on the falling edge of RSLDCLK1-4 and ROHFP1-4 is used to identify the MSB of the D1 or the D4 byte on RSLD1-4. The RRMP register contains the RSLD_SEL register bit used to select the section or line DCC and the RSLD_TS register bit that can be used to tri-state RSLDCLK1-4 and RSLD1-4 outputs.
RSLD1 RSLD2 RSLD3 RSLD4	Tristate Output	AN6 AP5 AP6 AM7	The **receive section or line data communication channel** (RSLD1-4) signal contains the received section DCC (D1-D3) or line DCC (D4-D12). In STS-192/STM-64 mode, only RSLD1 is active. RSLD2-4 is undefined. RSLD1-4 is updated on the falling edge of RSLDCLK1-4 and should be sampled externally on the rising edge of RSLDCLK1-4. ROHFP1-4 is used to identify the MSB of the D1 or the D4 byte on RSLD1-4. The RRMP register contains the RSLD_SEL register bit used to select the section or line DCC and the RSLD_TS register bit that can be used to tri-state RSLDCLK1-4 and RSLD1-4 outputs.
RLDCLK1 RLDCLK2 RLDCLK3 RLDCLK4	Tristate Output	AL9 AM8 AN7 AL8	The **receive line data communication channel clock** (RLDCLK1-4) signal is used to update the received line DCC (RLD1-4). In STS-192/STM-64 mode, only RLD1 is active. RLD2-4 is undefined. RLDCLK1-4 is a nominal 576 kHz clock 50 % duty cycle. RLD1-4 is updated on the falling edge of RLDCLK1-4 and ROHFP1-4 is used to identify the MSB of the D4 byte on RLD1-4. The RRMP register contains the RLD_TS register bit that can be used to tri-state RLDCLK1-4 and RLD1-4 outputs.
RLD1 RLD2 RLD3 RLD4	Tristate Output	AN10 AP9 AM11 AP10	The **receive line data communication channel** (RLD1-4) signal contains the received line DCC (D4-D12). In STS-192/STM-64 mode, only RLD1 is active. RLD2-4 is undefined. RLD1-4 is updated on the falling edge of RLDCLK1-4 and should be sampled externally on the rising edge of RLDCLK1-4. ROHFP1-4 is used to identify the MSB of the D4 byte on RLD1-4.

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Pin Name	Type	Pin No.	Function
			The RRMP register contains the RLD_TS register bit that can be used to tri-state RLDCLK1-4 and RLD1-4 outputs.

13.2 Transmit Section/Line DCC Insertion Signals

Pin Name	Type	Pin No.	Function
TSLDCLK1 TSLDCLK2 TSLDCLK3 TSLDCLK4	Tristate Output	D8 C7 D7 C6	The **transmit section or line data communication channel clock** (TSLDCLK1-4) signal is used to clock in the transmit section or line DCC (TSLD1-4). In STS-192/STM-64 mode, only TSLDCLK1 is active. TSLDCLK2-4 is undefined. When section DCC is selected (or TSLD port is not enabled), TSLDCLK1-4 is a nominal 192 kHz clock 50 % duty cycle. When line DCC is selected, TSLDCLK1-4 is a nominal 576 kHz clock 50 % duty cycle. TSLD1-4 is sampled on the rising edge of TSLDCLK1-4 and TOHFP1-4 is used to identify the MSB of the D1 or the D4 byte on TSLD1-4. The TRMP register contains the TSLD_SEL register bit used to select the section or line DCC and the TSLD_TS register bit that can be used to tri-state the TSLDCLK1-4 output.
TSLD1 TSLD2 TSLD3 TSLD4	Input	B7 A6 B6 A5	The **transmit section or line data communication channel** (TSLD) signal contains the section DCC (D1-D3) or the line DCC (D4-D12) to be transmitted. In STS-192/STM-64 mode, only TSLD1 is active. TSLD2-4 is undefined. TSLD is sampled on the rising edge of TSLDCLK and TOHFP1 is used to identify the MSB of the D1 or the D4 byte on TSLD. The TTOH and TTOHEN inputs take precedence over TSLD. The TRMP register contains the TSLD_SEL register bit used to select the section or line DCC.
TLDCLK1 TLDCLK2 TLDCLK3 TLDCLK4	Tristate Output	C11 A10 D9 C8	The **transmit line data communication channel clock** (TLDCLK1-4) signal is used to clock in the transmit line DCC (TLD1-4). In STS-192/STM-64 mode, only TLDCLK1 is active.TLDCLK2-4 is undefined. TLDCLK1-4 is a nominal 576 kHz clock 50 % duty cycle. TLD1-4 is sampled on the rising edge of TLDCLK1-4 and TOHFP1-4 is used to identify the MSB of the D4 byte on TLD1-4. The TRMP register contains the TLD_TS register bit that can

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Pin Name	Type	Pin No.	Function
			be used to tri-state the TLDCLK1-4 output.
TLD1 TLD2 TLD3 TLD4	Input	D12 B11 B10 A9	The **transmit line data communication channel** (TLD1-4) signal contains the line DCC (D4-D12) to be transmitted. In STS-192/STM-64 mode, only TLD1 is active.TLD2-4 is undefined. TLD1-4 is sampled on the rising edge of TLDCLK1-4 and TOHFP1-4 is used to identify the MSB of the D4 byte on TLD1-4. The TTOH1-4 and TTOHEN1-4 inputs take precedence over TLD1-4.

13.3 Receive Section/Line Overhead Extraction Signals

Pin Name	Type	Pin No.	Function
ROHCLK1 ROHCLK2 ROHCLK3 ROHCLK4	Output	AM12 AP11 AL12 AN11	The **receive overhead clock** (ROHCLK1-4) signal provides timing for the receive section, line overhead and B3E extraction. These clocks are derived from the receive line clocks RXCLK1-4. In STS-192/STM-64 mode, ROHCLK1 is a nominal 82.94 MHz clock generated by gapping a 103.68 MHz clock. ROHCLK1 has a 50% nominal high duty cycle. ROHCLK2-4 are not defined. In quad STS-48/STM-4 mode, ROHCLK1-4 is a nominal 82.94 MHz clock generated by gapping a 103.68 MHz clock. ROHCLK1-4 has a 50% nominal high duty cycle. ROHFP1-4, RTOH1-4 and B3E1-4 are updated on the rising edge of ROHCLK1-4.
ROHFP1 ROHFP2 ROHFP3 ROHFP4	Output	AL13 AN12 AM13 AP12	The **receive overhead frame pulse** (ROHFP1-4) signal provides timing for the receive section, line overhead and B3E extraction. In STS-192/STM-64 mode, ROHFP1 is used to indicate the most significant bit (MSB) on RSLD1, RLD1, RTOH1-4 and the first possible path BIP error on B3E1-4. ROHFP2-4 are not defined. In quad STS-48/STM-16 mode, ROHFP1-4 is used to indicate the most significant bit (MSB) on RSLD1-4, RLD1-4, RTOH1-4 and the first possible path BIP error on B3E1-4. ROHFP1-4 can be sampled on the rising edge of RSLDCLK1-4 and RLDCLK1-4. ROHFP1-4 can be sample on the rising edge of ROHCLK1-4. ROHFP1-4 is updated on the rising edge of ROHCLK1-4.
RTOH1 RTOH2 RTOH3 RTOH4	Output	AM14 AP15 AL14	The **receive transport overhead** (RTOH1-4) signal contains the received transport overhead bytes (A1, A2, J0, Z0, B1, E1, F1, D1-D3, H1-H3, B2, K1, K2, D4-D12, Z1/S1, Z2/M1, E2 and other overhead bytes) extracted from the incoming

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Pin Name	Type	Pin No.	Function
		AN13	stream. RTOH1-4 is updated on the rising edge of ROHCLK1-4.

13.4 Receive/Transmit Section/Line/Path Status and Alarms Signals

Pin Name	Type	Pin No.	Function
RRCPCLK	Output	P30	The **receive ring control port clock** (RCPCLK signal provides timing for the receive ring control port. RRCPCLK is a nominal 25.92 MHz clock, 33% high duty cycle and can be connected directly to the TRCPCLK input of a mate SPECTRA-9953 in ring-based Add/Drop multiplexer applications. When the Spectra-9953 is processing four STS-48/STM-16 data streams, the STM-16 slice #1 must be active (software slice reset is not set to 1) for the ring control port to operate normally. RRCPFP and RRCPDAT are generated on the falling edge of RRCPCLK.
RRCPFP	Output	P31	The **receive ring control port frame pulse** (RRCPFP) signal identifies bit positions in the receive ring control port data (RRCPDAT). RRCPFP is high to identify the OOF defect on the RRCPDAT data stream. RRCPFP can be connected directly to the TRCPFP input of a mate SPECTRA-9953 in ring-based Add/Drop multiplexer applications. RRCPFP is generated on the falling edge of RRCPCLK.

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Pin Name	Type	Pin No.	Function
RRCPDAT1 RRCPDAT2 RRCPDAT3 RRCPDAT4	Output	M31 L33 M32 L34	The **receive ring control port data** (RRCPDAT1-4) signal contains the receive ring control port data stream. The receive ring control port data consists of the filtered K1, K2 bytes, the change of APS indication, the APS byte failure indication, the line AIS indication, the line RDI indication, the line REI, the path RDI indication, the path ERDI indication and the path REI. RRCPDAT1-4 can be connected directly to the TRCPDAT1-4 input of a mate SPECTRA-9953 in ring-based Add/Drop multiplexer applications. If sysclk and the receive line clock (rxclk) are not frequency locked, then on RRCPDAT, a frame's worth of REI errors may be added to or subtracted from the correct REI count. The difference is proportional to the clock frequency difference, so for SONET compliant clocks, the REI counts from 1 frame out of 50000 could be added/dropped. RRCPDAT1-4 is updated on the falling edge of RRCPCLK
TRCPCLK	Input	R29	The **transmit ring control port clock** (TRCPCLK) signal provides timing for the transmit ring control port. TRCPCLK is a nominal 25.92 MHz clock, 33% high duty cycle and can be connected directly to the RRCPCLK output of a mate SPECTRA-9953 in ring-based add-drop multiplexer applications. When the Spectra-9953 is processing four STS-48/STM-16 data streams, the STM-16 slice #1 must be active (software slice reset is not set to 1) for the ring control port to operate normally. TRCPFP and TRCPDAT are sampled on the rising edge of TRCPCLK.
TRCPFP	Input	N32	The **transmit ring control port frame pulse** (TRCPFP) signal identifies bit positions in the transmit ring control port data (TRCPDAT). TRCPFP is high to identify the OOF defect on the TRCPDAT data stream. TRCPFP can be connected directly to the RRCPFP output of a mate SPECTRA-9953 in ring-based Add/Drop multiplexer applications. TRCPFP is sampled on the rising edge of TRCPCLK.

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Pin Name	Type	Pin No.	Function
TRCPDAT1 TRCPDAT2 TRCPDAT3 TRCPDAT4	Input	L32 K34 N27 K33	The **transmit ring control port data** (TRCPDAT1-4) signal contains the transmit ring control port data stream. The receive ring control port data consists of the filtered K1, K2 bytes, the change of APS indication, the APS byte failure indication, the line AIS indication, the line RDI indication, the line REI, the path RDI indication, the path ERDI indication and the path REI. TRCPDAT1-4 can be connected directly to the RRCPDAT1-4 output of a mate SPECTRA-9953 in ring-based Add/Drop multiplexer applications. TRCPDAT1-4 is sampled on the rising edge of TRCPCLK.
RSALM1 RSALM2 RSALM3 RSALM4	Output	U26 V26 T28 U27	The **section alarm** (RSALM1-4) signal is set high when an out of frame (OOF), loss of signal (LOS), loss of frame (LOF), line alarm indication signal (LAIS), line remote defect indication (LRDI), section trace identifier mismatch (TIM-S), section trace identifier unstable (TIU-S), signal fail (SF) or signal degrade (SD) alarm is detected. Each alarm indication can be independently enabled using bits in the SPECTRA-9953 Alarm Controller registers. RSALM1-4 is set low when none of the enabled alarms are active. RSALM1-4 are low speed asynchronous signals.
RALM1 RALM2 RALM3 RALM4	Output	R28 T27 R30 T29	The **receive alarm** (RALM1-4) signal is a multiplexed output of individual alarms of the receive paths. Each alarm represents the logical OR of the RSALM, LOP-P, AIS-P, RDI-P, ERDI-P, LOPC-P, PAISC-P, UNEQ-P, PSLU, PSLM, PDI-P, TIU-P, TIM-P status of the corresponding path. The selection of alarms to be reported is controlled by the SPECTRA-9953 Alarm controller registers. When the Spectra-9953 is processing four STS-48/STM-16 data streams, the STM-16 slice #1 must be active (software slice reset is not set to 1) for the RALM port to operate correctly. RALM1-4 is updated on the falling edge of RRCPCLK.Please refer to the individual alarm interrupt descriptions and Functional Description Section for more details on each alarm.

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13.5 Receive Path BIP-8 Error Signals

Pin Name	Type	Pin No.	Function
B3E1 B3E2 B3E3 B3E4	Output	AL15 AN16 AP16 AN17	The **bit interleaved parity error** (B3E1-4) signal carries the path BIP-8 errors detected for each STS-192c/STS-48c/ STS-12c /STS-3c/STS-1 SONET payload or AU4-64c/AU4-16c/AU4-4C/AU-4/AU-3 SDH payload. B3E1-4 is set high for one ROHCLK14 clock cycle for each path BIP-8 error detected (up to eight errors per path per frame). When BIP-8 errors are treated on a block basis, B3E1-4 is set high for one ROHCLK1 clock cycle for up to eight path BIP-8 errors detected (up to one error per path per frame). Path BIP-8 errors are detected by comparing the extracted path BIP-8 byte (B3) with the computed path BIP-8 byte of the previous frame. In STS-192/STM-64 mode, B3E1-4 is updated on the rising edge of ROHCLK1. In STS-48/STM-16 mode, B3E1-4 is updated on the rising edge of ROHCLK1-4.

13.6 Transmit Section/Line Overhead Insertion Signals

Pin Name	Type	Pin No.	Function
TOHCLK1 TOHCLK2 TOHCLK3 TOHCLK4	Output	C13 A12 C12 A11	The **transmit overhead clock** (TOHCLK1-4) signal provides timing for the transmit section and line overhead insertion. These clocks are derived from the transmit line clocks TXCLK1-4. In STS-192/STM-64 mode, TOHCLK1 is a nominal 82.94 MHz clock generated by gapping a 103.68 MHz clock. TOHCLK1 has a 50% nominal high duty cycle. TOHCLK2-4 are not defined. In quad STS-48/STM-16 mode, TOHCLK1-4 is a nominal 82.94 MHz clock generated by gapping a 103.68 MHz clock. TOHCLK1-4 has a 50% nominal high duty cycle. TOHFP1-4 is updated on the rising edge of TOHCLK1-4. TTOH1-4 and TTOHEN1-4 are sampled on the rising edge of TOHCLK1-4.

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Pin Name	Type	Pin No.	Function
TOHFP1 TOHFP2 TOHFP3 TOHFP4	Output	D14 B13 D13 B12	The **transmit overhead frame pulse** (TOHFP1-4) signal provides timing for the transmit section, line and path overhead insertion. In STS-192/STM-64 mode, TOHFP1 is used to indicate the most significant bit (MSB) on TSLD1, TLD1 and TTOH1-4. TOHFP2-4 are not defined. In quad STS-48/STM-16 mode, TOHFP1-4 is used to indicate the most significant bit (MSB) on TTOH1-4. TOHFP1 can be sampled on the rising edge of TSLDCLK and TLDCLK. TOHFP1-4 can be sampled on the rising edge of TOHCLK1-4 TOHFP1-4 is updated on the rising edge of TOHCLK1-4.
TTOH1 TTOH2 TTOH3 TTOH4	Input	A16 A17 C14 A15	The **transmit transport overhead** (TTOH1-4) signal contains the transport overhead bytes (A1, A2, J0, Z0, B1, E1, F1, D1-D3, H1-H3, B2, K1, K2, D4-D12, Z1/S1, Z2/M1, E2 and other overhead bytes) to be transmitted and the error masks to be applied on B1, B2, H1 and H2. TTOH1-4 is sampled on the rising edge of TOHCLK1-4.
TTOHEN1 TTOHEN2 TTOHEN3 TTOHEN4	Input	B17 A18 D15 B16	The **transmit transport overhead insert enable** (TTOHEN1-4) signal controls the insertion of the transmit transport overhead data which is inserted in the outgoing stream. When TTOHEN1-4 is high during a TOH byte on TTOH1-4, the sampled TOH byte is inserted into the corresponding transport overhead byte positions (A1, A2, J0, Z0, E1, F1, D1-D3, H3, K1, K2, D4-D12, Z1/S1, Z2/M1, and E2 bytes). When TTOHEN1-4 is low during a TOH byte on TTOH1-4, that sampled byte is ignored and the default values are inserted into these transport overhead bytes. TTOHEN1-4 is sampled on the rising edge of TOHCLK1-4.

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13.7 Drop/Add Serial TelecomBus Interface Signals

Pin Name	Type	Pin No.	Function
SYSCLK	Input	K30	The **system clock** signal (**SYSCLK**) is the master clock for the SPECTRA-9953 system interface. It provides the reference clock for the SPECTRA-9953 serial TelecomBus interface. SYSCLK must be a 77.76 MHz clock, with a nominal 50% duty cycle. Frequency offset between the transmit line side clock and the SYSCLK bus clock are accommodated by pointer justification events on the transmit line side. Frequency offset between the receive line side clock and the SYSCLK bus clock are accommodated by pointer justification events on the drop system side. AFP, DFP, TPAISFP and TPAIS[4:1] are sampled on the rising edge of SYSCLK. DFPO is updated on the rising edge of the SYSCLK.
DFP	Input	J31	The **drop frame pulse** Input (DFP) provides system timing of the Drop serial TelecomBus interface. DFP is optionally set high once every 9720 SYSCLK cycles, or multiple thereof, to force re-alignement of the differential DROP serial Telecombus (DD[N]_p/n[3:0]). DFPO is used to indicate a rough estimate of the J0 character being transmitted on the serial Drop bus. A software configurable delay (DFPDLY_REG) is used to delay internally the DFP pulse. DFP does not have to be present every frame. The Spectra-9953 keeps the same framing position if DFP is not asserted. DFP is sampled on the rising edge of SYSCLK.
DFPO[2]	Output	L28	The **drop frame pulse** Output (DFPO) provides system timing of the Drop serial TelecomBus interface. It gives a rough estimate of when the drop J0 characters have been transmitted on the serial TelecomBus. DFPO is asserted once (or twice) every 9720 sysclk cycles. DFPO is updated on the rising edge of SYSCLK.
AFP	Input	H32	The **add data frame pulse** signal (AFP) provides system timing of the Add serial TelecomBus interface. AFP is set high once every 9720 SYSCLK cycles, or multiple thereof, to indicate that the J0 frame boundary 8B/10B character has been delivered on the differential LVDS bus (AD[N]_p/n[3:0]). A software configurable delay (AFPDLY_REG) from AFP is used to indicate that the J0 frame boundary 8B/10B character has been delivered on all the add serial data links. Refer to operation section for a detailed description of the system side timings.

[2] DFPO can be asserted twice if the delay between the links J0 characters is bigger than two SYSCLK cycles.

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Pin Name	Type	Pin No.	Function
			AFP is sampled on the rising edge of SYSCLK.
DCMP	Input	M27	The **drop connection memory page** (DCMP) signal controls the selection of the connection memory page in the Drop space slot interchange. This input signal is XORED with an internal DSSI register bit to select the Connection Memory Page. When (DCMP XOR DCMP_REG) is set high, connection memory page 1 is selected. When low , connection memory page 0 is selected. Refer to Functional Timing Section 15.4 for details of when the page change takes place. DCMP is sampled on the rising edge of SYSCLK at the DFP frame position.
ACMP	Input	F34	The **add connection memory page** (ACMP) signal controls the selection of the connection memory page in the Add space slot interchange. This input signal is XORED with an internal ASSI register bit to select the Connection Memory Page. When (ACMP XOR ACMP_reg) is set high, connection memory page 1 is selected. When low, connection memory page 0 is selected. Refer to Functional Timing Section 15.4 for details of when the page change takes place. ACMP is sampled on the rising edge of SYSCLK at the AFP frame position.
DD4_p[3] DD4_n[3] DD4_p[2] DD4_n[2] DD4_p[1] DD4_n[1] DD4_p[0] DD4_n[0] DD3_p[3] DD3_n[3] DD3_p[2] DD3_n[2] DD3_p[1] DD3_n[1] DD3_p[0] DD3_n[0] DD2_p[3] DD2_n[3] DD2_p[2] DD2_n[2] DD2_p[1] DD2_n[1] DD2_p[0] DD2_n[0] DD1_p[3] DD1_n[3] DD1_p[2]	Analog LVDS Output	AK34 AJ33 AH32 AG31 AF30 AE29 AJ34 AH33 AD34 AC33 AE34 AD33 AC28 AB27 AD32 AC31 AA32 Y31 AA30 Y29 Y34 W33 W34 V33 T34 U33 W30	The **differential drop data** (DD[N]_p/n[3:0]) serial link carries in bit serial format the single STS-192/STM-64 or quad STS-48/STM-16 frame data received by the SPECTRA-9953. Each differential pair carries a constituent STS-12/STM-4 of the data stream. For quad STS-48/STM-16 mode, each DD[N] group carries a full STS-48/STM-16 stream. For STS-192/STM-64 mode, DD[1] carries STS-48 #1 (STM-16 #1) while DD[4] carries STS-48 #4 (STM-16 #4). Data on DD[N]_p/n[3:0] is encoded in an 8B/10B format extended from IEEE Std. 802.3. The 8B/10B character bit ‘a’ is transmitted first and the bit ‘j’ is transmitted last. The sixteen differential pairs in DD[N]_p/n[4:1] are frequency locked but not phase locked. DD[N]_p/n[4:1] are nominally 777.6 Mbps data streams.

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Pin Name	Type	Pin No.	Function
DD1_n[2] DD1_p[1] DD1_n[1] DD1_p[0] DD1_n[0]		V29 T30 U29 R34 T33	
AD4_p[3] AD4_n[3] AD4_p[2] AD4_n[2] AD4_p[1] AD4_n[1] AD4_p[0] AD4_n[0] AD3_p[3] AD3_n[3] AD3_p[2] AD3_n[2] AD3_p[1] AD3_n[1] AD3_p[0] AD3_n[0] AD2_p[3] AD2_n[3] AD2_p[2] AD2_n[2] AD2_p[1] AD2_n[1] AD2_p[0] AD2_n[0] AD1_p[3] AD1_n[3] AD1_p[2] AD1_n[2] AD1_p[1] AD1_n[1] AD1_p[0] AD1_n[0]	Analog LVDS Input	AF31 AG32 AD29 AE30 AE33 AF34 AC27 AD28 AB31 AC32 AB33 AC34 AA29 AB30 AA31 AB32 W29 Y30 V34 U34 V32 U32 W27 Y28 V27 W28 V28 U28 N33 M34 R31 P32	The differential **add data** (AD[N]_p/n[3:0]) serial link carries in bit serial format the single STS-192/STM-64 or quad STS-48/STM-16 frame data to be transmitted by the SPECTRA-9953. Each differential pair carries a constituent STS-12/STM-4 of the data stream. For quad STS-48/STM-16 mode, each AD[N] group carries a full STS-48/STM-16 stream. For STS-192/STM-64 mode, AD[1] carries STS-48 #1 (STM-16 #1) while AD[4] carries STS-48 #4 (STM-16 #4). Data on AD[N]_p/n[3:0] is encoded in an 8B/10B format extended from IEEE Std. 802.3. The 8B/10B character bit ‘a’ is transmitted first and the bit ‘j’ is transmitted last. The sixteen differential pairs in AD[N]_p/n[4:1] are frequency locked but not phase locked. AD[N]_p/n[4:1] are nominally 777.6 Mbit/s data streams.

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13.8 Transmit Path AIS Insertion Signals

Pin Name	Type	Pin No.	Function
TPAISFP	Input	G33	The active high **transmit path alarm indication frame pulse** signal (**TPAISFP**) marks the first path AIS assertion request for the transmit SONET/SDH streams on TPAIS[4:1]. TPAISFP is sampled on the rising edge of SYSCLK.
TPAIS[1] TPAIS[2] TPAIS[3] TPAIS[4]	Input	H31 G32 L27 K28	The active high Transmit Path Alarm Indication signal (TPAIS) controls the insertion of path AIS in the transmit stream on a per STS (AU) basis. A high level on TPAIS forces the insertion of the all ones pattern into the corresponding SPE and the payload pointer bytes (H1, H2 and H3). TPAIS is sampled on the rising edge of SYSCLK.

13.9 Microprocessor Interface Signals

Pin Name	Type	Pin No.	Function
CSB	Input	B24	The **active low chip select** (CSB) signal is low during SPECTRA-9953 register accesses. Note that if CSB is not required (i.e. register accesses controlled using the RDB and WRB signals only), CSB must be connected to an inverted version of the RSTB input.
RDB	Input	A26	The **active low read enable** (RDB) signal is low during a SPECTRA-9953 read access. The SPECTRA-9953 drives the D[15:0] bus with the contents of the addressed register while RDB and CSB are low.
WRB	Input	B25	The **active low write strobe** (WRB) signal is low during a SPECTRA-9953 register write access. The D[15:0] bus contents are clocked into the addressed register on the rising WRB edge while CSB is low.
D[15] D[14] D[13] D[12] D[11] D[10] D[9] D[8] D[7] D[6] D[5] D[4] D[3] D[2] D[1] D[0]	I/O	C34 D33 E32 F31 G30 H29 J28 K27 F32 G31 D34 E33 E34 F33 H30 J29	The **bi-directional data bus**, D[15:0], is used during SPECTRA-9953 read and write accesses.

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Pin Name	Type	Pin No.	Function
A[14]/TRS	Input	D27	The **test register select signal** (TRS) selects between normal and test mode register accesses. TRS is high during test mode register accesses, and is low during normal mode register accesses.
A[13] A[12] A[11] A[10] A[9] A[8] A[7] A[6] A[5] A[4] A[3] A[2] A[1] A[0]	Input	B28 C27 D26 C28 A29 A30 B29 A31 B30 C29 D28 D29 A32 B31	The **address bus** (A[14:0]) selects specific registers during SPECTRA-9953 register accesses.
RSTB	Schmidt TTL Input	B22	The **active low reset** (RSTB) signal provides an asynchronous SPECTRA-9953 reset. RSTB is a Schmidt triggered input with an integral pull-up resistor.
ALE	Input	A24	The **address latch enable** (ALE) is an active-high signal and latches the address bus A[14:0] when low. When ALE is high, the internal address latches are transparent. It allows the SPECTRA-9953 to interface to a multiplexed address/data bus. The ALE input has an integral pull up resistor.
INTB	OD Output	B23	The **active low interrupt** (INTB) is set low when a SPECTRA-9953 enabled interrupt source is active. The SPECTRA-9953 may be enabled to report many alarms or events via interrupts. INTB is tri-stated when the interrupt is acknowledged via the appropriate register access. INTB is an open drain output.

13.10 JTAG Test Access Port (TAP) Signals

Pin Name	Type	Pin No.	Function
TCK	Input	B18	The **test clock** (TCK) signal provides timing for test operations that can be carried out using the IEEE P1149.1 test access port. An external pull-up is required on TCK.
TMS	Input	B19	The **test mode select** (TMS) signal controls the test operations that can be carried out using the IEEE P1149.1 test access port. TMS is sampled on the rising edge of TCK. TMS has an integral pull up resistor.
TDI	Input	A19	When the SPECTRA-9953 is configured for JTAG operation, the **test data input** (TDI) signal carries test data into the SPECTRA-9953 via the IEEE P1149.1 test access port. TDI is sampled on the rising edge of TCK. TDI has an integral pull up resistor.

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Pin Name	Type	Pin No.	Function
TDO	Tristate Output	A20	The **test data output** (TDO) signal carries test data out of the SPECTRA-9953 via the IEEE P1149.1 test access port. TDO is updated on the falling edge of TCK. TDO is a tri-state output which is inactive except when scanning of data is in progress.
TRSTB	Schmidt TTL Input	A23	The **active low test reset** (TRSTB) signal provides an asynchronous SPECTRA-9953 test access port reset via the IEEE P1149.1 test access port. TRSTB is a Schmidt triggered input with an integral pull up resistor. In the event that TRSTB is not used, it must be connected to RSTB.

13.11 Digital Miscellaneous Signals

Pin Name	Type	Pin No.	Function
LINE_OOL	Output	H6	LINE_OOL is a reserved output used to test high speed line. NO CONNECT.
SYS_OOL	Output	N30	SYS_OOL is a reserved output used to test high speed system interfaces. NO CONNECT.
TEST_RCLK	Input	AN4	RESERVED FOR TEST PURPOSES. NO CONNECT.
TEST_TCLK	Input	B5	RESERVED FOR TEST PURPOSES. NO CONNECT.
NC[1-17]	Input	M28 P29 J30 K29 J34 M33 N31 C30 A25 B4 A3 AM5 AL6 K8 F4 M7 N8	RESERVED. NO CONNECT.

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13.12 Analog Miscellaneous Signals

Pin Name	Type	Pin No.	Function
RES	Analog	AP23	**Reference resistor connection**. An off-chip 3.16kΩ ±1% resistor is connected between the positive resistor reference pin RES and a Kelvin ground contact RESK. An on-chip negative feedback path will force an internal 0.80V reference (VREF) voltage onto RES , therefore forcing 252 µA of current to flow through the resistor. This current is used to bias the circuitry of the LVDS transmitter (TXLV).
RESK	Analog	AN24	**Reference resistor connection**. An off-chip 3.16 kΩ ±1% resistor is connected between the positive resistor reference pin RES and a Kelvin ground contact RESK. An on-chip negative feedback path will force a 0.8 V VREF voltage onto RES, therefore forcing 252 µA of current to flow through the resistor.
OSC OSCB	Analog LVDS Outputs	AJ32 AH30	For PMC Internal Use only. This is an LVDS version of DIVCLK/DIVCLKB that is transmitted off-chip for jitter analysis. During normal operation, these signals are not used.
ATB1 OIF_ATB1 ATB0 OIF_ATB0	Analog	AH31 V6 AG29 W5	For PMC Internal Use only. Two analog test ports (ATB0, ATB1) are provided for production testing only. If unused these pins should be left FLOATING.

13.13 Line Side Analog Power and Ground

Pin Name	Pin Type	PIN No.	Function
AVDHVREF	Analog	L7	The quiet TXLVREF analog power (AVDHVREF) is a +3.3 V power supply for the quiet analog blocks. This pin is de-coupled to VSS via an on-chip capacitor and is also de-coupled externally to GROUND via a 0.1 µF ceramic de-coupling capacitor for proper HF noise shunting.

13.14 System Side Analog Power and Ground

Pin Name	Pin Type	PIN No.	Function
AVDL1	CSU Analog Power	AK33	The **quiet CSU analog power** (AVDL3-AVDL1) pins are +1.8 V power supplies for the quiet analog blocks. The noisy analog power (AVDL4) pin is a +1.8 V power supply for the noisy analog blocks. AVDL4-AVDL1 are de-coupled from AVSL4-AVSL1 via on-chip capacitors and are also de-coupled externally via the following networks: AVDL1+AVDL2: These balls can be connected together.
AVDL2		AN29 AP26	
AVDL3		AK32 AP24	

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Pin Name	Pin Type	PIN No.	Function
AVDL4		AE27 AF29	They are connected to the 1.8 V supply via a series 1 Ω resistor with 10 μF, 1 μF, and 0.1 μF capacitors to the ground plane. The 0.1 μF capacitor is to be a high-quality ceramic capacitor placed as close as possible to the ADVL4 pins of the chip. AVDL3: A series 0.47 Ω resistor with 10 μF, 1 μF, and 0.1 μF capacitors to the ground plane. The 0.1 μF capacitor is to be a high-quality ceramic capacitor placed as close as possible to the ADVL4 pins of the chip. AVDL4: A series 1 Ω resistor with 10 μF, 1 μF, and 0.1 μFcapacitors to the ground plane. The 0.1 μF capacitor is to be a high-quality ceramic capacitor placed as close as possible to the ADVL4 pins of the chip.
AVSL1	CSU Analog Ground	AE28	The **quiet CSU analog ground** (AVSL3-AVSL1) pins are ground supplies for the quiet analog blocks powered from AVDL3-AVDL1. The noisy analog ground (AVSL4) pin is a ground supply for the noisy analog blocks powered from AVDL4. These pins should be connected to a low impedance off-chip GROUND plane.
AVSL2		AN25 AP25 AP30 AP31	
AVSL3		AL33 AN23	
AVSL4		AD27 AG30	
AVDH1	CSU Analog Power (3.3V)	AP29	The **quiet CSU analog power** (AVDH1) pin is a +3.3 V power supply for the quiet analog blocks. This pin is de-coupled to AVSH1 via an on-chip capacitor and is also de-coupled externally to GROUND via the following structure: a 3 Ω series resistor followed by a 10 μF, a 1 μF, and a 0.1 μF capacitor to the ground plane. The 0.1 μF capacitor must be a high-quality ceramic capacitor placed as close to the AVDH1 ball as possible.
AVSH1	CSU Analog Ground	AJ31 AL34 AN30	The **quiet CSU analog ground** (AVSH1) pin is a ground supply for the analog blocks powered from AVDH1. This pin should be connected to off-chip GROUND.
AVDH2	TXLVREF Analog Power (3.3V)	AN22	The **quiet TXLVREF analog power** (AVDH2) pin is a +3.3 V power supply for the quiet analog blocks. This pin is de-coupled to AVSH2 via an on-chip capacitor and is also de-coupled externally to GROUND via the following structure: a 4.7 Ω series resistor followed by a 1 μF capacitor and a 0.1 μF capacitor to the ground plane. The 0.1 μF capacitor must be a high-quality ceramic capacitor placed as close to the AVDH2 ball as possible.
AVSH2	TXLVREF Analog Ground	AN28	The **quiet TXLVREF analog ground** (AVSH2) pin is a ground supply for the analog blocks powered from AVDH2. This pin should be connected to off-chip GROUND.

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Pin Name	Pin Type	PIN No.	Function
QAVD	Isolation Power	AM34	The **analog isolation positive supply rail**. This QAVD pin should be connected to the 3.3 V(±5%) analog power plane. This pin is de-coupled to QAVS via an on-chip capacitor and is also de-coupled externally to GROUND via a 0.1 μF ceramic decoupling capacitor for proper HF noise shunting.
QAVS	Isolation Ground	AF28	The **analog isolation ground rail**. This QAVS pin should be connected to the ground plane.

13.15 Power and Ground

Pin Name	Pin Type	PIN No.	Function
VDDO	Digital Power	A8 A27 AA7 AA8 AA9 AA10 AA25 AA26 AA27 AA28 AB8 AB9 AB17 AB18 AB26 AC5 AC6 AC16	The **digital I/O power** (VDD) pins should be connected to a well-decoupled +3.3 V digital power supply.

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Pin Name	Pin Type	PIN No.	Function
VDDO		AC17 AC18 AC19 AC29 AC30 AD7 AD15 AD16 AD19 AD20 AE3 AE4 AE7 AE8 AE14 AE15 AE16 AE19 AE20 AE21 AE31 AE32 AF12 AF13 AF16 AF19 AG1 AG2 AG10 AG13 AG14 AG16 AG17 AG18 AG19 AG21 AG33	

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Pin Name	Pin Type	PIN No.	Function
VDDO		AG34 AH10 AH11 AH14 AH15 AH19 AH20 AH21 AJ8 AJ11 AJ12 AJ15 AJ16 AJ20 AJ23 AJ24 AJ25 AK8 AK9 AK12 AK13 AK16 AK23 AK25 AK26 AL3 AL4 AL10 AL21 AL25 AL26 AL31 AL32 AM4 AM10 AM21 AM22 AM25	

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Pin Name	Pin Type	PIN No.	Function
VDDO		AM30 AM31 AN8 AN18 AN19 AN27 AP8 AP19 AP20 AP27 B8 B27 C4 C5 C10 C24 C25 C31 D3 D4 D10 D25 D31 D32 E12 E13 E23 E26 E27 F12 F23 F24 F27 G14 G21 G24 G25	

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Pin Name	Pin Type	PIN No.	Function
VDDO		H1 H2 H12 H13 H14 H17 H18 H21 H33 H34 J13 J14 J16 J17 J18 J19 J21 J22 K3 K4 K14 K15 K16 K19 K20 K21 K31 K32 L15 L16 L19 L20 M5 M6 M16 M17 M18	

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Pin Name	Pin Type	PIN No.	Function
VDDO		M19 M29 M30 N9 N17 N18 N26 P7 P8 P9 P10 P25 P26 P27 P28 R10 R11 R24 R25 T9 T10 T11 T12 T23 T24 T25 T26 U9 U12 U13 U22 U23 V12 V13 V22 V23 W9 W10 W11 W12	

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Pin Name	Pin Type	PIN No.	Function
VDDO		W23 W24 W25 W26 Y7 Y10 Y11 Y24 Y25	

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Pin Name	Pin Type	PIN No.	Function
VDDI	Digital Power	A2 A14 A21 A33 AA1 AA2 AA11 AA12 AA13 AA14 AA16 AA17 AA18 AA19 AA21 AA22 AA23 AA24 AA33 AA34 AB10 AB11 AB14 AB15 AB16 AB19 AB20 AB21 AB24 AB25 AC9 AC10 AC11 AC12 AC14 AC15 AC20	The **core digital power** (VDDI) pins should be connected to a well-decoupled +1.8 V digital power supply.

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Pin Name	Pin Type	PIN No.	Function
VDDI		AC21 AC23 AC24 AC25 AC26 AD9 AD12 AD13 AD14 AD21 AD22 AD23 AD26 AE9 AE10 AE12 AE13 AE22 AE23 AE25 AE26 AF7 AF10 AF18 AF22 AF25 AG7 AG8 AG22 AG23 AG27 AG28 AH5 AH8 AH16 AH17	

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Pin Name	Pin Type	PIN No.	Function
VDDI		AH18 AH23 AH24 AH27 AJ5 AJ6 AJ17 AJ18 AJ19 AJ26 AJ27 AJ29 AJ30 AK6 AK7 AK19 AK20 AK27 AK28 AK29 AL16 AL19 AL20 AM16 AM17 AM19 AN1 AN2 AN14 AN21 AN33 AN34 AP2 AP14 AP17 AP18 AP21	

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Pin Name	Pin Type	PIN No.	Function
VDDI		AP33 B1 B2 B14 B21 B33 B34 C16 C17 C18 C19 C22 C23 D16 D19 D20 D23 E6 E9 E10 E14 E15 E20 E21 E28 E29 F5 F6 F8 F9 F14 F17 F18 F21 F26 F29 F30 G8	

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Pin Name	Pin Type	PIN No.	Function
VDDI		G11 G12 G16 G17 G18 G19 G26 G27 H7 H8 H10 H11 H16 H19 H22 H23 H24 H27 H28 J10 J11 J12 J23 J24 J25 K9 K10 K12 K13 K22 K23 K25 K26 L9 L12 L13 L14 L21	

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Pin Name	Pin Type	PIN No.	Function
VDDI		L22 L23 L26 M8 M9 M10 M11 M12 M14 M15 M20 M21 M23 M24 M25 M26 N10 N11 N14 N15 N16 N19 N20 N21 N24 N25 P1 P2 P11 P12 P13 P14 P16 P17 P18 P19	

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Pin Name	Pin Type	PIN No.	Function
VDDI		P21 P22 P23 P24 P33 P34 R12 R13 R16 R19 R22 R23 T3 T4 T7 T13 T14 T15 T16 T19 T20 T21 T22 T31 T32 U7 U8 U14 U21 V8 V9 V14 V21 W3 W4 W13 W14	

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Pin Name	Pin Type	PIN No.	Function
VDDI		W15 W16 W19 W20 W21 W22 W31 W32 Y12 Y13 Y16 Y19 Y22 Y23	
VSS	Digital Ground	A7 A13 A22 A28 AA15 AA20 AB1 AB6 AB7 AB12 AB13 AB22 AB23 AB28 AB29 AB34 AC7 AC8 AC13 AC22 AD4 AD5 AD8	The **digital ground** (VSS) pins should be connected to the digital ground of the digital power supply.

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Pin Name	Pin Type	PIN No.	Function
VSS		AD10 AD11 AD17 AD18 AD24 AD25 AD30 AD31 AE11 AE17 AE18 AE24 AF2 AF3 AF8 AF9 AF11 AF14 AF15 AF17 AF20 AF21 AF23 AF24 AF26 AF27 AF32 AF33 AG6 AG9 AG11 AG12 AG15 AG20 AG24 AG25 AG26	

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Pin Name	Pin Type	PIN No.	Function
VSS		AH1 AH6 AH7 AH9 AH12 AH13 AH22 AH25 AH26 AH28 AH29 AH34 AJ7 AJ9 AJ10 AJ13 AJ14 AJ21 AJ22 AJ28 AK4 AK5 AK10 AK11 AK14 AK15 AK17 AK18 AK21 AK22 AK24 AK30 AK31 AL5 AL11 AL17 AL18 AL22	

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Pin Name	Pin Type	PIN No.	Function
VSS		AL23 AL24 AL27 AL28 AL29 AL30 AM2 AM3 AM9 AM15 AM18 AM20 AM23 AM24 AM26 AM27 AM28 AM29 AM32 AM33 AN3 AN9 AN15 AN20 AN26 AN31 AN32 AP7 AP13 AP22 AP28 AP32 B3 B9 B15 B20 B26 B32	

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Pin Name	Pin Type	PIN No.	Function
VSS		C2 C3 C9 C15 C20 C21 C26 C32 C33 D5 D6 D11 D17 D18 D21 D22 D24 D30 E4 E5 E7 E8 E11 E16 E17 E18 E19 E22 E24 E25 E30 E31 F7 F10 F11 F13 F15 F16	

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Pin Name	Pin Type	PIN No.	Function
VSS		F19 F20 F22 F25 F28 G1 G6 G7 G9 G10 G13 G15 G20 G22 G23 G28 G29 G34 H9 H15 H20 H25 H26 J2 J3 J8 J9 J15 J20 J26 J27 J32 J33 K11 K17 K18 K24	

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Pin Name	Pin Type	PIN No.	Function
VSS		L4 L5 L10 L11 L17 L18 L24 L25 L30 L31 M13 M22 N1 N6 N7 N12 N13 N22 N23 N28 N29 N34 P15 P20 R2 R3 R7 R8 R9 R14 R15 R17 R18 R20 R21 R26 R27	

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Pin Name	Pin Type	PIN No.	Function
VSS		R32 R33 T8 T17 T18 U4 U5 U10 U11 U15 U16 U17 U18 U19 U20 U24 U25 U30 U31 V4 V5 V7 V10 V11 V15 V16 V17 V18 V19 V20 V24 V25 V30 V31 W7 W8 W17	

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Pin Name	Pin Type	PIN No.	Function
VSS		W18 Y2 Y3 Y8 Y9 Y14 Y15 Y17 Y18 Y20 Y21 Y26 Y27 Y32 Y33	

Notes on Pin Description

1. All SPECTRA-9953 inputs and bidirectionals present minimum capacitive loading and operate at TTL logic levels except the inputs (as marked) that operate at LVDS logic levels.

2. The SPECTRA-9953 digital outputs and bidirectionals that have 4 mA drive capability are: RLD[4:1], RLDCLK[4:1], RSLD[4:1], RSLDCLK[4:1], TSLDCLK[4:1], TLDCLK[4:1], PHASE_INIT[4:1], LINE_OOL[4:1], RSALM[4:1], RALM[4:1], RRCPCLK[4:1], RRCPFP[4:1], RRCPDAT[4:1], SYS_OOL, INTB, TDO, and D[15:0].

3. The SPECTRA-9953 digital outputs and bidirectionals that have 5 mA drive capability are: B3E[4:1], RTOH[4:1], ROHFP[4:1], ROHCLK[4:1], TOHCLK[4:1], TOHFP[4:1], TXFPO[4:1], PGMRCLK, PGMTCLK, and DFPO.

4. Inputs ALE, RSTB, TMS, TDI, and TRSTB have internal pull-up resistors.

5. It is mandatory that every digital ground pin (VSS) be connected to the printed circuit board ground plane to ensure reliable device operation. Refer to the Power Sequencing description in the Operations section.

6. It is mandatory that every digital power pin (VDDO & VDDI) be connected to the printed circuit board power plane to ensure reliable device operation.

7. All analog power and ground pins can be sensitive to noise. They must be isolated from the digital power and ground. Care must be taken to correctly de-couple these pins. Please refer to the Operations section.

8. Due to ESD protection structures in the pads it is necessary to exercise caution when powering a device up or down. ESD protection devices behave as diodes between power supply pins and from I/O pins to power supply pins. Under extreme conditions it is possible to damage these ESD protection devices or trigger latch up. Please adhere to the recommended power supply sequencing as described in the Operation section of this document.

9. Do not exceed 100 mA of current on any pin during the power-up or power-down sequence. Refer to the Power Sequencing description in the Operations section.

10. Before any input activity occurs, ensure that the device power supplies are within their nominal voltage range.

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11. Hold the device in the reset condition until the device power supplies are within their nominal voltage range.

12. Ensure that all digital power is applied simultaneously, and applied before or simultaneously with the analog power. Refer to the Power Sequencing description in the Operations section.

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14 Functional Description

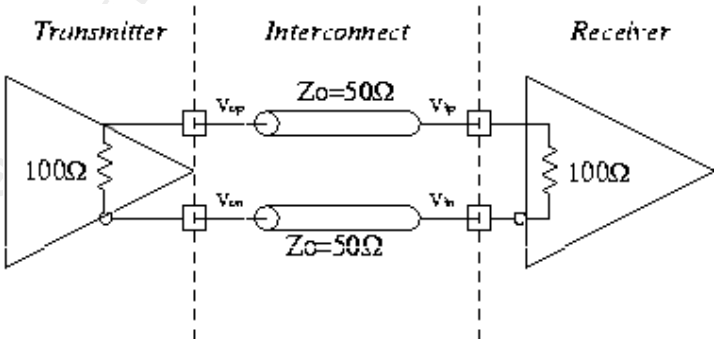
14.1 Line LVDS Overview

The family of LVDS cells use 622 Mbit/s LVDS links. Four 622 Mbit/s LVDS form a set of high-speed serial data links for passing an STS-48 aggregate data stream. Sixteen 622 Mbit/s LVDS form a set for passing an STS-192 aggregate data stream.

The LVDS interface implemented on the SPECTRA-9953 follows the IEEE 1596.3-1996 specification with some minor differences. Figure 6 shows a generic LVDS link. The changes, described in detail below, are implemented to customize and optimize the LVDS interface for the system. Even with these differences the LVDS interface should function with the physical layer of other LVDS interfaces. The differences include:

- Faster rise/fall times (200 – 400) ps versus (300 - 500) ps. Faster edge rates are commonly used with higher speed LVDS interfaces in the industry to ease the interfacing. The IEEE 1596.3-1996 edge rates are optimized for data rates of 400 Mbps and below.
- Hysteresis is not implemented on the receive LVDS interface. Hysteresis is used in many implementations to negate the effect of noise that may exist on any of the unused LVDS links. Hysteresis was not implemented in the SPECTRA-9953 device to minimize circuit complexity, power and cost.
- The LVDS transmitter contains an on-chip 100-ohm termination. Most implementations have single 100-ohm termination on the receiver. By implementing a double termination (on both the LVDS receiver and transmitter), a higher signal integrity and matching is ensured.

Figure 6 Generic LVDS Link Block Diagram



A simple SERDES transceiver functionality is provided on the line side. Serial line rate LVDS data is sampled and de-serialized to 8-bit parallel data. Parallel output transfers are synchronized to a line rate divided-by-eight clock.

The LVDS system is comprised of the LVDS Receiver (RXLV), LVDS Transmitter (TXLV), SIPO, and PISO blocks.

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14.2 LVDS Receivers and SIPO

The LVDS Receiver (RXLV) converts LVDS signaling levels to CMOS digital bit-serial data. A total of twenty RXLV blocks are instantiated in the SPECTRA-9953 line receive section. In single STS-192/STM-64 mode, the LVDS receive block supports a 16-bit 622.08 Mbit/s differential LVDS line side interface for direct connection to external clock recovery, clock synthesis, and serializer-deserializer components. In quad STS-48/STM-16 mode, the LVDS receive block supports four independent 4-bit 622.08 Mbit/s LVDS line side interface for direct connection to external clock recovery, clock synthesis, and serializer-deserializer components.

Note: In both modes, an external Serial to Parallel Converter (SIPO) must be used. If the SIPO supports A1/A2 framing, it must be disabled by negating its out of frame (OOF) input port.

This bit-serial data is fed to a serial-in-parallel-out (SIPO) block. The SIPO block divides the 622 MHz receive clock by eight and generates a parallel 8-bit (running at 77.76 MHz) data bus for each bit-serial data. Thus a total of sixteen internal parallel 8-bit buses running at 77.76 MHz are fed to the SRLI block.

14.3 SONET/SDH Receive Line Interface (SRLI)

The SONET/SDH receive line interface block performs byte and frame alignment on the incoming STS-192/STM-64 or four STS-48/STM-16 data streams based on the SONET/SDH A1/A2 framing pattern.

While out of frame, the SRLI monitors the receive data stream for an occurrence of the A1/A2 framing pattern. The SRLI adjusts its byte and frame alignment when three consecutive A1 bytes followed by three consecutive A2 bytes occur in the data stream. The SRLI informs the RRMP framer block when the framing pattern has been detected to reinitialize to the new transport frame alignment. While in frame, the SRLI maintains the same byte and frame alignment until the RRMP declares out of frame or an external synchronization error has been detected by the clock and data recovery device.

14.4 SONET/SDH Processing Slices

On the SPECTRA-9953 receive side, the SRLI produces sixteen 8-bit buses, each carrying an STS-12/STM-4 stream that is to be processed by a section/line/path termination slice (RRMP, RTTP_SECTION, SBER, RHPP, RTTP_PATH, RSVCA). As per SONET/SDH conventions, the SRLI performs four bytes interleaving on the received serial stream. The processing slices and order of transmission for the STS-192/STM-64 and quad STS-48/STM-16 streams are shown in Figure 7. The slices are numbered from 1,1 to 4,4. When processing an STS-192, the sixteen slices work in a master/slave type of configuration. When a quad STS-48/STM-16 mode is processed, four independent groups of four slices each constitute the processing power of the four STS-48/STM-16 streams. The output of each slice is fed to a Drop bus 8B/10B enocoder.

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On the transmit side, the 16 independent links of the Add bus are fed to 16 independent 8B/10B decoders. Each decoder feeds a transmit processing slice (SHPI, TSVCA, THPP, TTTP_PATH, TRMP, TTTP_SECTION). As on the receive side, there are 16 transmit processing slices that form one group when processing an STS-192/STM-64 stream or four groups when processing four STS-48/STM-16 streams. The output of each slice feeds the STLI that performs the required byte interleaving before line transmission.

While in Quad STS48 Mode, the Spectra-9953 can be configured to carry any mix of STS-1/3c/12c/24c/36c/48c payloads. STS-3c/12c concatenated paths cannot overlap more than one slice (i.e. an STS-3c could not start in slice 2,2 and finish in slice 2,3). STS-24c and STS-36c payloads must take exactly 2 and 3 slices, respectively.

While in Single STS192 mode, the Spectra9953 can be configured to carry any mix of STS-1/3c/12c/(Nx12)c/192c payloads. Payloads larger than STS48c can overlap processing quadrants, but must begin at slice x,1 in order to do so. For instance, an STS-72c payload is allowable, but it could not start at slice 1,2 and finish at slice 2,4. It could, however, exist from slice 3,1 to slice 4,3.

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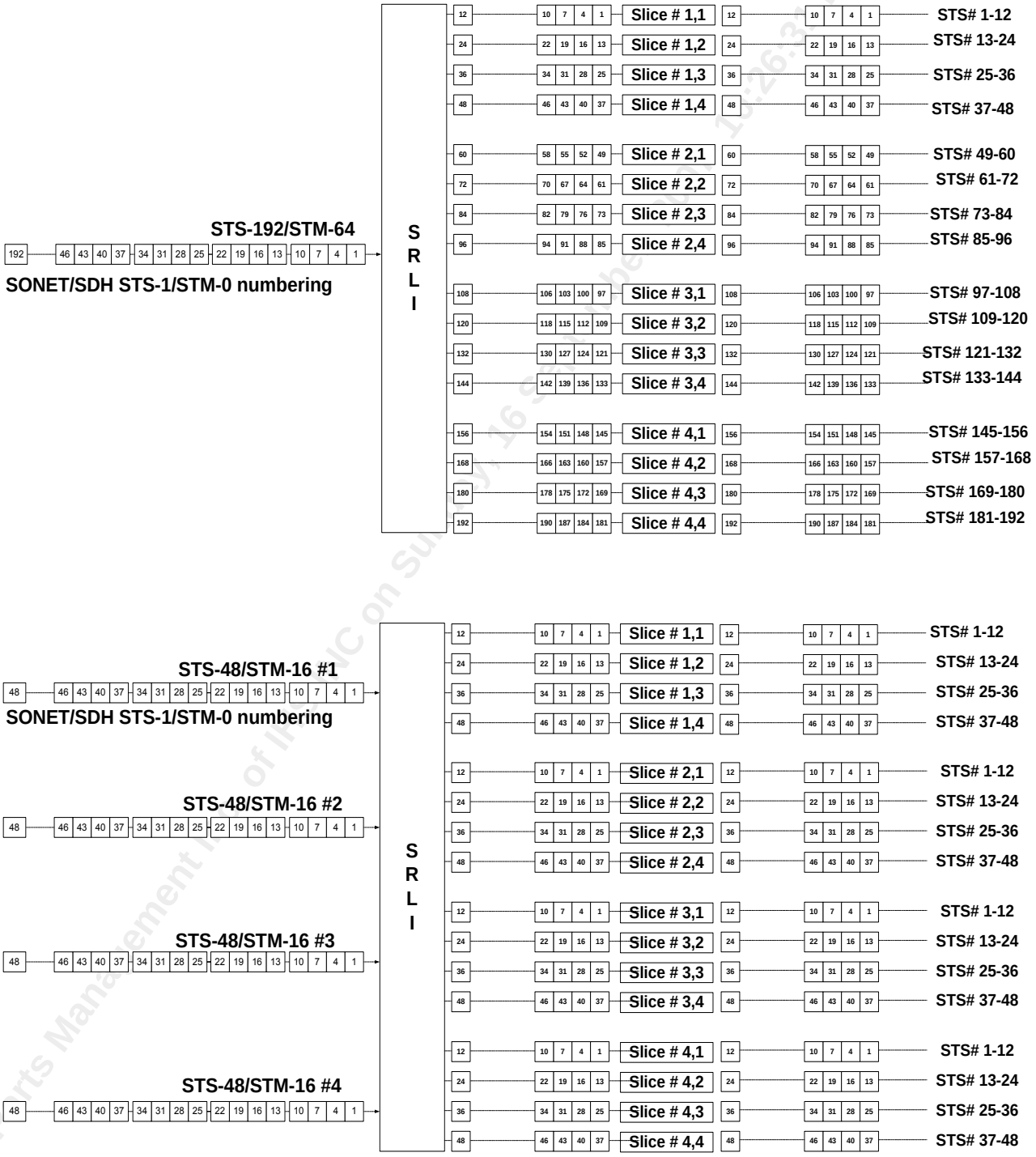
Figure 7 SPECTRA-9953 Processing Slices (STS-192/STM-64 and Quad STS-48/STM-16)



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14.5 Receive Regenerator and Multiplexer Processor (RRMP)

The Receive Regenerator and Multiplexer Processor (RRMP) block extracts and process the transport overhead of the received data stream.

The RRMP frames to the data stream by operating with an upstream pattern detector (SRLI) that searches for occurrences of the A1/A2 framing pattern. Once the SRLI has found an A1/A2 framing pattern, the RRMP monitors for the next occurrence of the framing pattern 125 µs later. Two framing pattern algorithms are provided to improve performance in the presence of bit errors. In algorithm 1, the RRMP declares frame alignment (removes OOF defect) when the 12 A1 and the 12 A2 bytes are seen error-free. In algorithm 2, the RRMP declares frame alignment (removes OOF defect) when only the first A1 byte and the first four bits of the last A2 byte are seen error-free. In single STS-192 (STM-64) mode, the RRMP frames only on the first STS-48 (STM-16) stream. Once in frame, the RRMP monitors the framing pattern and declares OOF when one or more bit errors in the framing pattern are detected for four consecutive frames. Again, depending upon the algorithm either 24 framing bytes or 12 framing bits are examined for bit errors in the framing pattern. Table 4 and Table 5 summarize these algorithms.

Table 4 A1/A2 Bytes Used for Out Of Frame Detection

SONET/SDH	Algorithm 1	Algorithm 2
STS-48/STM-16	STM-4 #1 All A1 bytes STM-4 #4 All A2 bytes	STM-4 #1 First A1 byte STM-4 #4 Last A2 byte (first four bits only)
STS-192/STM-64	STM-4 #1 All A1 bytes STM-4 #16 All A2 bytes	STM-4 #1 First A1 byte STM-4 #16 Last A2 byte (first four bits only)

Table 5 A1/A2 Bytes Used for In Frame Detection

SONET/SDH	Algorithm 1	Algorithm 2
STS-48/STM-16	STM-4 #1 All A1 bytes STM-4 #1 All A2 bytes	STM-4 #1 First A1 byte STM-4 #1 Last A2 byte (first four bits only)
STS-192/STM-64	STM-4 #1 All A1 bytes STM-4 #1 All A2 bytes	STM-4 #1 First A1 byte STM-4 #1 Last A2 byte (first four bits only)

The performance of these framing algorithms in the presence of bit errors and random data is robust. When looking for frame alignment the performance of each algorithm is dominated by the alignment algorithm used in the SRLI, which always examines three A1 and three A2 framing bytes. The probability of falsely framing to random data is less than 0.00001% for either algorithm. Once in frame alignment, the RRMP continuously monitors the framing pattern. When the incoming stream contains a 10^{-3} BER, the first algorithm provides a 99.75% probability that the mean time between OOF occurrences is 0.13 seconds and the second algorithm provides a 99.75% probability that the mean time between OOF occurrences is 7 minutes.

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The RRMP also detects loss of frame (LOF) defect and loss of signal (LOS) defect. LOF is declared when an OOF condition exists for a total period of 3 ms during which there is no continuous in frame period of 3 ms. LOF output is removed when an in frame condition exists for a continuous period of 3 ms. LOS is declared when a continuous period of 20 µs without transitions on the received data stream is detected. LOS is removed when two consecutive framing patterns are found (based on algorithm 1 or algorithm 2) and during the intervening time (one frame). There are no continuous periods of 20 µs without transitions on the received data stream.

The RRMP calculates the section BIP-8 error detection code on the scrambled data of the complete frame. The section BIP-8 code is based on a bit interleaved parity calculation using even parity. The calculated BIP-8 code is compared with the BIP-8 code extracted from the B1 byte of STS-1 (STM-0) #1 of the following frame after de-scrambling. Any difference indicates a section BIP-8 error. The RRMP accumulates section BIP-8 errors in a microprocessor readable 16 bits saturating counter (up to 1 second accumulation time). Optionally, block section BIP-8 errors can be accumulated.

The RRMP optionally de-scrambles the received data stream.

The RRMP calculates the line BIP-8 error detection codes on the de-scrambled line overhead and synchronous payload envelope (SPE) bytes of the constituent STS-1 (STM-0). The line BIP-8 code is based on a bit interleaved parity calculation using even parity. The calculated BIP-8 codes are compared with the BIP-8 codes extracted from the B2 byte of the constituent STS-1 (STM-0) of the following frame after de-scrambling. Any difference indicates a line BIP-8 error. The master RRMP accumulates line BIP-8 errors in a microprocessor readable 24 bits saturating counter (up to 1 second accumulation time). Optionally, block BIP-24 errors can be accumulated.

The RRMP extracts the line remote error indication (REI-L) errors from the M1 byte of STS-1 (STM-0) #3 and accumulates them in a microprocessor readable 24 bits saturating counter (up to 1 second accumulation time). Optionally, block line REI errors can be accumulated.

The RRMP extracts and filters the K1/K2 APS bytes for three frames. The filtered K1/K2 APS bytes are accessible through microprocessor readable registers. The RRMP also monitors the unfiltered K1/K2 APS bytes to detect APS byte failure (APSBF-L) defect, line alarm indication signal (AIS-L) defect and line remote defect indication (RDI-L) defect. APS byte failure is declared when 12 consecutive frames have been received where no three consecutive frames contain identical K1 bytes. The APS byte failure is removed upon detection of three consecutive frames containing identical K1 bytes. The detection of invalid APS codes must be done is done in software by polling the K1/K2 APS register. Line AIS is declared when the bit pattern 111 is observed in bits 6, 7, and 8 of the K2 byte for three or five consecutive frames. Line AIS is removed when any pattern other than 111 is observed for three or five consecutive frames. Line RDI is declared when the bit pattern 110 is observed in bits 6, 7, and 8 of the K2 byte for three or five consecutive frames. Line RDI is removed when any pattern other than 110 is observed for three or five consecutive frames.

The RRMP extracts and filters the synchronization status message (SSM) for eight frames. The filtered SSM is accessible through microprocessor readable registers.

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RRMP optionally inserts line alarm indication signal (AIS-L).

The RRMP extracts and serially outputs all the transport overhead (Used and Unused TOH) bytes on the RTOH port. The TOH bytes are output in the same order that they are received (A1, A2, J0/Z0, Unused, B1, E1, Unused, F1, D1-D3, H1-H3, B2, K1, K2, D4-D12, S1/Z1, Z2/M1/Z2 and E2). Figure 8 and Figure 9 show the transport overhead bytes on RTOH1-4 for the case where the SPECTRA-9953 is processing quad STS-48/STM-16 and STS-192/STM-64 streams. These figures do not show the multiplexing structure used to serially output the transport overhead on the RTOH port. Each processing RRMP extracts and outputs serially an STS-12/STM-4-worth of transport overhead. Four RRMPs transport overhead serial streams are multiplexed to generate an STS-48/STM-16 transport overhead. Refer to the Functional Timing section for a detailed description of the multiplexing structure. ROHCLK is the generated output clock used to provide timing for the RTOH port. ROHCLK is a nominal 82.94 MHz clock generated by gapping a 103.68 MHz clock. Sampling ROHFP high with the rising edge of ROHCLK identifies the MSB of the first A1 byte.

It should be noted that Figure 8 andFigure 9 use STS-1 ordering that is internal to SPECTRA-9953 and does not correspond exactly to the Bellcore STS-1 ordering found in Figure 7

Figure 8 STS-48 (STM-16) on RTOH 1-4

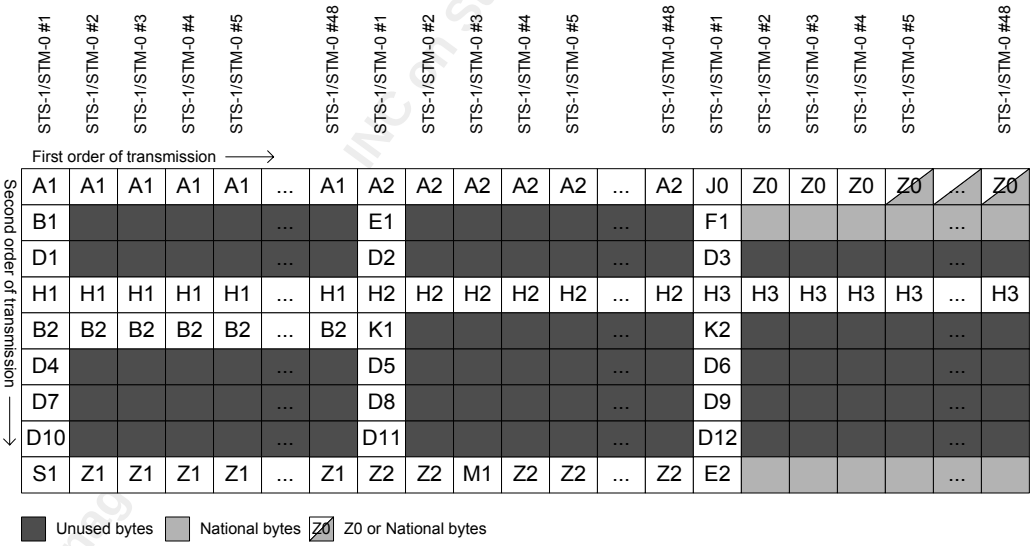

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Figure 9 STS-192 (STM-64) on RTOH1

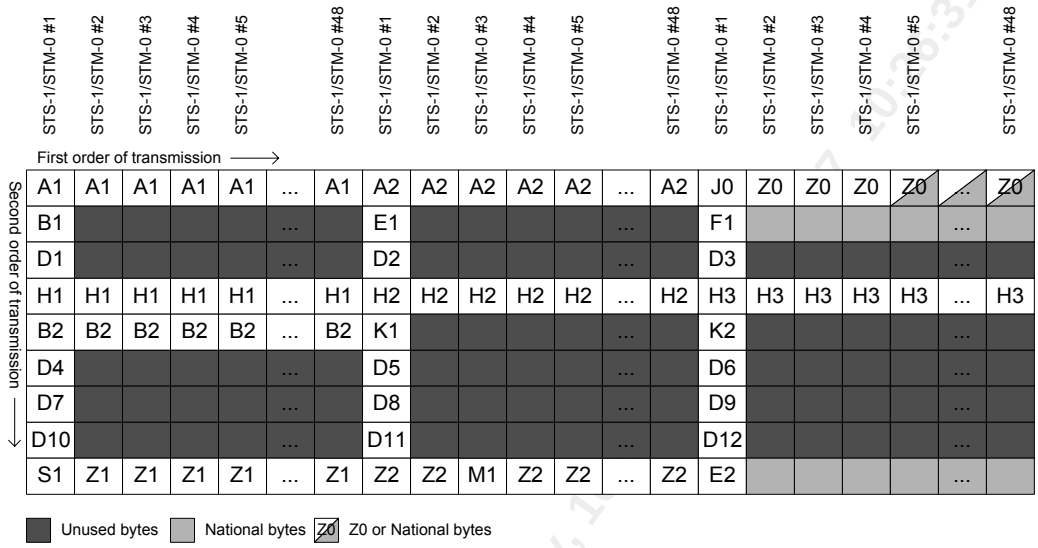
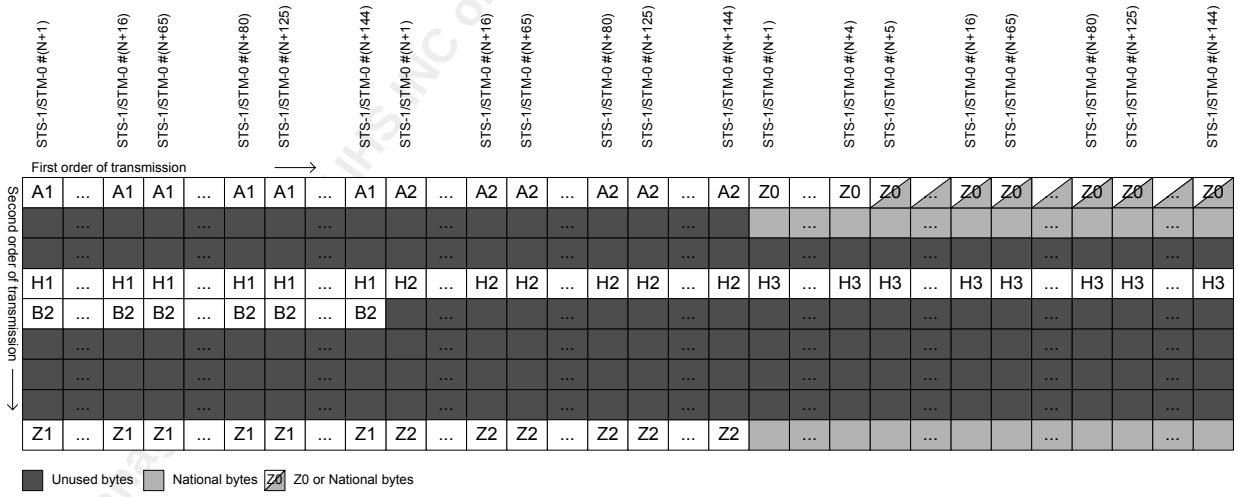


Figure 10 STS-192 (STM-64) on RTOH2-4



The RRMP serially outputs the line DCC bytes on the RLD and the RSLD ports. The line DCC bytes (D4-D12) are output on RLD. RSLD is selectable to output either the section DCC bytes (D1-D3) or the line DCC bytes (D4-D12). RLDCLK is the generated output clock used to provide timing for the RLD port. RLDCLK is a nominal 576 kHz clock. RSLDCLK is the generated output clock used to provide timing for the RSLD port. If RSLD carries the line DCC, RSLDCLK is a nominal 576 kHz clock or if RSLD carries the section DCC and RSLDCLK is a nominal 192 kHz clock. Sampling ROHFP high identifies the MSB of the first DCC byte on RLD (D4) and RSLD (D1 or D4).

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A maskable interrupt is activated to indicate any change in the status of OOF, LOF, LOS, line remote defect indication (RDI-L), line alarm indication signal (AIS-L), synchronization status message (COSSM), APS bytes (COAPS) and APS byte failure (APSBF) or any errors in section BIP-8, line BIP-8 and line remote error indication (REI-L).

The RRMP block provides de-scrambled data and frame alignment indication signals for use by the RHPP.

14.6 Receive Trail trace Processor (RTTP)

The Receive Trail trace Processor (RTTP) block monitors the trail trace messages of the receive data stream for trace identifier unstable (TIU) defect and trace identifier mismatch (TIM) defect. Three trail trace algorithms are defined. It is mandatory to select one of the algorithms for the RTTP to monitor the received message.

The first algorithm is Telcordia-compliant. The algorithm detects trace identifier mismatch (TIM) defect on a 16 or 64-byte trail trace message. A TIM defect is declared when none of the last 20 messages matches the expected message. A TIM defect is removed when 16 of the last 20 messages match the expected message. The expected trail trace message is a static message written in the expected page of the RTTP by an external microprocessor. Optionally, the expected message is matched when the trail trace message is all zeros.

The second algorithm is ITU compliant. The algorithm detects trace identifier unstable (TIU) defect and trace identifier mismatch (TIM) defect on a 16 or 64-byte trail trace message. The current trail trace message is stored in the captured page of the RTTP. If the length of the message is 16 bytes, the RTTP synchronizes on the MSB of the message. The byte with the MSB set high is placed in the first location of the captured page. If the length of the message is 64 bytes, the RTTP synchronizes on the CR/LF (CR = 0Dh, LF = 0Ah) characters of the message. The following byte is placed in the first location of the captured page.

A persistent trail trace message is declared when an identical message is received for three or five consecutive multi-frames (16 or 64 frames). A persistent message becomes the accepted message. The accepted message is stored in the accepted page of the RTTP. A TIU defect is declared when one or more erroneous bytes are detected in a total of eight messages without any persistent message in between. A TIU defect is removed when a persistent message is received.

A TIM defect is declared when the accepted message does not match the expected message. A TIM defect is removed when the accepted message matches the expected message. The expected message is a static message written in the expected page of the RTTP by an external microprocessor. Optionally, the algorithm declares a match trail trace message when the accepted message is all zeros.

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The third algorithm is not Telcordia/ITU-compliant. The algorithm detects trace identifier unstable (TIU) on a single continuous trail trace byte. A TIU defect is declared when one or more erroneous bytes are detected in three consecutive 16-byte windows. The first window starts on the first erroneous byte. A TIU defect is removed when an identical byte is received for 48 consecutive frames. A maskable interrupt is activated to indicate any change in the status of trace identifier unstable (TIU) and trace identifier mismatch (TIM).

14.7 Bit Error Monitor (SBER)

The SBER provides two independent bit error rate monitoring circuits (BERM block). They are used to monitor line bit error rate indicator (B2). One BERM block is dedicated to monitor the Signal Degrade (SD) alarm and the other BERM block dedicated to monitor the Signal Fail (SF) alarm. These alarms can then be used to control system level features such as Automatic Protection Switching (APS).

The BERM block uses a sliding window-based algorithm. This algorithm provides a much superior performance for detection, clearing and false detection than a simple jumping-window (resetable counter being polled at a regular interval) algorithm.

14.8 Receive High Order Path Processor (RHPP)

The Receive High Order Path Processor (RHPP) provides pointer interpretation, extraction of path overhead, extraction of the SPE (virtual container), and path level alarm and performance monitoring.

14.8.1 Pointer Interpreter

The pointer interpreter extracts and validates the H1 and H2 bytes in order to identify the location of the path overhead byte (J1) and all the SPEs of the constituent STS-1/3c/12c/48c/192c (VC3/4/4-4c/4-16c/4-64c) payloads. The pointer interpreter is a time multiplexed finite state machine that can process any mix of STS-1/3c/12c/(Nx12)c/ 48c/192c (AU3/4/4-4c/4-16c/4-64c) pointers. Within the pointer interpretation algorithm, three states are defined as shown below:

- NORM_state (NORM)
- AIS_state (AIS)
- LOP_state (LOP)

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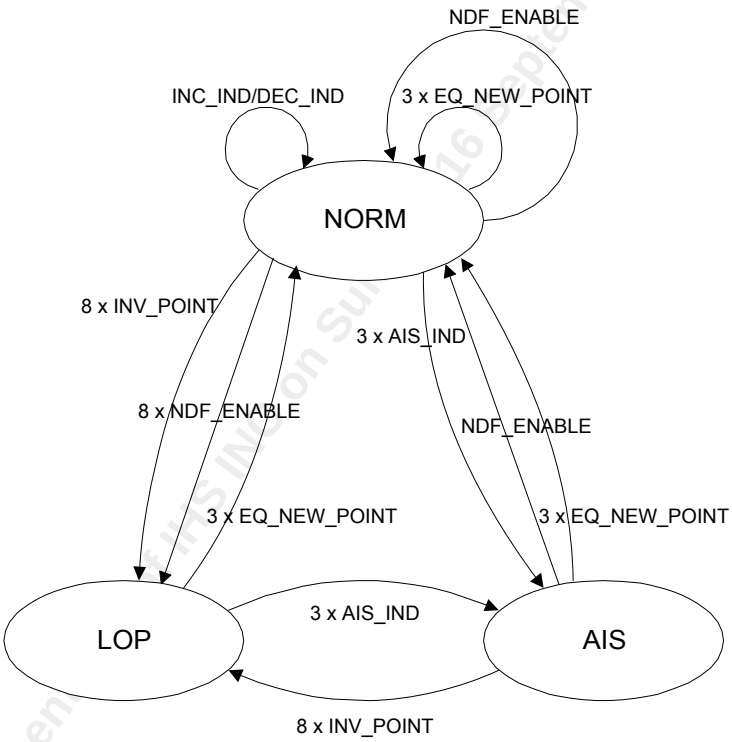
The transition between states will be consecutive events (indications), for example, three consecutive AIS indications to go from the NORM_state to the AIS_state. The kind and number of consecutive indications activating a transition is chosen such that the behavior is stable and insensitive to low BER. The only transition on a single event is the one from the AIS_state to the NORM_state after receiving a NDF enabled with a valid pointer value. Please note, since the algorithm only contains transitions based on consecutive indications, it is implied that, for example, non-consecutively received invalid indications do not activate the transitions to the LOP_state.

Figure 11 Pointer Interpretation State Diagram



The following events (indications) are defined:

NORM_POINT: Disabled NDF + ss + offset value equal to active offset.

NDF_ENABLE: Enabled NDF + ss + offset value in range of 0 to 782.

AIS_IND: H1 = FFh + H2 = FFh.

INC_IND: Disabled NDF + ss + majority of I bits inverted + no majority of D bits inverted + previous NDF_ENABLE, INC_IND or DEC_IND more than three frames ago.

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DEC_IND: Disabled NDF + ss + majority of D bits inverted + no majority of I bits inverted + previous NDF_ENABLE, INC_IND or DEC_IND more than three frames ago.

INV_POINT: Not any of the above (i.e.: not NORM_POINT, not NDF_ENABLE, not AIS_IND, not INC_IND and not DEC_IND).

NEW_POINT: Disabled NDF + ss + offset value in range of 0 to 782 but not equal to active offset.

Notes

1. Active offset is defined as the accepted current phase of the SPE (VC) in the NORM_state and is undefined in the other states.

13. Enabled NDF is defined as the following bit patterns: 1001, 0001, 1101, 1011 and 1000.

14. Disabled NDF is defined as the following bit patterns: 0110, 1110, 0010, 0100 and 0111.

15. The remaining six NDF bit patterns (0000, 0011, 0101, 1010, 1100, 1111) result in an INV_POINT indication.

16. ss bits are unspecified in SONET and have bit pattern 10 in SDH.

17. The use of ss bits in definition of indications may be optionally disabled.

18. The requirement for previous NDF_ENABLE, INC_IND or DEC_IND be more than 3 frames ago may be optionally disabled.

19. NEW_POINT is also an INV_POINT.

20. The requirement for the pointer to be within the range of 0 to 782 in 8 X NDF_ENABLE may be optionally disabled.

21. LOP is not declared if all the following conditions exist:
- the received pointer is out of range (>782),
- the received pointer is static,
- the received pointer can be interpreted, according to majority voting on the I and D bits, as a positive or negative justification indication, after making the requested justification, the received pointer continues to be interpretable as a pointer justification.
- When the received pointer returns to an in-range value, the SPECTRA-9953 will interpret it correctly.

The transitions indicated in the state diagram are defined as follows:

INC_IND/DEC_IND: Offset adjustment (increment or decrement indication)

3 x EQ_NEW_POINT: Three consecutive equal NEW_POINT indications

NDF_ENABLE: Single NDF_ENABLE indication

3 x AIS_IND: Three consecutive AIS indications

8 x INV_POINT: Eight consecutive INV_POINT indications

8 x NDF_ENABLE: Eight consecutive NDF_ENABLE indications

Notes

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1. The transitions from NORM_state to NORM_state do not represent state changes but imply offset changes.

22. 3 x EQ_NEW_POINT takes precedence over other events and may optionally reset the INV_POINT count.

23. All three offset values received in 3 x EQ_NEW_POINT must be identical.

24. "Consecutive event counters" are reset to zero on a change of state (except the INV_POINT counter).

LOP is declared on entry to the LOP_state after eight consecutive invalid pointers or eight consecutive NDF enabled indications. Path AIS is optionally inserted in the Drop bus when LOP is declared. The alarm condition is reported in the ring control port and is optionally returned to the source node by signaling the corresponding Transmit High Order Path Processor in the local SPECTRA-9953 device to insert a path RDI indication. Alternatively, if in-band error reporting is enabled, the path RDI bit in Drop bus G1 byte is set to indicate the LOP alarm to the THPP in a remote SPECTRA-9953.

PAIS is declared on entry to the AIS_state after three consecutive AIS indications. Path AIS is inserted in the Drop bus when AIS is declared. The alarm condition is reported in the ring control port and is optionally returned to the source node by signaling the corresponding Transmit High Order Path Processor in the local SPECTRA-9953 device to insert a path RDI indication. Alternatively, if in-band error reporting is enabled, the path RDI bit in Drop bus G1 byte is set to indicate the PAIS alarm to the THPP in a remote SPECTRA-9953.

14.8.2 Concatenation Pointer Interpreter State Machine

The concatenation pointer interpreter extracts and validates the H1 and H2 concatenation bytes. The concatenation pointer interpreter is a time multiplexed finite state machine that can process any mix of STS-1/3c/12c/48c/192c (AU3/4/4-4c/4-16c/4-64c) pointers. Within the pointer interpretation algorithm three states are defined as shown below.

- CONC_state (CONC)
- AISC_state (AISC)
- LOPC_state (LOPC)

The transitions between the states will be consecutive events (indications), for example, three consecutive AIS indications to go from the CONC_state to the AISC_state. The kind and number of consecutive indications activating a transition is chosen such that the behavior is stable and insensitive to low BER.

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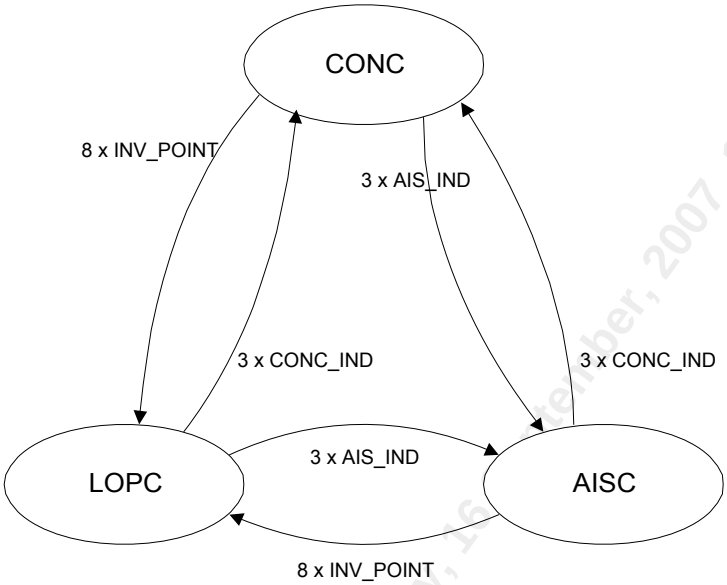
Figure 12 Concatenation Pointer Interpretation State Diagram



The following events (indications) are defined:

CONC_IND: Enabled NDF + dd + "1111111111"

AIS_IND: H1 = FFh + H2 = FFh

INV_POINT: Not any of the above (i.e.: not CONC_IND and not AIS_IND)

Notes

1. Enabled NDF is defined as the following bit patterns: 1001, 0001, 1101, 1011 and 1000.

25. The remaining eleven NDF bit patterns (0000, 0010, 0011, 0100, 0101, 0110, 0111, 1010, 1100, 1110, 1111) result in an INV_POINT indication.

26. dd bits are unspecified in SONET/SDH.

The transitions indicated in the state diagram are defined as follows:

3 X CONC_IND: Three consecutive CONC indications

3 x AIS_IND: Three consecutive AIS indications

8 x INV_POINT: Eight consecutive INV_POINT indications

Note

1. "Consecutive event counters" are reset to zero on a change of state.

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LOPC is declared on entry to the LOPC_state after eight consecutive pointers with values other than concatenation indications. Path AIS is optionally inserted in the Drop bus when LOPC is declared. The alarm condition is reported in the ring control port and is optionally returned to the source node by signaling the corresponding Transmit High Order Path Processor in the local SPECTRA-9953 device to insert a path RDI indication. Alternatively, if in-band error reporting is enabled, the path RDI bit in Drop bus G1 byte is set to indicate the LOP alarm to the THPP in a remote SPECTRA-9953 device.

PAISC is declared on entry to the AISC_state after three consecutive AIS indications. Path AIS is optionally inserted in the Drop bus when AISC is declared. The alarm condition reported in the ring control port and is optionally returned to the source node by signaling the corresponding Transmit High Order Path Processor in the local SPECTRA-9953 device to insert a path RDI indication. Alternatively, if in-band error reporting is enabled, the path RDI bit in Drop bus G1 byte is set to indicate the PAIS alarm to the THPP in a remote SPECTRA-9953 device.

14.8.3 Error Monitoring

The RHPP calculates the path BIP-8 error detection codes on the STS-1/3c/12c/48c/192c (VC-3/4/4-4c/4-16c/4-64c) payloads. When processing a VC-3 payload, the two fixed stuff columns can be excluded of the BIP-8 calculation if the FSBIPDIS register bit is set. The path BIP-8 code is based on a bit interleaved parity calculation using even parity. The calculated BIP-8 codes are compared with the BIP-8 codes extracted from the B3 byte of each constituent STS (VC) payload of the following frame. Any differences indicate a path BIP-8 error. The RHPP accumulates path BIP-8 errors in a microprocessor readable 16 bits saturating counter (up to 1 second accumulation time). Optionally, block BIP-8 errors can be accumulated.

The RHPP extracts the path remote error indication (REI-P) errors from bits 1, 2, 3 and 4 of the path status byte (G1) and accumulates them in a microprocessor readable 16 bits saturating counter (up to 1 second accumulation time). Optionally, block block REI errors can be accumulated.

The RHPP monitors the path signal label byte (C2) payload to validate change in the accepted path signal label (APSL). The same PSL byte must be received for three or five consecutive frames (selectable by the PSL5 bit in the configuration register) before being considered accepted.

The RHPP also monitors the path signal label byte (C2) to detect path payload label unstable (PLU-P) defect. A PSL unstable counter is increment every time the received PSL differs from the previously received PSL (an erroneous PSL will cause the counter to be increment twice, once when the erroneous PSL is received and once when the error free PSL is received). The PSL unstable counter is reset when the same PSL value is received for three or five consecutive frames (selectable by the PSL5 bit in the configuration register). PLU-P is declared when the PSL unstable counter reaches five. PLU-P is removed when the PSL unstable counter is reset.

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The RHPP also monitors the path signal label byte (C2) to detect path payload label mismatch (PLM-P) defect. PLM-P is declared when the accepted PSL does not match the expected PSL according to Table 6. PLM-P is removed when the accepted PSL match the expected PSL according to Table 6. The accepted PSL is the same PSL value received for three or five consecutive frames (selectable by the PSL5 bit in the configuration register). The expected PSL is a programmable PSL value.

The RHPP also monitors the path signal label byte (C2) to detect path unequipped (UNEQ-P) defect. UNEQ-P is declared when the accepted PSL is 00H and the expected PSL is not 00H. UNEQ-P is removed when the accepted PSL is not 00H or when the accepted PSL is 00H and the expected PSL is 00H. The accepted PSL is the same PSL value received for three or five consecutive frames (selectable by the PSL5 bit in the configuration register). The expected PSL is a register programmable PSL value.

The RHPP also monitors the path signal label byte (C2) to detect path payload defect indication (PDI-P) defect. PDI-P is declared when the accepted PSL is a PDI defect that matches the expected PDI defect. PPDI is removed when the accepted PSL is not a PDI defect or when the accepted PSL is a PDI defect that does not match the expected PDI defect. The accepted PSL is the same PSL value received for three or five consecutive frames (selectable by the PSL5 bit in the configuration register). Table 7 gives the expected PDI defect based on the programmable PDI and PDI range register values.

Table 6 PLM-P, UNEQ-P and PDI-P Defects Declaration

Expected PSL		Accepted PSL			PLM-P	UNEQ-P	PDI-P
00	Unequipped	00	Unequipped		Match	Inactive	Inactive
		01	Equipped non specific		Mismatch	Inactive	Inactive
		02-E0 FD-FF	Equipped specific		Mismatch	Inactive	Inactive
		E1-FC	PDI	=expPDI	Mismatch	Inactive	Active
				!=expPDI	Mismatch	Inactive	Inactive
01	Equipped non specific	00	Unequipped		Mismatch	Active	Inactive
		01	Equipped non specific		Match	Inactive	Inactive
		02-E0 FD-FF	Equipped specific		Match	Inactive	Inactive
		E1-FC	PDI	=expPDI	Match	Inactive	Active
				!=expPDI	Mismatch	Inactive	Inactive
02-FF	Equipped specific PDI	00	Unequipped		Mismatch	Active	Inactive
		01	Equipped non specific		Match	Inactive	Inactive
		02-E0 FD-FF	Equipped specific	= expPSL	Match	Inactive	Inactive
				!=expPSL	Mismatch	Inactive	Inactive
		E1-FC	PDI	=expPDI	Match	Inactive	Active
				!=expPDI	Mismatch	Inactive	Inactive

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Table 7 Expected PDI Defects Based on PDI and PDI Range Values

PDI register value	DPI range register value	Exp PDI	PDI register value	DPI range register value	Exp PDI
00000	Disable	None	01111	Disable	EF
	Enable			Enable	E1-EF
00001	Disable	E1	10000	Disable	F0
	Enable	E1-E1		Enable	E1-F0
00010	Disable	E2	10001	Disable	F1
	Enable	E1-E2		Enable	E1-F1
00011	Disable	E3	10010	Disable	F2
	Enable	E1-E3		Enable	E1-F2
00100	Disable	E4	10011	Disable	F3
	Enable	E1-E4		Enable	E1-F3
00101	Disable	E5	10100	Disable	F4
	Enable	E1-E5		Enable	E1-F4
00110	Disable	E6	10101	Disable	F5
	Enable	E1-E6		Enable	E1-F5
00111	Disable	E7	10110	Disable	F6
	Enable	E1-E7		Enable	E1-F6
01000	Disable	E8	10111	Disable	F7
	Enable	E1-E8		Enable	E1-F7
01001	Disable	E9	11000	Disable	F8
	Enable	E1-E9		Enable	E1-F8
01010	Disable	EA	11001	Disable	F9
	Enable	E1-EA		Enable	E1-F9
01011	Disable	EB	11010	Disable	FA
	Enable	E1-EB		Enable	E1-FA
01100	Disable	EC	11011	Disable	FB
	Enable	E1-EC		Enable	E1-FB
01101	Disable	ED	11100	Disable	FC
	Enable	E1-ED		Enable	E1-FC
01110	Disable	EE			
	Enable	E1-EE			

The RHPP monitors bits 5, 6 and 7 of the path status byte (G1) to detect path remote defect indication (RDI-P) and path enhanced remote defect indication (ERDI-P) defects.

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RDI-P is declared when bit 5 of the G1 byte is set high for five or ten consecutive frames (selectable by the PRDI10 bit in the configuration register). RDI-P is removed when bit 5 of the G1 byte is set low for five or ten consecutive frames. ERDI-P is declared when the same 010, 100, 101, 110 or 111 pattern is detected in bits 5, 6 and 7 of the G1 byte for five or ten consecutive frames (selectable by the PRDI10 bit in the configuration register). ERDI-P is removed when the same 000, 001 or 011 pattern is detected in bits 5, 6 and 7 of the G1 byte for five or ten consecutive frames.

14.9 SONET/SDH Alarm Reporting Controller (SARC)

The SARC receives all the section, line and path defects detected by the receive overhead processors and, according to the user's specific configuration, generates consequent action indications.

Receive section alarm (RSALM) indication: RSALM is asserted when a OOF, LOF, LOS. AIS-L, RDI-L, APSBF, TIU-S, TIM-S, SDBER or SFBER defect is detected in the receive data stream. Configuration registers allow the user to remove any defect from the previous enumeration.

Receive line AIS insertion (RLAISINS) indication: RLAISINS is asserted when a OOF, LOF, LOS. AIS-L, RDI-L, APSBF, TIU-S, TIM-S, SDBER or SFBER defect is detected in the receive data stream. Configuration register allow the user to enable/disable any defect from the previous enumeration.

Transmit line RDI insertion (TLRDIINS) indication: TLRDIINS is asserted when a OOF, LOF, LOS. AIS-L, RDI-L, APSBF, TIU-S, TIM-S, SDBER or SFBER defect is detected in the receive data stream. Configuration register allow the user to enable/disable any defect from the previous enumeration.

Receive path alarm (RPALM) indication: RPALM is asserted when a RSALM, MSRSALM[3], AIS-P, LOP-P, PLU-P. PLM-P, UNEQ-P, PDI-P, RDI-P, ERDI-P, TIU-P or TIM-P defect is detected in the receive data stream. Configuration registers allow the user to enable/disable any defect from the previous enumeration.

Receive path alarm insertion (RPAISINS) indication: RPAISINS is asserted when a RLAISINS, MSRLAISINS[4], AIS-P, LOP-P, PLU-P. PLM-P, UNEQ-P, PDI-P, RDI-P, ERDI-P, TIU-P or TIM-P defect is detected in the receive data stream. Configuration registers allow the user to enable/disable any defect from the previous enumeration.

[3] MSRSALM is asserted by the master SARC when processing an STS-192/STM-64 data stream to indicate a section alarm. This alarm is propagated to the slave SARCs.

[4] MSRLAISINS is asserted by the master SARC when processing an STS-192/STM-64 data stream to indicate a line alarm. This alarm is propagated to the slave SARCs.

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Transmit path ERDI insertion (TPERDIINS[2:0]) indication: TPERDIINS[2:0] is updated when a PLU-P, PLM-P, TIU-P, TIM-P, UNEQ-P, LOP-P or a AIS-P defect is detected in the receive data stream. Configuration register allow the user to enable/disable any defect from the previous enumeration.

In some applications, the receive overhead processor and the transmit overhead processor do not reside on the same device. The receive defects are returned to the far end through a ring control port (RCP). The SARC inserts all the section, line and path defects detected in the local receive data stream into the receive RCP output port. The SARC extracts the APS, line RDI, line REI, path ERDI and path REI defects to be inserted in the local transmit data stream from the transmit RCP input port. The RCP port is a low speed asynchronous serial interface operating at 20.736 MHz. The defects carried by the RRCP port is show in table

When the RCP port is enabled, the APS, line RDI, line REI, path ERDI and path REI defect indications to be inserted in the transmit data stream are extracted from the RCP port. When the RCP port is disabled, the defect indications to be inserted in the transmit data stream are derived from the defects detected in the receive data stream.

Table 8 Ring Control Port Bit Definition

Bit Position	Type	RRCPDAT Defect
0	Section	OOF
1	Section	LOF
2	Section	LOS
3	Section	LAIS
4	Section	LRDI
5	Section	APSBF
6	Section	STIU
7	Section	STIM
8	Section	SDBER
9	Section	SFBER
10-11	Section	00
12-15	Section	0
16-23	Section	LBIPCNT[7:0]
24-39	Section	APS[15:0]
40	Section	LRDIINS
41-47	Section	0
48	Path 1	PLOPTR
49	Path 1	PAISPTR
50	Path 1	PPLU
51	Path 1	PPLM
52	Path 1	PUNEQ
53	Path 1	PPDI
54	Path 1	PRDI

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Bit Position	Type	RRCPDAT Defect
55	Path 1	PERDI
56-58	Path 1	PERDIV[2:0]
59	Path 1	PTIU
60	Path 1	PTIM
61-62	Path 1	00
63	Path 1	0
64-67	Path 1	PBIPCNT[3:0]
68-70	Path 1	PERDIINS[2:0]
71	Path 1	0
72-95	Path 2	PLOPTR .. PERDIINS[2:0]
...	...	...
1176-1199	Path 48	PLOPTR .. PERDIINS[2:0]
1200-1223	Path 1	PLOPTR .. PERDIINS[2:0]
...	...	...
2328-2351	Path 48	PLOPTR .. PERDIINS[2:0]
2352-2591	None	0

14.10 SONET/SDH Transmit Line Interface (STLI)

The SONET/SDH transmit line interface block properly formats the outgoing STS-192/STM-64 or four STS-48/STM-16 data streams.

In single STS-192/STM-64 mode, the STLI supports a 16-bit 622.02 MHz LVDS line side interface for direct connection to external clock recovery, clock synthesis and serializer-deserializer components. In quad STS-48/STM-4 mode, the STLI supports four independent 4-bit 622.02 MHz LVDS line side interface for direct connection to external clock recovery, clock synthesis, and serializer-deserializer components.

14.11 Transmit Regenerator Multiplexer Processor (TRMP)

The Transmit Regenerator and Multiplexer Processor (TRMP) block inserts the transport overhead bytes in the transmit data stream.

The TRMP accumulates the line BIP-8 errors detected by the RRMP during the last receive frame. The line BIP-8 errors are returned to the far end as line remote error indication (REI-L) during the next transmit frame. Because the RRMP and the TRMP are in two different clock domains, none, one, or two line BIP-8 errors can be accumulated per transmit frame. The minimum value between the maximum REI-L given in Table 9 and the accumulator count is returned as the line REI-L in the M1 byte of STS-1 (STM-0) #3. Optionally, block BIP-24 errors can be accumulated.

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The TRMP serially inputs all the transport overhead (TOH) bytes from the TTOH port. The TOH bytes must be input in the same order that they are transmitted (A1, A2, J0/Z0, B1, E1, F1, D1-D3, H1-H3, B2, K1, K2, D4-D12, S1/Z1, Z2/M1/Z2 and E2). Figure 13 and Figure 14 show the transport overhead bytes on TTOH1-4 for the case where the SPECTRA-9953 is processing a QUAD STS-48/STM-16 and an STS-192/STM-64 streams. These figures do not show the multiplexing structure used to serially insert the transport overhead on the TTOH port. Each processing TRMP inserts serially an STS-12/STM-4 worth of transport overhead. Each TTOH port carries an STS-48/STM-16 worth of transport overhead. This stream is de-multiplexed to feed four RRMP processing slices. Refer to the Functional Timing section for a detailed description of the multiplexing structure. TTOHCLK is the generated output clock used to provide timing for the TTOH port. TTOHCLK is a nominal 82.94 MHz clock generated by gapping a 103.68 MHz clock. Sampling TTOHFP high with the rising edge of TTOHCLK identifies the MSB of the first A1 byte. TTOHEN port is used to validate the byte insertion on a byte per byte basis. When TTOHEN is sampled high on the MSB of the serial byte, the serial byte is inserted. When TTOHEN is sampled low on the MSB of the serial byte, the serial byte is discarded.

Table 9 Maximum Line REI Errors Per Transmit Frame

SONET/SDH	Maximum single BIP-8 errors LREIBLK=0	Maximum block BIP-24 errors LREIBLK=1
STS-3/STM-1	0001 1000	0000 0001
STS-12/STM-4	0110 0000	0000 0100
STS-48/STM-16	1111 1111	0001 0000
STS-192/STM-64	1111 1111	0100 0000

Figure 13 STS-48 (STM-16) on TTOH 1-4

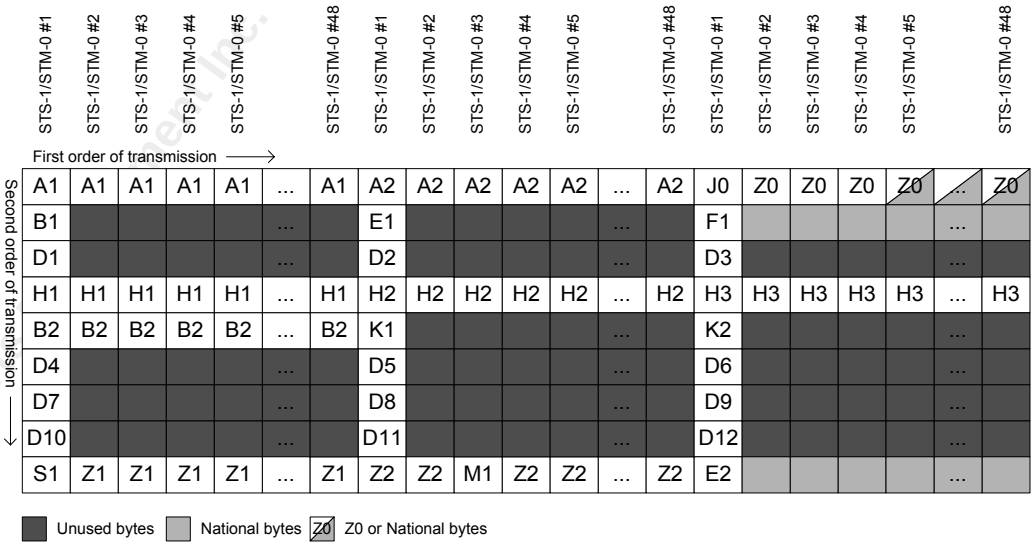

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Figure 14 STS-192 (STM-64) on TTOH1

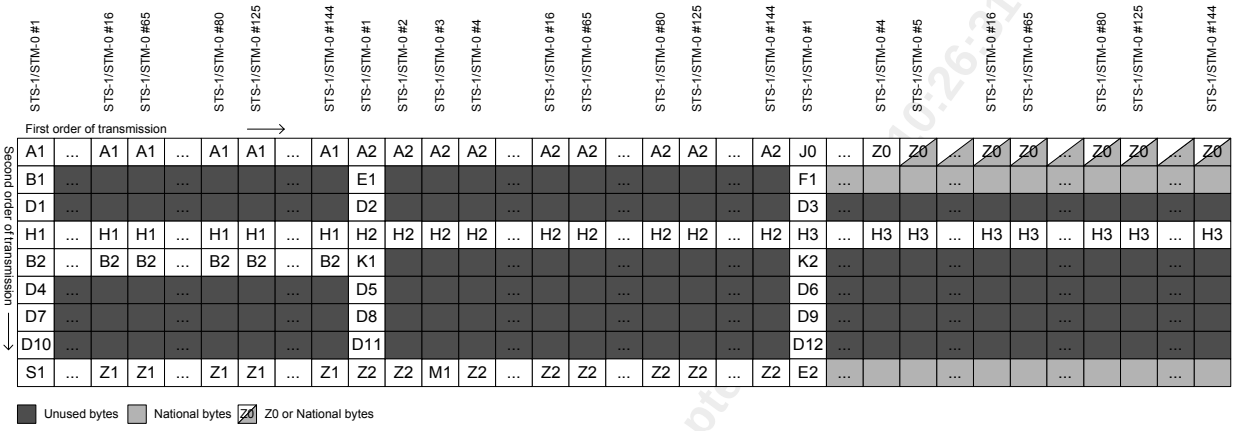
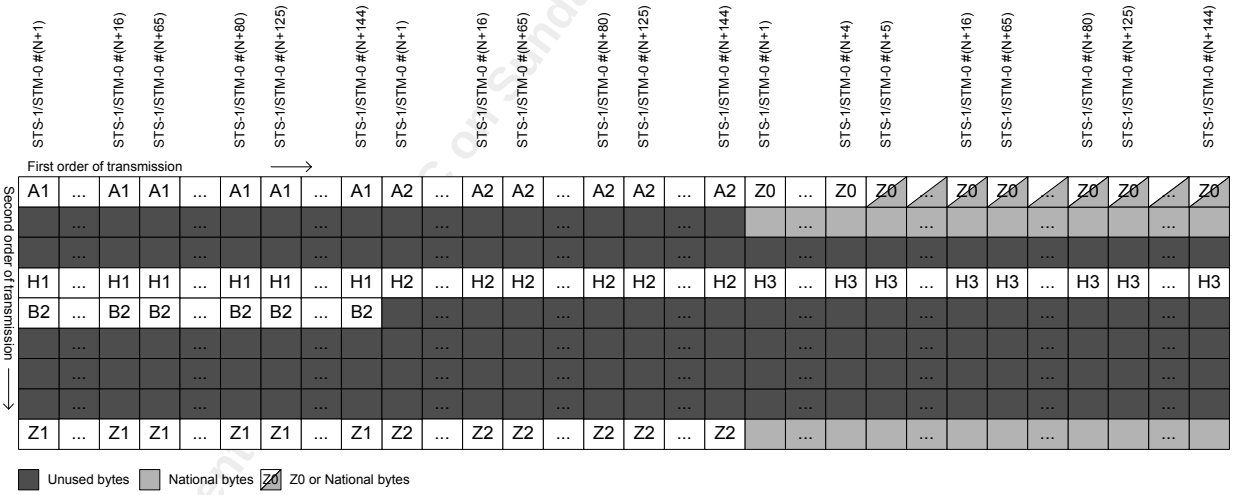


Figure 15 STS-192 (STM-64) on TTOH2-4



The TRMP serially inputs the line DCC bytes from the TLD and the TSLD ports. The line DCC bytes (D4-D12) are input from TLD. TSLD is selectable to input either the section DCC bytes (D4-D12) or the line DCC bytes (D1-D3). TLDCLK is the generated output clock used to provide timing for the TLD port. TLDCLK is a nominal 576 kHz clock. TSLDCLK is the generated output clock used to provide timing for the TSLD port. If TSLD carries the line DCC, TSLDCLK is a nominal 576 kHz clock or if TSLD carries the section DCC, TSLDCLK is a nominal 192 kHz clock. Sampling TTOHFP high identifies the MSB of the first DCC byte on TLD (D4) and TSLD (D1 or D4).

The TRMP also inserts most of the transport overhead bytes from internal registers. Since there is multiple sources for the same overhead byte, the TOH bytes must be prioritized according to Table 10 before being inserted into the data stream.

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The Z0DEF register bit defines the Z0/NATIONAL growth bytes for row #1. When Z0DEF is set to logic one, the Z0/NATIONAL bytes are defined according to ITU. When Z0DEF is set to logic zero, the Z0/NATIONAL bytes are defined according to Telcordia.

Table 10 TOH Insertion Priority

BYTE	HIGHEST Priority						LOWEST Priority
A1		76h (A1ERR=1)	F6h (A1A2EN=1)	TTOH (TTOHEN=1)			A1 pass through
A2			28h (A1A2EN=1)	TTOH (TTOHEN=1)			A2 pass through
J0	STS-1/STM-0 # (J0Z0INCEN=1)	J0[7:0] (TRACEEN=1)	J0V (J0REGEN=1)	TTOH (TTOHEN=1)			J0 pass through
Z0	STS-1/STM-0 # (J0Z0INCEN=1)		Z0V (Z0REGEN=1)	TTOH (TTOHEN=1)			Z0 pass through
B1				Calculated B1 xor TTOH (TTOHEN=1 & B1MASKEN=1) TTOH (TTOHEN=1 & B1MASKEN=0)			Calculated B1 xor B1MASK
E1			E1V (E1REGEN=1)	TTOH (TTOHEN=1)			E1 pass through
F1			F1V (F1REGEN=1)	TTOH (TTOHEN=1)			F1 pass through
D1-D3			D1D3V (D1D3REGEN=1)	TTOH (TTOHEN=1)	TSLD (TSLDSEL=0 & TSLDEN=1)		D1-D3 pass through
H1				H1 pass through xor TTOH (TTOHEN=1 & HMASKEN=1)			H1 pass through xor H1MASK

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BYTE	HIGHEST Priority						LOWEST Priority
				TTOH (TTOHEN=1 & HMASKEN=0)			
H2				H2 pass through xor TTOH (TTOHEN=1 & HMASKEN=1)			H2 pass through xor H2MASK
				TTOH (TTOHEN=1 & HMASKEN=0)			
H3				TTOH (TTOHEN=1)			H3 pass through
B2				Calculated B2 xor TTOH (TTOHEN=1 & B2MASKEN=1)			Calculated B2 xor B2MASK
				TTOH (TTOHEN=1 & B2MASKEN=0)			
K1		APS[15:8] (APSEN=1)	K1V (K1K2REGEN=1)	TTOH (TTOHEN=1)			K1 pass through
K2		APS[7:0] (APSEN=1)	K2V (K1K2REGEN=1)	TTOH (TTOHEN=1)			K2 pass through
D4-D12			D4D12V (D4D12REGEN=1)	TTOH (TTOHEN=1)	TSLD (TSLDSEL=1 & TSLDEN=1)	TLD (TLDEN=1)	D4-D12 pass through
S1			S1V (S1REGEN=1)	TTOH (TTOHEN=1)			S1 pass through
Z1			Z1V (Z1REGEN=1)	TTOH (TTOHEN=1)			Z1 pass through
Z2			Z2V (Z2REGEN=	TTOH (TTOHEN=			Z2 pass through

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BYTE	HIGHEST Priority						LOWEST Priority
			1)	1)			
M1			LREI[7:0] (LREIEN=1)	TTOH (TTOHEN= 1)			M1 pass through
E2			E2V (E2REGEN= 1)	TTOH (TTOHEN= 1)			E2 pass through
National			NATIONALV (NATIONAL EN=1)	TTOH (TTOHEN= 1)			National pass through
Unused			UNUSEDV (UNUSEDEN =1)	TTOH (TTOHEN= 1)			Unused pass through
PLD							PLD pass through

Table 11 Definition of Z0/National Growth Bytes for Row #1

TRMP Mode	Type	Z0DEF = 1	Z0DEF = 0
STS-3/STM-1	Z0	None	From STS-1/STM-0 #2 to #3
	National	From STS-1/STM-0 #2 to #3	None
STS-48/STM-4 master mode	Z0	From STS-1/STM-0 #2 to #4	From STS-1/STM-0 #2 to #12
	National	From STS-1/STM-0 #5 to #12	None
STS-192/STM-64 slave mode	Z0	From STS-1/STM-0 #1 to #4	From STS-1/STM-0 #1 to #12
	National	From STS-1/STM-0 #5 to #12	None

The H1, H2, B1 and B2 bytes input from the TTOH port are inserted or are used as a mask to toggle bits in the corresponding H1, H2, B1 and B2 bytes depending on the HMASK B1MASK and B2MASK register bits. When the HMASK, B1MASK or B2MASK register bit is set low and TTOHEN is sampled high on the MSB of the serial H1, H2, B1 or B2 byte, the serial byte is inserted in place of the corresponding byte. When the HMASK, B1MASK or B2MASK register bit is set high and TTOHEN is sampled high on the MSB of the serial H1, H2, B1 or B2 byte, the serial byte is XOR'd with the corresponding path payload pointer (already in the data stream) or the calculated BIP-8 byte before being inserted.

The TRMP inserts the APS bytes detected by the RRMP during the last receive frame. The APS bytes are returned to the far end by the TRMP during the next transmit frame. Because the RRMP and the TRMP are in two different clock domains, two, one, or no APS bytes can be sampled per transmit frame. The last received APS bytes are transmitted.

The TRMP inserts the line remote defect indication (RDI-L) into the data stream. When line RDI is inserted, the 110 pattern is inserted in bits 6, 7 and 8 of the K2 byte of STS-1 (STM-0) #1. Line RDI insertion has priority over TOH byte insertion. The TRMP also inserts the line alarm indication signal (AIS-L) into the data stream. When line AIS must be inserted, all ones are inserted in the line overhead and in the payload (all bytes of the frame except the section overhead bytes). Line AIS insertion has priority over line RDI insertion and TOH byte insertion.

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The TRMP calculates the line BIP-8 error detection codes on the transmit data stream. One line BIP-8 error detection code is calculated for each of the constituent STS-1 (STM-0). The line BIP-8 byte is calculated on the unscrambled bytes of the STS-1 (STM-0) except for the 9 SOH bytes. The line BIP-8 byte is based on a bit interleaved parity calculation using even parity. For each STS-1 (STM-0), the calculated BIP-8 error detection code is inserted in the B2 byte of the following frame before scrambling.

The TRMP optionally scrambles the transmit data stream.

The TRMP calculates the section BIP-8 error detection code on the transmit data stream. The section BIP-8 byte is calculated on the scrambled bytes of the complete frame. The section BIP-8 byte is based on a bit interleaved parity calculation using even parity. The calculated BIP-8 error detection code is inserted in the B1 byte of STS-1 (STM-0) #1 of the following frame before scrambling.

14.12 Transmit Trail trace Processor (TTTP)

The Transmit Trail trace Processor (TTTP) block generates the trail trace messages to be transmitted. The TTTP can generate a 16 or 64-byte trail trace message. The message is sourced from an internal RAM and must have been previously written by an external microprocessor. Optionally, the trail trace message can be reduced to a single continuous trail trace byte.

The trail trace message must include synchronization because the TTTP does not add synchronization. The synchronization mechanism is different for a 16-byte message and for a 64- byte message. When the message is 16 bytes, the synchronization is based on the MSB of the trail trace byte. Only for one of the 16 bytes is MSB set high. The byte with its MSB set high is considered the first byte of the message. When the message is 64 bytes, the synchronization is based on the CR/LF (CR = 0Dh, LF = 0Ah) characters of trail trace message. The byte following the CR/LF bytes is considered the first byte of the message.

To avoid generating an unstable/mismatch message, the TTTP forces the message to all zeros while the microprocessor updates the internal RAM.

14.13 Transmit High Order Path Processor (THPP)

The Transmit High Order Path Processor (THPP) block inserts the path overhead bytes in the transmit data stream. Path overhead bytes can be sourced from different possible sources. All overhead bytes may optionally be passed-through the THPP.

The path overhead bytes can be sourced from internal registers. There are 8 bits in the THPP Source & Pointer Control Register (TSPCR) that are used in determining the origin of path overhead bytes. They are SRCJ1, SRCC2, SRCG1, SRCF2, SRCH4, SRCZ3, SRCZ4, and SRCZ5.

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The THPP calculates the path BIP-8 error detection code on the transmit data stream. The path BIP-8 byte is calculated on all the payload bytes. The path BIP-8 byte is based on a bit interleaved parity calculation using even parity. The calculated BIP-8 error detection code is optionaly inserted in the B3 byte of the following frame. The path trace byte (J1) can be optionally sourced from the Transmit Path Trace Buffer.

The THPP accumulates the path BIP-8 errors detected by the RHPP during the last receive frame. The path BIP-8 errors are optionally returned to the far end as path remote error indication (REI-P : G1 Bytes) during the next transmit frame. Because the RHPP and the THPP are in two different clock domains, two, one or no path BIP-8 errors can be accumulated per transmit frame. The minimum value between the maximum REI-P and the accumulator count is returned as the path REI in the G1 byte. Optionally, block BIP-8 errors can be accumulated. T gives the source priority for each overhead byte.

Table 12 Path Overhead Byte Source Priority

Byte	Highest Priority					Lowest Priority
J1	UNEQV (UNEQ=1)	J1 pass through (TDIS=1 OR PAIS=1)	Path trace buffer (PTBJ1=1)	J1 ind. reg. (SRCJ1=1)		J1 pass through
B3	UNEQV (UNEQ=1)	B3 pass through (TDIS=1 OR PAIS=1)			Calculated B3	Calculated B3 XOR B3MASK
C2	UNEQV (UNEQ=1)	C2 pass through (TDIS=1 OR PAIS=1)	C2 ind. reg. (SRCC2=1)			C2 pass through
G1	UNEQV (UNEQ=1)	G1 pass through (TDIS=1 OR PAIS=1 OR IBER=1)	PRDI[2:0] and PREI[3:0] (ENG1REC=1)	G1 ind. reg. (SRCG1=1)		G1 pass through
F2	UNEQV (UNEQ=1)	F2 pass through (TDIS=1 OR PAIS=1)	F2 ind. reg. (SRCF2=1)			F2 pass through
H4	UNEQV (UNEQ=1)	H4 pass through (TDIS=1 OR PAIS=1)	H4 pass through XOR H4 ind. reg. (SRCH4=1 AND	H4 ind. reg. (SRCH4=1)	H4 pass through	H4 pass through

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Byte	Highest Priority					Lowest Priority
			ENH4MASK=1)			
Z3	UNEQV (UNEQ=1)	Z3 pass through (TDIS=1 OR PAIS=1)	Z3 ind. reg. (SRCZ3=1)			Z3 pass through
Z4	UNEQV (UNEQ=1)	Z4 pass through (TDIS=1 OR PAIS=1)	Z4 ind. reg. (SRCZ4=1)			Z4 pass through
Z5	UNEQV (UNEQ=1)	Z5 pass through (TDIS=1 OR PAIS=1)	Z5 ind. reg. (SRCZ5=1)			Z5 pass through

14.14 SONET/SDH High-order Pointer Interpreter (SHPI)

The SONET/SDH High-order Pointer Interpreter (SHPI) block is analogous to the RHPP block on the receive line side of the SPECTRA-9953. These blocks perform pointer processing by identifying the location of the H1 and H2 bytes for any given STS-1/3c/12c/48c/192c (AU3/4/4-4c/4-16c/4-64c) paths, and interpret the values in these bytes to locate the J1 path overhead byte, and therefore the start of the path's SPE. The SHPI also detects path alarm conditions.

The SHPI block allows the ADD TelecomBus of the SPECTRA-9953 to accommodate two methods of locating the SPE for a given STS-1/AU-3 path. One method is to mark the location of the J1 byte with a special control character (refer to telecom bus encoder and decoder blocks). This is accomplished when the SPECTRA-9953 or other serial TelecomBus devices are configured for HPT mode (via the TMODE[1:0] bits in the T8TE Time-slot Configuration #1 and #2 registers for the SPECTRA-9953). With this mode, the SHPI can be bypassed and the J1 control character will indicate where the start of the SPE is for each STS-1/AU-3 path. The other method is for the SHPI to perform pointer processing on the H1 and H2 bytes for each STS-1/AU-3 path to locate the start of the SPE. This is required to support devices that cannot provide the J1 control character.

14.15 SONET/SDH Virtual Container Aligner (SVCA)

The SONET/SDH Virtual Container Aligner (SVCA) block aligns the payload data from an incoming SONET/SDH data stream to a new transport frame reference. The alignment is accomplished by recalculating the STS (AU) payload pointer value based on the offset between the transport overhead of the incoming data stream and that of the outgoing data stream.

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Frequency offsets due, for example, to plesiochronous network boundaries, or the loss of a primary reference timing source, and phase differences, due to normal network operation, between the incoming data stream and the outgoing data stream are accommodated by pointer adjustments in the outgoing data stream.

The SVCA also terminates the transport overhead. All the transport overhead bytes are set to "00H" except A1,A2,H1,H2 and H3 bytes.

14.15.1 Elastic Store

The Elastic Store performs rate adaptation between the line side interface and the system side interface. The entire incoming payload, including path overhead bytes, is written into a first-in-first-out (FIFO) buffer at the incoming byte rate. Each FIFO word stores a payload data byte and a one bit tag labeling the J1 byte. Incoming pointer justifications are accommodated by writing into the FIFO during the negative stuff opportunity byte or by not writing during the positive stuff opportunity byte. Data is read out of the FIFO in the Elastic Store block at the outgoing byte rate by the Pointer Generator. Analogously, outgoing pointer justifications are accommodated by reading from the FIFO during the negative stuff opportunity byte or by not reading during the positive stuff opportunity byte.

After coming out of AIS, the SVCA may output one erroneous NDF indication. This is due to several non-deterministic factors after coming out of AIS such as FIFO fill levels and FIFO J1 content. After the one possibly incorrect NDF indication, another NDF is issued and all subsequent pointers and J1 indications are correct. Much of the same situation can occur when reframing. Depending of the FIFO contents, the first J1 indication coming out of the SVCA after reframing might take longer than one frame, but not longer than two frames. If there is constant reframing, and the new pointer is continually less then the previous pointer, then the SVCA can go multiple frames without a J1 indication. However, the H1/H2 values will always be correct.

The FIFO read and write addresses are monitored. Pointer justification requests will be made to the Pointer Generator based on the proximity of the addresses relative to programmable thresholds. The Pointer Generator schedules a pointer increment event if the FIFO depth is below the lower threshold and a pointer decrement event if the depth is above the upper threshold. FIFO underflow and overflow events are detected and path AIS is optionally inserted in the outgoing data stream for three frames to alert downstream elements of data corruption.

Pointer Generator

The Pointer Generator generates the H1 and H2 bytes in order to identify the location of the path overhead byte (J1) and all the SPE bytes of the constituent STS-1/3c/12c/48c/192c (VC3/4/4-4c/4-16c/4-64c) payloads. The pointer generator is a time multiplexed finite state machine that can process any mix of STS-1/3c/12c/48c/192c (AU3/4/4-4c/4-16c/4-64c) pointers. Within the pointer generator algorithm, five states are defined as shown below:

- NORM_state (NORM)
- AIS_state (AIS)

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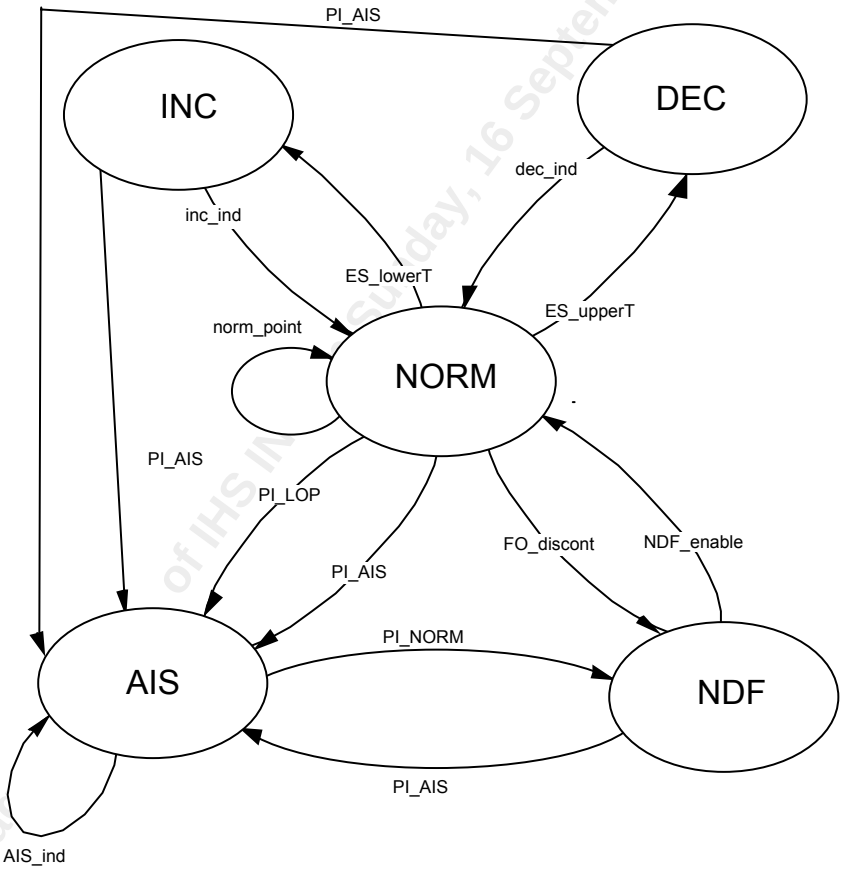
- NDF_state (NDF)
- INC_state (INC)
- DEC_state (DEC)

The transition from the NORM to the INC, DEC, and NDF states are initiated by events in the Elastic Store (ES) block. The transition to/from the AIS state are controlled by the pointer interpreter (PI) in the Receive High Order Path Processor block. The transitions from INC, DEC, and NDF states to the NORM state occur autonomously with the generation of special pointer patterns.

Figure 16 Pointer Generation State Diagram



The following events, indicated in the state diagram, are defined:

ES_lowerT: ES filling is below the lower threshold + previous inc_ind, dec_ind or NDF_enable more than three frames ago.

ES_upperT: ES filling is above the upper threshold + previous inc_ind, dec_ind or NDF_enable more than three frames ago.

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FO_discont: Frame offset discontinuity

PI_AIS: PI in AIS state

PI_LOP: PI in LOP state

PI_NORM: PI in NORM state

Note

1. A frame offset discontinuity occurs if an incoming NDF enabled is received, or if an ES overflow/underflow occurred.

The autonomous transitions indicated in the state diagram are defined as follows:

inc_ind: Transmit the pointer with NDF disabled and inverted I bits, transmit a stuff byte in the byte after H3, increment active offset.

dec_ind: Transmit the pointer with NDF disabled and inverted D bits, transmit a data byte in the H3 byte, decrement active offset.

NDF_enable: Accept new offset as active offset, transmit the pointer with NDF enabled and new offset.

norm_point: Transmit the pointer with NDF disabled and active offset.

AIS_ind: Active offset is undefined, transmit an all-1's pointer and payload.

Notes

1. Active offset is defined as the phase of the SPE (VC).
27. The ss bits are undefined in SONET, and has bit pattern 10 in SDH
28. Enabled NDF is defined as the bit pattern 1001.
29. Disabled NDF is defined as the bit pattern 0110.

14.16 System Side Interfaces

In single STS-192/STM-64 mode, the system side interface supports a 777.6 MHz 16-bit serial 8B/10B encoded TelecomBus interface. Each serial line carries an STS-12/STM-4 data stream. For an STS-192 (STM-64) receive stream, the sixteen constituent STS-12/STM-4 #1 - #16 are provided at the DD1[0]+/-, DD1[1]+/-, DD1[2]+/-, DD1[3]+/-, DD2[0]+/-, DD2[1]+/-, DD2[2]+/-, DD2[3]+/-, DD3[0]+/-, DD3[1]+/-, DD3[2]+/-, DD3[3]+/-, DD4[0]+/-, DD4[1]+/-, DD4[2]+/-, DD4[3]+/- LVDS serial links respectively. For an STS-192 (STM-64) transmit stream, the sixteen constituent STS-48/STM-4 #1 - #16 are accepted at AD1[0]+/-, AD1[1]+/-, AD1[2]+/-, AD1[3]+/-, AD2[0]+/-, AD2[1]+/-, AD2[2]+/-, AD2[3]+/-, AD3[0]+/-, AD3[1]+/-, AD3[2]+/-, AD3[3]+/-, AD4[0]+/-, AD4[1]+/-, AD4[2]+/-, AD4[3]+/- LVDS serial links respectively. As per SONET/SDH the STS-12/STM-4 constituents of an STS-192/STM-64 are four bytes interleaved as shown in Figure 17.

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In quad STS-48/STM-16 mode, the line side interface supports four independent 777.6 MHz 4-bit 8B/10B encoded serial TelecomBus interfaces. The four TelecomBus interfaces run on the same system clock. Each serial line carries an STS-12/STM-4 data stream. For an STS-48/48c (STM-16/AU4-16c) receive stream, the four independent STS-48/48c (STM-16/AU4-16c) #1 - #4 are provided at the DD1[3:0], DD2[3:0], DD3[3:0] and DD4[3:0] serial TelecomBus Drop buses, respectively. For an STS-48/48c (STM-16/AU4-16c) transmit stream, the four independent STS-48/48c (STM-16/AU4-16c) #1 - #4 are accepted at the AD1[3:0], AD2[3:0], AD3[3:0] and AD4[3:0] serial TelecomBus Add buses, respectively. For an STS-48/STM-16, each DDN[M] carries an STS-12/STM-4. Also, as per SONET/SDH the different STS-12/STM-4 constituents of an STS-48/STM-16 are four bytes interleaved as shown in Figure 18

Figure 17 Add/Drop Interface Byte Mapping in STS-192/STM-64 Mode

STS-192c/AU-4-64c												
	A1 #1	A1 #2	A1 #3	A1 #4	A1 #5	...	...	...	A1 #189	A1 #190	A1 #191	A1 #192

← Order of reception/ transmission

AD1_1[7:0]/DD1_1[7:0]	A1 #1	A1 #2	A1 #3	A1 #4	A1 #65	A1 #66	A1 #67	A1 #68	A1 #129			
AD1_2[7:0]/DD1_2[7:0]	A1 #5	A1 #6	A1 #7	A1 #8								
AD1_3[7:0]/DD1_3[7:0]	A1 #9	A1 #10	A1 #11	A1 #12								
AD1_4[7:0]/DD1_4[7:0]	A1 #13	A1 #14	A1 #15	A1 #16	A1 #77				A1 #141			
AD2_1[7:0]/DD2_1[7:0]	A1 #17	A1 #18	A1 #19	A1 #20	A1 #81				A1 #145			
AD2_2[7:0]/DD2_2[7:0]	A1 #21	A1 #22	A1 #23	A1 #24								
AD2_3[7:0]/DD2_3[7:0]	A1 #25	A1 #26	A1 #27	A1 #28								
AD2_4[7:0]/DD2_4[7:0]	A1 #29	A1 #30	A1 #31	A1 #32	A1 #93				A1 #157			
AD3_1[7:0]/DD3_1[7:0]	A1 #33	A1 #34	A1 #35	A1 #36	A1 #97				A1 #61			
AD3_2[7:0]/DD3_2[7:0]	A1 #37	A1 #38	A1 #39	A1 #40								
AD3_3[7:0]/DD3_3[7:0]	A1 #41	A1 #42	A1 #43	A1 #44								
AD3_4[7:0]/DD3_4[7:0]	A1 #45	A1 #46	A1 #47	A1 #48	A1 #109				A1 #173			
AD4_1[7:0]/DD4_1[7:0]	A1 #49	A1 #50	A1 #51	A1 #52	A1 #113			A1 #116	A1 #177			
AD4_2[7:0]/DD4_2[7:0]	A1 #53											
AD4_3[7:0]/DD4_3[7:0]	A1 #57											
AD4_4[7:0]/DD4_4[7:0]	A1 #61			A1 #64	A1 #125			A1 #128	A1 #189			A1 #192

← Order of reception/transmission

Figure 18 Add/Drop Interface Byte Mapping in Quad STS-48/STM-16 Mode

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STS-48c/AU-4-16c	A1 #1	A1 #2	A1 #3	A1 #4	...	...	...	...	A1 #45	A1 #46	A1 #47	A1 #48

← Order of transmission

AD1[7:0]/DD1[7:0]	A1 #1	A1 #2	A1 #3	A1 #4	A1 #17	A1 #18	A1 #19	A1 #20	A1 #33	A1 #34	A1 #35	A1 #36
AD2[7:0]/DD2[7:0]	A1 #5	A1 #6	A1 #7	A1 #8	A1 #21	A1 #22	A1 #23	A1 #24	A1 #37	A1 #38	A1 #39	A1 #40
AD3[7:0]/DD3[7:0]	A1 #9	A1 #10	A1 #11	A1 #12	A1 #25	A1 #26	A1 #27	A1 #28	A1 #41	A1 #42	A1 #43	A1 #44
AD4[7:0]/DD4[7:0]	A1 #13	A1 #14	A1 #15	A1 #16	A1 #29	A1 #30	A1 #31	A1 #32	A1 #45	A1 #46	A1 #47	A1 #48

← Order of transmission

14.17 Space Slot Interchange (SSI)

The SONET/SDH Space Slot Interchange (SSI) block grooms the SONET/SDH data stream by performing STS-12 (STM-4) space switching. Any STS-12 (STM-4) can be switched to any STS-12/STM-4 space slot.

14.18 8B/10B Encoder (T8TE)

The drop Data 8B/10B Encoder block (T8TE) constructs an 8B/10B character stream from an incoming TelecomBus carrying an STS-12/STM-4 stream. A total of 16 T8TE blocks are instantiated in the SPECTRA-9953 device.

The T8TE operates in one of two modes: multiplex section termination (MST) and high-order path termination (HPT) mode. In MST mode, the upstream block is a multiplex section terminator. It has identified transport frame boundaries. The first J0 byte (J0) On each DD[x][7:0] STS-12 link is encoded by an 8B/10B control character. In HPT mode, the upstream block is a high-order path terminator and has performed pointer processing to identify STS/AU level pointer justification events. It has processed all the STS/VC3/VC4 path overhead bytes. The H3 bytes in the absence of negative pointer justification events, the PSO byte in the presence of positive pointer justification events may be encoded. Alternately, the J1 byte may be encoded.

Table 13 shows the mapping of TelecomBus control bytes and signals into 8B/10B control characters. The table is divided into three sections, one for each software configurable mode of operation.

Table 13 Serial TelecomBus 8B/10B Character Mapping

Code Group Name	Curr. RD- abcdei fghj	Curr. RD+ abcdei fghj	Encoded Signals Description
Multiplex Section Termination (MST) Mode			

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Code Group Name	Curr. RD- abcdei fghj	Curr. RD+ abcdei fghj	Encoded Signals Description
K28.5	001111 101	110000 0101	IJ0 = 'b1 IPL = 'b0 Transport frame alignment
K.28.4-	001111 0010	-	IPAIS = 'b1 High-order path AIS
High-Order Path Termination (HPT) Mode			
K28.0-	001111 0100	-	IPL = 'b0 High-order path H3 byte position, no negative justification event
K28.0+	-	110000 1011	IPL = 'b0 High-order path PSO byte position, positive justification event
K28.6	001111 0110	110000 1001	IJ1 = 'b1 IPL = 'b1 High-order path frame alignment

14.19 Receive 8B/10B TelecomBus Decoder (R8TD)

The Receive 8B/10B TelecomBus Decoder (R8TD) block frames to the receive stream to find 8B/10B character boundaries. It also contains a FIFO to bridge between the timing domain of the receive LVDS links and the system clock timing domain. A total of 16 R8TD blocks are instantiated in the SPECTRA-9953 device.

14.19.1 FIFO Buffer

The FIFO buffer sub-block provides isolation between the timing domain of the associated 16 LVDS links and that of the system clock (SYSCLK) . Data with arbitrary alignment to 8B/10B characters are written into a 10-bit by 24-word deep FIFO at the link clock rate. Data is read from the FIFO at every SYSCLK cycle.

14.19.2 Frame Counter

The Frame Counter sub-block keeps track of the octet identity of the outgoing data stream. It is initialized by a delayed version of the AFP signal. It identifies the positive stuff opportunity (PSO) and negative stuff opportunity (H3) bytes within the transport frame so that high-order path pointer justification events can be identified and decoded.

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14.19.3 Character Alignment

The character alignment sub-block locates character boundaries in the incoming 8B/10B data stream. The framer logic may be in one of two states, SYNC state and HUNT state. It uses the 8B/10B control character (K28.5) used to encode the SONET/SDH J0 byte to locate character boundaries and to enter the SYNC state. It monitors the receive data stream for line code violations (LCV). An LCV is declared when the running disparity of the receive data is not consistent with the previous character or the data is not one of the characters defined in the IEEE standard 802.3. Excessive LCVs are used to transition the framer logic to the HUNT state.

Normal operation occurs when the character alignment sub-block is in the SYNC state. 8B/10B characters are extracted from the FIFO using the character alignment of the K28.5 character that caused entry to the SYNC state. Mimic K28.5 characters at other alignments are ignored. The receive data is constantly monitored for line code violations. If five or more LCVs are detected in a window of 15 characters, the character alignment sub-block transitions to the HUNT state. It will search all possible alignments in the receive data for the K28.5 character. In the meantime, the original character alignment is maintained until a K28.5 character is found. At that point, the character alignment is moved to this new location and the sub-block transitions to the SYNC state.

14.19.4 Frame Alignment

The frame alignment sub-block monitors the data read from the FIFO buffer sub-block for the J0 byte. When the frame counter sub-block indicates the J0 byte position, a J0 character is expected to be read from the FIFO. If a J0 byte is read out of the FIFO at other byte positions, a J0 byte error counter is incremented. When the counter reaches a count of 3, the frame alignment sub-block transitions to HUNT state. The next time a J0 character is read from the FIFO, the associated read address is latched and the sub-block transitions back to the SYNC state. The J0 byte error counter is cleared when a J0 byte is read from the FIFO at the expected position.

14.19.5 Character Decode

The character decode sub-block decodes the incoming 8B/10B control characters into an extended set of TelecomBus control signals. Table 14 shows the mapping of 8B/10B control characters into TelecomBus control signals. The table is divided into three sections, one for each mode of operation in the 8B/10B encoder in an external device upstream of the SPECTRA-9953 device. The character decoder sub-block itself is not mode-sensitive.

Table 14 Serial TelecomBus 8B/10B Character Decoding

Code Group Name	Curr. RD- abcdei fghj	Curr. RD+ abcdei fghj	Decoded Signals Description
Multiplex Section Termination (MST) Mode			
K28.5	001111 0100	110000 1011	OJ0='b1' Transport frame alignment

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Code Group Name	Curr. RD- abcdei fghj	Curr. RD+ abcdei fghj	Decoded Signals Description
			OD[7:0] = ‘h01
K.28.4-	001111 0010	-	OPAIS=’b1’ High-order path AIS OD[7:0] = ‘hFF
High-Order Path Termination (HPT) Mode			
K28.0-	001111 0100	-	OPL = ‘b0, High-order path H3 byte, no negative justification event OD[7:0] = ‘h00
K28.0+	-	110000 1011	OPL = ‘b0 High-order path PSO byte, positive justification event OD[7:0] = ‘h00
K28.6	001111 0110	110000 1001	OJ1=’b1’ High-order path frame alignment OD[7:0] = ‘h00

14.20 Add/Drop Clock Synthesis Unit

The CSU is a fully integrated clock synthesis unit. It generates low jitter multi-phase differential clocks at 777.6 MHz for use by the Add bus DRU and the Drop bus PISO.

14.21 Drop bus Transmit Serializer

The Drop bus PISO is a parallel-to-serial converter designed for high-speed transmit operation, supporting up to 777.6 Mbit/s. It converts 8B/10B characters to bit-serial format.

There are 16 instances of the PISO on the SPECTRA-9953 device.

14.22 Drop bus LVDS Transmitter

The TXLV block is a 777.6 Mbit/s Low Voltage Differential Signaling (LVDS) Transmitter according to the IEEE 1596.3-1996 LVDS specification.

The TXLV accepts 777.6 Mbit/s differential data from a “parallel-in, serial-out” (PISO) circuit and then transmits the data off-chip as a low voltage differential signal on TP[X]/TN[X] pins.

The TXLV uses a reference current and voltage from the TXLVREF block to control the output differential voltage amplitude and the output common-mode voltage.

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14.23 Transmit Reference Generator

The TXLVREF provides an on-chip bandgap voltage reference (1.20V ±5%) and a precision current to the TXLV (777.6 Mbit/s LVDS Transmitter) block's. The reference voltage is used to control the common-mode level of the TXLV output, while the reference current is used to control the output amplitude.

The precision currents are generated by forcing the reference voltage across an external, off-chip 3.16 kΩ (±1%) resistor. The resulting current is then mirrored through several individual reference current outputs, so each TXLV receives its own reference current.

There is one instance of the TXREF for the SPECTRA-9953 device.

14.24 LVDS Receiver

The RXLV block is a 777.6 Mbit/s LVDS receiver according to the IEEE 1596.3-1996 LVDS specification including the minor differences noted in the Line LVDS Overview at the beginning of the Functional Description.

The RXLV block is the receiver shown in Figure 6. It accepts up to 777.6 Mbit/s LVDS signals from the transmitter, over RP[X]/RN[X] pins, amplifying them and converting them to digital signals, then passing them to a data recovery unit (DRU). Holding to the IEEE 1596.3-1996 specification, the RXLV has a differential input sensitivity better than 100 mV.

These are LVDS receivers not CMOS. If a link is unused there is no electrical problem in leaving AD+/AD- floating (as opposed to a CMOS input). Power dissipation is the same regardless of whether the input is connected or not. No damage to the device will occur.

If the user knows a link is not used, they should disable it in software. This way, the power for that link will be nearly none. There is no requirement for how quickly this should be done. It simply results in lower power dissipation since circuitry will be shut down. This is not mandatory for the device to operate properly but is a good practice since it improves margins.

In terms of hot-swap, there is no problem. The channel can be left enabled at all time and the device will sync up once the far end transmitter is connected. There will be no effect on other channels.

A total of 16 RXLV blocks are instantiated in the SPECTRA-9953 device.

14.25 Add bus Data Recovery Unit

The DRU is a fully integrated data recovery and serial-to-parallel converter which can be used for 777.6 Mbit/s NRZ data. 8B/10B block code is used to guarantee transition density for optimal performance.

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The DRU recovers data and outputs a 10-bit word synchronized with a line rate divided by 10-gated clock to allow frequency deviations between the data source and the local oscillator. The output clock is not a recovered clock. The DRU accumulates 10 data bits, without regard to 8B/10B character boundaries, and outputs them on the next clock edge. If 10 bits are not available for transfer at a given clock cycle, the output clock is gated.

The DRU provides moderate high frequency jitter tolerance suitable for inter-chip serial link applications. It can support frequency deviations up to ±100ppm.

There are 16 instances of the DRU on the SPECTRA-9953 device.

14.26 JTAG Test Access Port Interface

The JTAG Test Access Port block provides JTAG support for boundary scan. The standard JTAG EXTEST, SAMPLE, BYPASS, IDCODE and STCTEST instructions are supported. The SPECTRA-9953 identification code is 053170CDH hexadecimal.

14.27 Microprocessor Interface

The Microprocessor Interface Block provides the logic required to interface the generic microprocessor bus with the normal mode and test mode registers within the SPECTRA-9953. The normal mode registers are used during normal operation to configure and monitor the SPECTRA-9953. The test mode registers are used to enhance the testability of the SPECTRA-9953. The register set is accessed as shown in Table 15. In the following section, every register is documented and identified using the register numbers. The corresponding memory map address is identified by the address column of the table. Addresses that are not shown are not used and must be treated as reserved.

Note: The SPECTRA-9953 device has three type of normal registers: top-level registers, STM-16 registers, and STM-4 registers on both the receive and transmit sides of the device. Bit 14 of the MPIF address bus is used to select between a test and a normal register. Bit 13 is used to select between the receive and transmit sides of the device. Bits[12:11] are used to select an STM-16 slice (“00H to select STM-16 channel#1, “01H” to select #2, “10H” for #3 and “11H” for #4). Bits[10:9] are used to select an STM4 slice (“00H to select STM-4 slice#1, “01H” to select #2, “10H” for #3 and “11H” for #4), and finally bits[8:0] provides the address of the register to be accessed.

Table 15 SPECTRA-9953 Register Mapping Table

TST A[14]	RX/TX A[13]	STM-16 Slice # A[12:11]	STM-4 Slice # A[10:9]	Address (HEX) A[8:0]	Register Description
TOP LEVEL REGISTERS					

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TST A[14]	RX/TX A[13]	STM-16 Slice # A[12:11]	STM-4 Slice # A[10:9]	Address (HEX) A[8:0]	Register Description
X	**0**	**– –**[1]	**– –**	**000-03F**	**Top-level configuration/status**
0	0	– –	– –	000	SP9953 Master Configuration
0	0	– –	– –	001	SP9953 Receive Configuration #1
0	0	– –	– –	002	SP9953 Receive Configuration #2
0	0	– –	– –	003	SP9953 Receive Configuration #3
0	0	– –	– –	004	SP9953 Transmit Configuration #1
0	0	– –	– –	005	SP9953 Transmit Configuration #2
0	0	– –	– –	006	SP9953 Transmit Configuration #3
0	**0**	**– –**	**– –**	**008-017**	**SP9953 System Side Line Loopback** (1 through 16)
0	0	– –	– –	018	RESERVED
0	0	– –	– –	019	SP9953 System Loopback
0	0	– –	– –	01A	AFPDLY
0	0	– –	– –	01B	DFPDLY
0	0	– –	– –	01C	System Side Analog Control
0	0	– –	– –	01D	Line Side Analog Control
0	0	– –	– –	01E	Free register
0	0	– –	– –	01F	Clocks Activity Monitor
0	0	– –	– –	020	RESERVED
0	0	– –	– –	021-02C	Unused
0	0	– –	– –	02D	JTAG_ID(31:16)
0	0	– –	– –	02E	JTAG_ID(15:0)
0	0	– –	– –	02F	Free register
0	**0**	**– –**	**– –**	**030-03F**	**SP9953 Interrupt Status (1 through 16)**
STM-16 AND STM-4 SLICE REGISTERS					
0	0	XX[2]	00	040	RESERVED
0	0	XX	XX	041	RESERVED
0	1	XX	00	040	RESERVED
0	1	XX	XX	041	RESERVED
0	**0**	**00**	**00**	**04C-04F**	**DLL**
0	0	00	00	04C	DLL – Configuration
0	0	00	00	04D	RESERVED
0	0	00	00	04E	DLL –
0	0	00	00	04F	DLL – Control Status
0	**0**	**XX**	**XX**	**050-05F**	**RRMP**
0	0	XX	XX	050	RRMP – Configuration

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TST A[14]	RX/TX A[13]	STM-16 Slice # A[12:11]	STM-4 Slice # A[10:9]	Address (HEX) A[8:0]	Register Description
0	0	XX	XX	051	RRMP – Status
0	0	XX	XX	052	RRMP – Interrupt Enable
0	0	XX	XX	053	RRMP – Interrupt Status
0	0	XX	XX	054	RRMP – Received APS
0	0	XX	XX	055	RRMP – Received SSM
0	0	XX	XX	056	RRMP – AIS Enable
0	0	XX	XX	057	RRMP – Section BIP Error Counter
0	0	XX	XX	058	RRMP – Line BIP Error Counter – LSB
0	0	XX	XX	059	RRMP – Line BIP Error Counter – MSB
0	0	XX	XX	05A	RRMP – Line REI Error Counter – LSB
0	0	XX	XX	05B	RRMP – Line REI Error Counter – MSB
0	**0**	**00**	**00**	**060-07F**	**SRLI_192**
0	0	00	00	060-068	SRLI – Unused
0	0	00	00	069	SRLI – Synchronization Error Interrupt Status
0	0	00	00	06A	SRLI – Sync Error Status
0	0	00	00	06B	SRLI – Sync Error Interrupt Enable
0	0	00	00	06C	SRLI – PGMclk Config
0	0	00	00	06D	SRLI – Sync Error Configuration
0	0	00	00	06E	SRLI – FBDI Control
0	0	00	00	06F	SRLI – Unused
0	**0**	**XX**	**00**	**080-09F**	**SBER**
0	0	XX	00	080	SBER – Configuration
0	0	XX	00	081	SBER – Status
0	0	XX	00	082	SBER – Interrupt Enable
0	0	XX	00	083	SBER – Interrupt Status
0	0	XX	00	084	SBER – SF BERM Accum. Period (LSB)
0	0	XX	00	085	SBER – SF BERM Accum. Period (MSB)
0	0	XX	00	086	SBER – SF BERM Saturatn. Trshld. (LSB)
0	0	XX	00	087	SBER – SF BERM Saturatn. Trshld. (MSB)
0	0	XX	00	088	SBER – SF BERM Declaratn. Trshld. (LSB)
0	0	XX	00	089	SBER – SF BERM Declaratn. Trshld.(MSB)
0	0	XX	00	08A	SBER – SF BERM Clearing Trshld. (LSB)
0	0	XX	00	08B	SBER – SF BERM Clearing Trshld. (MSB)
0	0	XX	00	08C	SBER – SD BERM Accum. Period (LSB)

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TST A[14]	RX/TX A[13]	STM-16 Slice # A[12:11]	STM-4 Slice # A[10:9]	Address (HEX) A[8:0]	Register Description
0	0	XX	00	08D	SBER – SD BERM Accum. Period (MSB)
0	0	XX	00	08E	SBER – SD BERM Saturatn. Trshld. (LSB)
0	0	XX	00	08F	SBER – SD BERM Saturatn. Trshld. (MSB)
0	0	XX	00	090	SBER – SD BERM Declaratn. Trshld. (LSB)
0	0	XX	00	091	SBER – SD BERM Declaratn. Trshld.(MSB)
0	0	XX	00	092	SBER – SD BERM Clearing Trshld. (LSB)
0	0	XX	00	093	SBER – SD BERM Clearing Trshld. (MSB)
0	**0**	**XX**	**00**	**0A0-0AF**	**RTTP Section**
0	0	XX	00	0A0	RTTP – Indirect Address
0	0	XX	00	0A1	RTTP – Indirect Data
0	0	XX	00	0A2	RTTP – Trace Unstable Status
0	0	XX	00	0A3	RTTP – Trace Unstable Interrupt Enable
0	0	XX	00	0A4	RTTP – Trace Unstable Interrupt Status
0	0	XX	00	0A5	RTTP – Trace Mismatch Status
0	0	XX	00	0A6	RTTP – Trace Mismatch Interrupt Enable
0	0	XX	00	0A7	RTTP – Trace Mismatch Interrupt Status
0	**0**	**XX**	**XX**	**0B0-0BF**	**RTTP Path**
0	0	XX	XX	0B0	RTTP – Indirect Address
0	0	XX	XX	0B1	RTTP – Indirect Data
0	0	XX	XX	0B2	RTTP – Trace Unstable Status
0	0	XX	XX	0B3	RTTP – Trace Unstable Interrupt Enable
0	0	XX	XX	0B4	RTTP – Trace Unstable Interrupt Status
0	0	XX	XX	0B5	RTTP – Trace Mismatch Status
0	0	XX	XX	0B6	RTTP – Trace Mismatch Interrupt Enable
0	0	XX	XX	0B7	RTTP – Trace Mismatch Interrupt Status
0	**0**	**XX**	**XX**	**0C0-0CF**	**RSVCA**
0	0	XX	XX	0C0	RSVCA – Indirect Address
0	0	XX	XX	0C1	RSVCA – Indirect Data
0	0	XX	XX	0C2	RSVCA – Payload Configuration
0	0	XX	XX	0C3	RSVCA – PosJust Interrupt Status
0	0	XX	XX	0C4	RSVCA – NegJust Interrupt Status
0	0	XX	XX	0C5	RSVCA – FIFO Overflow Interrupt Status
0	0	XX	XX	0C6	RSVCA – FIFO Underflow Interrupt Status
0	0	XX	XX	0C7	RSVCA – PtrJust Interrupt Enable
0	0	XX	XX	0C8	RSVCA – FIFO Interrupt Enable

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TST A[14]	RX/TX A[13]	STM-16 Slice # A[12:11]	STM-4 Slice # A[10:9]	Address (HEX) A[8:0]	Register Description
0	0	XX	XX	0C9	RSVCA – PtrJust Thresholds
0	0	XX	XX	0CA	RSVCA – Clear Fixed Stuff
0	0	XX	XX	0CB	RSVCA – Performance Monitor Trigger
0	**0**	**XX**	**XX**	**0D0-0DF**	**T8TE**
0	0	XX	XX	0D0	T8TE – Control Status
0	0	XX	XX	0D1	T8TE – Interrupt Status
0	0	XX	XX	0D2	T8TE – TS Config 1
0	0	XX	XX	0D3	T8TE – TS Config 2
0	0	XX	XX	0D4	T8TE – Test Pattern
0	0	XX	XX	0D5	
0	0	XX	XX	0D6	
0	**0**	**XX**	**00**	**0E0-0FF**	**SARC**
0	0	XX	00	0E0	SARC – Indirect Address
0	0	XX	00	0E1	SARC – Indirect Data
0	0	XX	00	0E2	SARC – Section Config
0	0	XX	00	0E3	SARC – Receive Section RSALM Enable
0	0	XX	00	0E4	SARC – Receive Section LAIS Enable
0	0	XX	00	0E5	SARC – Transmit Section LRDI Enable
0	0	XX	00	0E7	SARC – Transmit Path Config
0	0	XX	00	0E8-0EB	SARC – LOP Status (1 to 48)
0	0	XX	00	0EC-0EF	SARC – LOP Interrupt Enable (1 to48)
0	0	XX	00	0F0-0F3	SARC – LOP Interrupt Status (1 to 48)
0	0	XX	00	0F4-0F7	SARC – AIS Status (1 to 48)
0	0	XX	00	0F8-0FB	SARC – AIS Interrupt Enable (1 to 48)
0	0	XX	00	0FC-0FF	SARC – AIS Interrupt Status (1 to 48)
0	**0**	**XX**	**XX**	**100-17F**	**RHPP**
0	0	XX	XX	100	RHPP – Indirect Address
0	0	XX	XX	101	RHPP – Indirect Data
0	0	XX	XX	102	RHPP – Payload Config
0	0	XX	XX	103	RHPP – Counters Update
0	0	XX	XX	104	RHPP – Path Interrupt Status
0	0	XX	XX	105	RHPP – Ptr. Conc. Process Disable
0	0	XX	XX	b#10m000[3]	RHPP – Ptr. Interpreter Status – STS1 #m
0	0	XX	XX	b#10m001	RHPP – Ptr. Interpreter Int. Enable – STS1 #m
0	0	XX	XX	b#10m010	RHPP – Ptr. Interpreter Int. Status – STS1 #m

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TST A[14]	RX/TX A[13]	STM-16 Slice # A[12:11]	STM-4 Slice # A[10:9]	Address (HEX) A[8:0]	Register Description
0	0	XX	XX	b#10m011	RHPP – Error Monitor Status – STS1 #m
0	0	XX	XX	b#10m100	RHPP – Error Monitor Int. Enable – STS1 #m
0	0	XX	XX	b#10m101	RHPP – Error Monitor Int. Status – STS1 #m
0	**0**	**00**	**00**	**180-18F**	**DSSI**
0	0	00	00	180	SSI – Page 0 Source Select 1
0	0	00	00	181	SSI – Page 0 Source Select 2
0	0	00	00	182	SSI – Page 0 Source Select 3
0	0	00	00	183	SSI – Page 0 Source Select 4
0	0	00	00	184	SSI – Page 1 Source Select 1
0	0	00	00	185	SSI – Page 1 Source Select 2
0	0	00	00	186	SSI – Page 1 Source Select 3
0	0	00	00	187	SSI – Page 1 Source Select 4
0	0	00	00	188	SSI – Page Control
0	**0**	**00**	**00**	**190-19F**	**CSTRI**
0	0	00	00	190	CSTRI – Control
0	0	00	00	191	CSTRI – Control
0	0	00	00	192	CSTRI – Interrupt Status
0	**1**	**XX**	**XX**	**050-05F**	**TRMP**
0	1	XX	XX	050	TRMP – Config
0	1	XX	XX	051	TRMP – Register Insertion
0	1	XX	XX	052	TRMP – Error Insertion
0	1	XX	XX	053	TRMP – Transmit J0 and Z0
0	1	XX	XX	054	TRMP – Transmit E1 and F1
0	1	XX	XX	055	TRMP – Transmit D1D3 and D4D12
0	1	XX	XX	056	TRMP – Transmit K1 and K2
0	1	XX	XX	057	TRMP – Transmit S1 and Z1
0	1	XX	XX	058	TRMP – Transmit Z2 and E2
0	1	XX	XX	059	TRMP – Transmit H1 and H2 MASK
0	1	XX	XX	05A	TRMP – Transmit B1 and B2 MASK
0	**1**	**00**	**00**	**060-07F**	**STLI**
0	1	00	00	060	STLI – Config
0	1	00	00	061	STLI – PGMclk Config
0	1	00	00	062	STLI – Interrupt Enable
0	1	00	00	063	STLI – Interrupt Status
0	**1**	**XX**	**00**	**0A0-0AF**	**TTTP Section**

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TST A[14]	RX/TX A[13]	STM-16 Slice # A[12:11]	STM-4 Slice # A[10:9]	Address (HEX) A[8:0]	Register Description
0	1	XX	00	0A0	TTTP – Indirect Address
0	1	XX	00	0A1	TTTP – Indirect Data
0	**1**	**XX**	**XX**	**0B0-0BF**	**TTTP Path**
0	1	XX	XX	0B0	TTTP – Indirect Address
0	1	XX	XX	0B1	TTTP – Indirect Data
0	**1**	**XX**	**XX**	**0C0-0CF**	**TSVCA**
0	1	XX	XX	0C0	TSVCA – Indirect Address
0	1	XX	XX	0C1	TSVCA – Indirect Data
0	1	XX	XX	0C2	TSVCA – Payload Configuration
0	1	XX	XX	0C3	TSVCA – PosJust Interrupt Status
0	1	XX	XX	0C4	TSVCA – NegJust Interrupt Status
0	1	XX	XX	0C5	TSVCA – FIFO Overflow Interrupt Status
0	1	XX	XX	0C6	TSVCA – FIFO Underflow Interrupt Status
0	1	XX	XX	0C7	TSVCA – PtrJust Interrupt Enable
0	1	XX	XX	0C8	TSVCA – FIFO Interrupt Enable
0	1	XX	XX	0C9	TSVCA – PtrJust Thresholds
0	1	XX	XX	0CA	TSVCA – Clear Fixed Stuff
0	1	XX	XX	0CB	TSVCA – Performance Monitor Trigger
0	**1**	**XX**	**XX**	**0D0-0DF**	**R8TD**
0	1	XX	XX	0D0	R8TD – Control Status
0	1	XX	XX	0D1	R8TD – Interrupt Status
0	1	XX	XX	0D2	R8TD – LCV Count
0	1	XX	XX	0D3	R8TD – Analog Control 1
0	1	XX	XX	0D4	R8TD – Analog Control 2
0	1	XX	XX	0D5	R8TD – Analog Control 3
0	**1**	**XX**	**XX**	**0E0-0FF**	**THPP**
0	1	XX	XX	0E0	THPP – Indirect Address
0	1	XX	XX	0E1	THPP – Indirect Data
0	1	XX	XX	0E2	THPP – Payload Config
0	**1**	**XX**	**XX**	**100-17F**	**SHPI**
0	1	XX	XX	100	SHPI – Indirect Address
0	1	XX	XX	101	SHPI – Indirect Data
0	1	XX	XX	102	SHPI – Payload Config
0	1	XX	XX	103	SHPI – Counters Update
0	1	XX	XX	104	SHPI – Path Interrupt Status
0	1	XX	XX	105	SHPI – Ptr. Conc. Process Disable
0	1	XX	XX	106	SHPI – PT_PATH Enable Register

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TST A[14]	RX/TX A[13]	STM-16 Slice # A[12:11]	STM-4 Slice # A[10:9]	Address (HEX) A[8:0]	Register Description
0	1	XX	XX	b#10m000	SHPI – Ptr. Interpreter Status – STS1 #m
0	1	XX	XX	b#10m001	SHPI – Ptr. Interpreter Int. Enable – STS1 #m
0	1	XX	XX	b#10m010	SHPI – Ptr. Interpreter Int. Status – STS1 #m
0	1	XX	XX	b#10m100	SHPI – Error Monitor Int. Enable – STS1 #m
0	1	XX	XX	b#10m101	SHPI – Error Monitor Int. Status – STS1 #m
0	**1**	**00**	**00**	**180-18F**	**ASSI**
0	1	00	00	180	ASSI – Page 0 Source Select 1
0	1	00	00	181	ASSI – Page 0 Source Select 2
0	1	00	00	182	ASSI – Page 0 Source Select 3
0	1	00	00	183	ASSI – Page 0 Source Select 4
0	1	00	00	184	ASSI – Page 1 Source Select 1
0	1	00	00	185	ASSI – Page 1 Source Select 2
0	1	00	00	186	ASSI – Page 1 Source Select 3
0	1	00	00	187	ASSI – Page 1 Source Select 4
0	1	00	00	188	ASSI – Page Control

Notes on Register Memory Map:

1. For all register accesses, CSB must be low.

30. Addresses that are not shown must be treated as Reserved.

31. A[14] is the test register select (TRS) and should be set to logic 0 for normal mode register access.

32. '– –' means these bits are, in effect, ignored

33. 'XX' means that a different register (i.e. on a different slice) is accessed depending on the value of 'XX'

34. 'm' can take on any 4-bit binary value from 1 to 12 (0001 to 1100). Used only at RHPP and SHPI.

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15 Normal Mode Register Description

Normal mode registers are used to configure and monitor the operation of the SPECTRA-9953 device. Normal mode registers (as opposed to test mode registers) are selected when TRS (A[14]) is low.

Notes on Normal Mode Register Bits:

1. Writing values into unused register bits has no effect. However, to ensure software compatibility with future, feature-enhanced versions of this product, unused register bits must be written with logic 0. Reading back unused bits can produce either a logic 1 or a logic 0; hence, unused register bits should be masked off by software when read.

16. All configuration bits that can be written into can also be read back. This allows the processor controlling the SPECTRA-9953 device to determine the programming state of the device.

17. Writeable normal mode register bits are cleared to logic 0 upon reset unless otherwise noted.

18. Writing into read-only normal mode register bit locations does not affect SPECTRA-9953 operation unless otherwise noted.

19. Certain register bits are reserved. These bits are associated with megacell functions that are unused in this application. To ensure that the SPECTRA-9953 device operates as intended, reserved register bits must only be written with the logic level as specified. Writing to reserved registers should be avoided.

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Register 0000H: SP9953 Master Configuration

Bit	Type	Function	Default
Bit 15	R	TIP	X
Bit 14	R	QUAD2488	X
Bit 13	R/W	Unused	0
Bit 12	R/W	Unused	0
Bit 11	R/W	Unused	0
Bit 10	R/W	Unused	0
Bit 9	R/W	Unused	0
Bit 8	R/W	Unused	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	WCIMODE	0
Bit 5	R/W	RESET_CORE	0
Bit 4	R/W	RESETSL[4]	0
Bit 3	R/W	RESETSL[3]	0
Bit 2	R/W	RESETSL[2]	0
Bit 1	R/W	RESETSL[1]	0
Bit 0	R/W	RESET	0

The Master Configuration Register is provided at SP9953 Read/Write Address 00H.

RESET

The software reset (RESET) bit resets the whole device. When a logic 1 is written to RESET, the SP9953 is held in reset. When a logic 0 is written to RESET, the SP9953 operates normally.

RESETSL[1:4]

The slice software reset (RESETSL[1:4]) bits reset the corresponding STS-48/STM-16 slice. When a logic 1 is written to RESETSL[X], the STS-48/STM-16 slice is held in reset. When a logic 0 is written to RESETSL[X], the STS-48/STM-16 slice operates normally. Note that top-level registers with slice configuration are not reset with these bits.

RESET_CORE

The digital core software reset (CORE_RESET) bit along with the RESETSL[1:4] can be used to reset the whole digital core (The analog interfaces are not reset). When a logic 1 is written to CORE_RESET and RESETSL[1:4], the digital core is kept into a reset state. When a logic 0 is written to RESET_CORE and RESETSL[1:4], the digital core operates normally.

Notes:

(1) No top-level registers are reset with this bit.

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(2) Analog blocks are affected by resetting all T8TE and R8TD registers to their default values.

WCIMODE

The write on clear interrupt mode (WCIMODE) bit selects the clear interrupt mode. When a logic 1 is written to WCIMODE, the clear interrupt mode is clear on write. When a logic 0 is written to WCIMODE, the clear interrupt mode is clear on read.

QUAD2488

The QUAD2488 bit provides the state of the QUAD2488 device pin.

TIP

The transfer in progress (TIP) signal is asserted high while the performance monitors are being transferred to the holding registers. The transfer is initiated by written to the Master Configuration Register. TIP is negated when the transfer is completed. It will take a maximum of 300 ns to transfer all the device registers.

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Register 0001H: SP9953 Receive Configuration 1

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14	R/W	ROHI_RST_OOF_EN	0
Bit 13	R/W	ROHI_RESET[4]	0
Bit 12	R/W	ROHI_RESET[3]	0
Bit 11	R/W	ROHI_RESET[2]	0
Bit 10	R/W	ROHI_RESET[1]	0
Bit 9	R/W	DCMP_SAMPLE_DIS	0
Bit 8	R/W	SYNC_ERR_POL	0
Bit 7	R/W	Unused	0
Bit 6	R/W	DFP_DISABLE	0
Bit 5	R/W	AFP_DISABLE	0
Bit 4	R/W	DFP_ON_AFP	0
Bit 3	R/W	AFP_ON_DFP	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	RDDS	0
Bit 0	R/W	Reserved	0

The Receive Configuration Register is provided at SP9953 Read/Write Address 01H.

RDDS

The receive disable de-scrambling (RDDS) bit disables the de-scrambling of the input data stream. When a logic 1 is written to RDDS, the input data stream is not de-scrambled. When a logic 0 is written to RDDS, the input data stream is de-scrambled.

AFP_ON_DFP

The AFP_ON_DFP configures the SPECTRA-9953 to ignore DFP and use AFP as a frame pulse on the drop side. When set to 1, external DFP pulses are ignored: AFP and AFPDLY[13:0] determine the timing on the drop bus. When set to 0, the DFP pin operates normally.

DFP_ON_AFP

The DFP_ON_AFP configures the SPECTRA-9953 to ignore AFP and use DFP as a frame pulse on the add side. When set to 1, external AFP pulses are ignored: DFP and AFPDLY[13:0] determine the timing on the Add bus. Note that AFPDLY[13:0] is still used. . When set to 0, the AFP pin operates normally.

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AFP_DISABLE

The AFP_DISABLE configures the SPECTRA-9953 to ignore the Add bus frame pulse AFP. When set to 1, external AFP pulses are ignored. When set to 0, the AFP pin operates normally. This mode is provided for diagnostic purposes.

DFP_DISABLE

The DFP_DISABLE configures the SPECTRA-9953 to ignore the DFP input. When set to 1, external DFP pulses are ignored. When set to 0, the DFP pin operates normally. This mode is provided for diagnostic purposes.

SYNC_ERR_POL

The synchronization error polarity register bit is used to configure the polarity of the SYNC_ERR line side input pin. When set to 0, SYNC_ERR is active high signal. When set to 1, SYNC_ERR is active low. SYNC_ERR_POL is XORED with SYNC_ERR.

DCMP_SAMPLE_DIS

The DCMP sample disable bit (DCMP_SAMPLE_DIS) is used to disable the sampling of the DCMP input with the DFP external input. When DCMP_SAMPLE_DIS is set to 0, the DCMP is only used internally after a DFP pulse. When the bit is set to 1, DCMP is used without an external DFP pulse.

ROHI_RESET[1:4]

The ROHI_RESET[1:4] register bits are used to reset the receive transport overhead top-level blocks. When ROHI_RESET[x] is set to 1, ROHI[x] is kept into a reset mode. When ROHI_RESET is set to 0, ROHI[x] block operates normally. Note that OC-192 mode has no bearing on the bits behaviour, i.e. that to reset all four ROHIs, all four of the ROHI_RESET[1:4] bits have to be set.

ROHI_RST_OOF_EN

The ROHI reset OOF enable (ROHI_RST_OOF_EN) bit causes the ROHI to be reset when the RRMP is out of frame. In OC-192 mode, when ROHI_RST_OOF_EN is set to 1, all 4 ROHIs will be reset when RRMP # 1 is out of frame. In Quad OC-48 mode, when ROHI_RST_OOF_EN is set to 1 then when the master RRMP for each slice is out of frame, its respective ROHI will be reset. When ROHI_RST_OOF_EN is set to 0, then RRMP OOF never resets the ROHI.

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Register 0002H: SP9953 Receive Configuration 2

Bit	Type	Function	Default
Bit 15	R/W	RSTS12C[16]	0
Bit 14	R/W	RSTS12C[15]	0
Bit 13	R/W	RSTS12C[14	0
Bit 12	R/W	RSTS12C[13]	0
Bit 11	R/W	RSTS12C[12]	0
Bit 10	R/W	RSTS12C[11]	0
Bit 9	R/W	RSTS12C[10]	0
Bit 8	R/W	RSTS12C[9]	0
Bit 7	R/W	RSTS12C[8]	0
Bit 6	R/W	RSTS12C[7]	0
Bit 5	R/W	RSTS12C[6]	0
Bit 4	R/W	RSTS12C[5]	0
Bit 3	R/W	RSTS12C[4]	0
Bit 2	R/W	RSTS12C[3]	0
Bit 1	R/W	RSTS12C[2]	0
Bit 0	R/W	RSTS12C[1]	0

The Receive Configuration 2 Register is provided at SP9953 Read/Write Address 02H.

RSTS12C[1:16]

The receive STS-12 concatenation mode (RSTS12C[1:16 bits enable the processing of an STS-12c (VC-4-4c) payload for the corresponding STS-12/STM-4 slice. When a logic 1 is written to RSTS12CSL[X] and a logic 1 is written to RSTS12C[X], the receive STS-12/STM-4 slice processes a slave STS-12c (VC-4-4c) payload. When a logic 0 is written to RSTS12CSL[X] and a logic 1 is written to RSTS12C[X], the receive STS-12/STM-4 slice process a master STS-12c (VC-4-4c) payload. When a logic 0 is written to RSTS12CSL[X] and a logic 0 is written to RSTS12C[X], the receive STS-12/STM-4 slice is not processing a STS-12c (VC-4-4c) payload.

Note: there is a possibility that SVCA indirect registers can be corrupted upon path reconfiguration. Refer to section 14.13 for more explanation and how to avoid the problem.

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Register 0003H: SP9953 Receive Configuration 3

Bit	Type	Function	Default
Bit 15	R/W	RSTS12CSL[16]	0
Bit 14	R/W	RSTS12CSL[15]	0
Bit 13	R/W	RSTS12CSL[14]	0
Bit 12	R/W	RSTS12CSL[13]	0
Bit 11	R/W	RSTS12CSL[12]	0
Bit 10	R/W	RSTS12CSL[11]	0
Bit 9	R/W	RSTS12CSL[10]	0
Bit 8	R/W	RSTS12CSL[9]	0
Bit 7	R/W	RSTS12CSL[8]	0
Bit 6	R/W	RSTS12CSL[7]	0
Bit 5	R/W	RSTS12CSL[6]	0
Bit 4	R/W	RSTS12CSL[5]	0
Bit 3	R/W	RSTS12CSL[4]	0
Bit 2	R/W	RSTS12CSL[3]	0
Bit 1	R/W	RSTS12CSL[2]	0
Bit 0	R/W	RSTS12CSL[1]	0

The Receive Configuration Register 3 is provided at SP9953 Read/Write Address 03H.

RSTS12CSL[1:16]

The receive STS-12 slave concatenation mode (RSTS12CSL[1:16]) bits enable the slave processing of an STS-12c (VC-4-4c) payload for the corresponding STS-12/STM-4 slice. When a logic 1 is written to RSTS12CSL[X] and a logic 1 is written to RSTS12C[X], the receive STS-12/STM-4 slice process a slave STS-12c (VC-4-4c) payload. When a logic 0 is written to RSTS12CSL[X] and a logic 1 is written to RSTS12C[X], the receive STS-12/STM-4 slice processes a master STS-12c (VC-4-4c) payload. When a logic 0 is written to RSTS12CSL[X] and a logic 0 is written to RSTS12C[X], the receive STS-12/STM-4 slice is not processing an STS-12c (VC-4-4c) payload.

Note: there is a possibility that SVCA indirect registers can be corrupted upon path reconfiguration. Refer to section 14.13 for more explanation and how to avoid the problem.

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Register 0004H: SP9953 Transmit Configuration 1

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		TOHI_RESET[4]	
Bit 12		TOHI_RESET[3]	
Bit 11		TOHI_RESET[2]	
Bit 10		TOHI_RESET[1]	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6	R/W	ACMP_SAMPLE_DIS	0
Bit 5	R/W	Unused	0
Bit 4	R/W	TXFPI_DISABLE	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	TDS	0
Bit 0	R/W	Reserved	0

The Transmit Configuration 1 Register is provided at SP9953 Read/Write Address 04H.

TDS

The transmit disable scrambling (TDS) bit disables the scrambling of the output data stream. When a logic 1 is written to TDS, the output data stream is not scrambled. When a logic 0 is written to TDS, the output data stream is scrambled.

TXFPI_DISABLE

The TXFPI_DISABLE bit is used to kill activity on the line side TXFPI input. When set to 1, the TXFPI input is ignored. When set to 0, TXFPI operates normally.

ACMP_SAMPLE_DIS

The ACMP sample disable bit (ACMP_SAMPLE_DIS) is used to disable the sampling of the ACMP input with the AFP external input. When ACMP_SAMPLE_DIS is set to 0, the ACMP is only used internally after an AFP pulse. When the bit is set to 1, ACMP is used without an external AFP pulse.TOHI_RESET[1:4]

The TOHI_RESET[1:4] register bits are used to reset the transmit transport overhead top-level blocks. When TOHI_RESET[x] is set to 1, TOHI[x] is kept into a reset mode. When TOHI_RESET[x] is set to 0, the TOHI[x] block operates normally.

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Register 0005H: SP9953 Transmit Configuration 2

Bit	Type	Function	Default
Bit 15	R/W	TSTS12C[16]	0
Bit 14	R/W	TSTS12C[15]	0
Bit 13	R/W	TSTS12C[14]	0
Bit 12	R/W	TSTS12C[13]	0
Bit 11	R/W	TSTS12C[12]	0
Bit 10	R/W	TSTS12C[11]	0
Bit 9	R/W	TSTS12C[10]	0
Bit 8	R/W	TSTS12C[9]	0
Bit 7	R/W	TSTS12C[8]	0
Bit 6	R/W	TSTS12C[7]	0
Bit 5	R/W	TSTS12C[6]	0
Bit 4	R/W	TSTS12C[5]	0
Bit 3	R/W	TSTS12C[4]	0
Bit 2	R/W	TSTS12C[3]	0
Bit 1	R/W	TSTS12C[2]	0
Bit 0	R/W	TSTS12C[1]	0

The Transmit Configuration 3 Register is provided at SP9953 Read/Write Address 05H.

TSTS12C[1:16]

The transmit STS-12c concatenation mode (TSTS12C[1:16]) bits enable the processing of an STS-12c (VC-4-4c) payload for the corresponding STS-12/STM-4 slice. When a logic 1 is written to TSTS12CSL[X] and a logic 1 is written to TSTS12C[X], the transmit STS-12/STM-4 slice processes a slave STS-12c (VC-4-4c) payload. When a logic 0 is written to TSTS12CSL[X] and a logic 1 is written to TSTS12C[X], the transmit STS-12/STM-4 slice processes a master STS-12c (VC-4-4c) payload. When a logic 0 is written to TSTS12CSL[X] and a logic 0 is written to TSTS12C[X], the transmit STS-48/STM-4 slice is not processing a STS-12c (VC-4-4c) payload.

Note: there is a possibility that SVCA indirect registers can be corrupted upon path reconfiguration. Refer to section 14.13 for more explanation and how to avoid the problem.

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Register 0006H: SP9953 Transmit Configuration 3

Bit	Type	Function	Default
Bit 15	R/W	TSTS12CSL[16]	0
Bit 14	R/W	TSTS12CSL[15]	0
Bit 13	R/W	TSTS12CSL[14]	0
Bit 12	R/W	TSTS12CSL[13]	0
Bit 11	R/W	TSTS12CSL[12]	0
Bit 10	R/W	TSTS12CSL[11]	0
Bit 9	R/W	TSTS12CSL[10]	0
Bit 8	R/W	TSTS12CSL[9]	0
Bit 7	R/W	TSTS12CSL[8]	0
Bit 6	R/W	TSTS12CSL[7]	0
Bit 5	R/W	TSTS12CSL[6]	0
Bit 4	R/W	TSTS12CSL[5]	0
Bit 3	R/W	TSTS12CSL[4]	0
Bit 2	R/W	TSTS12CSL[3]	0
Bit 1	R/W	TSTS12CSL[2]	0
Bit 0	R/W	TSTS12CSL[1]	0

The Transmit Configuration 4 Register is provided at SP9953 Read/Write Address 06H.

TSTS12CSL[SL1:16]:

The transmit STS-12 slave concatenation mode (TSTS12CSL[1:16]) bits enable the slave processing of an STS-12c (VC-4-4c) payload for the corresponding STS-12/STM-4 slice. When a logic 1 is written to TSTS12CSL[X] and a logic 1 is written to TSTS12C[X], the transmit STS-12/STM-4 slice processes a slave STS-12c (VC-4-4c) payload. When a logic 0 is written to TSTS12CSL[X] and a logic 1 is written to TSTS12C[X], the transmit STS-12/STM-4 slice processes a master STS-12c (VC-4-4c) payload. When a logic 0 is written to TSTS12CSL[X] and a logic 0 is written to TSTS12C[X], the transmit STS-12/STM-4 slice is not processing an STS-12c (VC-4-4c) payload.

Note: there is a possibility that SVCA indirect registers can be corrupted upon path reconfiguration. Refer to section 14.13 for more explanation and how to avoid the problem.

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Register 0008H: SP9953 System Side Line Loopback #1

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R/W	SSLLB[1][12]	0
Bit 10	R/W	SSLLB[1][11]	0
Bit 9	R/W	SSLLB[1][10]	0
Bit 8	R/W	SSLLB[1][9]	0
Bit 7	R/W	SSLLB[1][8]	0
Bit 6	R/W	SSLLB[1][7]	0
Bit 5	R/W	SSLLB[1][6]	0
Bit 4	R/W	SSLLB[1][5]	0
Bit 3	R/W	SSLLB[1][4]	0
Bit 2	R/W	SSLLB[1][3]	0
Bit 1	R/W	SSLLB[1][2]	0
Bit 0	R/W	SSLLB[1][1]	0

The Loopback Register is provided at SP9953 Read/Write Address 08H.

SSLLB[1][1:12]

The system side/line loopback (SSLLB[1][1:12]) bits enable the SSLLB for the first STS-12/STM-4 slice. When a logic 1 is written to SSLLB[1][X], the drop system data of STS-1/STM-0 path X is looped back into the add system data of STS-1/STM-0 path X. When a logic 0 is written to SSLLB[1][X], the SSLLB is inactive.

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Register 0009H: SP9953 System Side Line Loopback #2

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R/W	SSLLB[2][12]	0
Bit 10	R/W	SSLLB[2][11]	0
Bit 9	R/W	SSLLB[2][10]	0
Bit 8	R/W	SSLLB[2][9]	0
Bit 7	R/W	SSLLB[2][8]	0
Bit 6	R/W	SSLLB[2][7]	0
Bit 5	R/W	SSLLB[2][6]	0
Bit 4	R/W	SSLLB[2][5]	0
Bit 3	R/W	SSLLB[2][4]	0
Bit 2	R/W	SSLLB[2][3]	0
Bit 1	R/W	SSLLB[2][2]	0
Bit 0	R/W	SSLLB[2][1]	0

The Loopback Register is provided at SP9953 Read/Write Address 09H.

SSLLB[2][1:12]

The system side/line loopback (SSLLB[2][1:12]) bits enable the SSLLB for the second STS-12/STM-4 slice. When a logic 1 is written to SSLLB[1][X], the drop system data of STS-1/STM-0 path X is looped back into the add system data of STS-1/STM-0 path X. When a logic 0 is written to SSLLB[1][X], the SSLLB is inactive.

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Register 000AH: SP9953 System Side Line Loopback #3

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R/W	SSLLB[3][12]	0
Bit 10	R/W	SSLLB[3][11]	0
Bit 9	R/W	SSLLB[3][10]	0
Bit 8	R/W	SSLLB[3][9]	0
Bit 7	R/W	SSLLB[3][8]	0
Bit 6	R/W	SSLLB[3][7]	0
Bit 5	R/W	SSLLB[3][6]	0
Bit 4	R/W	SSLLB[3][5]	0
Bit 3	R/W	SSLLB[3][4]	0
Bit 2	R/W	SSLLB[3][3]	0
Bit 1	R/W	SSLLB[3][2]	0
Bit 0	R/W	SSLLB[3][1]	0

The Loopback Register is provided at SP9953 Read/Write Address 0AH.

SSLLB[3][1:12]

The system side/line loopback (SSLLB[3][1:12]) bits enable the SSLLB for the third STS-12/STM-4 slice. When a logic 1 is written to SSLLB[3][X], the drop system data of STS-1/STM-0 path X is looped back into the add system data of STS-1/STM-0 path X. When a logic 0 is written to SSLLB[1][X], the SSLLB is inactive.

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Register 000BH: SP9953 System Side Line Loopback #4

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R/W	SSLLB[4][12]	0
Bit 10	R/W	SSLLB[4][11]	0
Bit 9	R/W	SSLLB[4][10]	0
Bit 8	R/W	SSLLB[4][9]	0
Bit 7	R/W	SSLLB[4][8]	0
Bit 6	R/W	SSLLB[4][7]	0
Bit 5	R/W	SSLLB[4][6]	0
Bit 4	R/W	SSLLB[4][5]	0
Bit 3	R/W	SSLLB[4][4]	0
Bit 2	R/W	SSLLB[4][3]	0
Bit 1	R/W	SSLLB[4][2]	0
Bit 0	R/W	SSLLB[4][1]	0

The Loopback Register is provided at SP9953 Read/Write Address 0BH.

SSLLB[4][1:12]

The system side/line loopback (SSLLB[4][1:12]) bits enable the SSLLB for the fourth STS-12/STM-4 slice. When a logic 1 is written to SSLLB[4][X], the drop system data of STS-1/STM-0 path X is looped back into the add system data of STS-1/STM-0 path X. When a logic 0 is written to SSLLB[1][X], the SSLLB is inactive.

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Register 000CH: SP9953 System Side Line Loopback #5

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R/W	SSLLB[5][12]	0
Bit 10	R/W	SSLLB[5][11]	0
Bit 9	R/W	SSLLB[5][10]	0
Bit 8	R/W	SSLLB[5][9]	0
Bit 7	R/W	SSLLB[5][8]	0
Bit 6	R/W	SSLLB[5][7]	0
Bit 5	R/W	SSLLB[5][6]	0
Bit 4	R/W	SSLLB[5][5]	0
Bit 3	R/W	SSLLB[5][4]	0
Bit 2	R/W	SSLLB[5][3]	0
Bit 1	R/W	SSLLB[5][2]	0
Bit 0	R/W	SSLLB[5][1]	0

The Loopback Register is provided at SP9953 Read/Write Address 0CH.

SSLLB[5][1:12]

The system side/line loopback (SSLLB[5][1:12]) bits enable the SSLLB for the fifth STS-12/STM-4 slice. When a logic 1 is written to SSLLB[5][X], the drop system data of STS-1/STM-0 path X is looped back into the add system data of STS-1/STM-0 path X. When a logic 0 is written to SSLLB[1][X], the SSLLB is inactive.

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Register 000DH: SP9953 System Side Line Loopback #6

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R/W	SSLLB[6][12]	0
Bit 10	R/W	SSLLB[6][11]	0
Bit 9	R/W	SSLLB[6][10]	0
Bit 8	R/W	SSLLB[6][9]	0
Bit 7	R/W	SSLLB[6][8]	0
Bit 6	R/W	SSLLB[6][7]	0
Bit 5	R/W	SSLLB[6][6]	0
Bit 4	R/W	SSLLB[6][5]	0
Bit 3	R/W	SSLLB[6][4]	0
Bit 2	R/W	SSLLB[6][3]	0
Bit 1	R/W	SSLLB[6][2]	0
Bit 0	R/W	SSLLB[6][1]	0

The Loopback Register is provided at SP9953 Read/Write Address 0DH.

SSLLB[6][1:12]

The system side/line loopback (SSLLB[6][1:12]) bits enable the SSLLB for the sixth STS-12/STM-4 slice. When a logic 1 is written to SSLLB[6][X], the drop system data of STS-1/STM-0 path X is looped back into the add system data of STS-1/STM-0 path X. When a logic 0 is written to SSLLB[1][X], the SSLLB is inactive.

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Register 000EH: SP9953 System Side Line Loopback #7

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R/W	SSLLB[7][12]	0
Bit 10	R/W	SSLLB[7][11]	0
Bit 9	R/W	SSLLB[7][10]	0
Bit 8	R/W	SSLLB[7][9]	0
Bit 7	R/W	SSLLB[7][8]	0
Bit 6	R/W	SSLLB[7][7]	0
Bit 5	R/W	SSLLB[7][6]	0
Bit 4	R/W	SSLLB[7][5]	0
Bit 3	R/W	SSLLB[7][4]	0
Bit 2	R/W	SSLLB[7][3]	0
Bit 1	R/W	SSLLB[7][2]	0
Bit 0	R/W	SSLLB[7][1]	0

The Loopback Register is provided at SP9953 Read/Write Address 0EH.

SSLLB[7][1:12]

The system side/line Loopback (SSLLB[7][1:12]) bits enable the SSLLB for the seventh STS-12/STM-4 slice. When a logic 1 is written to SSLLB[7][X], the drop system data of STS-1/STM-0 path X is looped back into the add system data of STS-1/STM-0 path X. When a logic 0 is written to SSLLB[1][X], the SSLLB is inactive.

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Register 000FH: SP9953 System Side Line Loopback #8

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R/W	SSLLB[8][12]	0
Bit 10	R/W	SSLLB[8][11]	0
Bit 9	R/W	SSLLB[8][10]	0
Bit 8	R/W	SSLLB[8][9]	0
Bit 7	R/W	SSLLB[8][8]	0
Bit 6	R/W	SSLLB[8][7]	0
Bit 5	R/W	SSLLB[8][6]	0
Bit 4	R/W	SSLLB[8][5]	0
Bit 3	R/W	SSLLB[8][4]	0
Bit 2	R/W	SSLLB[8][3]	0
Bit 1	R/W	SSLLB[8][2]	0
Bit 0	R/W	SSLLB[8][1]	0

The Loopback Register is provided at SP9953 Read/Write Address FH.

SSLLB[8][1:12]

The system side/line loopback (SSLLB[8][1:12]) bits enable the SSLLB for the eighth STS-12/STM-4 slice. When a logic 1 is written to SSLLB[8][X], the drop system data of STS-1/STM-0 path X is looped back into the add system data of STS-1/STM-0 path X. When a logic 0 is written to SSLLB[1][X], the SSLLB is inactive.

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Register 0010H: SP9953 System Side Line Loopback #9

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R/W	SSLLB[9][12]	0
Bit 10	R/W	SSLLB[9][11]	0
Bit 9	R/W	SSLLB[9][10]	0
Bit 8	R/W	SSLLB[9][9]	0
Bit 7	R/W	SSLLB[9][8]	0
Bit 6	R/W	SSLLB[9][7]	0
Bit 5	R/W	SSLLB[9][6]	0
Bit 4	R/W	SSLLB[9][5]	0
Bit 3	R/W	SSLLB[9][4]	0
Bit 2	R/W	SSLLB[9][3]	0
Bit 1	R/W	SSLLB[9][2]	0
Bit 0	R/W	SSLLB[9][1]	0

The Loopback Register is provided at SP9953 Read/Write Address 10H.

SSLLB[9][1:12]

The system side/line loopback (SSLLB[9][1:12]) bits enable the SSLLB for the ninth STS-12/STM-4 slice. When a logic 1 is written to SSLLB[9][X], the drop system data of STS-1/STM-0 path X is looped back into the add system data of STS-1/STM-0 path X. When a logic 0 is written to SSLLB[1][X], the SSLLB is inactive.

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Register 0011H: SP9953 System Side Line Loopback #10

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R/W	SSLLB[10][12]	0
Bit 10	R/W	SSLLB[10][11]	0
Bit 9	R/W	SSLLB[10][10]	0
Bit 8	R/W	SSLLB[10][9]	0
Bit 7	R/W	SSLLB[10][8]	0
Bit 6	R/W	SSLLB[10][7]	0
Bit 5	R/W	SSLLB[10][6]	0
Bit 4	R/W	SSLLB[10][5]	0
Bit 3	R/W	SSLLB[10][4]	0
Bit 2	R/W	SSLLB[10][3]	0
Bit 1	R/W	SSLLB[10][2]	0
Bit 0	R/W	SSLLB[10][1]	0

The Loopback Register is provided at SP9953 Read/Write Address 11H.

SSLLB[10][1:12]

The system side/line loopback (SSLLB[10][1:12]) bits enable the SSLLB for the 10th STS-12/STM-4 slice. When a logic 1 is written to SSLLB[10][X], the drop system data of STS-1/STM-0 path X is looped back into the add system data of STS-1/STM-0 path X. When a logic 0 is written to SSLLB[1][X], the SSLLB is inactive.

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Register 0012H: SP9953 System Side Line Loopback #11

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R/W	SSLLB[11][12]	0
Bit 10	R/W	SSLLB[11][11]	0
Bit 9	R/W	SSLLB[11][10]	0
Bit 8	R/W	SSLLB[11][9]	0
Bit 7	R/W	SSLLB[11][8]	0
Bit 6	R/W	SSLLB[11][7]	0
Bit 5	R/W	SSLLB[11][6]	0
Bit 4	R/W	SSLLB[11][5]	0
Bit 3	R/W	SSLLB[11][4]	0
Bit 2	R/W	SSLLB[11][3]	0
Bit 1	R/W	SSLLB[11][2]	0
Bit 0	R/W	SSLLB[11][1]	0

The Loopback Register is provided at SP9953 Read/Write Address 12H.

SSLLB[11][1:12]

The system side/line loopback (SSLLB[11][1:12]) bits enable the SSLLB for the 11th STS-12/STM-4 slice. When a logic 1 is written to SSLLB[11][X], the drop system data of STS-1/STM-0 path X is looped back into the add system data of STS-1/STM-0 path X. When a logic 0 is written to SSLLB[1][X], the SSLLB is inactive.

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Register 0013H: SP9953 System Side Line Loopback #12

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R/W	SSLLB[12][12]	0
Bit 10	R/W	SSLLB[12][11]	0
Bit 9	R/W	SSLLB[12][10]	0
Bit 8	R/W	SSLLB[12][9]	0
Bit 7	R/W	SSLLB[12][8]	0
Bit 6	R/W	SSLLB[12][7]	0
Bit 5	R/W	SSLLB[12][6]	0
Bit 4	R/W	SSLLB[12][5]	0
Bit 3	R/W	SSLLB[12][4]	0
Bit 2	R/W	SSLLB[12][3]	0
Bit 1	R/W	SSLLB[12][2]	0
Bit 0	R/W	SSLLB[12][1]	0

The Loopback Register is provided at SP9953 Read/Write Address 13H.

SSLLB[12][1:12]

The system side/line Loopback (SSLLB[12][1:12]) bits enable the SSLLB for the 12th STS-12/STM-4 slice. When a logic 1 is written to SSLLB[12][X], the drop system data of STS-1/STM-0 path X is looped back into the add system data of STS-1/STM-0 path X. When a logic 0 is written to SSLLB[12][X], the SSLLB is inactive.

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Register 0014H: SP9953 System Side Line Loopback #13

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R/W	SSLLB[13][12]	0
Bit 10	R/W	SSLLB[13][11]	0
Bit 9	R/W	SSLLB[13][10]	0
Bit 8	R/W	SSLLB[13][9]	0
Bit 7	R/W	SSLLB[13][8]	0
Bit 6	R/W	SSLLB[13][7]	0
Bit 5	R/W	SSLLB[13][6]	0
Bit 4	R/W	SSLLB[13][5]	0
Bit 3	R/W	SSLLB[13][4]	0
Bit 2	R/W	SSLLB[13][3]	0
Bit 1	R/W	SSLLB[13][2]	0
Bit 0	R/W	SSLLB[13][1]	0

The Loopback Register is provided at SP9953 Read/Write Address 14H.

SSLLB[13][1:12]

The system side/line Loopback (SSLLB[13][1:13]) bits enable the SSLLB for the 13th STS-12/STM-4 slice. When a logic 1 is written to SSLLB[13][X], the drop system data of STS-1/STM-0 path X is looped back into the add system data of STS-1/STM-0 path X. When a logic 0 is written to SSLLB[13][X], the SSLLB is inactive.

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Register 0015H: SP9953 System Side Line Loopback #14

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R/W	SSLLB[14][12]	0
Bit 10	R/W	SSLLB[14][11]	0
Bit 9	R/W	SSLLB[14][10]	0
Bit 8	R/W	SSLLB[14][9]	0
Bit 7	R/W	SSLLB[14][8]	0
Bit 6	R/W	SSLLB[14][7]	0
Bit 5	R/W	SSLLB[14][6]	0
Bit 4	R/W	SSLLB[14][5]	0
Bit 3	R/W	SSLLB[14][4]	0
Bit 2	R/W	SSLLB[14][3]	0
Bit 1	R/W	SSLLB[14][2]	0
Bit 0	R/W	SSLLB[14][1]	0

The Loopback Register is provided at SP9953 Read/Write Address 15H.

SSLLB[14][1:12]

The system side/line Loopback (SSLLB[14][1:12]) bits enable the SSLLB for the 14th STS-12/STM-4 slice. When a logic 1 is written to SSLLB[14][X], the drop system data of STS-1/STM-0 path X is looped back into the add system data of STS-1/STM-0 path X. When a logic 0 is written to SSLLB[14][X], the SSLLB is inactive.

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Register 0016H: SP9953 System Side Line Loopback #15

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R/W	SSLLB[15][12]	0
Bit 10	R/W	SSLLB[15][11]	0
Bit 9	R/W	SSLLB[15][10]	0
Bit 8	R/W	SSLLB[15][9]	0
Bit 7	R/W	SSLLB[15][8]	0
Bit 6	R/W	SSLLB[15][7]	0
Bit 5	R/W	SSLLB[15][6]	0
Bit 4	R/W	SSLLB[15][5]	0
Bit 3	R/W	SSLLB[15][4]	0
Bit 2	R/W	SSLLB[15][3]	0
Bit 1	R/W	SSLLB[15][2]	0
Bit 0	R/W	SSLLB[15][1]	0

The Loopback Register is provided at SP9953 Read/Write Address 16H.

SSLLB[15][1:12]

The system side/line Loopback (SSLLB[15][1:12]) bits enable the SSLLB for the 15th STS-12/STM-4 slice. When a logic 1 is written to SSLLB[15][X], the drop system data of STS-1/STM-0 path X is looped back into the add system data of STS-1/STM-0 path X. When a logic 0 is written to SSLLB[15][X], the SSLLB is inactive.

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Register 0017H: SP9953 System Side Line Loopback #16

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R/W	SSLLB[16][12]	0
Bit 10	R/W	SSLLB[16][11]	0
Bit 9	R/W	SSLLB[16][10]	0
Bit 8	R/W	SSLLB[16][9]	0
Bit 7	R/W	SSLLB[16][8]	0
Bit 6	R/W	SSLLB[16][7]	0
Bit 5	R/W	SSLLB[16][6]	0
Bit 4	R/W	SSLLB[16][5]	0
Bit 3	R/W	SSLLB[16][4]	0
Bit 2	R/W	SSLLB[16][3]	0
Bit 1	R/W	SSLLB[16][2]	0
Bit 0	R/W	SSLLB[16][1]	0

The Loopback Register is provided at SP9953 Read/Write Address 17H.

SSLLB[16][1:12]

The system side/line loopback (SSLLB[16][1:12]) bits enable the SSLLB for the 16th STS-12/STM-4 slice. When a logic 1 is written to SSLLB[16][X], the drop system data of STS-1/STM-0 path X is looped back into the add system data of STS-1/STM-0 path X. When a logic 0 is written to SSLLB[16][X], the SSLLB is inactive.

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Register 0019H: SP9953 System Loopback Configuration

Bit	Type	Function	Default
Bit 15	R/W	Unused	0
Bit 14	R/W	Unused	0
Bit 13	R/W	Unused	0
Bit 12	R/W	Unused	0
Bit 11	R/W	SDLB[4]	0
Bit 10	R/W	SDLB[3]	0
Bit 9	R/W	SDLB[2]	0
Bit 8	R/W	SDLB[1]	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	LSSLB[4]	0
Bit 2	R/W	LSSLB[3]	0
Bit 1	R/W	LSSLB[2]	0
Bit 0	R/W	LSSLB[1]	0

The System Loopback Register is provided at SP9953 Read/Write Address 19H.

LSSLB[1:4]

The Line side/system Loopback (LSSLB[N]) bits enable the LSSLB for the N^h STS-48/STM-16 slice. When a logic 1 is written to LSSLB[N], the Transmit TRMP data of STS-48/STM-16 slice N is looped back into the Receive RRMPdata of STS-48/STM-16 slice N. When a logic 0 is written to LSSLB[N], the line side/system loopback is inactive.

Note that while enabling LSSLB[n], the Receive Overhead Port is not reliable and should not be used.

SDLB[1:4]

The System Diagnostic Loopback (SDLB[N]) bits enable the SDLB for the N^h STS-48/STM-16 slice. When a logic 1 is written to SDLB[N], the ASSI add data of STS-48/STM-16 slice N is looped back into the DSSI Drop data of STS-48/STM-16 slice N. When a logic 0 is written to SDLB[N], the system diagnostic loopback is inactive.

Note: For the SDLB to function properly, the Add and Drop frame pulses must be aligned. The easiest way to do this is to assert AFP_ON_DFP (reg 0001H), but it can also be done by adjusting AFPDLY and/or DFPDLY (registers 001AH and 001BH).

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Register 001AH: AFPDLY

Bit	Type	Function	Default
Bit 15	R/W	Unused	0
Bit 14	R/W	Unused	0
Bit 13	R/W	AFPDLY[13]	0
Bit 12	R/W	AFPDLY[12]	0
Bit 11	R/W	AFPDLY[11]	0
Bit 10	R/W	AFPDLY[10]	0
Bit 9	R/W	AFPDLY[9]	0
Bit 8	R/W	AFPDLY[8]	0
Bit 7	R/W	AFPDLY[7]	0
Bit 6	R/W	AFPDLY[6]	0
Bit 5	R/W	AFPDLY[5]	0
Bit 4	R/W	AFPDLY[4]	0
Bit 3	R/W	AFPDLY[3]	0
Bit 2	R/W	AFPDLY[2]	0
Bit 1	R/W	AFPDLY[1]	0
Bit 0	R/W	AFPDLY[0]	0

This register controls the delay from the AFP input signal to the time when the SPECTRA-9953 may safely process the J0 characters delivered by the add data links.

AFPDLY[13:0]

The Add Frame Pulse Delay bits (AFPDLY[13:0]) control the delay from the AFP pulse clock cycle, in SYSCLK cycles, inserted by the SPECTRA-9953 before processing the J0 characters delivered by the add serial data links. AFPDLY is set such that after the specified delay, all active receive links would have delivered the J0 character. AFPDLY has valid range between 0 to 9718 inclusive. The relationships of AFP, AFPDLY[13:0] and the system configuration are described later in the system add interface section

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Register 001BH: DFPDLY

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13	R/W	DFPDLY[13]	0
Bit 12	R/W	DFPDLY[12]	0
Bit 11	R/W	DFPDLY[11]	0
Bit 10	R/W	DFPDLY[10]	0
Bit 9	R/W	DFPDLY[9]	0
Bit 8	R/W	DFPDLY[8]	0
Bit 7	R/W	DFPDLY[7]	0
Bit 6	R/W	DFPDLY[6]	0
Bit 5	R/W	DFPDLY[5]	0
Bit 4	R/W	DFPDLY[4]	0
Bit 3	R/W	DFPDLY[3]	0
Bit 2	R/W	DFPDLY[2]	0
Bit 1	R/W	DFPDLY[1]	0
Bit 0	R/W	DFPDLY[0]	0

This register controls the delay from the DFP input signal to the internal DFP signal used by the SPECTRA-9953 to set the Drop bus timings.

DFPDLY[13:0]

The Drop Frame Pulse Delay bits (DFPDLY[13:0]) controls the delay from the DFP pulse clock cycle, in SYSCLK cycles, inserted by the SPECTRA-9953 before generating an internal DFP pulse. DFPDLY has valid range between 0 to 9718 inclusive.

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Register 001CH: System Side Analog Control

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	T8TE_ARSTB	1
Bit 3	R/W	R8TD_ARSTB	1
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	1
Bit 0	R/W	SYS_ARB	1

This register provides some control bits for the system side analog circuitry. This register is used for diagnostic purposes.

SYS_ARB

This is an analog reset signal for the system side CSU. To properly reset the CSU, this signal should be held low for at least 1 ms.

R8TD_ARSTB

This is an analog reset signal for the system side SIPO.

T8TE_ARSTB

This is an analog reset signal for the system side PISO.

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Register 001DH: Line Side Analog Control

Bit	Type	Function	Default
Bit 15	R/W	Unused	0
Bit 14	R/W	Unused	0
Bit 13	R/W	Unused	0
Bit 12	R/W	Unused	0
Bit 11	R/W	Unused	0
Bit 10	R/W	Unused	0
Bit 9	R/W	Unused	0
Bit 8	R/W	RESERVED	0
Bit 7	R/W	Line_ACPENB	0
Bit 6	R/W	Line_ACEN	0
Bit 5	R/W	Line_AENB	0
Bit 4	R/W	RESERVED	0
Bit 3	R/W	RESERVED	0
Bit 2	R/W	RESERVED	0
Bit 1	R/W	RESERVED	0
Bit 0	R/W	Line_ARST	0

This register provides some control bits for the line side analog circuitry. This register is used for diagnostic purposes only.

Line_ARST

Line OIF interface analog reset . When high , the line interface is held in reset. For normal operation, this bit must be set to 0

Line_AENB

OIFs interface enable bar. When low, the OIF line interface is enabled. For normal operation, this bit must be set to 0. When the OIF line interface is disabled, its clocks are not guaranteed and may currupt some indirect registers in the RHPP, THPP and TSVCA. In such a case, the entire device should be reset or the four slices reset in order to clear any currupt values on the registers. Alternately, the affected registers can be reprogrammed.

Line_ACEN

OIFs analog interface chopper clock enable. When high, offset correction circuitry is enabled.

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Line_ACPENB

Line side Charge Pump Enable bar (CPENB). When low, the charge pumps HVCPUMP within the OIFs analog interface for the LVDS receivers are enabled to increase the input range of the receivers.

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Register 001FH: Clocks Activity Monitors

Bit	Type	Function	Default
Bit 15	R	RCLKACT_155_4	0
Bit 14	R	RCLKACT_155_3	0
Bit 13	R	RCLKACT_155_2	0
Bit 12	R	RCLKACT_155_1	0
Bit 11	R	RCLKACT_77_4	0
Bit 10	R	RCLKACT_77_3	0
Bit 9	R	RCLKACT_77_2	0
Bit 8	R	RCLKACT_77_1	0
Bit 7	R	TCLKACT_155_4	0
Bit 6	R	TCLKACT_155_3	0
Bit 5	R	TCLKACT_155_2	0
Bit 4	R	TCLKACT_155_1	0
Bit 3	R	TCLKACT_77_4	0
Bit 2	R	TCLKACT_77_3	0
Bit 1	R	TCLKACT_77_2	0
Bit 0	R	TCLKACT_77_1	0

This register provides line clocks activity monitors. These bits do not necessarily detect clocking problems such as floating clocks

RCLKACT_155_[1:4]

The receive line activity monitor (RCLKACT_155_[1:4]) signals are event detectors. RCLKACT_155_[X] is asserted when a low to high transition occurs on the internal 155 MHz receive clock of slice X. RCLKACT_155 [X] is cleared when the line activity monitor register is read.

RCLKACT_77_[1:4]

The receive line activity monitor (RCLKACT_77_[1:4]) signals are event detectors. RCLKACT_77_[X] is asserted when a low to high transition occurs on the internal 77 MHz receive clock of slice X. RCLKACT_77 [X] is cleared when the line activity monitor register is read..

TCLKACT_155_[1:4]

The receive line activity monitor (TCLKACT_155_[1:4]) signals are event detectors. TCLKACT_155_[X] is asserted when a low to high transition occurs on the internal 155 MHz receive clock of slice X. TCLKACT_155 [X] is cleared when the line activity monitor register is read.

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TCLKACT_77_[1:4]

The receive line activity monitor (TCLKACT_77_[1:4]) signals are event detectors. TCLKACT_77_[X] is asserted when a low to high transition occurs on the internal 77MHz receive clock of slice X. TCLKACT_77 [X] is cleared when the line activity monitor register is read.

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Register 002DH: SPECTRA-9953 Master JTAG ID High

Bit	Type	Function	Default
Bit 15	R	ID[3]	0
Bit 14	R	ID[2]	0
Bit 13	R	ID[1]	1
Bit 12	R	ID[0]	0
Bit 11	R	DEVID[15]	0
Bit 10	R	DEVID[14]	1
Bit 9	R	DEVID[13]	0
Bit 8	R	DEVID[12]	1
Bit 7	R	DEVID[11]	0
Bit 6	R	DEVID[10]	0
Bit 5	R	DEVID[9]	1
Bit 4	R	DEVID[8]	1
Bit 3	R	DEVID[7]	0
Bit 2	R	DEVID[6]	0
Bit 1	R	DEVID[5]	0
Bit 0	R	DEVID[4]	1

The SPECTRA-9953 Master JTAG ID registers hold the jtag identification code for the device. The device revision number and device ID are available through these registers.

ID[3:0]

The ID bits can be read to provide a binary SPECTRA-9953 revision number.

DEVID[15:0]

The DEVID bits can be read to distinguish the SPECTRA-9953 from other devices. DEVID returns 5317H when read.

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Register 002EH: SPECTRA-9953 Master JTAG ID Low

Bit	Type	Function	Default
Bit 15	R	DEVID[3]	0
Bit 14	R	DEVID[2]	1
Bit 13	R	DEVID[1]	1
Bit 12	R	DEVID[0]	1
Bit 11	R	MID[11]	0
Bit 10	R	MID[10]	0
Bit 9	R	MID[9]	0
Bit 8	R	MID[8]	0
Bit 7	R	MID[7]	1
Bit 6	R	MID[6]	1
Bit 5	R	MID[5]	0
Bit 4	R	MID[4]	0
Bit 3	R	MID[3]	1
Bit 2	R	MID[2]	1
Bit 1	R	MID[1]	0
Bit 0	R	MID[0]	1

MID[11:0]

The MID bits provide the manufacturer identify field in the JTAG identification code. MID returns 0CDH when read.

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Register 002FH: SPECTRA-9953 Master User Defined

Bit	Type	Function	Default
Bit 15	R/W	FREE[15]	0
Bit 14	R/W	FREE[14]	0
Bit 13	R/W	FREE[13]	0
Bit 12	R/W	FREE[12]	0
Bit 11	R/W	FREE[11]	0
Bit 10	R/W	FREE[10]	0
Bit 9	R/W	FREE[9]	0
Bit 8	R/W	FREE[8]	0
Bit 7	R/W	FREE[7]	0
Bit 6	R/W	FREE[6]	0
Bit 5	R/W	FREE[5]	0
Bit 4	R/W	FREE[4]	0
Bit 3	R/W	FREE[3]	0
Bit 2	R/W	FREE[2]	0
Bit 1	R/W	FREE[1]	0
Bit 0	R/W	FREE[0]	0

FREE[15:0]

The FREE[15:0] register bits do not perform any function. They are free for user defined read/write operations.

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Register 0030H-003F: SP9953 Interrupt Status #1 to #16

Bit	Type	Function	Default
Bit 15	R/W	INTE[N]	0
Bit 14	R	R8TDI[N]	X
Bit 13	R	SHPII[N]	X
Bit 12	R	TSVCAI[N]	X
Bit 11	R	DLLI	X
Bit 10	R	CSTRI	X
Bit 9	R	STLII	X
Bit 8	R	SRLII	X
Bit 7	R	T8TEI[N]	X
Bit 6	R	SARCI[N]	X
Bit 5	R	RSVCAI[N]	X
Bit 4	R	PATHRTTPI[N]	X
Bit 3	R	RHPPI[N]	X
Bit 2	R	SBERI[N]	X
Bit 1	R	RTTPI[N]	X
Bit 0	R	RRMPI[N]	X

The Interrupt Status Registers are provided at SP9953 Read/Write Address 30H to 3FH.

RRMPI[N]…R8TDI[N]

The RRMPI[N] to R8TDI[N] are interrupt status indicators for the corresponding block within the STS-12/STM-4 Nth slice. The interrupt status is set to logic 1 to indicate a pending interrupt from the corresponding block. The interrupt status bits are independent of the interrupt enable bit.

Note that CSTRI, STLII, SRLII and DLLI are defined only for N=1. All others are kept at zero.

Note that SARCI, SBERI, RTTPI are defined only for N=1,5,9,13. All others are kept at zero.

INTE[N]

The interrupt enable (INTE[N]) bit controls the activation of the interrupt (INTB) output. When a logic 1 is written to INTE[N], the RRMP[N]…R8TD[N] pending interrupt will assert the interrupt (INTB) output. When a logic 0 is written to INTE[N], the RRMP[N]…R8TD[N] pending interrupt will not assert the interrupt (INTB) output.

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15.1 DLL Normal Registers

The DLL is a digital delay lock loop that is used to meet the required control signals timings on the system side bus.

Register 004CH: Configuration

Bit	Type	Function	Default
Bit 15-8	R	RESERVED	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3		Unused	X
Bit 2	R/W	ERRORE	X
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

The DLL Configuration Register controls the basic operation of the DLL.

ERRORE

The ERROR interrupt enable (ERRORE) bit enables the error indication interrupt. When ERRORE is set high, an interrupt is generated upon assertion event of the ERR output and ERROR register. When ERRORE is set low, changes in the ERROR and ERR status do not generate an interrupt.

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Register 004EH: DLL Reset

Bit	Type	Function	Default
Bit 15-8	R	Reserved	X
Bit 7	R	Reserved	X
Bit 6	R	Reserved	X
Bit 5	R	Reserved	X
Bit 4	R	Reserved	X
Bit 3	R	Reserved	X
Bit 2	R	Reserved	X
Bit 1	R	Reserved	X
Bit 0	R	Reserved	X

Writing to this register performs a software reset of the DLL. A software reset requires a maximum of 24*256 SYSCLK cycles for the DLL to regain lock. During this time the DLLCLK phase is adjusting from its current position to delay tap 0 and back to a lock position.

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Register 004FH: DLL Control Status

Bit	Type	Function	Default
Bit 15-8	R	RESERVED	X
Bit 7	R	SYSCLKI	X
Bit 6	R	REFCLKI	X
Bit 5	R	ERRORI	X
Bit 4	R	CHANGEI	X
Bit 3		Unused	X
Bit 2	R	ERROR	X
Bit 1	R	CHANGE	0
Bit 0	R	RUN	0

The DLL Control Status Register provides information of the DLL operation.

RUN

The DLL lock status register bit (RUN) indicates the DLL found a delay line tap in which the phase difference between the rising edge of REFCLK and the rising edge of SYSLCK is zero. After system reset, RUN is logic zero until the phase detector indicates an initial lock condition. When the phase detector indicates lock, RUN is set to logic 1.

The RUN register bit is cleared only by a system reset or a software reset (writing to register 4EH).

CHANGE

The delay line tap change register bit (CHANGE) indicates the DLL has moved to a new delay line tap. CHANGE is set high for eight SYSCLK cycles when the DLL moves to a new delay line tap.

ERROR

The delay line error register bit (ERROR) indicates the DLL has run out of dynamic range. When the DLL attempts to move beyond the end of the delay line, ERROR is set high. When ERROR is high, the DLL cannot generate a DLLCLK phase which causes the rising edge of REFCLK to be aligned to the rising edge of SYSCLK. ERROR is set low, when the DLL captures lock again.

CHANGEI

The delay line tap change event register bit (CHANGEI) indicates the CHANGE register bit has changed value. When the CHANGE register changes from a logic zero to a logic one, the CHANGEI register bit is set to logic one.

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When WCIMODE is low, the CHANGEI register bit is cleared immediately after it is read, thus acknowledging the event has been recorded. When WCIMODE is high, the CHANGEI register bit is cleared immediately after a logic one is written to the CHANGEI register, thus acknowledging the event has been recorded.

ERRORI

The delay line error event register bit (ERRORI) indicates the ERROR register bit has gone high. When the ERROR register changes from a logic zero to a logic one, the ERRORI register bit is set to logic one. If the ERRORE interrupt enable is high, the INT output is also asserted when ERRORI asserts.

When WCIMODE is low, the ERRORI register bit is cleared immediately after it is read, thus acknowledging the event has been recorded. When WCIMODE is high, the ERRORI register bit is cleared immediately after a logic one is written to the ERRORI register, thus acknowledging the event has been recorded.

REFCLKI

The reference clock event register bit REFCLKI provides a method to monitor activity on the reference clock. When the REFCLK primary input changes from a logic zero to a logic one, the REFCLKI register bit is set to logic one.

When WCIMODE is low, the REFCLKI register bit is cleared immediately after it is read, thus acknowledging the event has been recorded. When WCIMODE is high, the REFCLKI register bit is cleared immediately after a logic one is written to the REFCLKI register, thus acknowledging the event has been recorded.

SYSCLKI

The system clock event register bit SYSLCKI provides a method to monitor activity on the system clock. When the SYSCLK primary input changes from a logic zero to a logic one, the SYSCLKI register bit is set to logic one. The SYSCLKI register bit is cleared immediately after it is read, thus acknowledging the event has been recorded.

When WCIMODE is low, the SYSCLKI register bit is cleared immediately after it is read, thus acknowledging the event has been recorded. When WCIMODE is high, the SYSCLKI register bit is cleared immediately after a logic one is written to the SYSCLKI register, thus acknowledging the event has been recorded.

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15.2 RRMP Normal Registers

There are 16 RRMP (#1 - #16) blocks in 16 STM-4 processing slices with independent register sets. When the SPECTRA-9953 is configured for quad STS-48/STM-16 mode, RRMP #1, #5, #9, #13 are configured as masters and the remaining RRMP blocks are configured as slaves. When configured for STS-192/STM-64 mode, only RRMP #1 is configured as master and the remaining blocks are configured as slaves.

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Register 0050H: RRMP Configuration

Bit	Type	Function	Default
Bit 15	R	Reserved	X
Bit 14		Unused	
Bit 13	R/W	Reserved	0
Bit 12	R/W	LREIACCBLK	0
Bit 11	R/W	LBIPEREIBLK	0
Bit 10	R/W	LBIPEBERBLK	0
Bit 9	R/W	LBIPEACCBLK	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	SBIPEACCBLK	0
Bit 6	R/W	RLDTS	1
Bit 5	R/W	RSLDSEL	0
Bit 4	R/W	RSLDTS	1
Bit 3	R/W	LRDI3	0
Bit 2	R/W	LAIS3	0
Bit 1	R/W	ALGO2	0
Bit 0	W	FOOF	X

The Configuration Register is provided at RRMP Read/Write Address 00H. This register is only valid for master slices.

FOOF

The force out of frame (FOOF) bit forces out of frame condition. When a logic 1 is written to FOOF, the framer block is forced out of frame at the next frame boundary regardless of the framing pattern value. The OOF event initiates re framing in an upstream frame detector.

ALGO2

The ALGO2 bit selects the framing pattern used to determine and maintain the frame alignment. When ALGO2 is set to logic 1, the framing pattern consist of the 8 bits of the first A1 framing bytes and the first 4 bits of the last A2 framing bytes (12 bits total). When ALGO2 is set to logic 0, the framing patterns consist of all the A1 framing bytes and all the A2 framing bytes.

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LAIS3

The line alarm indication signal detection (LAIS3) bit selects the Line AIS detection algorithm. When LAIS3 is set to logic 1, Line AIS is declared when a 111 pattern is detected in bits 6,7,8 of the K2 byte for three consecutive frames. When LAIS3 is set to logic 0, Line AIS is declared when a 111 pattern is detected in bits 6,7,8 of the K2 byte for five consecutive frames.

LRDI3

The line remote defect indication detection (LRDI3) bit selects the Line RDI detection algorithm. When LRDI3 is set to logic 1, Line RDI is declared when a 110 pattern is detected in bits 6,7,8 of the K2 byte for three consecutive frames. When LRDI3 is set to logic 0, Line RDI is declared when a 110 pattern is detected in bits 6,7,8 of the K2 byte for five consecutive frames.

RSLDTS

The RSLD tri-state control (RSLDTS) bit controls the RSLDCLK and RSLD output ports. When RSLDTS is set to logic 1, the RSLDCLK and RSLD output ports are tri-state. When RSLDTS is set to logic 0, the RSLDCLK and RSLD output ports are enabled.

RSLDSEL

The receive section line data communication channel select (RSLDSEL) bit selects the contents of the RSLD serial output and the frequency of the RSLDCLK clock.

RSLDSEL	Contents	RSLDCLK
0	Section DCC (D1-D3)	Nominal 192 kHz
1	Line DCC (D4-D12)	Nominal 576 kHz

RLDTS

The RLD tri-state control (RLDTS) bit controls the RLDCLK and RLD output ports. When RLDTS is set to logic 1, the RLDCLK and RLD output ports are tri-state. When RLDTS is set to logic 0, the RLDCLK and RLD output ports are enabled.

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SBIPEACCBLK

The section BIP error accumulation block (SBIPEACCBLK) bit controls the accumulation of section BIP errors. When SBIPEACCBLK is set to logic 1, the section BIP accumulation represents BIP-8 block errors (a maximum of 1 error per frame). When SBIPEACCBLK is set to logic 0, the section BIP accumulation represents BIP-8 errors (a maximum of 8 errors per frame).

LBIPEACCBLK

The line BIP error accumulation block (LBIPEACCBLK) bit controls the accumulation of line BIP errors. When LBIPEACCBLK is set to logic 1, the line BIP accumulation represents BIP-24 block errors (a maximum of 1 error per STS-3/STM-1 per frame). When LBIPEACCBLK is set to logic 0, the line BIP accumulation represents BIP-8 errors (a maximum of 8 errors per STS-1/STM-0 per frame).

LBIPEBERBLK:

The line BIP error BER block (LBIPEBERBLK) bit controls the indication of line BIP errors for the BER. When LBIPEBERBLK is set to logic 1, the line BIP represents BIP-24 block errors (a maximum of 1 error per STS-3/STM-1 per frame). When LBIPEBERBLK is set to logic 0, the line BIP represents BIP-8 errors (a maximum of 8 errors per STS-1/STM-0 per frame).

LBIPEREIBLK

The line BIP error REI block (LBIPEREIBLK) bit controls the indication of line BIP errors for the REI. When LBIPEREIBLK is set to logic 1, the line BIP represents BIP-24 block errors (a maximum of 1 error per STS-3/STM-1 per frame saturated to 255). When LBIPEREIBLK is set to logic 0, the line BIP represents BIP-8 errors (a maximum of 8 errors per STS-1/STM-0 per frame saturated to 255).

LREIACCBLK

The line REI accumulation block (LREIACCBLK) bit controls the extraction and accumulation of line REI errors from the M1 byte. When LREIACCBLK is set to logic 1, the extracted line REI are interpreted as block BIP-24 errors (a maximum of 1 error per STS-3/STM-1 per frame). When LREIACCBLK is set to logic 0, the extracted line REI are interpreted as BIP-8 errors (a maximum of 8 errors per STS-1/STM-0 per frame).

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Register 0051H: RRMP Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R	APSBFV	X
Bit 4	R	LRDIV	X
Bit 3	R	LAISV	X
Bit 2	R	LOSV	X
Bit 1	R	LOFV	X
Bit 0	R	OOFV	X

These register bits are only valid for master slices.

OOFV

The OOFV bit reflects the current status of the out of frame defect. The OOF defect is declared when four consecutive frames have one or more bit error in their framing pattern. The OOF defect is cleared when two error free framing pattern are found.

LOFV

The LOFV bit reflects the current status of the loss of frame defect. The LOF defect is declared when an out of frame condition exists for a total period of 3 ms during which there is no continuous in frame period of 3 ms. The LOF defect is cleared when an in frame condition exists for a continuous period of 3 ms.

LOSV

The LOSV bit reflects the current status of the loss of signal defect. The LOS defect is declared when 20 µs of consecutive all zeros pattern is detected. The LOS defect is cleared when two consecutive error free framing patterns are found and during the intervening time (one frame) there is no violating period of consecutive all zeros pattern.

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LAISV

The LAISV bit reflects the current status of the line alarm indication signal defect. The AIS-L defect is declared when the 111 pattern is detected in bits 6,7 and 8 of the K2 byte for three or five consecutive frames. The AIS-L defect is cleared when any pattern other than 111 is detected in bits 6, 7, and 8 of the K2 byte for three or five consecutive frames.

LRDIV

The LRDIV bit reflects the current status of the line remote defect indication signal defect. The RDI-L defect is declared when the 110 pattern is detected in bits 6, 7, and 8 of the k2 byte for three or five consecutive frames. The RDI-L defect is cleared when any pattern other than 110 is detected in bits 6, 7, and 8 of the K2 byte for three or five consecutive frames.

APSBFV

The APSBF bit reflects the current status of the APS byte failure defect. The APS byte failure defect is declared when no three consecutive identical K1 bytes are received in the last twelve consecutive frames starting with the last frame containing a previously consistent byte. The APS byte failure defect is cleared when three consecutive identical K1 bytes are received.

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Register 0052H: RRMP Interrupt Enable

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10	R/W	LREIEE	0
Bit 9	R/W	LBIPEE	0
Bit 8	R/W	SBIPEE	0
Bit 7	R/W	COSSME	0
Bit 6	R/W	COAPSE	0
Bit 5	R/W	APSBFE	0
Bit 4	R/W	LRDIE	0
Bit 3	R/W	LAISE	0
Bit 2	R/W	LOSE	0
Bit 1	R/W	LOFE	0
Bit 0	R/W	OOFE	0

These register bits are only valid for master slices. For slave slices, they should be set to their default values.

OOFE, LOFE, LOSE, LAISE, LRDIE, APSBFE, COAPSE, COSSME, SBIPEE, LBIPEE, LREIEE

The interrupt enable bits controls the activation of the interrupt (INTB) output. When the interrupt enable bit is set to logic 1, the corresponding pending interrupt will assert the interrupt (INTB) output. When the interrupt enable bit is set to logic 0, the corresponding pending interrupt will not assert the interrupt (INTB) output.

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Register 0053H: RRMP Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10	R/W	LREIEI	X
Bit 9	R/W	LBIPEI	X
Bit 8	R/W	SBIPEI	X
Bit 7	R/W	COSSMI	X
Bit 6	R/W	COAPSI	X
Bit 5	R/W	APSBFI	X
Bit 4	R/W	LRDII	X
Bit 3	R/W	LAISI	X
Bit 2	R/W	LOSI	X
Bit 1	R/W	LOFI	X
Bit 0	R/W	OOFI	X

These register bits are only valid for master slices. For slave slices, they should be ignored.

If the WCIMODE bit in the SPECTRA-9953 Master Reset and Configuration Register (Register 0000H) is set high, these interrupt status bits are cleared on a write of logic one. Otherwise, these interrupt status bits are cleared on read.

OOFI

The out of frame interrupt status (OOFI) bit is an event indicator. OOFI is set to logic 1 to indicate any change in the status of OOFV. The interrupt status bit is independent of the interrupt enable bit. OOFI is cleared to logic 0 when this register is read or written as described above.

LOFI

The loss of frame interrupt status (LOFI) bit is an event indicator. LOFI is set to logic 1 to indicate any change in the status of LOFV. The interrupt status bit is independent of the interrupt enable bit. LOFI is cleared to logic 0 when this register is read or written as described above.

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LOSI

The loss of signal interrupt status (LOSI) bit is an event indicator. LOSI is set to logic 1 to indicate any change in the status of LOSV. The interrupt status bit is independent of the interrupt enable bit. LOSI is cleared to logic 0 when this register is read or written as described above.

LAISI

The line alarm indication signal interrupt status (LAISI) bit is an event indicator. LAISI is set to logic 1 to indicate any change in the status of LAISV. The interrupt status bit is independent of the interrupt enable bit. LAISI is cleared to logic 0 when this register is read or written as described above.

LRDII

The line remote defect indication interrupt status (LRDII) bit is an event indicator. LRDII is set to logic 1 to indicate any change in the status of LRDIV. The interrupt status bit is independent of the interrupt enable bit. LRDII is cleared to logic 0 when this register is read or written as described above.

APSBFI

The APS byte failure interrupt status (APSBFI) bit is an event indicator. APSBFI is set to logic 1 to indicate any change in the status of APSBFV. The interrupt status bit is independent of the interrupt enable bit. APSBFI is cleared to logic 0 when this register is read or written as described above.

COAPSI

The change of APS bytes interrupt status (COAPSI) bit is an event indicator. COAPSI is set to logic 1 to indicate a new APS bytes, which is declared when new a K1/K2 pattern has been received for 3 consecutive frames. The interrupt status bit is independent of the interrupt enable bit. COAPSI is cleared to logic 0 when this register is read or written as described above.

COSSMI

The change of SSM message interrupt status (COSSMI) bit is an event indicator. COSSMI is set to logic 1 to indicate a new SSM message, which is declared when a new S1 byte has been received for 1 or 8 consecutive frames (depending on the FLTRSSM setting). The interrupt status bit is independent of the interrupt enable bit. COSSMI is cleared to logic 0 when this register is read or written as described above.

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SBIPEI

The section BIP error interrupt status (SBIPEI) bit is an event indicator. SBIPEI is set to logic 1 to indicate a section BIP error. The interrupt status bit is independent of the interrupt enable bit. SBIPEI is cleared to logic 0 when this register is read or written as described above.

LBIPEI

The line BIP error interrupt status (LBIPEI) bit is an event indicator. LBIPEI is set to logic 1 to indicate a line BIP error. The interrupt status bit is independent of the interrupt enable bit. LBIPEI is cleared to logic 0 when this register is read or written as described above.

LREIEI

The line REI error interrupt status (LREIEI) bit is an event indicator. LREIEI is set to logic 1 to indicate a line REI error. The interrupt status bit is independent of the interrupt enable bit. LREIEI is cleared to logic 0 when this register is read or written as described above.

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Register 0054H: RRMP Receive APS

Bit	Type	Function	Default
Bit 15	R	K1V[7]	X
Bit 14	R	K1V[6]	X
Bit 13	R	K1V[5]	X
Bit 12	R	K1V[4]	X
Bit 11	R	K1V[3]	X
Bit 10	R	K1V[2]	X
Bit 9	R	K1V[1]	X
Bit 8	R	K1V[0]	X
Bit 7	R	K2V[7]	X
Bit 6	R	K2V[6]	X
Bit 5	R	K2V[5]	X
Bit 4	R	K2V[4]	X
Bit 3	R	K2V[3]	X
Bit 2	R	K2V[2]	X
Bit 1	R	K2V[1]	X
Bit 0	R	K2V[0]	X

These register bits are only valid for master slices. For slave slices, they should be ignored.

K1V[7:0]/K2V[7:0]

The APS K1/K2 bytes value (K1V[7:0]/K2V[7:0]) bits represent the extracted K1/K2 APS bytes. K1V/K2V is updated when the same K1 and K2 bytes (forming a single entity) are received for three consecutive frames.

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Register 0055H: RRMP Receive SSM

Bit	Type	Function	Default
Bit 15	R/W	BYTESSM	0
Bit 14	R/W	FLTRSSM	0
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R	SSMV[7]	X
Bit 6	R	SSMV[6]	X
Bit 5	R	SSMV[5]	X
Bit 4	R	SSMV[4]	X
Bit 3	R	SSMV[3]	X
Bit 2	R	SSMV[2]	X
Bit 1	R	SSMV[1]	X
Bit 0	R	SSMV[0]	X

These register bits are only valid for master slices. For slave slices, they should be ignored or written to their default values.

SSMV[7:0]

The synchronization status message value (SSMV[7:0]) bits represent the extracted S1 nibble (or byte). When filtering is enabled via the FLTRSSM register bit, SSMV is updated when the same S1 nibble (or byte) is received for eight consecutive frames. When filtering is disabled, SSMV is updated every frame.

FLTRSSM

The filter synchronization status message (FLTRSSM) bit enables the filtering of the SSM nibble (or byte). When FLTRSSM is set to logic 1, the SSM value is updated when the same SSM is received for eight consecutive frames. When FLTRSSM is set to logic 0, the SSM value is updated every frame.

BYTESSM

The byte synchronization status message (BYTESSM) bit extends the SSM from a nibble to a byte. When BYTESSM is set to logic 1, the SSM is a byte and bits 1 to 8 of the S1 byte are considered. When BYTESSM is set to logic 0, the SSM is a nibble and only bits 5 to 8 of the S1 byte are considered.

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Register 0056H: RRMP AIS Enable

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	Unused	0
Bit 3	R/W	RLAISINS	0
Bit 2	R/W	RLAISEN	0
Bit 1	R/W	RLOHAISEN	0
Bit 0	R/W	RSOHAISEN	0

These register bits are valid for both master and slave slices. Please refer to individual bit for details.

RSOHAISEN

The receive section overhead AIS enable (RSOHAISEN) bit enables AIS insertion on RTOH and RSLD when carrying section overhead bytes. When RSOHAISEN is set to logic 1, all ones are forced on the section overhead bytes when AIS-L is declared. When RSOHAISEN is set to logic 0, no AIS are forced on the section overhead bytes regardless of the AIS-L status.

This bit should be set to logic 1 for normal operation. This bit is valid for master and slave slices.

RLOHAISEN

The receive line overhead AIS enable (RLOHAISEN) bit enables AIS insertion on RTOH, RLD and RSLD when carrying line overhead bytes. When RLOHAISEN is set to logic 1, all ones are forced on the line overhead bytes when AIS-L is declared. When RLOHAISEN is set to logic 0, no AIS are forced on the line overhead bytes regardless of the AIS-L status.

This bit should be set to logic 1 for normal operation. This bit is valid for master and slave slices.

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RLAISEN

The receive line AIS enable (RLAISEN) bit enables line AIS insertion in the outgoing data stream. When RLAISEN is set to logic 1, line AIS is inserted in the outgoing data stream when AIS-L is declared. When RLAISEN is set to logic 0, no line AIS is inserted regardless of the AIS-L status.

This bit should be set to logic 1 for normal operation. This bit is valid for master and slave slices.

RLAISINS

The receive line AIS insertion (RLAISIN) bit forces line AIS insertion in the outgoing data stream. When RLAISINS is set to logic 1, all ones are inserted in the line overhead bytes and in the payload bytes (all the bytes of the frame except the section overhead bytes) to force a line AIS condition. When RLAISINS is set to logic 0, the line AIS condition is removed.

This bit is valid for master and slave slices.

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Register 0057H: RRMP Section BIP Error Counter

Bit	Type	Function	Default
Bit 15	R	SBIPE[15]	X
Bit 14	R	SBIPE[14]	X
Bit 13	R	SBIPE[13]	X
Bit 12	R	SBIPE[12]	X
Bit 11	R	SBIPE[11]	X
Bit 10	R	SBIPE[10]	X
Bit 9	R	SBIPE[9]	X
Bit 8	R	SBIPE[8]	X
Bit 7	R	SBIPE[7]	X
Bit 6	R	SBIPE[6]	X
Bit 5	R	SBIPE[5]	X
Bit 4	R	SBIPE[4]	X
Bit 3	R	SBIPE[3]	X
Bit 2	R	SBIPE[2]	X
Bit 1	R	SBIPE[1]	X
Bit 0	R	SBIPE[0]	X

These register bits are only valid for master slices.

SBIPE[15:0]

The section BIP error (SBIPE[15:0]) bits represent the number of section BIP errors that have been detected since the last accumulation interval. The error counter is transferred to the holding registers by a microprocessor write to any of the RRMP counter registers of a particular master slice or the SPECTRA-9953 master configuration register (0000H).

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Register 0058H: RRMP Line BIP Error Counter (LSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R	LBIPE[15:0]	XXXX

Register 0059H: RRMP Line BIP Error Counter (MSB)

Bit	Type	Function	Default
Bit 15 to Bit 8		Unused	
Bit 7 to Bit 0	R	LBIPE[23:16]	XX

These register bits are only valid for master slices.

LBIPE[23:0]

The line BIP error (LBIPE[23:0]) bits represent the number of line BIP errors that have been detected since the last accumulation interval. The error counter is transferred to the holding registers by a microprocessor write to any of the RRMP counter registers or the SPECTRA-9953 master configuration register (0000H).

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Register 005AH: RRMP Line REI Error Counter (LSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R	LREIE[15:0]	XXXX

Register 005BH: RRMP Line REI Error Counter (MSB)

Bit	Type	Function	Default
Bit 15 to Bit 8		Unused	
Bit 7 to Bit 0	R	LREIE[23:16]	XX

These register bits are only valid for master slices.

LREIE[23:0]

The line REI error (LREIE[23:0]) bits represent the number of line REI errors that have been detected since the last accumulation interval. The error counter is transferred to the holding registers by a microprocessor write to any of the RRMP counter registers or the SPECTRA-9953 master configuration register (0000H).

15.3 SRLI_192 Normal Registers

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Register 0069H: Synchronization Error Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6		Unused	
Bit 5		Unused	
Bit 4		Unused	
Bit 3	R/W	SYNC_ERR4I	0
Bit 2	R/W	SYNC_ERR3I	0
Bit 1	R/W	SYNC_ERR2I	0
Bit 0	R/W	SYNC_ERR1I	0

Clear mode of interrupts depends on the WCIMODE input value. When WCIMODE is zero, all the interrupts are cleared when they are read. When WCIMODE is one, a given interrupt is cleared only if a logic one is being written in its corresponding bit.

SYNC_ERR1-4I

The Synchronization Error Interrupt status (SYNC_ERR1-4I) bit is an event indicator. SYNC_ERR1-4I is set to logic one to indicate a change in the status of SYNC_ERR1-4V. The interrupt bit is independent of the interrupt enable.

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Register 006AH: Synchronization Error Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6		Unused	
Bit 5		Unused	
Bit 4		Unused	
Bit 3	R	SYNC_ERR4V	X0
Bit 2	R	SYNC_ERR3V	X0
Bit 1	R	SYNC_ERR2V	X0
Bit 0	R	SYNC_ERR1V	X0

SYNC_ERR1-4V

The Synchronization Error status (SYNC_ERR1-4V) bits, reflects the current status of the SYNC_ERR1-4 input signals. The SYNC_ERR1-4 is logic one when the CRSU detects that there might be a synchronization problem.

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Register 006BH: Synchronization Error Interrupt Enable

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6		Unused	
Bit 5		Unused	
Bit 4		Unused	
Bit 3	R/W	SYNC_ERR4E	0
Bit 2	R/W	SYNC_ERR3E	0
Bit 1	R/W	SYNC_ERR2E	0
Bit 0	R/W	SYNC_ERR1E	0

SYNC_ERR1-4E

The Synchronization Error Interrupt Enable (SYNC_ERR1-4E) bit controls the activation of the interrupt (INTB) output upon reception of an SYNC_ERR1-4I. If SYNC_ERR1-4E is set to logic one, the SYNC_ERR1-4I will assert the interrupt (INTB) output. When SYNC_ERR1-4E is logic zero, the SYNC_ERR1-4I pending interrupt will not assert the interrupt (INTB).

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Register 006CH: Programmable Clock Configuration

Bit	Type	Function	Default
Bit 15	R/W	PGMRCLKSEL[1]	0
Bit 14	R/W	PGMRCLKSEL[0]	0
Bit 13	R/W	PGMRCLKSRC[1]	0
Bit 12	R/W	PGMRCLKSRC[0]	0
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

PGMRCLKSEL[1:0]

The receive programmable clock frequency, enables and selects the frequency of the outputted clock on PGMRCLK.

PGMRCLKSEL[1:0]	Clock Frequency
00	Disabled
01	8 kHz
10	19.44 MHz
11	77.76 MHz

PGMRCLKSRC[1:0]

In Quad mode, the receive programmable clock source, selects which one of the four input clocks is used to generate the PGMRCLK clock.

PGMRCLKSRC[1:0]	Clock source
00	RXCLK1
01	RXCLK2
10	RXCLK3
11	RXCLK4

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Register 006DH: Synchronize Error Configuration

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6		Unused	
Bit 5		Unused	
Bit 4		Unused	
Bit 3	R/W	ERR_ENA4	0
Bit 2	R/W	ERR_ENA3	0
Bit 1	R/W	ERR_ENA2	0
Bit 0	R/W	ERR_ENA1	0

ERR_ENA1-4

The error enable register bits enable the SYNC_ERR1-4 inputs.

When processing an STS-192/STM-64, the received data-stream is zeroed when ERR_ENA1 is logic 1 and SYNC_ERR1 is asserted. When processing a QUAD-STS-48/STM-16, the received STS-48(I) is zeroed when ERR_ENA(I) is set to logic1 and SYNC_ERR(I) is asserted.

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Register 006EH: Four Bytes De-Interleaver (FBDI) Control

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6		Unused	
Bit 5		Unused	
Bit 4		Unused	
Bit 3	R/W	FBDIEN4	1
Bit 2	R/W	FBDIEN3	1
Bit 1	R/W	FBDIEN2	1
Bit 0	R/W	FBDIEN1	1

The Four Bytes De-Interleaver control Register is provided at SRLI_192 Read/Write Address EH.

FBDIEN1-4

The FBDI enable (FBDIEN1-4) bit controls the Four-Byte De-Interleaver (FBDI) block. When FBDIENx is set to logic 1, the FBDI block is active and the bytes on the SRLI output bus are de-interleaved. When FBDIENx is set to logic 0, the FBDI block is inactive.

When used in STS-192 (STM-64), only FBDIEN1 is valid and FBDIEN2-4 are ignored.

15.4 SBER Normal Registers

There are 4 SBER (#1 - #4) blocks in 4 STM-16 processing groups with independent register sets. When the SPECTRA-9953 is configured for quad STS-48/STM-16 mode, all four blocks are configured as masters to process the STS-48c/STM-16c data streams. When configured for STS-192/STM-64 mode, only SBER#1 is configured as master and the other three (#2 - #4) blocks are inactive and may be considered as slaves.

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Register 0080H: SBER Configuration

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	SFBERTEN	0
Bit 4	R/W	SFSMODE	0
Bit 3	R/W	SFCMODE	0
Bit 2	R/W	SDBERTEN	0
Bit 1	R/W	SDSMODE	0
Bit 0	R/W	SDCMODE	0

SDCMODE

The SDCMODE alarm bit selects the Signal Degrade BERM window size to use for clearing alarms. When SDCMODE is a logic 0, the SD BERM will clear an alarm using the same window size used for declaration. When SDCMODE is a logic 1, the SD BERM will clear an alarm using a window size that is 8 times longer than alarm declaration window size. The declaration window size is defined by the SBER SD BERM Accumulation Period register.

SDSMODE

The SDSMODE bit selects the Signal Degrade BERM saturation mode. When SDSMODE is a logic 0, the SD BERM will saturate the BIP count on a per frame basis using the SBER SD Saturation Threshold register value. When SDSMODE is a logic 1, the SD BERM will saturate the BIP count on a per window subtotals accumulation period basis using the SBER SD Saturation Threshold register value.

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SDBERTEN

The SDBERTEN bit enables automatic monitoring of line bit error rate threshold events by the Signal Degrade BERM. When SDBERTEN is a logic one, the SD BERM continuously monitors line BIP errors over a period defined in the BERM configuration registers. When SDBERTEN is a logic zero, the SD BERM BIP accumulation logic is disabled and the BERM logic is reset to restart in the declaration monitoring state.

All SD BERM configuration registers should be set up before the monitoring is enabled.

SFCMODE

The SFCMODE alarm bit selects the Signal Failure BERM window size to use for clearing alarms. When SFCMODE is a logic 0, the SF BERM will clear an alarm using the same window size used for declaration. When SFCMODE is a logic 1, the SF BERM will clear an alarm using a window size that is 8 times longer than alarm declaration window size. The declaration window size is defined by the SBER SF BERM Accumulation Period register.

SFSMODE

The SFSMODE bit selects the Signal Failure BERM saturation mode. When SFSMODE is a logic 0, the SF BERM will saturate the BIP count on a per frame basis using the SBER SF Saturation Threshold register value. When SFSMODE is a logic 1, the SF BERM will saturate the BIP count on a per window subtotals accumulation period basis using the SBER SD Saturation Threshold register value.

SFBERTEN

The SFBERTEN bit enables automatic monitoring of line bit error rate threshold events by the Signal Failure BERM. When SFBERTEN is a logic one, the SF BERM continuously monitors line BIP errors over a period defined in the BERM configuration registers. When SFBERTEN is a logic zero, the SF BERM BIP accumulation logic is disabled, and the BERM logic is reset to restart in the declaration monitoring state.

All SF BERM configuration registers should be set up before the monitoring is enabled.

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Register 0081H: SBER Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R	SFBERV	X
Bit 0	R	SDBERV	X

SDBERV

The SDBERV bit indicates the Signal Failure BERM alarm state. The alarm is declared (SDBERV is a logic one) when the declaring threshold has been exceeded. The alarm is removed (SDBERV is a logic zero) when the clearing threshold has been reached.

SFBERV

The SFBERV bit indicates the Signal Failure BERM alarm state. The alarm is declared (SFBERV is a logic one) when the declaring threshold has been exceeded. The alarm is removed (SFBERV is a logic zero) when the clearing threshold has been reached.

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Register 0082H: SBER Interrupt Enable

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	SFBERE	0
Bit 0	R/W	SDBERE	0

SDBERE

The SDBERE bit is the interrupt enable for the SDBER alarm. When SDBERE set to logic 1, the pending interrupt in the SBER Interrupt Status register, SDBERI, will assert the interrupt (INTB) output. When SDBERE is set to logic 0, the pending interrupt will not assert the interrupt (INTB) output.

SFBERE

The SFBERE bit is the interrupt enable for the SFBER alarm. When SFBERE set to logic 1, the pending interrupt in the SBER Interrupt Status Register, SFBERI, will assert the interrupt (INTB) output. When SFBERE is set to logic 0, the pending interrupt will not assert the interrupt (INTB) output.

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Register 0083H: SBER Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R	SFBERI	X
Bit 0	R	SDBERI	X

If the WCIMODE bit in the SPECTRA-9953 Master Reset and Configuration Register (Register 0000H) is set high, these interrupt status bits are cleared on a write of logic one. Otherwise, these interrupt status bits are cleared on read.

SDBERI

The SDBERI bit is an event indicator set to logic 1 to indicate any changes in the status of SDBERV. This interrupt status bit is independent of the SDBERE interrupt enable bits.

SFBERI

The SFBERI bit is an event indicator set to logic 1 to indicate any changes in the status of SFBERV. This interrupt status bit is independent of the SFBERE interrupt enable bits.

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Register 0084H: SBER SF BERM Accumulation Period (LSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R/W	SFSAP[15:0]	0000

Register 0085H: SBER SF BERM Accumulation Period (MSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R/W	SFSAP[31:16]	0000

SFSAP[31:0]

The SFSAP[31:0] bits represent the number of STS-N frames to be used to accumulate a BIP error subtotal. The total evaluation window to declare an alarm is broken into 8 subtotals, so this register value represents 1/8 of the total sliding window size. Refer to the Operation section for the recommended settings.

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Register 0086H: SBER SF BERM Saturation Threshold (LSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R/W	SFSATH[15:0]	FFFF

Register 0087H: SBER SF BERM Saturation Threshold (MSB)

Bit	Type	Function	Default
Bit 15 to Bit 8		Unused	XX
Bit 7 to Bit 0	R/W	SFSATH[23:16]	FF

SFSATH[23:0]

The SFSTH[23:0] bits represent the allowable number of BIP errors that can be accumulated during a BIP accumulation period before a BER threshold event is asserted. Setting this threshold to 0xFFFFFF disables the saturation functionality. Refer to the Operation section for the recommended settings..

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Register 0088H: SBER SF BERM Declaring Threshold (LSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R/W	SFDECTH[15:0]	0000

Register 0089H: SBER SF BERM Declaring Threshold (MSB)

Bit	Type	Function	Default
Bit 15 to Bit 8		Unused	XX
Bit 7 to Bit 0	R/W	SFDECTH [23:16]	00

SFDECTH[23:0]

The SFDECTH[23:0] register represents the number of BIP errors that must be accumulated during a full evaluation window in order to declare a BER alarm. Refer to the Operation section for the recommended settings.

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Register 008AH: SBER SF BERM Clearing Threshold (LSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R/W	SFCLRTH[15:0]	0000

Register 008BH: SBER SF BERM Clearing Threshold (MSB)

Bit	Type	Function	Default
Bit 15 to Bit 8		Unused	XX
Bit 7 to Bit 0	R/W	SFCLRTH [23:16]	00

SFCLRTH[23:0]

The SFCLRTH[23:0] register represents the number of BIP errors that can be accumulated but not exceeded during a full evaluation window in order to clear a BER alarm. Refer to the Operation section for the recommended settings.

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Register 008CH: SBER SD BERM Accumulation Period (LSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R/W	SDSAP[15:0]	0000

Register 008DH: SBER SD BERM Accumulation Period (MSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R/W	SDSAP[31:16]	0000

SDSAP[31:0]

The SDSAP[31:0] bits represent the number of STS-N frames to be used to accumulate a BIP error subtotal. The total evaluation window to declare an alarm is broken into 8 subtotals, so this register value represents 1/8 of the total sliding window size. Refer to the Operation section for the recommended settings.

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Register 008EH: SBER SD BERM Saturation Threshold (LSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R/W	SDSATH[15:0]	FFFF

Register 008FH: SBER SD BERM Saturation Threshold (MSB)

Bit	Type	Function	Default
Bit 15 to Bit 8		Unused	XX
Bit 7 to Bit 0	R/W	SDSATH[23:16]	FF

SDSATH[23:0]

The SDSATH[23:0] bits represent the allowable number of BIP errors that can be accumulated during a BIP accumulation period before a BER threshold event is asserted. Setting this threshold to 0xFFFFFFFF disables the saturation functionality. Refer to the Operation section for the recommended settings.

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Register 0090H: SBER SD BERM Declaring Threshold (LSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R/W	SDDECTH[15:0]	0000

Register 0091H: SBER SD BERM Declaring Threshold (MSB)

Bit	Type	Function	Default
Bit 15 to Bit 8		Unused	XX
Bit 7 to Bit 0	R/W	SDDECTH[23:16]	00

SDDECTH[23:0]

The SDDECTH[23:0] register represents the number of BIP errors that must be accumulated during a full evaluation window in order to declare a BER alarm. Refer to the Operation section for the recommended settings.

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Register 0092H: SBER SD BERM Clearing Threshold (LSB)

Bit	Type	Function	Default
Bit 15 to Bit 0	R/W	SDCLRTH[15:0]	0000

Register 0093H: SBER SD BERM Clearing Threshold (MSB)

Bit	Type	Function	Default
Bit 15 to Bit 8		Unused	XX
Bit 7 to Bit 0	R/W	SDCLRTH[23:16]	00

SDCLRTH[23:0]

The SDCLRTH[23:0] register represents the number of BIP errors that can be accumulated but not exceeded during a full evaluation window in order to clear a BER alarm. Refer to the Operation section for the recommended settings.

15.5 RTTP Section Normal Registers

There are 4 Section RTTP (#1 - #4) blocks in 4 STM-16 processing groups with independent register sets. When the SPECTRA-9953 is configured for quad STS-48/STM-16 mode, all four blocks are configured as masters to process the STS-48c/STM-16c data streams. When configured for STS-192/STM-64 mode, only RTTP #1 is configured as master and the other three (#2 - #4) blocks are inactive and may be considered as slaves.

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Register 00A0H: RTTP Section Indirect Address

Bit	Type	Function	Default
Bit 15	R	BUSY	X
Bit 14	R/W	RWB	0
Bit 13	R/W	IADDR[7]	0
Bit 12	R/W	IADDR[6]	0
Bit 11	R/W	IADDR[5]	0
Bit 10	R/W	IADDR[4]	0
Bit 9	R/W	IADDR[3]	0
Bit 8	R/W	IADDR[2]	0
Bit 7	R/W	IADDR[1]	0
Bit 6	R/W	IADDR[0]	0
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	PATH[3]	0
Bit 2	R/W	PATH[2]	0
Bit 1	R/W	PATH[1]	0
Bit 0	R/W	PATH[0]	0

PATH[3:0]

PATH[3:0] must be set to “0001” for proper operation of the RTTP Section.

IADDR[7:0]

The indirect address location (IADDR[7:0]) bits select which indirect address location is accessed by the current indirect transfer.

Indirect Address IADDR[7:0]	Indirect Data
0000 0000	Configuration
0000 0001 to 0011 1111	Invalid address
0100 0000	First byte of the 1/16/64 byte captured trace
0100 0001 to 0111 1111	Other bytes of the 16/64 byte captured trace
1000 0000	First byte of the 1/16/64 byte accepted trace
1000 0001 to 1011 1111	Other bytes of the 16/64 byte accepted trace
1100 0000	First byte of the 16/64 byte expected trace

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Indirect Address IADDR[7:0]	Indirect Data
1100 0001 to 1111 1111	Other bytes of the 16/64 byte expected trace

RWB

The active high read and active low write (RWB) bit selects if the current access to the internal RAM is an indirect read or an indirect write. Writing to the Indirect Address Register initiates an access to the internal RAM. When RWB is set to logic 1, an indirect read access to the RAM is initiated. The data from the addressed location in the internal RAM will be transferred to the Indirect Data Register. When RWB is set to logic 0, an indirect write access to the RAM is initiated. The data from the Indirect Data Register will be transferred to the addressed location in the internal RAM.

BUSY

The active high RAM busy (BUSY) bit reports if a previously initiated indirect access to the internal RAM has been completed. BUSY is set to logic 1 upon writing to the Indirect Address Register. BUSY is set to logic 0, upon completion of the RAM access. This register should be polled to determine when new data is available in the Indirect Data Register.

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Register 00A1H: RTTP Section Indirect Data

Bit	Type	Function	Default
Bit 15	R/W	Unused	X
Bit 14	R/W	Unused	X
Bit 13	R/W	Unused	X
Bit 12	R/W	Unused	X
Bit 11	R/W	Unused	X
Bit 10	R/W	Unused	X
Bit 9	R/W	Unused	X
Bit 8	R/W	Unused	X
Bit 7	R/W	DATA[7]	X
Bit 6	R/W	DATA[6]	X
Bit 5	R/W	DATA[5]	X
Bit 4	R/W	DATA[4]	X
Bit 3	R/W	DATA[3]	X
Bit 2	R/W	DATA[2]	X
Bit 1	R/W	DATA[1]	X
Bit 0	R/W	DATA[0]	X

DATA[7:0]

The indirect access data (DATA[7:0]) bits hold the data transfer to or from the internal RAM during indirect access. When RWB is set to logic 1 (indirect read), the data from the addressed location in the internal RAM will be transfer to DATA[7:0]. BUSY should be polled to determine when the new data is available in DATA[7:0]. When RWB is set to logic 0 (indirect write), the data from DATA[7:0] will be transferred to the addressed location in the internal RAM. The Indirect Data register must contain valid data before the indirect write is initiated by writing to the Indirect Address Register.

DATA[7:0] has a different meaning depending on which address of the internal RAM is being accessed.

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Register 00A1H (Indirect Register 00H): RTTP Section Trace Configuration

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6	R/W	SYNC_CRLF	0
Bit 5	R/W	ZEROEN	0
Bit 4	R/W	PER5	0
Bit 3	R/W	NOSYNC	0
Bit 2	R/W	LENGTH16	0
Bit 1	R/W	ALGO[1]	0
Bit 0	R/W	ALGO[0]	0

ALGO[1:0]

The trail trace algorithm select (ALGO[1:0]) bits select the algorithm used to process the trail trace message.

ALGO[1:0]	Trail Trace Algorithm
00	Algorithm disable
01	Algorithm 1
10	Algorithm 2
11	Algorithm 3

When ALGO[1:0] is set to logic 00b, the trail trace algorithms are disabled and received messages are not monitored. The corresponding TIUV, TIMV register bits and the corresponding TIU, TIM output signals are set to logic 0.

LENGTH16

The message length (LENGTH16) bit selects the length of the trail trace message used by algorithm 1 and algorithm 2. When LENGTH16 is set to logic 1, the length of the trail trace message is 16 bytes. When LENGTH16 is set to logic 0, the length of the trail trace message is 64 bytes.

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NOSYNC

The synchronization disable (NOSYNC) bit disables the synchronization of the trail trace message in algorithm 1 and algorithm 2. When NOSYNC is set to logic 1, no synchronization is done on the trail trace message. The bytes of the trail trace message are written in the captured page as in a circular buffer. When NOSYNC is set to logic 0, synchronization is done on the trail trace message. See SYNC_CRLF to determine how synchronization is handled when NOSYNC = 0.

PER5

The message persistency (PER5) bit selects the number of multi-frames (messages) a trail trace message must receive in order to be declared persistent in algorithm 2. When PER5 is set to logic 1, the same trail trace message must be received for 5 consecutive multi-frames to be declared persistent. When PER5 is set to logic 0, the same trail trace message must be received for 3 consecutive multi-frames to be declared persistent.

ZEROEN

The all zero message enable (ZEROEN) bit selects if the all zero messages are validated or not against the expected message in algorithm 1 and algorithm 2. When ZEROEN is set to logic 1, all zero captured messages in algorithm 1 and all zero accepted messages in algorithm 2 are validated against the expected message. A match is declared when both the captured/accepted message and the expected message are all zero. When ZEROEN is set to logic 0, all zero captured messages in algorithm 1 and all zero accepted messages in algorithm 2 are not validated against the expected message but are considered match. A match is declared when the captured/accepted message is all zero regardless of the expected message.

SYNC_CRLF

The synchronization on CR/LF characters (SYNC_CRLF) bit selects if the current algorithm (except algo3) synchronizes on the CR/LF ASCII characters or on the byte with its MSB set high. When SYNC_CRLF is set to logic 1, the current algorithm synchronizes when it receives a byte containing the ASCII character “CR” (carriage return) followed by a byte containing “LF” (line feed). The current active byte then becomes the last byte of the message. When SYNC_CRLF is set to 0, the current algorithm synchronizes when receiving a byte with its MSB set to logic 1. The current active byte then becomes the first byte of the message.

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Register 00A1H (Indirect Register 40H to 7FH): RTTP Section Captured Trace

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R	CTRACE[7]	X
Bit 6	R	CTRACE[6]	X
Bit 5	R	CTRACE[5]	X
Bit 4	R	CTRACE[4]	X
Bit 3	R	CTRACE[3]	X
Bit 2	R	CTRACE[2]	X
Bit 1	R	CTRACE[1]	X
Bit 0	R	CTRACE[0]	X

CTRACE[7:0]

The captured trail trace message (CTRACE[7:0]) bits contain the currently received trail trace message. When algorithm 1 or 2 is selected and LENGTH16 is set to logic 1, the captured message is stored between address 40h and 4Fh. When algorithm 1 or 2 is selected and LENGTH16 is set to logic 0, the captured message is stored between address 40h and 7Fh. When NOSYNC is set to logic 1, the captured message is not synchronized. When NOSYNC is set to logic 0, the captured message is synchronized and the first byte of the message is stored at address 40h. When algorithm 3 is selected, the captured byte is stored at address 40h.

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Register 00A1H (Indirect Register 80H to BFH): RTTP Section Accepted Trace

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R	ATRACE[7]	X
Bit 6	R	ATRACE[6]	X
Bit 5	R	ATRACE[5]	X
Bit 4	R	ATRACE[4]	X
Bit 3	R	ATRACE[3]	X
Bit 2	R	ATRACE[2]	X
Bit 1	R	ATRACE[1]	X
Bit 0	R	ATRACE[0]	X

ATRACE[7:0]

The accepted trail trace message (ATRACE[7:0]) bits contain the persistent trail trace message. When algorithm 1 is selected, the accepted trail trace will not be updated. When algorithm 2 is selected and PER5 is set to logic 1, the accepted message is the same trail trace message received for 5 consecutive multi-frames. When algorithm 2 is selected and PER5 is set to logic 0, the accepted message is the same trail trace message received for 3 consecutive multi-frames. When algorithm 2 is selected and LENGTH16 is set to logic 1, the accepted message is stored between address 80h and 8Fh. When algorithm 2 is selected and LENGTH16 is set to logic 0, the accepted message is stored between address 80h and BFh. When algorithm 3 is selected, the accepted byte is the same trail trace byte received for 48 frames. When algorithm 3 is selected, the accepted byte is stored at address 80h.

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Register 00A1H (Indirect Register C0H to FFH): RTTP Section Expected Trace

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R/W	ETRACE[7]	X
Bit 6	R/W	ETRACE[6]	X
Bit 5	R/W	ETRACE[5]	X
Bit 4	R/W	ETRACE[4]	X
Bit 3	R/W	ETRACE[3]	X
Bit 2	R/W	ETRACE[2]	X
Bit 1	R/W	ETRACE[1]	X
Bit 0	R/W	ETRACE[0]	X

ETRACE[7:0]

The expected trail trace message (ETRACE[7:0]) bits contain a static message written by an external microprocessor. In algorithm 1 the expected message is used to validated the captured message. In algorithm 2 the expected message is used to validate the accepted message. When LENGTH16 is set to logic 1, the expected message must be written between address C0h and CFh. When LENGTH16 is set to logic 0, the accepted message must be written between address C0h and FFh.

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Register 00A2H: RTTP Section Trace Unstable Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R	TIUV	X

TIUV

Algorithm 1: TIUV is set to logic 0.

Algorithm 2: TIUV is set to logic 1 when one or more erroneous bytes are detected between the current message and the previous message in a total of 8 trail trace messages without any persistent message in between. TIUV is set to logic 0 when a persistent message is found. A persistent message is found when the same message is receive for 3 or 5 consecutive multi-frames.

Algorithm 3: TIUV is set to logic 1 when one or more erroneous bytes are detected in three consecutive sixteen byte windows. The first window starts on the first erroneous trail trace byte. TIUV is set to logic 0 when the same trail trace byte is received for 48 consecutive frames.

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Register 00A3H: RTTP Section Trace Unstable Interrupt Enable

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R/W	TIUE	0

TIUE

The trace identifier unstable interrupt enable (TIUE) bit controls the activation of the interrupt (INTB) output. When this bit location is set to logic 1, the corresponding pending interrupt will assert the interrupt (INTB) output. When this bit location is set to logic 0, the corresponding pending interrupt will not assert the interrupt (INTB) output.

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Register 00A4H: RTTP Section Trace Unstable Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R	TIUI	X

If the WCIMODE bit in the SPECTRA-9953 Master Reset and Configuration Register (Register 0000H) is set high, these interrupt status bits are cleared on a write of logic one. Otherwise, these interrupt status bits are cleared on read.

TIUI

The trace identifier unstable interrupt status (TIUI) bit is an event indicator. TIUI is set to logic 1 to indicate any changes in the status of TIUV (stable to unstable, unstable to stable). This interrupt status bit is independent of the interrupt enable bit.

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Register 00A5H: RTTP Section Trace Mismatch Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R	TIMV	X

TIMV

Algorithm 1: TIMV is set to logic 1 when none of the last 20 messages matches the expected message. TIMV is set to logic 0 when 16 of the last 20 messages match the expected message.

Algorithm 2: TIMV is set to logic 1 when the accepted message does not match the expected message. TIMV is set to logic 0 when the accepted message matches the expected message.

Algorithm 3: TIMV is set to logic 0.

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Register 00A6H: RTTP Section Trace Mismatch Interrupt Enable

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R/W	TIME	0

TIME

The trace identifier mismatch interrupt enable (TIME) bit controls the activation of the interrupt (INTB) output. When this bit location is set to logic 1, the corresponding pending interrupt will assert the interrupt (INTB) output. When this bit location is set to logic 0, the corresponding pending interrupt will not assert the interrupt (INTB) output.

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Register 00A7H: RTTP Section Trace Mismatch Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R	TIMI	X

If the WCIMODE bit in the SPECTRA-9953 Master Reset and Configuration Register (Register 0000H) is set high, these interrupt status bits are cleared on a write of logic one. Otherwise, these interrupt status bits are cleared on read.

TIMI

The trace identifier mismatch interrupt status (TIMI) bit is an event indicator. TIMI is set to logic 1 to indicate any changes in the status of TIMV (match to mismatch, mismatch to match). This interrupt status bit is independent of the interrupt enable bit.

15.6 RTTP Path Normal Registers

There are 16 Path RTTP (#1 - #16) blocks in 16 STM-4 processing groups with independent register sets. Each RTTP Path processes up to 12 paths.

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Register 00B0H: RTTP Path Indirect Address

Bit	Type	Function	Default
Bit 15	R	BUSY	X
Bit 14	R/W	RWB	0
Bit 13	R/W	IADDR[7]	0
Bit 12	R/W	IADDR[6]	0
Bit 11	R/W	IADDR[5]	0
Bit 10	R/W	IADDR[4]	0
Bit 9	R/W	IADDR[3]	0
Bit 8	R/W	IADDR[2]	0
Bit 7	R/W	IADDR[1]	0
Bit 6	R/W	IADDR[0]	0
Bit 5		Unused	
Bit 4		Unused	
Bit 3	R/W	PATH[3]	0
Bit 2	R/W	PATH[2]	0
Bit 1	R/W	PATH[1]	0
Bit 0	R/W	PATH[0]	0

PATH[3:0]

The STS-1/STM-0 path (PATH[3:0]) bits select which STS-1/STM-0 path is accessed by the current indirect transfer. Only values “0001” to “1100” are valid. Paths #1 to #12 are valid when processing 12 STS-1/STM-0. Paths #1 to #4 are valid when processing 4 STS-3c/STM-1 and finally only path #1 is valid when processing an STS-12c/STM-4.

IADDR[7:0]

The indirect address location (IADDR[7:0]) bits select which indirect address location is accessed by the current indirect transfer.

Indirect Address IADDR[7:0]	Indirect Data
0000 0000	Configuration
0000 0001 to 0011 1111	Invalid address
0100 0000	First byte of the 1/16/64 byte captured trace
0100 0001 to 0111 1111	Other bytes of the 16/64 byte captured trace
1000 0000	First byte of the 1/16/64 byte accepted trace
1000 0001 to	Other bytes of the 16/64 byte accepted trace

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Indirect Address IADDR[7:0]	Indirect Data
1011 1111	
1100 0000	First byte of the 16/64 byte expected trace
1100 0001 to 1111 1111	Other bytes of the 16/64 byte expected trace

RWB

The active high read and active low write (RWB) bit selects if the current access to the internal RAM is an indirect read or an indirect write. Writing to the Indirect Address Register initiates an access to the internal RAM. When RWB is set to logic 1, an indirect read access to the RAM is initiated. The data from the addressed location in the internal RAM will be transferred to the Indirect Data Register. When RWB is set to logic 0, an indirect write access to the RAM is initiated. The data from the Indirect Data Register will be transferred to the addressed location in the internal RAM.

BUSY

The active high RAM busy (BUSY) bit reports if a previously initiated indirect access to the internal RAM has been completed. BUSY is set to logic 1 upon writing to the Indirect Address Register. BUSY is set to logic 0, upon completion of the RAM access. This register should be polled to determine when new data is available in the Indirect Data Register.

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Register 00B1H: RTTP Path Indirect Data

Bit	Type	Function	Default
Bit 15	R/W	Unused	X
Bit 14	R/W	Unused	X
Bit 13	R/W	Unused	X
Bit 12	R/W	Unused	X
Bit 11	R/W	Unused	X
Bit 10	R/W	Unused	X
Bit 9	R/W	Unused	X
Bit 8	R/W	Unused	X
Bit 7	R/W	DATA[7]	X
Bit 6	R/W	DATA[6]	X
Bit 5	R/W	DATA[5]	X
Bit 4	R/W	DATA[4]	X
Bit 3	R/W	DATA[3]	X
Bit 2	R/W	DATA[2]	X
Bit 1	R/W	DATA[1]	X
Bit 0	R/W	DATA[0]	X

DATA[7:0]

The indirect access data (DATA[7:0]) bits hold the data transfer to or from the internal RAM during indirect access. When RWB is set to logic 1 (indirect read), the data from the addressed location in the internal RAM will be transfer to DATA[7:0]. BUSY should be polled to determine when the new data is available in DATA[7:0]. When RWB is set to logic 0 (indirect write), the data from DATA[7:0] will be transferred to the addressed location in the internal RAM. The Indirect Data register must contain valid data before the indirect write is initiated by writing to the Indirect Address Register.

DATA[7:0] has a different meaning depending on which address of the internal RAM is being accessed.

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Register 00B1H (Indirect Register 00H): RTTP Path Trace Configuration

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6	R/W	SYNC_CRLF	0
Bit 5	R/W	ZEROEN	0
Bit 4	R/W	PER5	0
Bit 3	R/W	NOSYNC	0
Bit 2	R/W	LENGTH16	0
Bit 1	R/W	ALGO[1]	0
Bit 0	R/W	ALGO[0]	0

ALGO[1:0]

The trail trace algorithm select (ALGO[1:0]) bits select the algorithm used to process the trail trace message.

ALGO[1:0]	Trail trace algorithm
00	Algorithm disable
01	Algorithm 1
10	Algorithm 2
11	Algorithm 3

When ALGO[1:0] is set to logic 00b, the trail trace algorithms are disabled. The corresponding TIUV, TIMV register bits and the corresponding TIU, TIM output signals are set to logic 0. The ALGO[1:0] bits should be set to 00b for slave paths. Otherwise, TIMV and TIUV alarms may persist for slave timeslots.

LENGTH16

The message length (LENGTH16) bit selects the length of the trail trace message used by algorithm 1 and algorithm 2. When LENGTH16 is set to logic 1, the length of the trail trace message is 16 bytes. When LENGTH16 is set to logic 0, the length of the trail trace message is 64 bytes.

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NOSYNC

The synchronization disable (NOSYNC) bit disables the synchronization of the trail trace message in algorithm 1 and algorithm 2. When NOSYNC is set to logic 1, no synchronization is done on the trail trace message. The bytes of the trail trace message are written in the captured page as in a circular buffer. When NOSYNC is set to logic 0, synchronization is done on the trail trace message. See SYNC_CRLF to determine how synchronization is handled when NOSYNC = 0.

PER5

The message persistency (PER5) bit selects the number of multi-frames (messages) a trail trace message must receive in order to be declared persistent in algorithm 2. When PER5 is set to logic 1, the same trail trace message must be received for 5 consecutive multi-frames to be declared persistent. When PER5 is set to logic 0, the same trail trace message must be received for 3 consecutive multi-frames to be declared persistent.

ZEROEN

The all zero message enable (ZEROEN) bit selects if the all zero messages are validated or not against the expected message in algorithm 1 and algorithm 2. When ZEROEN is set to logic 1, all zero captured messages in algorithm 1 and all zero accepted messages in algorithm 2 are validated against the expected message. A match is declared when both the captured/accepted message and the expected message are all zero. When ZEROEN is set to logic 0, all zero captured messages in algorithm 1 and all zero accepted messages in algorithm 2 are not validated against the expected message but are considered match. A match is declared when the captured/accepted message is all zero regardless of the expected message.

SYNC_CRLF

The synchronization on CR/LF characters (SYNC_CRLF) bit selects if the current algorithm (except algo3) synchronizes on the CR/LF ASCII characters or on the byte with its MSB set high. When SYNC_CRLF is set to logic 1, the current algorithm synchronizes when it receives a byte containing the ASCII character “CR” (carriage return) followed by a byte containing “LF” (line feed). The current active byte then becomes the last byte of the message. When SYNC_CRLF is set to 0, the current algorithm synchronizes when receiving a byte with its MSB set to logic 1. The current active byte then becomes the first byte of the message.

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Register 00B1H (Indirect Register 40H to 7FH): RTTP Path Captured Trace

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7	R	CTRACE[7]	X
Bit 6	R	CTRACE[6]	X
Bit 5	R	CTRACE[5]	X
Bit 4	R	CTRACE[4]	X
Bit 3	R	CTRACE[3]	X
Bit 2	R	CTRACE[2]	X
Bit 1	R	CTRACE[1]	X
Bit 0	R	CTRACE[0]	X

CTRACE[7:0]

The captured trail trace message (CTRACE[7:0]) bits contain the currently received trail trace message. When algorithm 1 or 2 is selected and LENGTH16 is set to logic 1, the captured message is stored between address 40h and 4Fh. When algorithm 1 or 2 is selected and LENGTH16 is set to logic 0, the captured message is stored between address 40h and 7Fh. When NOSYNC is set to logic 1, the captured message is not synchronized. When NOSYNC is set to logic 0, the captured message is synchronized and the first byte of the message is stored at address 40h. When algorithm 3 is selected, the captured byte is stored at address 40h.

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Register 00B1H (Indirect Register 80H to BFH): RTTP Path Accepted Trace

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7	R	ATRACE[7]	X
Bit 6	R	ATRACE[6]	X
Bit 5	R	ATRACE[5]	X
Bit 4	R	ATRACE[4]	X
Bit 3	R	ATRACE[3]	X
Bit 2	R	ATRACE[2]	X
Bit 1	R	ATRACE[1]	X
Bit 0	R	ATRACE[0]	X

ATRACE[7:0]

The accepted trail trace message (ATRACE[7:0]) bits contain the persistent trail trace message. When algorithm 1 is selected, the accepted trail trace message will not be updated. When algorithm 2 is selected and PER5 is set to logic 1, the accepted message is the same trail trace message received for 5 consecutive multi-frames. When algorithm 2 is selected and PER5 is set to logic 0, the accepted message is the same trail trace message received for 3 consecutive multi-frames. When algorithm 2 is selected and LENGTH16 is set to logic 1, the accepted message is stored between address 80h and 8Fh. When algorithm 2 is selected and LENGTH16 is set to logic 0, the accepted message is stored between address 80h and BFh. When algorithm 3 is selected, the accepted byte is the same trail trace byte received for 48 frames. When algorithm 3 is selected, the accepted byte is stored at address 80h.

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Register 00B1H (Indirect Register C0H to FFH): RTTP Path Expected Trace

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7	R/W	ETRACE[7]	X
Bit 6	R/W	ETRACE[6]	X
Bit 5	R/W	ETRACE[5]	X
Bit 4	R/W	ETRACE[4]	X
Bit 3	R/W	ETRACE[3]	X
Bit 2	R/W	ETRACE[2]	X
Bit 1	R/W	ETRACE[1]	X
Bit 0	R/W	ETRACE[0]	X

ETRACE[7:0]

The expected trail trace message (ETRACE[7:0]) bits contain a static message written by an external microprocessor. In algorithm 1 the expected message is used to validated the captured message. In algorithm 2 the expected message is used to validate the accepted message. When LENGTH16 is set to logic 1, the expected message must be written between address C0h and CFh. When LENGTH16 is set to logic 0, the accepted message must be written between address C0h and FFh.

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Register 00B2H: RTTP Path Trace Unstable Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R	TIUV[12]	X
Bit 10	R	TIUV[11]	X
Bit 9	R	TIUV[10]	X
Bit 8	R	TIUV[9]	X
Bit 7	R	TIUV[8]	X
Bit 6	R	TIUV[7]	X
Bit 5	R	TIUV[6]	X
Bit 4	R	TIUV[5]	X
Bit 3	R	TIUV[4]	X
Bit 2	R	TIUV[3]	X
Bit 1	R	TIUV[2]	X
Bit 0	R	TIUV[1]	X

TIUV[12:1].

The trace identifier unstable status bits indicate the current status of the TIU defects for STS-1/STM-0 paths #1 to #12

Algorithm 1: TIUV is set to logic 0.

Algorithm 2: TIUV is set to logic 1 when one or more erroneous bytes are detected between the current message and the previous message in a total of 8 trail trace messages without any persistent message in between. TIUV is set to logic 0 when a persistent message is found. A persistent message is found when the same message is receive for 3 or 5 consecutive multi-frames.

Algorithm 3: TIUV is set to logic 1 when one or more erroneous bytes are detected in three consecutive sixteen byte windows. The first window starts on the first erroneous trail trace byte. TIUV is set to logic 0 when the same trail trace byte is received for 48 consecutive frames.

Note: If a path is reconfigured from master to slave, and the path previously had a TIU defect, then the defect may persist after the config change. For this reason, ALGO[1:0] bits should be set to 00b (algorithm disable) for slave paths. This will clear any lingering defects on slave paths.

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Register 00B3H: RTTP Path Trace Unstable Interrupt Enable

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R/W	TIUE[12]	0
Bit 10	R/W	TIUE[11]	0
Bit 9	R/W	TIUE[10]	0
Bit 8	R/W	TIUE[9]	0
Bit 7	R/W	TIUE[8]	0
Bit 6	R/W	TIUE[7]	0
Bit 5	R/W	TIUE[6]	0
Bit 4	R/W	TIUE[5]	0
Bit 3	R/W	TIUE[4]	0
Bit 2	R/W	TIUE[3]	0
Bit 1	R/W	TIUE[2]	0
Bit 0	R/W	TIUE[1]	0

TIUE[12:1]

The trace identifier unstable interrupt enable (TIUE[12:1]) bits control the activation of the interrupt (INTB) output for the corresponding STS-1/STM-0 paths #1 to #12. When this bit location is set to logic 1, the corresponding pending interrupt will assert the interrupt (INTB) output. When this bit location is set to logic 0, the corresponding pending interrupt will not assert the interrupt (INTB) output.

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Register 00B4H: RTTP Path Trace Unstable Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R	TIUI[12]	X
Bit 10	R	TIUI[11]	X
Bit 9	R	TIUI[10]	X
Bit 8	R	TIUI[9]	X
Bit 7	R	TIUI[8]	X
Bit 6	R	TIUI[7]	X
Bit 5	R	TIUI[6]	X
Bit 4	R	TIUI[5]	X
Bit 3	R	TIUI[4]	X
Bit 2	R	TIUI[3]	X
Bit 1	R	TIUI[2]	X
Bit 0	R	TIUI[1]	X

If the WCIMODE bit in the SPECTRA-9953 Master Reset and Configuration Register (Register 0000H) is set high, these interrupt status bits are cleared on a write of logic one. Otherwise, these interrupt status bits are cleared on read.

TIUI[12:1]

The trace identifier unstable interrupt status (TIUI[12:1]) bit is an event indicator. TIUI[N] is set to logic 1 to indicate any changes in the status of TIUV[N] (stable to unstable, unstable to stable) for the corresponding STS-1/STM-0 path #1 to #12. This interrupt status bit is independent of the interrupt enable bit.

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Register 00B5H: RTTP Path Trace Mismatch Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R	TIMV[12]	X
Bit 10	R	TIMV[11]	X
Bit 9	R	TIMV[10]	X
Bit 8	R	TIMV[9]	X
Bit 7	R	TIMV[8]	X
Bit 6	R	TIMV[7]	X
Bit 5	R	TIMV[6]	X
Bit 4	R	TIMV[5]	X
Bit 3	R	TIMV[4]	X
Bit 2	R	TIMV[3]	X
Bit 1	R	TIMV[2]	X
Bit 0	R	TIMV[1]	X

TIMV[12:1]

The trace identifier mismatch status TIMV[12:1] bit indicate the current status of the TIM defects for STS-1/STM-0 paths #1 to #12.

Algorithm 1: TIMV is set to logic 1 when none of the last 20 messages matches the expected message. TIMV is set to logic 0 when 16 of the last 20 messages match the expected message.

Algorithm 2: TIMV is set to logic 1 when the accepted message does not match the expected message. TIMV is set to logic 0 when the accepted message matches the expected message.

Algorithm 3: TIMV is set to logic 0.

Note: If a path is reconfigured from master to slave, and the path previously had a TIM defect, then the defect may persist after the config change. For this reason, ALGO[1:0] bits should be set to 00b (algorithm disable) for slave paths. This will clear any lingering defects on slave paths.

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Register 00B6H: RTTP Path Trace Mismatch Interrupt Enable

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R/W	TIME[12]	0
Bit 10	R/W	TIME[11]	0
Bit 9	R/W	TIME[10]	0
Bit 8	R/W	TIME[9]	0
Bit 7	R/W	TIME[8]	0
Bit 6	R/W	TIME[7]	0
Bit 5	R/W	TIME[6]	0
Bit 4	R/W	TIME[5]	0
Bit 3	R/W	TIME[4]	0
Bit 2	R/W	TIME[3]	0
Bit 1	R/W	TIME[2]	0
Bit 0	R/W	TIME[1]	0

TIME[12:1]

The trace identifier mismatch interrupt enable (TIME) bit controls the activation of the interrupt (INTB) output for the corresponding STS-1/STM-0 paths #1 to #12. When this bit location is set to logic 1, the corresponding pending interrupt will assert the interrupt (INTB) output. When this bit location is set to logic 0, the corresponding pending interrupt will not assert the interrupt (INTB) output.

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Register 00B7H: RTTP Path Trace Mismatch Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R	TIMI[12]	X
Bit 10	R	TIMI[11]	X
Bit 9	R	TIMI[10]	X
Bit 8	R	TIMI[9]	X
Bit 7	R	TIMI[8]	X
Bit 6	R	TIMI[7]	X
Bit 5	R	TIMI[6]	X
Bit 4	R	TIMI[5]	X
Bit 3	R	TIMI[4]	X
Bit 2	R	TIMI[3]	X
Bit 1	R	TIMI[2]	X
Bit 0	R	TIMI[1]	X

If the WCIMODE bit in the SPECTRA-9953 Master Reset and Configuration Register (Register 0000H) is set high, these interrupt status bits are cleared on a write of logic one. Otherwise, these interrupt status bits are cleared on read.

TIMI[12:1]

The trace identifier mismatch interrupt status (TIMI) bits are event indicators. TIMI[N] is set to logic 1 to indicate any changes in the status of TIMV[N] (match to mismatch, mismatch to match). This interrupt status bit is independent of the interrupt enable bit.

15.7 RSVCA Normal Registers

There are 16 RSVCA (#1 - #16) blocks in 16 STM-4 processing slices with independent register sets. The master/slave configuration for the RSVCAs depends on the payload mapping and is thus defined using top-level registers 0002H and 0003H as well as each RSVCA Payload Configuration register.

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Register 00C0H: RSVCA Indirect Address

Bit	Type	Function	Default
Bit 15	R	BUSY	X
Bit 14	R/W	RWB	0
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7	R/W	IADDR[1]	0
Bit 6	R/W	IADDR[0]	0
Bit 5		Unused	
Bit 4		Unused	
Bit 3	R/W	PATH[3]	0
Bit 2	R/W	PATH[2]	0
Bit 1	R/W	PATH[1]	0
Bit 0	R/W	PATH[0]	0

The Indirect Address Register is provided at SVCA Read/Write Address 00H.

RWB

The active high read and active low write (RWB) bit selects if the current access to the internal RAM is an indirect read or an indirect write. Writing to the Indirect Address Register initiates an access to the internal RAM. When RWB is set to logic 1, an indirect read access to the RAM is initiated. The data from the addressed location in the internal RAM will be transferred to the Indirect Data Register. When RWB is set to logic 0, an indirect write access to the RAM is initiated. The data from the Indirect Data Register will be transferred to the addressed location in the internal RAM.

BUSY

The active high RAM busy (BUSY) bit reports if a previously initiated indirect access to the internal RAM has been completed. BUSY is set to logic 1 upon writing to the Indirect Address Register. BUSY is set to logic 0, upon completion of the RAM access. This register should be polled to determine when new data is available in the Indirect Data Register.

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PATH[3:0]

The STS-1/STM-0 path (PATH[3:0]) bits select which STS-1/STM-0 path is accessed by the current indirect transfer. PATH[3:0] should only be written with master path locations. A read operation from an indirect register on a slave path returns the value from the master path. Also, slave path indirect registers are overwritten with the master path's indirect value. As such, when an RSVCA processes 12 x STS-1, all 12 indirect register paths are valid, while when an RSVCA processes an STS-12c, only the path #1 is valid. When an RSVCA is configured as a slave, path #1 is still valid.

PATH[3:0]	STS-1/STM-0 path #
0000	Invalid path
0001-1100	Path #1 to Path #12
1101-1111	Invalid path

IADDR[1:0]

The address location (ADDR[1:0]) bits select which address location is accessed by the current indirect transfer.

IADDR[1:0]	Indirect Register
00	SVCA Outgoing Positive Justification Performance Monitor
01	SVCA Outgoing Negative Justification Performance Monitor
10	SVCA Diagnostic/Configuration Register
11	Unused

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Register 00C1H: RSVCA Indirect Read/Write Data

Bit	Type	Function	Default
Bit 15	R/W	DATA[15]	0
Bit 14	R/W	DATA[14]	0
Bit 13	R/W	DATA[13]	0
Bit 12	R/W	DATA[12]	0
Bit 11	R/W	DATA[11]	0
Bit 10	R/W	DATA[10]	0
Bit 9	R/W	DATA[9]	0
Bit 8	R/W	DATA[8]	0
Bit 7	R/W	DATA[7]	0
Bit 6	R/W	DATA[6]	0
Bit 5	R/W	DATA[5]	0
Bit 4	R/W	DATA[4]	0
Bit 3	R/W	DATA[3]	0
Bit 2	R/W	DATA[2]	0
Bit 1	R/W	DATA[1]	0
Bit 0	R/W	DATA[0]	0

The Indirect Data Register is provided at SVCA Read/Write Address 01H.

DATA[15:0]

The indirect access data (DATA[15:0]) bits hold the data transfer to or from the internal RAM during indirect access. When RWB is set to logic 1 (indirect read), the data from the addressed location in the internal RAM will be transferred to DATA[15:0]. BUSY should be polled to determine when the new data is available in DATA[15:0]. When RWB is set to logic 0 (indirect write), the data from DATA[15:0] will be transferred to the addressed location in the internal RAM. The indirect Data register must contain valid data before the indirect write is initiated by writing to the Indirect Address Register.

DATA[15:0] has a different meaning depending on which address of the internal RAM is being accessed.

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Register 00C2H: RSVCA Payload Configuration Register[5]

Bit	Type	Function	Default
Bit 15	R/W	STS12CSL	0
Bit 14	R/W	STS12C	0
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	STS3C[4]	0
Bit 2	R/W	STS3C[3]	0
Bit 1	R/W	STS3C[2]	0
Bit 0	R/W	STS3C[1]	0

The Payload Configuration Register is provided at SVCA Read/Write Address 02H.

Note: there is a possibility that SVCA indirect registers can be corrupted upon path reconfiguration. Refer to section 14.13 for more explanation and how to avoid the problem.

STS3C[1]

The STS-3c (VC-4) payload configuration (STS3C[1]) bit selects the payload configuration. When STS3C[1] is set to logic 1, the STS-1/STM-0 paths #1, #5 and #9 are part of an STS-3c (VC-4) payload. When STS3C[1] is set to logic 0, the paths are STS-1 (VC-3) payloads. The STS12C register bit has precedence over the STS3C[1] register bit.

STS3C[2]

The STS-3c (VC-4) payload configuration (STS3C[2]) bit selects the payload configuration. When STS3C[2] is set to logic 1, the STS-1/STM-0 paths #2, #6 and #10 are part of an STS-3c (VC-4) payload. When STS3C[2] is set to logic 0, the paths are STS-1 (VC-3) payloads. The STS12C register bit has precedence over the STS3C[2] register bit.

[5] STS12CSL has precedence over all.

STS12C has precedence over STS3C configuration bits.

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STS3C[3]

The STS-3c (VC-4) payload configuration (STS3C[3]) bit selects the payload configuration. When STS3C[3] is set to logic 1, the STS-1/STM-0 paths #3, #7 and #11 are part of an STS-3c (VC-4) payload. When STS3C[3] is set to logic 0, the paths are STS-1 (VC-3) payloads. The STS12C register bit has precedence over the STS3C[3] register bit.

STS3C[4]

The STS-3c (VC-4) payload configuration (STS3C[4]) bit selects the payload configuration. When STS3C[4] is set to logic 1, the STS-1/STM-0 paths #4, #8 and #12 are part of an STS-3c (VC-4) payload. When STS3C[4] is set to logic 0, the paths are STS-1 (VC-3) payloads. The STS12C register bit has precedence over the STS3C[4] register bit.

STS12C

The STS-12c (VC-4-4c) payload configuration (STS12C) bit selects the payload configuration. When STS12C is set to logic 1, the STS-1/STM-0 paths #1 to #12 are part of an STS-12c (VC-4-4c) payload. When STS12C is set to logic 0, the STS-1/STM-0 paths are defined with the STS3C[1:4] register bit. The STS12C register bit is OR'ed with the STS12C device receive configuration 2 (0002H) register bit. The STS12C register bit has precedence over the STS3C[1:4] register bit.

STS12CSL

The STS-12c/VC-4-4c slave concatenation (STS12CSL) signal enables the slave processing of an STS-12c/VC-4-4c payload. When STS12CSL is logic one, the SVCA process a slave STS-12c/VC-4-4c payload. When STS12CSL is logic zero, the SVCA process a master STS-12c/VC-4-4c payload. One master SVCA and three slaves SVCA can be used to process an STS-48c/VC-4-16c payload. One master SVCA and fifteen slaves SVCA can be used to process an STS-192c/VC-4-64c payload. The STS12CSL register bit is OR'ed with the device receive configuration 3 (0003H) STS12CSL register bit. The STS12CSL register bit has precedence over the STS3C[1:4] register bit.

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Register 00C3H: RSVCA Positive Pointer Justification Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R	PPJI[12]	0
Bit 10	R	PPJI[11]	0
Bit 9	R	PPJI[10]	0
Bit 8	R	PPJI[9]	0
Bit 7	R	PPJI[8]	0
Bit 6	R	PPJI[7]	0
Bit 5	R	PPJI[6]	0
Bit 4	R	PPJI[5]	0
Bit 3	R	PPJI[4]	0
Bit 2	R	PPJI[3]	0
Bit 1	R	PPJI[2]	0
Bit 0	R	PPJI[1]	0

The Positive Pointer Justification Interrupt Status Register is provided at SVCA Read/Write Address 03H.

PPJI[12:1]

The positive pointer justification interrupt status (PPJI[12:1]) bits are event indicators for STS-1/STM-0 paths #1 to #12. PPJI[12:1] are set to logic 1 to indicate a positive pointer justification event in the outgoing data stream. These interrupt status bits are independent of the interrupt enable bits. PPJI[12:1] are cleared to logic 0 when this register is read and WCIMODE input is logic 0. Each bit is independently cleared when WCIMODE is logic 1 and a write access with the corresponding bit is set to 1 is performed.

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Register 00C4H: RSVCA Negative Pointer Justification Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R	NPJI[12]	0
Bit 10	R	NPJI[11]	0
Bit 9	R	NPJI[10]	0
Bit 8	R	NPJI[9]	0
Bit 7	R	NPJI[8]	0
Bit 6	R	NPJI[7]	0
Bit 5	R	NPJI[6]	0
Bit 4	R	NPJI[5]	0
Bit 3	R	NPJI[4]	0
Bit 2	R	NPJI[3]	0
Bit 1	R	NPJI[2]	0
Bit 0	R	NPJI[1]	0

The Negative Pointer Justification Interrupt Status Register is provided at SVCA Read/Write Address 04H.

NPJI[12:1]

The negative pointer justification interrupt status (NPJI[12:1]) bits are event indicators for STS-1/STM-0 paths #1 to #12. NPJI[12:1] are set to logic 1 to indicate a negative pointer justification event in the outgoing data stream. These interrupt status bits are independent of the interrupt enable bits. NPJI[12:1] are cleared to logic 0 when this register is read and WCIMODE input is logic 0. Each bit is independently cleared when WCIMODE is logic 1 and a write access with the corresponding bit is set to 1 is performed.

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Register 00C5H: RSVCA FIFO Overflow Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R	FOVRI[12]	0
Bit 10	R	FOVRI[11]	0
Bit 9	R	FOVRI[10]	0
Bit 8	R	FOVRI[9]	0
Bit 7	R	FOVRI[8]	0
Bit 6	R	FOVRI[7]	0
Bit 5	R	FOVRI[6]	0
Bit 4	R	FOVRI[5]	0
Bit 3	R	FOVRI[4]	0
Bit 2	R	FOVRI[3]	0
Bit 1	R	FOVRI[2]	0
Bit 0	R	FOVRI[1]	0

The FIFO overflow Event Interrupt Status Register is provided at SVCA Read/Write Address 05H.

FOVRI[12:1]

The FIFO overflow event interrupt status (FOVRI[12:1]) bits are event indicators for STS-1/STM-0 paths #1 to #12. FOVRI[12:1] are set to logic 1 to indicate a FIFO overflow event. These interrupt status bits are independent of the interrupt enable bits. FOVRI[12:1] are cleared to logic 0 when this register is read and WCIMODE input is logic 0. Each bit is independently cleared when WCIMODE is logic 1 and a write access with the corresponding bit is set to 1 is performed.

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Register 00C6H: RSVCA FIFO Underflow Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R	FUDRI[12]	0
Bit 10	R	FUDRI[11]	0
Bit 9	R	FUDRI[10]	0
Bit 8	R	FUDRI[9]	0
Bit 7	R	FUDRI[8]	0
Bit 6	R	FUDRI[7]	0
Bit 5	R	FUDRI[6]	0
Bit 4	R	FUDRI[5]	0
Bit 3	R	FUDRI[4]	0
Bit 2	R	FUDRI[3]	0
Bit 1	R	FUDRI[2]	0
Bit 0	R	FUDRI[1]	0

The FIFO underflow Event Interrupt Status Register is provided at SVCA Read/Write Address 06H.

FUDRI[12:1]

The FIFO underflow event interrupt status (FUDR[12:1]) bits are event indicators for STS-1/STM-0 paths #1 to #12. FUDRI[12:1] are set to logic 1 to indicate a FIFO underflow event. These interrupt status bits are independent of the interrupt enable bits. FUDRI[12:1] are cleared to logic 0 when this register is read and WCIMODE input is logic 0. Each bit is independently cleared when WCIMODE is logic 1 and a write access with the corresponding bit is set to 1 is performed.

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Register 00C7H: RSVCA Pointer Justification Interrupt Enable

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R/W	PJIE[12]	0
Bit 10	R/W	PJIE[11]	0
Bit 9	R/W	PJIE[10]	0
Bit 8	R/W	PJIE[9]	0
Bit 7	R/W	PJIE[8]	0
Bit 6	R/W	PJIE[7]	0
Bit 5	R/W	PJIE[6]	0
Bit 4	R/W	PJIE[5]	0
Bit 3	R/W	PJIE[4]	0
Bit 2	R/W	PJIE[3]	0
Bit 1	R/W	PJIE[2]	0
Bit 0	R/W	PJIE[1]	0

The Pointer Justification Interrupt Enable Register is provided at SVCA direct Read/Write Address 07H.

PJIEN[12:1]

The pointer justification event interrupt enable (PJIE[12:1]) bits controls the activation of the interrupt (INTB) output for STS-1/STM-0 paths #1 to #12. When any of these bit locations is set to logic 1, the corresponding pending interrupt will assert the interrupt (INTB) output. When any of these bit locations is set to logic 0, the corresponding pending interrupt will not assert the interrupt (INTB) output.

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Register 00C8H: RSVCA FIFO Interrupt Enable

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R/W	FIE[12]	0
Bit 10	R/W	FIE[11]	0
Bit 9	R/W	FIE[10]	0
Bit 8	R/W	FIE[9]	0
Bit 7	R/W	FIE[8]	0
Bit 6	R/W	FIE[7]	0
Bit 5	R/W	FIE[6]	0
Bit 4	R/W	FIE[5]	0
Bit 3	R/W	FIE[4]	0
Bit 2	R/W	FIE[3]	0
Bit 1	R/W	FIE[2]	0
Bit 0	R/W	FIE[1]	0

The FIFO Event Interrupt Enable Register is provided at SVCA Read/Write Address 08H.

FIEN[12:1]

The FIFO event interrupt enable (FIE[12:1]) bits controls the activation of the interrupt (INTB) output for STS-1/STM-0 paths #1 to #12 caused by a FIFO overflow or a FIFO underflow. When any of these bit locations is set to logic 1, the corresponding pending interrupt will assert the interrupt (INTB) output. When any of these bit locations is set to logic 0, the corresponding pending interrupt will not assert the interrupt (INTB) output.

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Register 00C9H: RSVCA Pointer Justification Thresholds

Bit	Type	Function	Default
Bit 15	R/W	NTHRES[3]	0
Bit 14	R/W	NTHRES[2]	1
Bit 13	R/W	NTHRES[1]	1
Bit 12	R/W	NTHRES[0]	1
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6		Unused	
Bit 5		Unused	
Bit 4		Unused	
Bit 3	R/W	PTHRES[3]	0
Bit 2	R/W	PTHRES[2]	1
Bit 1	R/W	PTHRES[1]	1
Bit 0	R/W	PTHRES[0]	1

The SVCA pointer justification thresholds is provided at SVCA Read/Write Address 08H.

PTHRES[3:0]

The SVCA positive pointer justification thresholds determines the FIFO fill thresholds that triggers a positive pointer justification is requested. If the FIFO fill level is less than the PTHRES, than a positive justification is performed.

NTHRES[3:0]

The SVCA positive pointer justification thresholds determines the FIFO fill thresholds that triggers a negative pointer justification is requested. If the FIFO fill level is greater than the NTHRES, than a negative justification is performed.

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Register 00CAH: RSVCA MISC Register

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W		0
Bit 13		Unused	
Bit 12		Unused	0
Bit 11	R/W	CLRFS[12]	0
Bit 10	R/W	CLRFS[11]	0
Bit 9	R/W	CLRFS[10]	0
Bit 8	R/W	CLRFS[9]	0
Bit 7	R/W	CLRFS[8]	0
Bit 6	R/W	CLRFS[7]	0
Bit 5	R/W	CLRFS[6]	0
Bit 4	R/W	CLRFS[5]	0
Bit 3	R/W	CLRFS[4]	0
Bit 2	R/W	CLRFS[3]	0
Bit 1	R/W	CLRFS[2]	0
Bit 0	R/W	CLRFS[1]	0

The FIFO MISC register provides miscellaneous control bits. It is provided at Read/Write Address 0AH.

CLRFS

The Clear Fixed Stuff (CLRFS) enables the regeneration of fixed stuff columns (#30, 59) of an STS-1/VC-3. When set to logic one, STS-1/VC-3 incoming fixed stuff columns (#30, #59) are discarded and regenerated (set to 00h) on the outgoing stream . When set to logic 0, these fixed stuff columns are relayed through the SVCA.

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Register 00CBH: RSVCA Performance Monitor Trigger

The Performance monitor transfer register is provided at Read/Write Address 00CBH. Any write to this register triggers a transfer of all performance monitor counters to holding registers that can be read by the ecbi interface.

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Indirect Register 00H: RSVCA Positive Justifications Performance Monitor

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12	R	PJPMON[12]	0
Bit 11	R	PJPMON[11]	0
Bit 10	R	PJPMON[10]	0
Bit 9	R	PJPMON[9]	0
Bit 8	R	PJPMON[8]	0
Bit 7	R	PJPMON[7]	0
Bit 6	R	PJPMON[6]	0
Bit 5	R	PJPMON[5]	0
Bit 4	R	PJPMON[4]	0
Bit 3	R	PJPMON[3]	0
Bit 2	R	PJPMON[2]	0
Bit 1	R	PJPMON[1]	0
Bit 0	R	PJPMON[0]	0

The Outgoing Positive justifications performance monitor is provided at SVCA indirect Read/Write Address 00H.

PJPMON[12:0][12:1]

This register reports the number of positive pointer justification events that occurred on the outgoing side in the previous accumulation interval. The content of this register becomes valid a maximum of 155ns (12 clock cycles) after a transfer is triggered by writing the SVCA performance monitor trigger direct register or a write to the SPECTRA-9953 master configuration register . The value of PJPMON is only valid for master slices. If PJPMON[12:0] is read for a slave slice, the master path's value will be returned.

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Indirect Register 01H: RSVCA Negative Justifications Performance Monitor

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12	R	NJPMON[12]	0
Bit 11	R	NJPMON[11]	0
Bit 10	R	NJPMON[10]	0
Bit 9	R	NJPMON[9]	0
Bit 8	R	NJPMON[8]	0
Bit 7	R	NJPMON[7]	0
Bit 6	R	NJPMON[6]	0
Bit 5	R	NJPMON[5]	0
Bit 4	R	NJPMON[4]	0
Bit 3	R	NJPMON[3]	0
Bit 2	R	NJPMON[2]	0
Bit 1	R	NJPMON[1]	0
Bit 0	R	NJPMON[0]	0

The outgoing Negative justifications performance monitor is provided at SVCA indirect Read/Write Address 01H.

NJPMON[12:0]

This register reports the number of negative pointer justification events that occurred on the outgoing side in the previous accumulation interval. The content of this register becomes valid a maximum of 155ns (12 clockPOCLK cycles) after a transfer is triggered by writing the SVCA performance monitor trigger direct register or a write to the SPECTRA-9953 master configuration register . The value of NJPMON is only valid for master slices. If NJPMON[12:0] is read for a slave slice, the master path's value will be returned.

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Indirect Register 02H: RSVCA Diagnostic/Config register

Bit	Type	Function	Default
Bit 15	R/W	PTRRST	0
Bit 14	R/W	PTRSS[1]	0
Bit 13	R/W	PTRSS[0]	0
Bit 12	R/W	JUS3DIS	0
Bit 11	R/W	PTRDD[1]	0
Bit 10	R/W	PTRDD[0]	0
Bit 9	R/W	Unused	0
Bit 8	R/W	Unused	0
Bit 7	R/W	unused	0
Bit 6	R/W	Diag_TOH_PAIS	0
Bit 5	R/W	Diag_NDFREQ	0
Bit 4	R/W	Diag_FifoAISDis	0
Bit 3	R/W	Diag_PAIS	0
Bit 2	R/W	Diag_LOP	0
Bit 1	R/W	Diag_NegJust	0
Bit 0	R/W	Diag_PosJust	0

The SVCA Diagnostic Register is provided at SVCA Read/Write Address 02H. These bits should be set to their default values during normal operation of the SVCA. The Diagnostic/Config register is only valid for master paths. Slave path Diagnostic/Config registers are overwritten with the master path's Diagnostic/Config register value.

Diag_PosJust

The Diag_PosJust bit forces the SVCA to generate outgoing positive justification events on the selected path(s). When set to 1, the SVCA generates positive justification events at the rate of one every four frames regardless of the current level of the internal FIFO. Prolonged application may cause the FIFO to overflow. However, the fifo monitor block has priority over the diagnostic justifications, so if the fifo level gets too high, then Negative justifications will be performed, even if the Diag_PosJust bit is written high. As such, it is difficult to make the fifo overflow.

Diag_NegJust

When set high, The Diag_NegJust bit forces the SVCA to generate outgoing negative justification events on the selected path(s). When set to 1, the SVCA generates negative justification events at the rate of one every four frames regardless of the current level of the internal FIFO. Prolonged application may cause the FIFO to underflow. However, the fifo monitor block has priority over the diagnostic justifications, so if the fifo level gets too low, then positive justifications will be performed, even if the Diag_NegJust bit is written high. As such, it is difficult to make the fifo underflow.

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Note : Diag_PosJust and Diag_NegJust must not be set to one at the same time. If that occurs, their operation is disabled.

Diag_LOP

When set high, the Diag_LOP bit forces the SVCA to invert the outgoing NDF field of the payload (selected path(s)) pointer causing downstream pointer processing elements to enter a loss of pointer (LOP) state.

Diag_PAIS

When set high, the Diag_PAIS bit forces the SVCA to insert path AIS in the selected outgoing stream for at least three consecutive frames. AIS is inserted by writing an all ones pattern in the transport overhead bytes H1, H2, and H3, as well as in the entire STS synchronous payload envelope. The first frame after PAIS negates will contain a new data flag in the transport overhead H1 byte.

Diag_FifoAISDis

When set high, Diag_FifoAISDis bit forces the SVCA not to insert path AIS upon FIFO overflow/underflow detection. When set low (normal operation), detection of FIFO overflow/underflow causes path AIS to be inserted in the outgoing stream for at least three consecutive frames. Also, both overflow and underflow interrupts are triggered. (FOVR and FUDR).

Diag_NDFREQ

When set high, Diag_NDFREQ bit forces the SVCA to insert a NEW DATA FLAG indication in the frame regardless of the state of the pointer generation state machine. This register bit is not slef clearing.

Diag_TOH_PAIS

When set high, the Diag_TOH_PAIS bit allows path AIS to be inserted even during the section/line overhead. When Diag_TOH_PAIS is zero, path AIS can only be inserted during the payload or during the H1, H2, and H3 bytes.

PTRDD[1:0]

The PTRDD[1:0] defines the STS-N/AU-N concatenation pointer bits DD. ITU requires that DD be set to 10 when processing AU-4, AU-3 or TU-3. On the other side, TELCORDIA does not specify these two bits.

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JUST3DIS

When set high, JUST3DIS allows the SVCA to perform 1 justification per frame when necessary. When set to zero, pointer justifications are allowed only every 4 frames.

PTRSS[1:0]

The PTRSS[1:0] defines the STS-N/AU-N pointer bits SS. ITU requires that SS be set to 10 when processing AU-4, AU-3 or TU-3. On the other side, TELCORDIA does not specify these two bits. The ss bits are set to 00 when processing a slave STS-1.

PTR_RST

When set high, Incoming and outgoing pointers are reset to their default values. This bit is level sensitive

15.8 T8TE Normal Registers

There are 16 T8TE (#1 - #16) blocks in 16 STM-4 processing slices with independent register sets. All 16 T8TE are masters and process and STS-12/STM-4 SONET/SDH stream.

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Register 00D0H: T8TE Control and Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	RESERVED	0
Bit 4	R/W	FIFOERRE	0
Bit 3	R/W	TPINS	0
Bit 2	R/W	RESERVED	0
Bit 1	W	CENTER	0
Bit 0	R/W	DLCV	0

This register provides control and reports the status of the T8TE.

DLCV

The diagnose line code violation bit (DLCV) controls the insertion of line code violation in the outgoing data stream. When this bit is set high, the transmit encoded data bus TED[9:0] are inverted to generate the complementary running disparity. The T8TE never inverts TelecomBus control characters, regardless of the DLCV bit.

CENTER

The FIFO centering control bit (CENTER) controls the separation of the FIFO read and write pointers. CENTER is a write only bit. When a logic high is written to CENTER, and the current FIFO depth is not in the range of 3, 4 or 5 characters, the FIFO depth is forced to be four 8B/10B characters deep, with a momentary data corruption. Writing to the CENTER bit when the FIFO depth is in the 3, 4 or 5 character range produces no effect. CENTER always returns a logic low when read.

TPINS

The Test Pattern Insertion (TPINS) controls the insertion of test pattern in the outgoing data stream for jitter testing purpose. When this bit is set high, the test pattern stored in the registers (TP[9:0]) is used to replace all the overhead and payload bytes of the output data stream. When TPINS is set low, no test pattern is inserted.

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FIFOERRE

The FIFO overrun/underrun error interrupt enable bit (FIFOERRE) controls the FIFO overrun/underrun interrupt event. An interrupt is generated on a FIFO error event if the FIFOERRE is set to logic 1. No interrupt is generated if FIFOERRE if is set to logic 0.

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Register 00D1H: T8TE Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R	FIFOERRI	0
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

This register reports interrupt status due the detection of FIFO error.

FIFOERRI

The FIFO overrun/underrun error interrupt indication bit (FIFOERRI) reports a FIFO overrun/underrun error event. FIFO overrun/underrun errors occur when FIFO logic detects FIFO read and write pointers in close proximity to each other. FIFOERRI is set to logic 1 on a FIFO overrun/underrun error. FIFOERRI is set to logic 0 when the T8TD Interrupt status register is read.

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Register 00D2H: T8TE Time-slot Configuration #1

Bit	Type	Function	Default
Bit 15	R/W	TMODE8[1]	0
Bit 14	R/W	TMODE8[0]	0
Bit 13	R/W	TMODE7[1]	0
Bit 12	R/W	TMODE7[0]	0
Bit 11	R/W	TMODE6[1]	0
Bit 10	R/W	TMODE6[0]	0
Bit 9	R/W	TMODE5[1]	0
Bit 8	R/W	TMODE5[0]	0
Bit 7	R/W	TMODE4[1]	0
Bit 6	R/W	TMODE4[0]	0
Bit 5	R/W	TMODE3[1]	0
Bit 4	R/W	TMODE3[0]	0
Bit 3	R/W	TMODE2[1]	0
Bit 2	R/W	TMODE2[0]	0
Bit 1	R/W	TMODE1[1]	0
Bit 0	R/W	TMODE1[0]	0

Register 00D2H configures the path termination mode of time-slots 1 to 8 of the T8TE.

TMODE1[1:0]-TMODE8[1:0]

The time-slot path termination mode select register bits (TMODE1[1:0]-TMODE8[1:0]) configures the mode settings for time-slots 1 to 8 of the T8TE. Time-slots are numbered in order of transmission in the Incoming TelecomBus stream (ID[7:0]). Time-slot #1 is the first byte transmitted and time-slot #12 is the last byte transmitted. The setting stored in TMODEx[1:0] (x can be 1-8) determines which set of TelecomBus control signals are to be encoded in 8B/10B characters.

TMODEx[1]	TMODEx[0]	Functional Description
0	0	MST mode
0	1	HPT mode
1	0	Rserved
1	1	Reserved

Note: If the user wants to employ the HPT mode, Section 14.12 (HPT mode Considerations) should be read first.

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Register 00D3H: T8TE Time-slot Configuration #2

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R/W	TMODE12[1]	0
Bit 6	R/W	TMODE12[0]	0
Bit 5	R/W	TMODE11[1]	0
Bit 4	R/W	TMODE11[0]	0
Bit 3	R/W	TMODE10[1]	0
Bit 2	R/W	TMODE10[0]	0
Bit 1	R/W	TMODE9[1]	0
Bit 0	R/W	TMODE9[0]	0

Register 00D3H configures the path termination mode of time-slots 9 to 12 of the T8TE.

TMODE9[1:0]-TMODE12[1:0]

The time-slot path termination mode select register bits (TMODE9[1:0]-TMODE12[1:0]) configures the mode settings for time-slots 9 to 12 of the T8TE. Time-slots are numbered in order of transmission in the Incoming TelecomBus stream (ID[7:0]). Time-slot #1 is the first byte transmitted and time-slot #12 is the last byte transmitted. The setting stored in TMODEx[1:0] (x can be 9-12) determines which set of TelecomBus control signals are to be encoded in 8B/10B characters.

TMODEx[1]	TMODEx[0]	Functional Description
0	0	MST mode
0	1	HPT mode
1	0	Rserved
1	1	Reserved

Note: If the user wants to employ the HPT mode, Section 14.12 (HPT mode Considerations) should be read first.

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Register 00D4H: T8TE Test Pattern

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9	R/W	TP[9]	1
Bit 8	R/W	TP[8]	0
Bit 7	R/W	TP[7]	1
Bit 6	R/W	TP[6]	0
Bit 5	R/W	TP[5]	1
Bit 4	R/W	TP[4]	0
Bit 3	R/W	TP[3]	1
Bit 2	R/W	TP[2]	0
Bit 1	R/W	TP[1]	1
Bit 0	R/W	TP[0]	0

These registers store test pattern.

TP[9:0]

The Test Pattern registers (TP[9:0]) contains the test pattern that is used to insert into the outgoing data stream for jitter test purpose. When the TPINS bit is set high, the test pattern stored in TP[9:0] is used to replace all the overhead and payload bytes of the output data stream.

15.9 SARC Normal Registers

There are four SARC (#1 - #4) blocks in four STM-16 processing groups with independent register sets. When the SPECTRA-9953 is configured for quad STS-48/STM-16 mode, all four blocks are configured as masters to process the STS-48c/STM-16c data streams. When configured for STS-192/STM-64 mode, only SARC #1 is configured as master and the other three (#2 - #4) blocks are inactive and are considered as slaves.

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Register 00E0H: SARC Indirect Address

Bit	Type	Function	Default
Bit 15	R	BUSY	0
Bit 14	R/W	RWB	0
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7	R/W	IADDR[1]	0
Bit 6	R/W	IADDR[0]	0
Bit 5	R/W	CHANNEL[1]	0
Bit 4	R/W	CHANNEL[0]	0
Bit 3	R/W	PATH[3]	0
Bit 2	R/W	PATH[2]	0
Bit 1	R/W	PATH[1]	0
Bit 0	R/W	PATH[0]	0

A write access to this register, Indirect Address Register, can initiates a write transfer from the Indirect (Write) Data Register to the internal Indirect Registers, and always initiates a read transfer from the internal Indirect Registers to the Indirect (Read) Data Register.

A read access to this register, Indirect Address Register, doesn't affect the internal Indirect Registers and doesn't affect the Indirect (Read/Write) Data Register.

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PATH[3:0]

The STS-1/STM-0 path (PATH[3:0]) bits select which STS-1/STM-0 path is accessed by the current transfer to internal Indirect Registers 0H, 1H, 2H or 3H.

CHANNEL[1:0]

The STS-1/STM-0 channel (CHANNEL[1:0]) bits select which STS-1/STM-0 channel is accessed by the current transfer to internal Indirect Registers 0H, 1H, 2H or 3H.

The fields PATH[3:0] and CHANNEL[1:0] together give the following selection:

CHANNEL [1:0] Hex	CHANNEL #	PATH [3:0] Hex	STS-1/STM-0 path #
0	1	0	Invalid path
		1-C	Path #1-#12
		D-F	Invalid path
1	2	0	Invalid path
		1-C	Path #13-#24
		D-F	Invalid path
2	3	0	Invalid path
		1-C	Path #25-#36
		D-F	Invalid path
3	4	0	Invalid path
		1-C	Path #37-#48
		D-F	Invalid path

Write transfer to invalid path doesn't affect the internal Indirect Registers. Read transfer to invalid path returns all zeros when the busy bit is low and return an unpredictable value when the busy bit is high.

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IADDR[1:0]

The Indirect address (IADDR[1:0]) indicates which internal Indirect Registers is written and read by the current transfer. The following table indicates the internal Indirect Registers address mapping.

IADDR[1:0] Hex	Indirect Register
0H	SARC Path Configuration Indirect Data (48 Paths)
1H	SARC Path RPALM Enable Indirect Data (48 Paths)
2H	SARC Path RPAISINS Enable Indirect Data (48 Paths)
3H	SARC Path TPAISINS Enable Indirect Data (48 Paths)

BUSY

The BUSY (BUSY) bit reports the status of the transfer to, or from, the internal Indirect Registers (SARC Path Configuration Indirect Data, SARC Path RPALM Enable Indirect Data, SARC Path RPAISINSEN Enable Indirect Data, and SARC Path TPAISINS Enable Indirect Data). BUSY is set to logic 1 upon writing to the indirect address register. BUSY is set to logic 0, upon completion of the transfer.

This bit should be polled to determine when a new address (PATH, CHANNEL, IADDR, RWB) could be written in the Indirect Address Register. This bit should be polled to determine for read access when the data to the Indirect (Read) Data Register is available and stable and for write access when a new data to the Indirect (Write) Data Register can be written.

When previously RWB is set to logic 0 (indirect write access) a new write access to the Indirect Address Register or a new write access to the Indirect (Write) Data Register during the busy bit is high (‘1’) can corrupt the current transaction.

When previously RWB is set to logic 1 (indirect read access) a new write access to the Indirect Address Register during the busy bit is high (‘1’) can corrupt the current transaction.

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RWB

The active high read and active low write (RWB) bit selects if the current access to the internal Indirect Registers is an indirect read or an indirect write. Writing to the Indirect Address Register initiates an access to the indirect registers. When RWB is set to logic 1, an indirect read access from the internal Indirect Registers is initiated. The data from the addressed location in the internal Indirect Registers will be transferred to the Indirect (Read) Data Register. When RWB is set to logic 0, an indirect write access to the internal Indirect Registers is initiated and also an indirect read access from the internal Indirect Registers is initiated. The data from the Indirect (Write) Data Register will be transferred to the addressed location in the internal Indirect Registers and this written data is return back to the Indirect (Read) Data Register.

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Register 00E1H: SARC Indirect Read/Write Data

Bit	Type	Function	Default
Bit 15	R/W	DATA[15]	0
Bit 14	R/W	DATA[14]	0
Bit 13	R/W	DATA[13]	0
Bit 12	R/W	DATA[12]	0
Bit 11	R/W	DATA[11]	0
Bit 10	R/W	DATA[10]	0
Bit 9	R/W	DATA[9]	0
Bit 8	R/W	DATA[8]	0
Bit 7	R/W	DATA[7]	0
Bit 6	R/W	DATA[6]	0
Bit 5	R/W	DATA[5]	0
Bit 4	R/W	DATA[4]	0
Bit 3	R/W	DATA[3]	0
Bit 2	R/W	DATA[2]	0
Bit 1	R/W	DATA[1]	0
Bit 0	R/W	DATA[0]	0

DATA[15:0]

The indirect access data (DATA[15:0]) bits hold the data transfer to or from the internal Indirect Registers during indirect access. When RWB is set to logic 1 (indirect read), the data from the addressed location in the internal Indirect Registers will be transferred to DATA[15:0]. BUSY should be polled to determine when the new data is available in DATA[15:0]. When RWB is set to logic 0 (indirect write), the data from DATA[15:0] will be transferred to the addressed location in the internal Indirect Registers. The indirect (Write) Data register must contain valid data before the indirect write is initiated by writing to the Indirect Address Register. DATA[15:0] has a different meaning depending on which address of the internal Indirect Registers is being accessed.

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Register 00E2H: SARC Section Configuration

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6		Unused	
Bit 5		Unused	
Bit 4		Unused	
Bit 3		Unused	
Bit 2		Unused	
Bit 1	R/W	LRDI22	0
Bit 0	R/W	TLRCPEN	0

TLRCPEN

The transmit line ring control port enable (TLRCPEN) bit enables the TRCP port. When TLRCPEN is set to logic 1, the APS, RDI-L and REI-L insertion indication are extracted from the TRCP port. When TRCPEN is set to logic 0, the APS, RDI-L and REI-L insertion indication are derived from the defect detected on the receive data stream.

LRDI22

The line remote defect indication (LRDI22) bit selects the line RDI persistence. When LRDI22 is set to logic 1, a new line RDI indication is transmitted on TLRDIINS for at least 22 frames. When LRDI22 is set to logic 0, a new line RDI indication is transmitted on TLRDIINS for at least 12 frames.

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Register 00E3H: SARC Section RSALM Enable

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R/W	Unused	0
Bit 10	R/W	Unused	0
Bit 9	R/W	SFBEREN	0
Bit 8	R/W	SDBEREN	0
Bit 7	R/W	STIMEN	0
Bit 6	R/W	STIUEN	0
Bit 5	R/W	APSBFEN	0
Bit 4	R/W	LRDIEN	0
Bit 3	R/W	LAISEN	0
Bit 2	R/W	LOSEN	0
Bit 1	R/W	LOFEN	0
Bit 0	R/W	OOFEN	0

OOFEN to SFBERENEN[1]

The enable bit allows the indication associated defect to be ORed into the output alarm. When the enable bit is set high, the corresponding defect indication is ORed with other defect indications and goes on the output alarm. When the enable bit is set low, the corresponding defect indication does not affect the output alarm.

The following table summarizes the enable bit, the defect and the output alarm.

Enable Bit	Defect	Output Alarm
		RSALM
SFBEREN	SFBER	
SDBEREN	SDBER	
STIMEN	STIM	
STIUEN	STIU	
APSBFEN	APSBF	
LRDIEN	LRDI	
LAISEN	LAIS	
LOSEN	LOS	
LOFEN	LOF	
OOFEN	OOF	

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Register 00E4H: SARC Section Receive AIS-L Insert Enable

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R/W	Reserved	0
Bit 10	R/W	UnusedReserved	0
Bit 9	R/W	SFBEREN	0
Bit 8	R/W	SDBEREN	0
Bit 7	R/W	STIMEN	0
Bit 6	R/W	STIUEN	0
Bit 5	R/W	APSBFEN	0
Bit 4	R/W	LRDIEN	0
Bit 3	R/W	LAISEN	0
Bit 2	R/W	LOSEN	1
Bit 1	R/W	LOFEN	0
Bit 0	R/W	OOFEN	0

OOFEN to SFBEREN[1]

The enable bit allows the indication associated defect to be ORed into the output alarm. When the enable bit is set high, the corresponding defect indication is ORed with other defect indications and goes on the output alarm. When the enable bit is set low, the corresponding defect indication does not affect the output alarm.

The following table summarizes the enable bit, the defect and the output alarm.

Enable bit	Defect	Output alarm
		RLAISINS
SFBEREN	SFBER	
SDBEREN	SDBER	
STIMEN	STIM	
STIUEN	STIU	
APSBFEN	APSBF	
LRDIEN	LRDI	
LAISEN	LAIS	
LOSEN	LOS	
LOFEN	LOF	
OOFEN	OOF	

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Register 00E5H: SARC Section Transmit RDI-L Insert Enable

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R/W	Unused	0
Bit 10	R/W	Unused	0
Bit 9	R/W	SFBEREN	0
Bit 8	R/W	SDBEREN	0
Bit 7	R/W	STIMEN	0
Bit 6	R/W	STIUEN	0
Bit 5	R/W	APSBFEN	0
Bit 4	R/W	LRDIEN	0
Bit 3	R/W	LAISEN	0
Bit 2	R/W	LOSEN	0
Bit 1	R/W	LOFEN	0
Bit 0	R/W	OOFEN	0

OOFEN to SFBEREN[1]

The enable bit allows the indication associated defect to be ORed into the output alarm. When the enable bit is set high, the corresponding defect indication is ORed with other defect indications and goes on the output alarm. When the enable bit is set low, the corresponding defect indication does not affect the output alarm. The following table summarizes the enable bit, the defect and the output alarm.

Enable Bit	Defect	Output Alarm
		TLRDIINS
SFBEREN	SFBER	
SDBEREN	SDBER	
STIMEN	STIM	
STIUEN	STIU	
APSBFEN	APSBF	
LRDIEN	LRDI	
LAISEN	LAIS	
LOSEN	LOS	
LOFEN	LOF	
OOFEN	OOF	

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Register 00E7H: SARC Transmit Path Configuration

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6		Unused	
Bit 5		Unused	
Bit 4	R/W	TPLOPTREND	0
Bit 3	R/W	TPAISPTRCFG[1]	0
Bit 2	R/W	TPAISPTRCFG[0]	0
Bit 1	R/W	TPLOPTRCFG[1]	0
Bit 0	R/W	TPLOPTRCFG[0]	0

Note: There is only one register for 48 transmit paths.

TPLOPTRCFG[1:0]

The transmit path loss of pointer configuration (TPLOPTRCFG[1:0]) bits define the LOP-P defect. When TPLOPTRCFG[1:0] is set to 00b, a transmit LOP-P defect is declared when the pointer from the SHPI is in the LOP state and a transmit LOP-P defect is removed when the pointer is not in the LOP state. When TPLOPTRCFG[1:0] is set to 01b, a transmit LOP-P defect is declared when the pointer or any of the concatenated pointers at the SHPI is in the LOP state and a transmit LOP-P defect is removed when the pointer and all the concatenation pointers are not in the LOP state. When TPLOPTRCFG[1:0] is set to 10b, a transmit LOP-P defect is declared when the SHPI pointer or any of the concatenated SHPI pointers is in the LOP state or in the AIS state and an LOP-P defect is removed when the pointer and all the concatenation pointers are not in the LOP state or in the AIS state.

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TPAISPTRCFG[1:0]

The transmit path AIS pointer configuration (TPAISPTRCFG[1:0]) bits define the transmit AIS-P defect. When TPAISPTRCFG[1:0] is set to 00b, a transmit AIS-P defect is declared when the SHPI pointer is in the AIS state and an AIS-P defect is removed when the pointer is not in the AIS state. When TPAISPTRCFG[1:0] is set to 01b, a transmit AIS-P defect is declared when the SHPI pointer or any of the concatenated SHPI pointers is in the AIS state and an AIS-P defect is removed when the pointer and all the concatenation pointers are not in the AIS state. When TPAISPTRCFG[1:0] is set to 10b, a transmit AIS-P defect is declared when the pointer and all the SHPI concatenated pointers are in the AIS state and an AIS-P defect is removed when the pointer or any of the concatenation pointers is not in the AIS state.

TPLOPTREND

The transmit path loss of pointer removal (TPLOPTREND) bit controls the removal of a transmit LOP-P defect when a transmit AIS-P defect is declared. When TPLOPTREND is set to logic 1, a transmit LOP-P defect is terminated when a transmit AIS-P defect is declared. When TPLOPTREND is set to logic 0, a transmit LOP-P defect is not terminated when a transmit AIS-P defect is declared.

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Register 00E8H: SARC LOP Pointer Status Path #1 to #12

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R	PLOPTRV[12]	X
Bit 10	R	PLOPTRV[11]	X
Bit 9	R	PLOPTRV[10]	X
Bit 8	R	PLOPTRV[9]	X
Bit 7	R	PLOPTRV[8]	X
Bit 6	R	PLOPTRV[7]	X
Bit 5	R	PLOPTRV[6]	X
Bit 4	R	PLOPTRV[5]	X
Bit 3	R	PLOPTRV[4]	X
Bit 2	R	PLOPTRV[3]	X
Bit 1	R	PLOPTRV[2]	X
Bit 0	R	PLOPTRV[1]	X

PLOPTRV[1:12]

The path loss of pointer status (PLOPTRV[1:12]) bits indicate the current status of the LOP-P defect STS-1/STM-0 paths #1 to #12. These bits reflect the assertion of the LOP condition for a specific path on the RALM output.

When PLOPTRCFG register bits are set to **00b**, PLOPTRV is asserted when the pointer is in the LOP state and PLOPTRV is negated when the pointer is not in the LOP state. When PLOPTRCFG register bits are set to **01b**, PLOPTRV is asserted when the pointer or any of the concatenated pointers is in the LOP state and PLOPTRV is negated when the pointer and all the concatenation pointers are not in the LOP state. When PLOPTRCFG register bits are set to **10b**, PLOPTRV is asserted when the pointer or any of the concatenated pointers is in the LOP state or in the AIS state, and PLOPTRV is negated when the pointer and all the concatenation pointers are not in the LOP state or in the AIS state. When the PLOPTREND register bit is set to one, PLOPPTRV is negated when an AIS-P defect is detected.

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Register 00E9H: SARC LOP Pointer Status Path #13 to #24

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R	PLOPTRV[24]	X
Bit 10	R	PLOPTRV[23]	X
Bit 9	R	PLOPTRV[22]	X
Bit 8	R	PLOPTRV[21]	X
Bit 7	R	PLOPTRV[20]	X
Bit 6	R	PLOPTRV[19]	X
Bit 5	R	PLOPTRV[18]	X
Bit 4	R	PLOPTRV[17]	X
Bit 3	R	PLOPTRV[16]	X
Bit 2	R	PLOPTRV[15]	X
Bit 1	R	PLOPTRV[14]	X
Bit 0	R	PLOPTRV[13]	X

PLOPTRV[13:24]

The path loss of pointer status (PLOPTRV[13:24]) bits indicate the current status of the LOP-P defect STS-1/STM-0 paths #13 to #24.

Same definition as Register 00E8H SARC LOP Pointer Status Path #1 to #12 but for path #13 to #24.

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Register 00EAH: SARC LOP Pointer Status Path #25 to #36

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R	PLOPTRV[36]	X
Bit 10	R	PLOPTRV[35]	X
Bit 9	R	PLOPTRV[34]	X
Bit 8	R	PLOPTRV[33]	X
Bit 7	R	PLOPTRV[32]	X
Bit 6	R	PLOPTRV[31]	X
Bit 5	R	PLOPTRV[30]	X
Bit 4	R	PLOPTRV[29]	X
Bit 3	R	PLOPTRV[28]	X
Bit 2	R	PLOPTRV[27]	X
Bit 1	R	PLOPTRV[26]	X
Bit 0	R	PLOPTRV[25]	X

PLOPTRV[25:36]

The path loss of pointer status (PLOPTRV[25:36]) bits indicate the current status of the LOP-P defect STS-1/STM-0 paths #25 to #36.

Same definition as Register 00E8H SARC LOP Pointer Status Path #1 to #12 but for path #25 to #36.

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Register 00EBH: SARC LOP Pointer Status Path #37 to #48

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R	PLOPTRV[48]	X
Bit 10	R	PLOPTRV[47]	X
Bit 9	R	PLOPTRV[46]	X
Bit 8	R	PLOPTRV[45]	X
Bit 7	R	PLOPTRV[44]	X
Bit 6	R	PLOPTRV[43]	X
Bit 5	R	PLOPTRV[42]	X
Bit 4	R	PLOPTRV[41]	X
Bit 3	R	PLOPTRV[40]	X
Bit 2	R	PLOPTRV[39]	X
Bit 1	R	PLOPTRV[38]	X
Bit 0	R	PLOPTRV[37]	X

PLOPTRV[37:48]

The path loss of pointer status (PLOPTRV[37:48]) bits indicate the current status of the LOP-P defect STS-1/STM-0 paths #37 to #48.

Same definition as Register 00E8H SARC LOP Pointer Status Path #1 to #12 but for path #37 to #48.

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Register 00ECH: SARC LOP Pointer Interrupt Enable Path #1 to #12

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R/W	PLOPTRE[12]	0
Bit 10	R/W	PLOPTRE[11]	0
Bit 9	R/W	PLOPTRE[10]	0
Bit 8	R/W	PLOPTRE[9]	0
Bit 7	R/W	PLOPTRE[8]	0
Bit 6	R/W	PLOPTRE[7]	0
Bit 5	R/W	PLOPTRE[6]	0
Bit 4	R/W	PLOPTRE[5]	0
Bit 3	R/W	PLOPTRE[4]	0
Bit 2	R/W	PLOPTRE[3]	0
Bit 1	R/W	PLOPTRE[2]	0
Bit 0	R/W	PLOPTRE[1]	0

PLOPTRE[1:12]

The path loss of pointer interrupt enable (PLOPTRE[1:12]) bits control the activation of the interrupt (INTB) output for STS-1/STM-0 paths #1 to #12.

When any of these bit locations is set to logic 1, the corresponding pending interrupt will assert the interrupt (INTB) output. When any of these bit locations is set to logic 0, the corresponding pending interrupt will not assert the interrupt (INTB) output.

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Register 00EDH: SARC LOP Pointer Interrupt Enable Path #13 to #24

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R/W	PLOPTRE[24]	0
Bit 10	R/W	PLOPTRE[23]	0
Bit 9	R/W	PLOPTRE[22]	0
Bit 8	R/W	PLOPTRE[21]	0
Bit 7	R/W	PLOPTRE[20]	0
Bit 6	R/W	PLOPTRE[19]	0
Bit 5	R/W	PLOPTRE[18]	0
Bit 4	R/W	PLOPTRE[17]	0
Bit 3	R/W	PLOPTRE[16]	0
Bit 2	R/W	PLOPTRE[15]	0
Bit 1	R/W	PLOPTRE[14]	0
Bit 0	R/W	PLOPTRE[13]	0

PLOPTRE[13:24]

The path loss of pointer interrupt enable (PLOPTRE[13:24]) bits control the activation of the interrupt (INTB) output for STS-1/STM-0 paths #13 to #24.

When any of these bit locations is set to logic 1, the corresponding pending interrupt will assert the interrupt (INTB) output. When any of these bit locations is set to logic 0, the corresponding pending interrupt will not assert the interrupt (INTB) output.

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Register 00EEH: SARC LOP Pointer Interrupt Enable Path #25 to #36

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R/W	PLOPTRE[36]	0
Bit 10	R/W	PLOPTRE[35]	0
Bit 9	R/W	PLOPTRE[34]	0
Bit 8	R/W	PLOPTRE[33]	0
Bit 7	R/W	PLOPTRE[32]	0
Bit 6	R/W	PLOPTRE[31]	0
Bit 5	R/W	PLOPTRE[30]	0
Bit 4	R/W	PLOPTRE[29]	0
Bit 3	R/W	PLOPTRE[28]	0
Bit 2	R/W	PLOPTRE[27]	0
Bit 1	R/W	PLOPTRE[26]	0
Bit 0	R/W	PLOPTRE[25]	0

PLOPTRE[25:36]

The path loss of pointer interrupt enable (PLOPTRE[25:36]) bits control the activation of the interrupt (INTB) output for STS-1/STM-0 paths #25 to #36.

When any of these bit locations is set to logic 1, the corresponding pending interrupt will assert the interrupt (INTB) output. When any of these bit locations is set to logic 0, the corresponding pending interrupt will not assert the interrupt (INTB) output.

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Register 00EFH: SARC LOP Pointer Interrupt Enable Path #37 to #48

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R/W	PLOPTRE[48]	0
Bit 10	R/W	PLOPTRE[47]	0
Bit 9	R/W	PLOPTRE[46]	0
Bit 8	R/W	PLOPTRE[45]	0
Bit 7	R/W	PLOPTRE[44]	0
Bit 6	R/W	PLOPTRE[43]	0
Bit 5	R/W	PLOPTRE[42]	0
Bit 4	R/W	PLOPTRE[41]	0
Bit 3	R/W	PLOPTRE[40]	0
Bit 2	R/W	PLOPTRE[39]	0
Bit 1	R/W	PLOPTRE[38]	0
Bit 0	R/W	PLOPTRE[37]	0

PLOPTRE[37:48]

The path loss of pointer interrupt enable (PLOPTRE[37:48]) bits control the activation of the interrupt (INTB) output for STS-1/STM-0 paths #37 to #48.

When any of these bit locations is set to logic 1, the corresponding pending interrupt will assert the interrupt (INTB) output. When any of these bit locations is set to logic 0, the corresponding pending interrupt will not assert the interrupt (INTB) output.

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Register 00F0H: SARC LOP Pointer Interrupt Status Path #1 to #12

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R	PLOPTRI[12]	X
Bit 10	R	PLOPTRI[11]	X
Bit 9	R	PLOPTRI[10]	X
Bit 8	R	PLOPTRI[9]	X
Bit 7	R	PLOPTRI[8]	X
Bit 6	R	PLOPTRI[7]	X
Bit 5	R	PLOPTRI[6]	X
Bit 4	R	PLOPTRI[5]	X
Bit 3	R	PLOPTRI[4]	X
Bit 2	R	PLOPTRI[3]	X
Bit 1	R	PLOPTRI[2]	X
Bit 0	R	PLOPTRI[1]	X

Clear mode of interrupts depends on the WCIMODE input value. When WCIMODE input is logic 0, all the interrupts are cleared when the Interrupt Status Register is read. When WCIMODE input is logic 1, a given interrupt is cleared only if the corresponding bit is logic 1 when the Interrupt Status Register is written.

PLOPTRI[1:12]

The path loss of pointer interrupt status (PLOPTRI[1:12]) bits are event indicators for STS-1/STM-0 paths #1 to #12,

PLOPTRI[1:12] are set to logic 1 to indicate any changes in the status of PLOPTRV[1:12]. These interrupt status bits are independent of the interrupt enable bits. PLOPTRI[1:12] are cleared to logic 0 when this register is read.

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Register 00F1H: SARC LOP Pointer Interrupt Status Path #13 to #24

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R	PLOPTRI[24]	X
Bit 10	R	PLOPTRI[23]	X
Bit 9	R	PLOPTRI[22]	X
Bit 8	R	PLOPTRI[21]	X
Bit 7	R	PLOPTRI[20]	X
Bit 6	R	PLOPTRI[19]	X
Bit 5	R	PLOPTRI[18]	X
Bit 4	R	PLOPTRI[17]	X
Bit 3	R	PLOPTRI[16]	X
Bit 2	R	PLOPTRI[15]	X
Bit 1	R	PLOPTRI[14]	X
Bit 0	R	PLOPTRI[13]	X

Clear mode of interrupts depends on the WCIMODE input value. When WCIMODE input is logic 0, all the interrupts are cleared when the Interrupt Status Register is read. When WCIMODE input is logic 1, a given interrupt is cleared only if the corresponding bit is logic 1 when the Interrupt Status Register is written.

PLOPTRI[13:24]

The path loss of pointer interrupt status (PLOPTRI[13:24]) bits are event indicators for STS-1/STM-0 paths #13 to #24,

PLOPTRI[13:24] are set to logic 1 to indicate any changes in the status of PLOPTRV[13:24]. These interrupt status bits are independent of the interrupt enable bits. PLOPTRI[13:24] are cleared to logic 0 when this register is read.

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Register 00F2H: SARC LOP Pointer Interrupt Status Path #25 to #36

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R	PLOPTRI[36]	X
Bit 10	R	PLOPTRI[35]	X
Bit 9	R	PLOPTRI[34]	X
Bit 8	R	PLOPTRI[33	X
Bit 7	R	PLOPTRI[32]	X
Bit 6	R	PLOPTRI[31]	X
Bit 5	R	PLOPTRI[30]	X
Bit 4	R	PLOPTRI[29]	X
Bit 3	R	PLOPTRI[28]	X
Bit 2	R	PLOPTRI[27]	X
Bit 1	R	PLOPTRI[26]	X
Bit 0	R	PLOPTRI[25]	X

Clear mode of interrupts depends on the WCIMODE input value. When WCIMODE input is logic 0, all the interrupts are cleared when the Interrupt Status Register is read. When WCIMODE input is logic 1, a given interrupt is cleared only if the corresponding bit is logic 1 when the Interrupt Status Register is written.

PLOPTRI[25:36]

The path loss of pointer interrupt status (PLOPTRI[25:36]) bits are event indicators for STS-1/STM-0 paths #25 to #36,

PLOPTRI[25:36] are set to logic 1 to indicate any changes in the status of PLOPTRV[25:36]. These interrupt status bits are independent of the interrupt enable bits. PLOPTRI[25:36] are cleared to logic 0 when this register is read.

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Register 00F3H: SARC LOP Pointer Interrupt Status Path #37 to #48

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R	PLOPTRI[48]	X
Bit 10	R	PLOPTRI[47]	X
Bit 9	R	PLOPTRI[46]	X
Bit 8	R	PLOPTRI[45]	X
Bit 7	R	PLOPTRI[44]	X
Bit 6	R	PLOPTRI[43]	X
Bit 5	R	PLOPTRI[42]	X
Bit 4	R	PLOPTRI[41]	X
Bit 3	R	PLOPTRI[40]	X
Bit 2	R	PLOPTRI[39]	X
Bit 1	R	PLOPTRI[38]	X
Bit 0	R	PLOPTRI[37]	X

Clear mode of interrupts depends on the WCIMODE input value. When WCIMODE input is logic 0, all the interrupts are cleared when the Interrupt Status Register is read. When WCIMODE input is logic 1, a given interrupt is cleared only if the corresponding bit is logic 1 when the Interrupt Status Register is written.

PLOPTRI[37:48]

The path loss of pointer interrupt status (PLOPTRI[37:48]) bits are event indicators for STS-1/STM-0 paths #37 to #48,

PLOPTRI[37:48] are set to logic 1 to indicate any changes in the status of PLOPTRV[37:48]. These interrupt status bits are independent of the interrupt enable bits. PLOPTRI[37:48] are cleared to logic 0 when this register is read.

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Register 00F4H: SARC AIS Pointer Status Path #1 to #12

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R	PAISPTRV[12]	X
Bit 10	R	PAISPTRV[11]	X
Bit 9	R	PAISPTRV[10]	X
Bit 8	R	PAISPTRV[9]	X
Bit 7	R	PAISPTRV[8]	X
Bit 6	R	PAISPTRV[7]	X
Bit 5	R	PAISPTRV[6]	X
Bit 4	R	PAISPTRV[5]	X
Bit 3	R	PAISPTRV[4]	X
Bit 2	R	PAISPTRV[3]	X
Bit 1	R	PAISPTRV[2]	X
Bit 0	R	PAISPTRV[1]	X

PAISPTRV[1:12]

The path AIS pointer status (PAISPTRV[1:12]) bits indicate the current status of the AIS-P defect STS-1/STM-0 paths #1 to #12.

When PAISPTRCFG register bits are set to **00b**, PAISPTRV is asserted when the pointer is in the AIS state and PAISPTRV is negated when the pointer is not in the AIS state. When PAISPTRCFG register bits are set to **01b**, PAISPTRV is asserted when the pointer or any of the concatenated pointers is in the AIS state and PAISPTRV is negated when the pointer and all the concatenation pointers are not in the AIS state. When PAISPTRCFG register bits are set to **10b**, PAISPTRV is asserted when the pointer and all the concatenated pointers are in the AIS state and PAISPTRV is negated when the pointer or any of the concatenation pointers are not in the AIS state.

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Register 00F5H: SARC AIS Pointer Status Path #13 to #24

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R	PAISPTRV[24]	X
Bit 10	R	PAISPTRV[23]	X
Bit 9	R	PAISPTRV[22]	X
Bit 8	R	PAISPTRV[21]	X
Bit 7	R	PAISPTRV[20]	X
Bit 6	R	PAISPTRV[19]	X
Bit 5	R	PAISPTRV[18]	X
Bit 4	R	PAISPTRV[17]	X
Bit 3	R	PAISPTRV[16]	X
Bit 2	R	PAISPTRV[15]	X
Bit 1	R	PAISPTRV[14]	X
Bit 0	R	PAISPTRV[13]	X

PAISPTRV[13:24]

The path AIS pointer status (PAISPTRV[13:24]) bits indicate the current status of the AIS-P defect STS-1/STM-0 paths #13 to #24.

Same definition as Register 00F4H SARC AIS Pointer Status Path #1 to #12 but for path #13 to #24.

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Register 00F6H: SARC AIS Pointer Status Path #25 to #36

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R	PAISPTRV[36]	X
Bit 10	R	PAISPTRV[35]	X
Bit 9	R	PAISPTRV[34]	X
Bit 8	R	PAISPTRV[33]	X
Bit 7	R	PAISPTRV[32]	X
Bit 6	R	PAISPTRV[31]	X
Bit 5	R	PAISPTRV[30]	X
Bit 4	R	PAISPTRV[29]	X
Bit 3	R	PAISPTRV[28]	X
Bit 2	R	PAISPTRV[27]	X
Bit 1	R	PAISPTRV[26]	X
Bit 0	R	PAISPTRV[25]	X

PAISPTRV[25:36]

The path AIS pointer status (PAISPTRV[25:36]) bits indicate the current status of the AIS-P defect STS-1/STM-0 paths #25 to #36.

Same definition as Register 00F4H SARC AIS Pointer Status Path #1 to #12 but for path #25 to #36.

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Register 00F7H: SARC AIS Pointer Status Path #37 to #48

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R	PAISPTRV[48]	X
Bit 10	R	PAISPTRV[47]	X
Bit 9	R	PAISPTRV[46]	X
Bit 8	R	PAISPTRV[45]	X
Bit 7	R	PAISPTRV[44]	X
Bit 6	R	PAISPTRV[43]	X
Bit 5	R	PAISPTRV[42]	X
Bit 4	R	PAISPTRV[41]	X
Bit 3	R	PAISPTRV[40]	X
Bit 2	R	PAISPTRV[39]	X
Bit 1	R	PAISPTRV[38]	X
Bit 0	R	PAISPTRV[37]	X

PAISPTRV[37:48]

The path AIS pointer status (PAISPTRV[37:48]) bits indicate the current status of the AIS-P defect STS-1/STM-0 paths #37 to #48.

Same definition as Register 00F4H SARC AIS Pointer Status Path #1 to #12 but for path #37 to #48.

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Register 00F8H: SARC AIS Pointer Interrupt Enable Path #1 to #12

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R/W	PAISPTRE[12]	0
Bit 10	R/W	PAISPTRE[11]	0
Bit 9	R/W	PAISPTRE[10]	0
Bit 8	R/W	PAISPTRE[9]	0
Bit 7	R/W	PAISPTRE[8]	0
Bit 6	R/W	PAISPTRE[7]	0
Bit 5	R/W	PAISPTRE[6]	0
Bit 4	R/W	PAISPTRE[5]	0
Bit 3	R/W	PAISPTRE[4]	0
Bit 2	R/W	PAISPTRE[3]	0
Bit 1	R/W	PAISPTRE[2]	0
Bit 0	R/W	PAISPTRE[1]	0

PAISPTRE[1:12]

The path AIS signal pointer interrupt enable (PAISPTRE[1:12]) bits control the activation of the interrupt (INTB) output for STS-1/STM-0 paths #1 to #12.

When any of these bit locations is set to logic 1, the corresponding pending interrupt will assert the interrupt (INTB) output. When any of these bit locations is set to logic 0, the corresponding pending interrupt will not assert the interrupt (INTB) output.

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Register 00F9H: SARC AIS Pointer Interrupt Enable Path #13 to #24

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R/W	PAISPTRE[24]	0
Bit 10	R/W	PAISPTRE[23]	0
Bit 9	R/W	PAISPTRE[22]	0
Bit 8	R/W	PAISPTRE[21]	0
Bit 7	R/W	PAISPTRE[20]	0
Bit 6	R/W	PAISPTRE[19]	0
Bit 5	R/W	PAISPTRE[18]	0
Bit 4	R/W	PAISPTRE[17]	0
Bit 3	R/W	PAISPTRE[16]	0
Bit 2	R/W	PAISPTRE[15]	0
Bit 1	R/W	PAISPTRE[14]	0
Bit 0	R/W	PAISPTRE[13]	0

PAISPTRE[13:24]

The path AIS signal pointer interrupt enable (PAISPTRE[13:24]) bits control the activation of the interrupt (INTB) output for STS-1/STM-0 paths #13 to #24.

When any of these bit locations is set to logic 1, the corresponding pending interrupt will assert the interrupt (INTB) output. When any of these bit locations is set to logic 0, the corresponding pending interrupt will not assert the interrupt (INTB) output.

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Register 00FAH: SARC AIS Pointer Interrupt Enable Path #25 to #36

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R/W	PAISPTRE[36]	0
Bit 10	R/W	PAISPTRE[35]	0
Bit 9	R/W	PAISPTRE[34]	0
Bit 8	R/W	PAISPTRE[33]	0
Bit 7	R/W	PAISPTRE[32]	0
Bit 6	R/W	PAISPTRE[31]	0
Bit 5	R/W	PAISPTRE[30]	0
Bit 4	R/W	PAISPTRE[29]	0
Bit 3	R/W	PAISPTRE[28]	0
Bit 2	R/W	PAISPTRE[27]	0
Bit 1	R/W	PAISPTRE[26]	0
Bit 0	R/W	PAISPTRE[25]	0

PAISPTRE[25:36]

The path AIS signal pointer interrupt enable (PAISPTRE[25:36]) bits control the activation of the interrupt (INTB) output for STS-1/STM-0 paths #25 to #36.

When any of these bit locations is set to logic 1, the corresponding pending interrupt will assert the interrupt (INTB) output. When any of these bit locations is set to logic 0, the corresponding pending interrupt will not assert the interrupt (INTB) output.

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Register 00FBH: SARC AIS Pointer Interrupt Enable Path #37 to #48

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R/W	PAISPTRE[48]	0
Bit 10	R/W	PAISPTRE[47]	0
Bit 9	R/W	PAISPTRE[46]	0
Bit 8	R/W	PAISPTRE[45]	0
Bit 7	R/W	PAISPTRE[44]	0
Bit 6	R/W	PAISPTRE[43]	0
Bit 5	R/W	PAISPTRE[42]	0
Bit 4	R/W	PAISPTRE[41]	0
Bit 3	R/W	PAISPTRE[40]	0
Bit 2	R/W	PAISPTRE[39]	0
Bit 1	R/W	PAISPTRE[38]	0
Bit 0	R/W	PAISPTRE[37]	0

PAISPTRE[37:48]

The path AIS signal pointer interrupt enable (PAISPTRE[37:48]) bits control the activation of the interrupt (INTB) output for STS-1/STM-0 paths #37 to #48.

When any of these bit locations is set to logic 1, the corresponding pending interrupt will assert the interrupt (INTB) output. When any of these bit locations is set to logic 0, the corresponding pending interrupt will not assert the interrupt (INTB) output.

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Register 00FCH: SARC AIS Pointer Interrupt Status Path #1 to #12

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R	PAISPTRI[12]	X
Bit 10	R	PAISPTRI[11]	X
Bit 9	R	PAISPTRI[10]	X
Bit 8	R	PAISPTRI[9]	X
Bit 7	R	PAISPTRI[8]	X
Bit 6	R	PAISPTRI[7]	X
Bit 5	R	PAISPTRI[6]	X
Bit 4	R	PAISPTRI[5]	X
Bit 3	R	PAISPTRI[4]	X
Bit 2	R	PAISPTRI[3]	X
Bit 1	R	PAISPTRI[2]	X
Bit 0	R	PAISPTRI[1]	X

Clear mode of interrupts depends on the WCIMODE input value. When WCIMODE input is logic 0, all the interrupts are cleared when the Interrupt Status Register is read. When WCIMODE input is logic 1, a given interrupt is cleared only if the corresponding bit is logic 1 when the Interrupt Status Register is written.

PAISPTRI[1:12]

The path AIS pointer interrupt status (PAISPTRI[1:12]) bits are event indicators for STS-1/STM-0 paths #1 to #12,

PAISPTRI[1:12] are set to logic 1 to indicate any changes in the status of PAISPTRV[1:12]. These interrupt status bits are independent of the interrupt enable bits. PAISPTRI[1:12] are cleared to logic 0 when this register is read.

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Register 00FDH: SARC AIS Pointer Interrupt Status Path #13 to #24

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R	PAISPTRI[24]	X
Bit 10	R	PAISPTRI[23]	X
Bit 9	R	PAISPTRI[22]	X
Bit 8	R	PAISPTRI[21]	X
Bit 7	R	PAISPTRI[20]	X
Bit 6	R	PAISPTRI[19]	X
Bit 5	R	PAISPTRI[18]	X
Bit 4	R	PAISPTRI[17]	X
Bit 3	R	PAISPTRI[16]	X
Bit 2	R	PAISPTRI[15]	X
Bit 1	R	PAISPTRI[14]	X
Bit 0	R	PAISPTRI[13]	X

Clear mode of interrupts depends on the WCIMODE input value. When WCIMODE input is logic 0, all the interrupts are cleared when the Interrupt Status Register is read. When WCIMODE input is logic 1, a given interrupt is cleared only if the corresponding bit is logic 1 when the Interrupt Status Register is written.

PAISPTRI[13:24]

The path AIS pointer interrupt status (PAISPTRI[13:24]) bits are event indicators for STS-1/STM-0 paths #13 to #24.

PAISPTRI[13:24] are set to logic 1 to indicate any changes in the status of PAISPTRV[13:24]. These interrupt status bits are independent of the interrupt enable bits. PAISPTRI[13:24] are cleared to logic 0 when this register is read.

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Register 00FEH: SARC AIS Pointer Interrupt Status Path #25 to #36

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R	PAISPTRI[36]	X
Bit 10	R	PAISPTRI[35]	X
Bit 9	R	PAISPTRI[34]	X
Bit 8	R	PAISPTRI[33]	X
Bit 7	R	PAISPTRI[32]	X
Bit 6	R	PAISPTRI[31]	X
Bit 5	R	PAISPTRI[30]	X
Bit 4	R	PAISPTRI[29]	X
Bit 3	R	PAISPTRI[28]	X
Bit 2	R	PAISPTRI[27]	X
Bit 1	R	PAISPTRI[26]	X
Bit 0	R	PAISPTRI[25]	X

Clear mode of interrupts depends on the WCIMODE input value. When WCIMODE input is logic 0, all the interrupts are cleared when the Interrupt Status Register is read. When WCIMODE input is logic 1, a given interrupt is cleared only if the corresponding bit is logic 1 when the Interrupt Status Register is written.

PAISPTRI[25:36]

The path AIS pointer interrupt status (PAISPTRI[35:36]) bits are event indicators for STS-1/STM-0 paths #25 to #36,

PAISPTRI[25:36] are set to logic 1 to indicate any changes in the status of PAISPTRV[25:36]. These interrupt status bits are independent of the interrupt enable bits. PAISPTRI[25:36] are cleared to logic 0 when this register is read.

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Register 00FFH: SARC AIS Pointer Interrupt Status Path #37 to #48

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R	PAISPTRI[48]	X
Bit 10	R	PAISPTRI[47]	X
Bit 9	R	PAISPTRI[46]	X
Bit 8	R	PAISPTRI[45]	X
Bit 7	R	PAISPTRI[44]	X
Bit 6	R	PAISPTRI[43]	X
Bit 5	R	PAISPTRI[42]	X
Bit 4	R	PAISPTRI[41]	X
Bit 3	R	PAISPTRI[40]	X
Bit 2	R	PAISPTRI[39]	X
Bit 1	R	PAISPTRI[38]	X
Bit 0	R	PAISPTRI[37]	X

Clear mode of interrupts depends on the WCIMODE input value. When WCIMODE input is logic 0, all the interrupts are cleared when the Interrupt Status Register is read. When WCIMODE input is logic 1, a given interrupt is cleared only if the corresponding bit is logic 1 when the Interrupt Status Register is written.

PAISPTRI[37:48]

The path AIS pointer interrupt status (PAISPTRI[37:48]) bits are event indicators for STS-1/STM-0 paths #37 to #48,

PAISPTRI[37:48] are set to logic 1 to indicate any changes in the status of PAISPTRV[37:48]. These interrupt status bits are independent of the interrupt enable bits. PAISPTRI[37:48] are cleared to logic 0 when this register is read.

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Indirect Register 0H: SARC Path Configuration Indirect Data (48 path)

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7	R/W	RDIEN	0
Bit 6	R/W	PERDI22	0
Bit 5	R/W	TPRCPEN	0
Bit 4	R/W	PLOPTREND	0
Bit 3	R/W	PAISPTRCFG[1]	0
Bit 2	R/W	PAISPTRCFG[0]	0
Bit 1	R/W	PLOPTRCFG[1]	0
Bit 0	R/W	PLOPTRCFG[0]	0

This register is indirect 48 times for 48 paths.

PLOPTRCFG[1:0]

The path loss of pointer configuration (PLOPTRCFG[1:0]) bits define the LOP-P defect. When PLOPTRCFG[1:0] is set to **00b**, an LOP-P defect is declared when the pointer is in the LOP state and an LOP-P defect is removed when the pointer is not in the LOP state. When PLOPTRCFG[1:0] is set to **01b**, an LOP-P defect is declared when the pointer or any of the concatenated pointers is in the LOP state and an LOP-P defect is removed when the pointer and all the concatenation pointers are not in the LOP state. When PLOPTRCFG[1:0] is set to **10b**, an LOP-P defect is declared when the pointer or any of the concatenated pointers is in the LOP state or in the AIS state and an LOP-P defect is removed when the pointer and all the concatenation pointers are not in the LOP state or in the AIS state. For slave STS-1/STM0 slices, the PLOPTRCFG[1:0] bits should be left at **00b**; otherwise, LOP-P could be declared unexpectedly on non-master timeslots.

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PAISPTRCFG[1:0]

The path AIS pointer configuration (PAISPTRCFG[1:0]) bits define the AIS-P defect. When PAISPTRCFG[1:0] is set to **00b**, an AIS-P defect is declared when the pointer is in the AIS state and an AIS-P defect is removed when the pointer is not in the AIS state. When PAISPTRCFG[1:0] is set to **01b**, an AIS-P defect is declared when the pointer or any of the concatenated pointers is in the AIS state and an AIS-P defect is removed when the pointer and all the concatenation pointers are not in the AIS state. When PAISPTRCFG[1:0] is set to **10b**, an AIS-P defect is declared when the pointer and all the concatenated pointers are in the AIS state and an AIS-P defect is removed when the pointer or any of the concatenation pointers is not in the AIS state. For slave STS-1/STM0 slices, the PAISPTRCFG[1:0] bits should be left at **00b**; otherwise, AIS-P could be declared unexpectedly on non-master timeslots.

PLOPTREND

The path loss of pointer removal (PLOPTREND) bit controls the removal of a LOP-P defect when an AIS-P defect is declared. When PLOPTREND is set to logic 1, a LOP-P defect is terminated when an AIS-P defect is declared. When PLOPTREND is set to logic 0, a LOP-P defect is not terminated when an AIS-P defect is declared.

TPRCPEN

The transmit path ring control port enable (TPRCPEN) bit enables the TRCP port. When TPRPEN is set to logic 1, ERDI-P and REI-P insertion indication are extracted from the TRCP port. When TRCPEN is set to logic 0, ERDI-P and REI-P insertion indication are derived from the defect detected on the receive data stream.

PERDI22

The path enhance remote defect indication (PERDI22) bit selects the path ERDI persistence. When PERDI22 is set to logic 1, a new path ERDI indication is transmitted on TPERDIINS[2:0] for at least 20 frames. When PERDI22 is set to logic 0, a new path ERDI indication is transmitted for at least 10 frames.

RDIEN

The path remote defect indication enable (RDIEN) bit selects between the 1 bit RDI code and the 3 bits ERDI code. When PRDIEN is set to logic 1, the 1 bit RDI code is transmitted. When PRDIEN is set to logic 0, the 3 bit ERDI code is transmitted.

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Indirect Register 1H: SARC Path RPALM Enable Indirect Data (48 path)

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13	R/W	Unused	0
Bit 12	R/W	Unused	0
Bit 11	R/W	PTIMEN	0
Bit 10	R/W	PTIUEN	0
Bit 9	R/W	PERDIEN	0
Bit 8	R/W	PRDIEN	0
Bit 7	R/W	PPDIEN	0
Bit 6	R/W	PUNEQEN	0
Bit 5	R/W	PPLMEN	0
Bit 4	R/W	PPLUEN	0
Bit 3	R/W	PAISPTREN	0
Bit 2	R/W	PLOPTREN	0
Bit 1	R/W	MSRSALMEN	0
Bit 0	R/W	RSALMEN	0

This register is indirect 48 times for 48 paths.

RSALMEN to PTIMEN[1]

The enable bit allows the indication associated defect to be ORed into the output alarm, which is indicated at the RALM chip output. When the enable bit is set high, the corresponding defect indication is ORed with other defect indications and goes on the output alarm. When the enable bit is set low, the corresponding defect indication does not affect the output alarm.

The following table summarizes the enable bit, the defect and the output alarm.

Enable Bit	Defect	Output Alarm
		RPALM
PTIMEN	PTIM	
PTIUEN	PTIU	
PERDIEN	PERDI	
PRDIEN	PRDI	
PPDIEN	PPDI	
PUNEQUEN	PUNEQU	
PPLMEN	PPLM	

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Enable Bit	Defect	Output Alarm
PPLUEN	PPLU	
PAISPTREN	PAISPTR	
PLOPTREN	PLOPTR	
MSRSALMEN	MSRSALM	
RSALMEN	RSALMEN	

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Indirect Register 2H: SARC Path Receive AIS-P Insert Enable Indirect Data (48 path)

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13	R/W	Unused	0
Bit 12	R/W	Unused	0
Bit 11	R/W	PTIMEN	0
Bit 10	R/W	PTIUEN	0
Bit 9	R/W	PERDIEN	0
Bit 8	R/W	PRDIEN	0
Bit 7	R/W	PPDIEN	0
Bit 6	R/W	PUNEQEN	0
Bit 5	R/W	PPLMEN	0
Bit 4	R/W	PPLUEN	0
Bit 3	R/W	PAISPTREN	0
Bit 2	R/W	PLOPTREN	0
Bit 1	R/W	MSRLAISINSEN	0
Bit 0	R/W	RLAISINSEN	0

This register is indirect 48 times for 48 paths.

RLAISINSEN to PTIMEN[1]

The enable bit allows the indication associated defect to be ORed into the output alarm. When the enable bit is set high, the corresponding defect indication is ORed with other defect indications and goes on the output alarm. When the enable bit is set low, the corresponding defect indication does not affect the output alarm.

The following table summarizes the enable bit, the defect and the output alarm.

Enable Bit	Defect	Output Alarm
		RPAISINS
PTIMEN	PTIM	
PTIUEN	PTIU	
PERDIEN	PERDI	
PRDIEN	PRDI	
PPDIEN	PPDI	
PUNEQUEN	PUNEQU	
PPLMEN	PPLM	
PPLUEN	PPLU	

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Enable Bit	Defect	Output Alarm
PAISPTREN	PAISPTR	
PLOPTREN	PLOPTR	
MSRLAISINSEN	MSRLAISINS	
RLAISINSEN	RLAISINS	

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Indirect Register 3H: SARC Path Transmit AIS-P Insert Enable Indirect Data (48 path)

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6		Unused	
Bit 5		Unused	
Bit 4		Unused	
Bit 3		Unused	
Bit 2	R/W	TPAISPTREN	0
Bit 1	R/W	TPLOPTREN	0
Bit 0	R/W	ADDPAISEN	0

This register is indirect 48 times for 48 paths.

ADDPAISEN to TPAISPTREN

The enable bit allows the indication associated defect to be ORed into the output alarm. When the enable bit is set high, the corresponding defect indication is ORed with other defect indications and goes on the output alarm, which is fed to the TSVCA. When the enable bit is set low, the corresponding defect indication does not affect the TPAISINS alarm. TPAISPTR and TPLOPTR come from the SHPI, while ADDPAIS comes from the TPAIS input port.

The following table summarizes the enable bit, the defect and the output alarm.

Enable Bit	Defect	Output Alarm
TPAISPTREN	TPAISPTR	TPAISINS
TPLOPTREN	TPLOPTR	
ADDPAISEN	ADDPAIS	

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15.10 RHPP Normal Registers

There are 16 RHPP (#1 - #16) blocks in 16 STM-4 processing slices with independent register sets. The master/slave configuration for the RHPPs depends on the payload mapping and is thus defined using top-level registers 0002H and 0003H as well as each RHPP Payload Config register (0102H).

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Register 0100H: RHPP Indirect Address

Bit	Type	Function	Default
Bit 15	R	BUSY	X
Bit 14	R/W	RWB	0
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9	R/W	ADDR[3]	0
Bit 8	R/W	ADDR[2]	0
Bit 7	R/W	ADDR[1]	0
Bit 6	R/W	ADDR[0]	0
Bit 5		Unused	
Bit 4		Unused	
Bit 3	R/W	PATH[3]	0
Bit 2	R/W	PATH[2]	0
Bit 1	R/W	PATH[1]	0
Bit 0	R/W	PATH[0]	0

PATH[3:0]

The STS-1/STM-0 path (PATH[3:0]) bits select which STS-1/STM-0 path is accessed by the current indirect transfer.

PATH[3:0]	STS-1/STM-0 path #
0000	Invalid path
0001-1100	Path #1 to Path #12
1101-1111	Invalid path

ADDR[3:0]

The address location (ADDR[3:0]) bits select which address location is accessed by the current indirect transfer.

Indirect Address ADDR[3:0]	Indirect Data
0000	Pointer Interpreter Configuration
0001	Error Monitor Configuration
0010	Pointer Value and ERDI
0011	Captured and Accepted PSL
0100	Expected PSL and PDI
0101	RHPP Pointer Interpreter status
0110	RHPP Path BIP Error Counter

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Indirect Address ADDR[3:0]	Indirect Data
0111	RHPP Path REI Error Counter
1000	RHPP Path Negative Justification Event Counter
1001	RHPP Path Positive Justification Event Counter
1010 to 1111	Unused

RWB

The active high read and active low write (RWB) bit selects if the current access to the internal RAM is an indirect read or an indirect write. Writing to the Indirect Address Register initiates an access to the internal RAM. When RWB is set to logic 1, an indirect read access to the RAM is initiated. The data from the addressed location in the internal RAM will be transferred to the Indirect Data Register. When RWB is set to logic 0, an indirect write access to the RAM is initiated. The data from the Indirect Data Register will be transferred to the addressed location in the internal RAM.

BUSY

The active high RAM busy (BUSY) bit reports if a previously initiated indirect access to the internal RAM has been completed. BUSY is set to logic 1 upon writing to the Indirect Address Register. BUSY is set to logic 0, upon completion of the RAM access. This register should be polled to determine when new data is available in the Indirect Data Register.

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Register 0101H: RHPP Indirect Data

Bit	Type	Function	Default
Bit 15	R/W	DATA[15]	0
Bit 14	R/W	DATA[14]	0
Bit 13	R/W	DATA[13]	0
Bit 12	R/W	DATA[12]	0
Bit 11	R/W	DATA[11]	0
Bit 10	R/W	DATA[10]	0
Bit 9	R/W	DATA[9]	0
Bit 8	R/W	DATA[8]	0
Bit 7	R/W	DATA[7]	0
Bit 6	R/W	DATA[6]	0
Bit 5	R/W	DATA[5]	0
Bit 4	R/W	DATA[4]	0
Bit 3	R/W	DATA[3]	0
Bit 2	R/W	DATA[2]	0
Bit 1	R/W	DATA[1]	0
Bit 0	R/W	DATA[0]	0

DATA[15:0]

The indirect access data (DATA[15:0]) bits hold the data transfer to or from the internal RAM during indirect access. When RWB is set to logic 1 (indirect read), the data from the addressed location in the internal RAM will be transferred to DATA[15:0]. BUSY should be polled to determine when the new data is available in DATA[15:0]. When RWB is set to logic 0 (indirect write), the data from DATA[15:0] will be transferred to the addressed location in the internal RAM. The indirect Data register must contain valid data before the indirect write is initiated by writing to the Indirect Address Register.

DATA[15:0] has a different meaning depending on which address of the internal RAM is being accessed.

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Indirect Register 00H: RHPP Pointer Interpreter Configuration

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R/W	Unused	0
Bit 6	R/W	Unused	0
Bit 5	R/W	NDFCNT	0
Bit 4	R/W	Reserved	0*
Bit 3	R/W	RELAYPAIS	0
Bit 2	R/W	JUST3DIS	0
Bit 1	R/W	SSEN	0
Bit 0		Unused	

*Bit #4 defaults to 0 but should be written to 1 in order to ensure compliant device operation. This is explained further in Section 14.2.2.

SSEN

The SS bits enable (SSEN) bit selects whether or not the SS bits are taking into account in the pointer interpreter state machine. When SSEN is set to logic 1, the SS bits must be set to 10 for a valid NORM_POINT, NDF_ENABLE, INC_IND, DEC_IND or NEW_POINT indication. When SSEN is set to logic 0, the SS bits are ignored.

JUST3DIS

The “justification more than 3 frames ago disable” (JUST3DIS) bit selects whether or not the INC_IND or DEC_IND pointer justifications must be more than 3 frames apart to be considered valid. When JUST3DIS is set to logic 0, the previous NDF_ENABLE, INC_IND or DEC_IND indication must be more than 3 frames ago or the present INC_IND or DEC_IND indication is considered an INV_POINT indication. NDF_ENABLE indications can be every frame regardless of the JUST3DIS bit. When JUST3DIS is set to logic 1, INC_IND or DEC_IND indication can be every frame.

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RELAYPAIS

The relay path AIS (RELAYPAIS) bit selects the condition to enter the path AIS state in the pointer interpreter state machine. When RELAYPAIS is set to logic 1, the path AIS state is entered with 1 X AIS_ind indication. When RELAYPAIS is set to logic 0, the path AIS state is entered with 3 X AIS_ind indications. This configuration bit also affects the concatenation pointer interpreter state machine.

NDFCNT

The new data flag counter (NDFCNT) bit selects the behavior of the consecutive NDF_ENABLE event counter in the pointer interpreter state machine. When NDFCNT is set to logic 1, the NDF_ENABLE definition is enabled NDF + ss. When NDFCNT is set to logic 0, the NDF_ENABLE definition is enabled NDF + ss + offset value in the range 0 to 782 (764 in TU-3 mode). This configuration bit only changes the NDF_ENABLE definition for the consecutive NDF_ENABLE even counter to count towards LOP-P defect when the pointer is out of range. This configuration bit has no bearing on pointer justification indication. It should be noted that this bit has no bearing on the INV_POINT counter, so an out of range NDF_ENABLE indication will always increment the INV_POINT counter irrespective of the NDFCNT bit setting.

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Indirect Register 01H: RHPP Error Monitor Configuration

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11	R/W	Unused	0
Bit 10	R/W	IPREIBLK	0
Bit 9	R/W	IBER	0
Bit 8	R/W	PREIBLKACC	0
Bit 7	R/W	B3EBLK	0
Bit 6	R/W	PBIPEBLKREI	0
Bit 5	R/W	PBIPEBLKACC	0
Bit 4	R/W	FSBIPDIS	0
Bit 3	R/W	PRDI10	0
Bit 2	R/W	PLMEND	0
Bit 1	R/W	PSL5	0
Bit 0	R/W	ALGO2	0

ALGO2

The payload signal label algorithm 2 (ALGO2) bit selects the algorithm for the PSL monitoring. When ALGO2 is set to logic 1, the ITU compliant algorithm is (algorithm 2) is used to monitor the PSL. When ALGO2 is set to logic 0, the TELCORDIA compliant algorithm (algorithm 1) is used to monitor the PSL. ALGO2 changes the PLU-P, PLM-P and PDI-P defect definitions but has no effect on UNEQ-P defect, accepted PSL and change of PSL definitions

PSL5

The payload signal label detection (PSL5) bit selects the path PSL persistence. When PSL5 is set to logic 1, a new PSL is accepted when the same PSL value is detected in the C2 byte for five consecutive frames. When PSL5 is set to logic 0, a new PSL is accepted when the same PSL value is detected in the C2 byte for three consecutive frames.

PLMEND

The payload label mismatch removal (PLMEND) bit controls the removal of a PLM-P defect when an UNEQ-P defect is declared. When PLMEND is set to logic 1, a PLM-P defect is terminated when an UNEQ-P defect is declared. When PLMEND is set to logic 0, a PLM-P defect is not terminated when an UNEQ-P defect is declared.

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PRDI10

The path remote defect indication detection (PRDI10) bit selects the path RDI and path ERDI persistence. When PRDI10 is set to logic 1, path RDI and path ERDI are accepted when the same pattern is detected in bits 5,6,7 of the G1 byte for ten consecutive frames. When PRDI10 is set to logic 0, path RDI and path ERDI are accepted when the same pattern is detected in bits 5,6,7 of the G1 byte for five consecutive frames.

FSBIPDIS

The disable fixed stuff columns during BIP-8 calculation (FSBIPDIS) bit controls the path BIP-8 calculation for an STS-1 (VC-3) payload. When FSBIPDIS is set to logic 1, the fixed stuff columns are not part of the BIP-8 calculation when processing an STS-1 (VC-3) payload. When FSBIPDIS is set to logic 0, the fixed stuff columns are part of the BIP-8 calculation when processing an STS-1 (VC-3) payload.

PBIPEBLKACC

The path block BIP-8 errors accumulation (PBIPEBLKACC) bit controls the accumulation of path BIP-8 errors. When PBIPEBLKACC is set to logic 1, the path BIP-8 error accumulation represents block BIP-8 errors (a maximum of 1 error per frame). When PBIPEBLKACC is set to logic 0, the path BIP-8 error accumulation represents BIP-8 errors (a maximum of 8 errors per frame).

PBIPEBLKREI

The path block BIP-8 errors (PBIPEBLKREI) bit controls the path REI errors returned to the THPP. When PBIPEBLKREI is set to logic 1, the path REI is updated with block BIP-8 errors (a maximum of 1 error per frame). When PBIPEBLKREI is set to logic 0, the path REI is updated with BIP-8 errors (a maximum of 8 errors per frame).

B3EBLK

The serial path block BIP-8 errors (B3EBLK) bit controls the indication of path BIP-8 errors on the B3E serial output. When B3EBLK is set to logic 1, B3E outputs block BIP-8 errors (a maximum of 1 error per frame). When B3EBLK is set to logic 0, B3E outputs BIP-8 errors (a maximum of 8 errors per frame).

PREIBLKACC

The path block REI errors accumulation (PREIBLKACC) bit controls the accumulation of path REI errors from the path status (G1) byte. When PREIBLK is set to logic 1, the extracted path REI errors are interpreted as block BIP-8 errors (a maximum of 1 error per frame). When PREIBLK is set to logic 0, the extracted path REI errors are interpret as BIP-8 errors (a maximum of 8 errors per frame).

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IBER

The inband error reporting (IBER) bit controls the inband regeneration of the path status (G1) byte. When IBER is set to logic 1, the path status byte is updated with the REI-P and the ERDI-P defects that must be returned to the far end. When IBER is set to logic 0, the path status byte is not altered.

IPREIBLK

The inband path REI block errors (IPREIBLK) bit controls the regeneration of the path REI errors in the path status (G1) byte. When IPREIBLK is set to logic 1, the path REI is updated with block BIP-8 errors (a maximum of 1 error per frame). When IPREIBLK is set to logic 0, the path REI is updated with BIP-8 errors (a maximum of 8 errors per frame).

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Indirect Register 02H: RHPP Pointer value and ERDI

Bit	Type	Function	Default
Bit 15	R	PERDIV[2]	X
Bit 14	R	PERDIV[1]	X
Bit 13	R	PERDIV[0]	X
Bit 12		Unused	X
Bit 11	R	SSV[1]	X
Bit 10	R	SSV[0]	X
Bit 9	R	PTRV[9]	X
Bit 8	R	PTRV[8]	X
Bit 7	R	PTRV[7]	X
Bit 6	R	PTRV[6]	X
Bit 5	R	PTRV[5]	X
Bit 4	R	PTRV[4]	X
Bit 3	R	PTRV[3]	X
Bit 2	R	PTRV[2]	X
Bit 1	R	PTRV[1]	X
Bit 0	R	PTRV[0]	X

PTRV[9:0]

The path pointer value (PTRV[9:0]) bits represent the current STS (AU) pointer being process by the pointer interpreter state machine or by the concatenation pointer interpreter state machine.

SSV[1:0]

The SS value (SSV[1:0]) bits represent the current SS (DD) bits being processed by the pointer interpreter state machine or by the concatenation pointer interpreter state machine.

PERDIV[2:0]

The path enhanced remote defect indication value (PERDIV[2:0]) bits represent the filtered path enhanced remote defect indication value. PERDIV[2:0] is updated when the same ERDI pattern is detected in bits 5,6,7 of the G1 byte for five or ten consecutive frames (selectable with the PRDI10 register bit).

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Indirect Register 03H: RHPP captured and accepted PSL

Bit	Type	Function	Default
Bit 15	R	CPSLV[7]	X
Bit 14	R	CPSLV[6]	X
Bit 13	R	CPSLV[5]	X
Bit 12	R	CPSLV[4]	X
Bit 11	R	CPSLV[3]	X
Bit 10	R	CPSLV[2]	X
Bit 9	R	CPSLV[1]	X
Bit 8	R	CPSLV[0]	X
Bit 7	R	APSLV[7]	X
Bit 6	R	APSLV[6]	X
Bit 5	R	APSLV[5]	X
Bit 4	R	APSLV[4]	X
Bit 3	R	APSLV[3]	X
Bit 2	R	APSLV[2]	X
Bit 1	R	APSLV[1]	X
Bit 0	R	APSLV[0]	X

APSLV[7:0]

The accepted path signal label value (APSLV[7:0]) bits represent the last accepted path signal label value. A new PSL is accepted when the same PSL value is detected in the C2 byte for three or five consecutive frames. (selectable with the PSL5 register bit). The APSLV[7:0] register bits are irrelevant when ALGO2 register bit is set to zero.

CPSLV[7:0]

The captured path signal label value (CPSLV[7:0]) bits represent the last captured path signal label value. A new PSL is captured every frame from the C2 byte.

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Indirect Register 04H: RHPP Expected PSL and PDI

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13	R/W	PDIRANGE	0
Bit 12	R/W	PDI[4]	0
Bit 11	R/W	PDI[3]	0
Bit 10	R/W	PDI[2]	0
Bit 9	R/W	PDI[1]	0
Bit 8	R/W	PDI[0]	0
Bit 7	R/W	EPSL[7]	0
Bit 6	R/W	EPSL[6]	0
Bit 5	R/W	EPSL[5]	0
Bit 4	R/W	EPSL[4]	0
Bit 3	R/W	EPSL[3]	0
Bit 2	R/W	EPSL[2]	0
Bit 1	R/W	EPSL[1]	0
Bit 0	R/W	EPSL[0]	0

EPSL[7:0]

The expected path signal label (EPSL[7:0]) bits represent the expected path signal label. The expected PSL and the expected PDI validate the received or the accepted PSL to declare PLM-P, UNEQ-P and PDI-P defects according Table 6.

PDI[4:0], PDIRANGE

The payload defect indication (PDI[4:0]) bits and the payload defect indication range (PDIRANGE) bit determine the expected payload defect indication according to Table 7. When PDIRANGE is set to logic 1, the PDI range is enabled and the expected PDI range is from E1H to E0H+PDI[4:0]. When PDIRANGE is set to logic 0, the PDI range is disable and the expected PDI value is E0H+PDI[4:0]. The expected PSL and the expected PDI validate the received or the accepted PSL to declare PLM-P, UNEQ-P and PDI-P defects according Table 6.

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Indirect Register 05H: RHPP Pointer Interpreter status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6	R	NDF	X
Bit 5	R	ILLPTR	X
Bit 4	R	INVNDF	X
Bit 3	R	DISCOPA	X
Bit 2	R	CONCAT	X
Bit 1	R	ILLJREQ	X
Bit 0		Unused	X

Note: The Pointer Interpreter Status bits are don't care for slave time slots, except for the CONCAT bit, which is defined for slave timeslots. The other bits may be set high for slave timeslots, but should be ignored.

ILLJREQ

The illegal pointer justification request (ILLJREQ) signal is set high when a positive and/or negative pointer adjustment is received within three frames of a pointer justification event (inc_ind, dec_ind) or an NDF triggered active offset adjustment (NDF_enable).

CONCAT

The CONCAT bit is set high if the H1 and H2 pointer bytes received match the concatenation indication (one of the five NDF_enable patterns in the NDF field, don't care in the size field, and all-ones in the pointer offset field).

DISCOPA

The discontinuous change of pointer alignment (DISCOPA) signal is set high when there is a pointer adjustment due to receiving a pointer repeated three times.

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INVNDF

The invalid new data flag (INVNDF) signal is set high when an invalid NDF code is received.

ILLPTR

The illegal pointer offset (ILLPTR) signal is set high when the pointer received is out of the range. Legal values are from 0 to 782. Pointer justification requests (inc_req, dec_req) are not considered illegal. The ILLPTR bit is set high for AIS indication

NDF

The new data flag (NDF) signal is set high when an enabled New Data Flag is received indicating a pointer adjustment (NDF_enabled indication).

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Indirect Register 06H: RHPP Path BIP Error Counter

Bit	Type	Function	Default
Bit 15	R	PBIPE[15]	X
Bit 14	R	PBIPE[14]	X
Bit 13	R	PBIPE[13]	X
Bit 12	R	PBIPE[12]	X
Bit 11	R	PBIPE[11]	X
Bit 10	R	PBIPE[10]	X
Bit 9	R	PBIPE[9]	X
Bit 8	R	PBIPE[8]	X
Bit 7	R	PBIPE[7]	X
Bit 6	R	PBIPE[6]	X
Bit 5	R	PBIPE[5]	X
Bit 4	R	PBIPE[4]	X
Bit 3	R	PBIPE[3]	X
Bit 2	R	PBIPE[2]	X
Bit 1	R	PBIPE[1]	X
Bit 0	R	PBIPE[0]	X

PBIPE[15:0]

The path BIP error (PBIPE[15:0]) bits represent the number of path BIP errors that have been detected in the B3 byte since the last accumulation interval. The error counters are transferred to the holding registers by a microprocessor write to the RHPP Counters Update register (Address 03H) or a write to the SPECTRA-9953 master configuration register. The TIP output indicates the transfer status.

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Indirect Register 07H: RHPP Path REI Error Counter

Bit	Type	Function	Default
Bit 15	R	PREIE[15]	X
Bit 14	R	PREIE[14]	X
Bit 13	R	PREIE[13]	X
Bit 12	R	PREIE[12]	X
Bit 11	R	PREIE[11]	X
Bit 10	R	PREIE[10]	X
Bit 9	R	PREIE[9]	X
Bit 8	R	PREIE[8]	X
Bit 7	R	PREIE[7]	X
Bit 6	R	PREIE[6]	X
Bit 5	R	PREIE[5]	X
Bit 4	R	PREIE[4]	X
Bit 3	R	PREIE[3]	X
Bit 2	R	PREIE[2]	X
Bit 1	R	PREIE[1]	X
Bit 0	R	PREIE[0]	X

PREIE[15:0]

The path REI error (PREIE[15:0]) bits represent the number of path REI errors that have been extracted from the G1 byte since the last accumulation interval. The error counters are transferred to the holding registers by a microprocessor write to the RHPP Counters Update register (Address 03H) or a write to the SPECTRA-9953 master configuration register. The TIP output indicates the transfer status.

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Indirect Register 08H: RHPP Path Negative Justification Event Counter

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12	R	PNJE[12]	X
Bit 11	R	PNJE[11]	X
Bit 10	R	PNJE[10]	X
Bit 9	R	PNJE[9]	X
Bit 8	R	PNJE[8]	X
Bit 7	R	PNJE[7]	X
Bit 6	R	PNJE[6]	X
Bit 5	R	PNJE[5]	X
Bit 4	R	PNJE[4]	X
Bit 3	R	PNJE[3]	X
Bit 2	R	PNJE[2]	X
Bit 1	R	PNJE[1]	X
Bit 0	R	PNJE[0]	X

PNJE[12:0]

The Path Negative Justification Event (PNJE[12:0]) bits represent the number of Path Negative Justification Events that have occured since the last accumulation interval. The event counters are transferred to the holding registers by a microprocessor write to RHPP Counters Update register (address 03H) or a write to the SPECTRA-9953 master configuration register . The TIP output indicates the transfer status.

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Indirect Register 09H: RHPP Path Positive Justification Event Counter

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12	R	PPJE[12]	X
Bit 11	R	PPJE[11]	X
Bit 10	R	PPJE[10]	X
Bit 9	R	PPJE[9]	X
Bit 8	R	PPJE[8]	X
Bit 7	R	PPJE[7]	X
Bit 6	R	PPJE[6]	X
Bit 5	R	PPJE[5]	X
Bit 4	R	PPJE[4]	X
Bit 3	R	PPJE[3]	X
Bit 2	R	PPJE[2]	X
Bit 1	R	PPJE[1]	X
Bit 0	R	PPJE[0]	X

PPJE[12:0]

The Path Positive Justification Event (PPJE[12:0]) bits represent the number of Path Positive Justification Events that have occured since the last accumulation interval. The event counters are transferred to the holding registers by a microprocessor write to RHPP Counters Update register (address X6H) or a write to the SPECTRA-9953 master configuration register . The TIP output indicates the transfer status.

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Register 0102H: RHPP Payload Configuration

Bit	Type	Function	Default
Bit 15	R/W	STS12CSL	0
Bit 14	R/W	STS12C	0
Bit 13	R/W	Reserved	0
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8	R/W	Reserved	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	STS3C[4]	0
Bit 2	R/W	STS3C[3]	0
Bit 1	R/W	STS3C[2]	0
Bit 0	R/W	STS3C[1]	0

STS3C[1]

The STS-3c (VC-4) payload configuration (STS3C[1]) bit selects the payload configuration. When STS3C[1] is set to logic 1, the STS-1/STM-0 paths #1, #5 and #9 are part of a STS-3c (VC-4) payload. When STS3C[1] is set to logic 0, the paths are STS-1 (VC-3) payloads. The STS12C register bit has precedence over the STS3C[1] register bit.

STS3C[2]

The STS-3c (VC-4) payload configuration (STS3C[2]) bit selects the payload configuration. When STS3C[2] is set to logic 1, the STS-1/STM-0 paths #2, #6 and #10 are part of a STS-3c (VC-4) payload. When STS3C[2] is set to logic 0, the paths are STS-1 (VC-3) payloads. The STS12C register bit has precedence over the STS3C[2] register bit.

STS3C[3]

The STS-3c (VC-4) payload configuration (STS3C[3]) bit selects the payload configuration. When STS3C[3] is set to logic 1, the STS-1/STM-0 paths #3, #7 and #11 are part of a STS-3c (VC-4) payload. When STS3C[3] is set to logic 0, the paths are STS-1 (VC-3) payloads. The STS12C register bit has precedence over the STS3C[3] register bit.

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STS3C[4]

The STS-3c (VC-4) payload configuration (STS3C[4]) bit selects the payload configuration. When STS3C[4] is set to logic 1, the STS-1/STM-0 paths #4, #8 and #12 are part of a STS-3c (VC-4) payload. When STS3C[4] is set to logic 0, the paths are STS-1 (VC-3) payloads. The STS12C register bit has precedence over the STS3C[4] register bit.

STS12C

The STS-12c (VC-4-4c) payload configuration (STS12C) bit selects the payload configuration. When STS12C is set to logic 1, the STS-1/STM-0 paths #1 to #12 are part of a STS-12c (VC-4-4c) payload. When STS12C is set to logic 0, the STS-1/STM-0 paths are defined with the STS3C[1:4] register bit. The STS12C register bit is OR'ed with the STS12C top-level receive configuration register 2. The STS12C register bit has precedence over the STS3C[1:4] register bit.

STS12CSL

The slave STS-12c (VC-4-4c) payload configuration (STS12CSL) bit selects the slave payload configuration. When STS12CSL is set to logic 1, the STS-1/STM-0 paths #1 to #12 are part of a STS-12c (VC-4-4c) slave payload. When STS12CSL is set to logic 0, the STS-1/STM-0 paths #1 to # 12 are part of a STS-12c (VC-4-4c) master payload. The STS12CSL register bit is OR'ed with the STS12CSL top-level receive configuration register 3. When STS12C is set to logic 0, the STS12CSL register bit has no effect.

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Register 0103H: RHPP Counters update

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

Any write to the RHPP Counters Update Register (address 03H) will trigger the transfer of all counter values to their holding registers. It is equivalent to a write to the SPECTRA-9953 master configuration register (0000H). Master configuration register TIP bit indicates the transfer status.

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Register 0104H: RHPP Path Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11	R	P_INT[12]	X
Bit 10	R	P_INT[11]	X
Bit 9	R	P_INT[10]	X
Bit 8	R	P_INT[9]	X
Bit 7	R	P_INT[8]	X
Bit 6	R	P_INT[7]	X
Bit 5	R	P_INT[6]	X
Bit 4	R	P_INT[5]	X
Bit 3	R	P_INT[4]	X
Bit 2	R	P_INT[3]	X
Bit 1	R	P_INT[2]	X
Bit 0	R	P_INT[1]	X

P_INT[1:12]

The Path Interrupt Status bit (P_INT[1:12]) tells which path(s) have interrupts that are still active. Reading from this register will not clear any of the interrupts, it is simply added to reduce the average number of accesses required to service interrupts.

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Register 0105H: Pointer Concatenation processing Disable

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11	R/W	PTRCDIS[12]	0
Bit 10	R/W	PTRCDIS[11]	0
Bit 9	R/W	PTRCDIS[10]	0
Bit 8	R/W	PTRCDIS[9]	0
Bit 7	R/W	PTRCDIS[8]	0
Bit 6	R/W	PTRCDIS[7]	0
Bit 5	R/W	PTRCDIS[6]	0
Bit 4	R/W	PTRCDIS[5]	0
Bit 3	R/W	PTRCDIS[4]	0
Bit 2	R/W	PTRCDIS[3]	0
Bit 1	R/W	PTRCDIS[2]	0
Bit 0	R/W	PTRCDIS[1]	0

PTRCDIS[1:12]

The concatenation pointer processing disable (PTRCDIS[1:12]) bits disable the relaying of LOPC-P, AISC-P and ALLAISC-P to the SARC. When PTRCDIS[n] is set to logic 1, the path concatenation pointer interpreter state-machine (for the path n) is enabled and the Pointer interpreter Status can be read at their register locations, but the information is not relayed to the Alarm Controller (SARC). When PTRCDIS is set to logic 0, the above defects are relayed to the SARC.

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Register 0108H 0110H 0118H 0120H 0128H 0130H 0138H 0140H 0148H 0150H 0158H and 0160H: RHPP Pointer Interpreter Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R	PAISCV	X
Bit 4	R	PLOPCV	X
Bit 3	R	PAISV	X
Bit 2	R	PLOPV	X
Bit 1		Unused	X
Bit 0		Unused	X

PLOPV

The path lost of pointer state (PLOPV) bit indicates the current status of the pointer interpreter state machine. PLOPV is set to logic 1 when the state machine is in the LOP_state. PLOPV is set to logic 0 when the state machine is not in the LOP_state.

PAISV

The path alarm indication signal state (PAISV) bit indicates the current status of the pointer interpreter state machine. PAISV is set to logic 1 when the state machine is in the AIS_state. PAISV is set to logic 0 when the state machine is not in the AIS_state.

PLOPCV

The path lost of pointer concatenation state (PLOPCV) bit indicates the current status of the concatenation pointer interpreter state machine. PLOPCV is set to logic 1 when the state machine is in the LOPC_state. PLOPCV is set to logic 0 when the state machine is not in the LOPC_state.

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PAISCV

The path concatenation alarm indication signal state (PAISCV) bit indicates the current status of the concatenation pointer interpreter state machine. PAISCV is set to logic 1 when the state machine is in the AISC_state. PAISCV is set to logic 0 when the state machine is not in the LOPC_state.

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Register 0109H 0111H 0119H 0121H 0129H 0131H 0139H 0141H 0149H 0151H 0159H and 0161H: RHPP Pointer Interpreter Interrupt Enable

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	PAISCE	0
Bit 4	R/W	PLOPCE	0
Bit 3	R/W	PAISE	0
Bit 2	R/W	PLOPE	0
Bit 1		Unused	X
Bit 0	R/W	PTRJEE	0

PTRJEE

The pointer justification event interrupt enable (PTRJEE) bit control the activation of the interrupt (INTB) output. When PTRJEE is set to logic 1, the NJEI and PJEI pending interrupt will assert the interrupt (INTB) output. When PTRJEE is set to logic 0, the NJEI and PJEI pending interrupt will not assert the interrupt (INTB) output.

PLOPE

The path loss of pointer interrupt enable (PLOPE) bit controls the activation of the interrupt (INTB) output. When PLOPE is set to logic 1, the PLOPI pending interrupt will assert the interrupt (INTB) output. When PLOPE is set to logic 0, the PLOPI pending interrupt will not assert the interrupt (INTB) output.

PAISE

The path alarm indication signal interrupt enable (PAISE) bit controls the activation of the interrupt (INTB) output. When PAISE is set to logic 1, the PAISI pending interrupt will assert the interrupt (INTB) output. When PAISE is set to logic 0, the PAISI pending interrupt will not assert the interrupt (INTB) output.

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PLOPCE

The path loss of pointer concatenation interrupt enable (PLOPCE) bit controls the activation of the interrupt (INTB) output. When PLOPCE is set to logic 1, the PLOPCI pending interrupt will assert the interrupt (INTB) output. When PLOPCE is set to logic 0, the PLOPCI pending interrupt will not assert the interrupt (INTB) output.

PAISCE

The path concatenation alarm indication signal interrupt enable (PAISCE) bit controls the activation of the interrupt (INTB) output. When PAISCE is set to logic 1, the PAISCI pending interrupt will assert the interrupt (INTB) output. When PAISCE is set to logic 0, the PAISCI pending interrupt will not assert the interrupt (INTB) output.

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Register 010AH 0112H 011AH 0122H 012AH 0132H 013AH 0142H 014AH 0152H 015AH and 0162H: RHPP Pointer Interpreter Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R	PAISCI	X
Bit 4	R	PLOPCI	X
Bit 3	R	PAISI	X
Bit 2	R	PLOPI	X
Bit 1	R	PJEI	X
Bit 0	R	NJEI	X

NJEI

The negative pointer justification event interrupt status (NJEI) bit is an event indicator. NJEI is set to logic 1 to indicate a negative pointer justification event. The interrupt status bit is independent of the interrupt enable bit. NJEI is cleared to logic 0 when this register is read.

PJEI

The positive pointer justification event interrupt status (PJEI) bit is an event indicator. PJEI is set to logic 1 to indicate a positive pointer justification event. The interrupt status bit is independent of the interrupt enable bit. PJEI is cleared to logic 0 when this register is read.

PLOPI

The path loss of pointer interrupt status (PLOPI) bit is an event indicator. PLOPI is set to logic 1 to indicate any change in the status of PLOPV (entry to the LOP_state or exit from the LOP_state). The interrupt status bit is independent of the interrupt enable bit. PLOPI is cleared to logic 0 when this register is read.

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PAISI

The path alarm indication signal interrupt status (PAISI) bit is an event indicator. PAISI is set to logic 1 to indicate any change in the status of PAISV (entry to the AIS_state or exit from the AIS_state). The interrupt status bit is independent of the interrupt enable bit. PAISI is cleared to logic 0 when this register is read.

PLOPCI

The path loss of pointer concatenation interrupt status (PLOPCI) bit is an event indicator. PLOPCI is set to logic 1 to indicate any change in the status of PLOPCV (entry to the LOPC_state or exit from the LOPC_state). The interrupt status bit is independent of the interrupt enable bit. PLOPCI is cleared to logic 0 when this register is read.

PAISCI

The path concatenation alarm indication signal interrupt status (PAISCI) bit is an event indicator. PAISCI is set to logic 1 to indicate any change in the status of PAISCV (entry to the AISC_state or exit from the AISC_state). The interrupt status bit is independent of the interrupt enable bit. PAISCI is cleared to logic 0 when this register is read.

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Register 010BH 0113H 011BH 0123H 012BH 0133H 013BH 0143H 014BH 0153H 015BH and 0163H: RHPP Error Monitor Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6	R	PERDIV	X
Bit 5	R	PRDIV	X
Bit 4	R	PPDIV	X
Bit 3	R	PUNEQV	X
Bit 2	R	PPLMV	X
Bit 1	R	PPLUV	X
Bit 0		Unused	X

PPLUV

The path payload label unstable status (PPLUV) bit indicates the current status of the PLU-P defect.

Algorithm 1: PPLUV is set to logic 0.

Algorithm 2: PPLUV is set to logic 1 when a total of 5 received PSL differs from the previously accepted PSL without any persistent PSL in between. PPLUV is set to logic 0 when a persistent PSL is found. A persistent PSL is found when the same PSL is received for 3 or 5 consecutive frames.

PPLMV

The path payload label mismatch status (PPLMV) bit indicates the current status of the PLM-P defect.

Algorithm 1: PPLMV is set to logic 1 when the received PSL does not match, according to Table 6, the expected PSL for 3 or 5 consecutive frames (selectable with the PSL5 register bit). PPLMV is set to logic 0 when the received PSL matches, according to Table 6, the expected PSL for 3 or 5 consecutive frames.

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Algorithm 2: PPLMV is set to logic 1 when the accepted PSL does not match, according to Table 6, the expected PSL. PPLMV is set to logic 0 when the accepted PSL matches, according to Table 6, the expected PSL.

PUNEQV

The path unequipped status (PUNEQV) bit indicates the current status of the UNEQ-P defect.

PUNEQV is set to logic 1 when the received PSL indicates unequipped, according to Table 6, for 3 or 5 consecutive frames (selectable with the PSL5 register bit). An PUNEQV is set to logic 0 when the received PSL indicates not unequipped, according to Table 6, for 3 or 5 consecutive frames.

PPDIV

The path payload defect indication status (PPDIV) bit indicates the current status of the PPDI-P defect.

Algorithm 1: PPDIV is set to logic one when the received PSL is a defect, according to Table 6, for 3 or 5 consecutive frames (selectable with the PSL5 register bit). PPDIV is set to logic 0 when the received PSL is not a defect, according to Table 6, for 3 or 5 consecutive frames.

Algorithm 2: PPDIV is set to logic 1 when the accepted PSL is a defect, according to Table 6. PPDI is set to logic 0 when the accepted PSL is not a defect, according to Table 6.

PRDIV

The path remote defect indication status (PRDIV) bit indicates the current status of the RDI-P defect. PRDIV is set to logic 1 when bit 5 of the G1 byte is set high for five or ten consecutive frames (selectable with the PRDI10 register bit). PRDIV is set to logic 0 when bit 5 of the G1 byte is set low for five or ten consecutive frames.

PERDIV

The path enhanced remote defect indication status (PERDIV) bit indicates the current status of the ERDI-P defect. PERDIV is set to logic 1 when the same 010, 100, 101, 110 or 111 pattern is detected in bits 5, 6 and 7 of the G1 byte for five or ten consecutive frames (selectable with the PRDI10 register bit). PERDIV is set to logic 0 when the same 000, 001 or 011 pattern is detected in bits 5, 6 and 7 of the G1 byte for five or ten consecutive frames.

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Register 010CH 0114H 011CH 0124H 012CH 0134H 013CH 0144H 014CH 0154H 015CH and 0164H: RHPP Error Monitor Interrupt Enable

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9	R/W	PREIEE	0
Bit 8	R/W	PBIPEE	0
Bit 7	R/W	COPERDIE	0
Bit 6	R/W	PERDIE	0
Bit 5	R/W	PRDIE	0
Bit 4	R/W	PPDIE	0
Bit 3	R/W	PUNEQE	0
Bit 2	R/W	PPLME	0
Bit 1	R/W	PPLUE	0
Bit 0	R/W	COPSLE	0

COPSLE

The change of path payload signal label interrupt enable (COPSLE) bit controls the activation of the interrupt (INTB) output. When COPSLE is set to logic 1, the COPSLI pending interrupt will assert the interrupt (INTB) output. When COPSLE is set to logic 0, the COPSLI pending interrupt will not assert the interrupt (INTB) output.

PPLUE

The path payload label unstable interrupt enable (PPLUE) bit controls the activation of the interrupt (INTB) output. When PPLUE is set to logic 1, the PPLUI pending interrupt will assert the interrupt (INTB) output. When PPLUE is set to logic 0, the PPLUI pending interrupt will not assert the interrupt (INTB) output.

PPLME

The path payload label mismatch interrupt enable (PPLME) bit controls the activation of the interrupt (INTB) output. When PPLME is set to logic 1, the PPLMI pending interrupt will assert the interrupt (INTB) output. When PPLME is set to logic 0, the PPLMI pending interrupt will not assert the interrupt (INTB) output.

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PUNEQE

The path payload unequipped interrupt enable (PUNEQE) bit controls the activation of the interrupt (INTB) output. When PUNEQE is set to logic 1, the PUNEQI pending interrupt will assert the interrupt (INTB) output. When PUNEQE is set to logic 0, the PUNEQI pending interrupt will not assert the interrupt (INTB) output.

PPDIE

The path payload defect indication interrupt enable (PPDIE) bit controls the activation of the interrupt (INTB) output. When PPDIE is set to logic 1, the PPDI pending interrupt will assert the interrupt (INTB) output. When PPDIE is set to logic 0, the PPDI pending interrupt will not assert the interrupt (INTB) output.

PRDIE

The path remote defect indication interrupt enable (PRDIE) bit controls the activation of the interrupt (INTB) output. When PRDIE is set to logic 1, the PRDII pending interrupt will assert the interrupt (INTB) output. When PRDIE is set to logic 0, the PRDII pending interrupt will not assert the interrupt (INTB) output.

PERDIE

The path enhanced remote defect indication interrupt enable (PERDIE) bit controls the activation of the interrupt (INTB) output. When PERDIE is set to logic 1, the PERDII pending interrupt will assert the interrupt (INTB) output. When PERDIE is set to logic 0, the PERDII pending interrupt will not assert the interrupt (INTB) output.

COPERDIE

The change of path enhanced remote defect indication interrupt enable (COPERDIE) bit controls the activation of the interrupt (INTB) output. When COPERDIE is set to logic 1, the COPERDII pending interrupt will assert the interrupt (INTB) output. When COPERDIE is set to logic 0, the COPERDII pending interrupt will not assert the interrupt (INTB) output.

PBIPEE

The path BIP-8 error interrupt enable (PBIPEE) bit controls the activation of the interrupt (INTB) output. When PBIPEE is set to logic 1, the PBIPEI pending interrupt will assert the interrupt (INTB) output. When PBIPEE is set to logic 0, the PBIPEI pending interrupt will not assert the interrupt (INTB) output.

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PREIEE

The path REI error interrupt enable (PREIEE) bit controls the activation of the interrupt (INTB) output. When PREIEE is set to logic 1, the PREIEI pending interrupt will assert the interrupt (INTB) output. When PREIEE is set to logic 0, the PREIEI pending interrupt will not assert the interrupt (INTB) output.

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Register 010DH 0115H 011DH 0125H 012DH 0135H 013DH 0145H 014DH 0155H 015DH and 0165H: RHPP Error Monitor Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9	R	PREIEI	X
Bit 8	R	PBIPEI	X
Bit 7	R	COPERDII	X
Bit 6	R	PERDII	X
Bit 5	R	PRDII	X
Bit 4	R	PPDII	X
Bit 3	R	PUNEQI	X
Bit 2	R	PPLMI	X
Bit 1	R	PPLUI	X
Bit 0	R	COPSLI	X

COPSLI

The change of path payload signal label interrupt status (COPSLI) bit is an event indicator. COPSLI is set to logic 1 to indicate a new PSL-P value. The interrupt status bit is independent of the interrupt enable bit. COPSLI is cleared to logic 0 when this register is read. ALGO2 register bit has no effect on COPSLI.

PPLUI

The path payload label unstable interrupt status (PPLUI) bit is an event indicator. PPLUI is set to logic 1 to indicate any change in the status of PPLUV (stable to unstable or unstable to stable). The interrupt status bit is independent of the interrupt enable bit. PPLUI is cleared to logic 0 when this register is read.

PPLMI

The path payload label mismatch interrupt status (PPLMI) bit is an event indicator. PPLMI is set to logic 1 to indicate any change in the status of PPLMV (match to mismatch or mismatch to match). The interrupt status bit is independent of the interrupt enable bit. PPLMI is cleared to logic 0 when this register is read.

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PUNEQI

The path payload unequipped interrupt status (PUNEQI) bit is an event indicator. PUNEQI is set to logic 1 to indicate any change in the status of PUNEQV (equipped to unequipped or unequipped to equipped). The interrupt status bit is independent of the interrupt enable bit. PUNEQI is cleared to logic 0 when this register is read.

PPDII

The path payload defect indication interrupt status (PPDII) bit is an event indicator. PPDII is set to logic 1 to indicate any change in the status of PPDIV (no defect to payload defect or payload defect to no defect). The interrupt status bit is independent of the interrupt enable bit. PPDII is cleared to logic 0 when this register is read.

PRDII

The path remote defect indication interrupt status (PRDII) bit is an event indicator. PRDII is set to logic 1 to indicate any change in the status of PRDIV (no defect to RDI defect or RDI defect to no defect). The interrupt status bit is independent of the interrupt enable bit. PRDII is cleared to logic 0 when this register is read.

PERDII

The path enhanced remote defect indication interrupt status (PERDII) bit is an event indicator. PERDII is set to logic 1 to indicate any change in the status of PERDIV (no defect to ERDI defect or ERDI defect to no defect). The interrupt status bit is independent of the interrupt enable bit. PERDII is cleared to logic 0 when this register is read.

COPERDII

The change of path enhanced remote defect indication interrupt status (COPERDII) bit is an event indicator. COPERDII is set to logic 1 to indicate a new ERDI-P value. The interrupt status bit is independent of the interrupt enable bit. COPERDII is cleared to logic 0 when this register is read.

PBIPEI

The path BIP-8 error interrupt status (PBIPEI) bit is an event indicator. PBIPEI is set to logic 1 to indicate a path BIP-8 error. The interrupt status bit is independent of the interrupt enable bit. PBIPEI is cleared to logic 0 when this register is read.

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PREIEI

The path REI error interrupt status (PREIEI) bit is an event indicator. PREIEI is set to logic 1 to indicate a path REI error. The interrupt status bit is independent of the interrupt enable bit. PREIEI is cleared to logic 0 when this register is read.

15.11 DSSI Normal Registers

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Register 0180H : DSSI Page 0 Source Selection for STS-12/STM-4 #1 to #4

Bit	Type	Function	Default
Bit 15	R/W	PG0[3][3]	0
Bit 14	R/W	PG0[3][2]	0
Bit 13	R/W	PG0[3][1]	1
Bit 12	R/W	PG0[3][0]	1
Bit 11	R/W	PG0[2][3]	0
Bit 10	R/W	PG0[2][2]	0
Bit 9	R/W	PG0[2][1]	1
Bit 8	R/W	PG0[2][0]	0
Bit 7	R/W	PG0[1][3]	0
Bit 6	R/W	PG0[1][2]	0
Bit 5	R/W	PG0[1][1]	0
Bit 4	R/W	PG0[1][0]	1
Bit 3	R/W	PG0[0][3]	0
Bit 2	R/W	PG0[0][2]	0
Bit 1	R/W	PG0[0][1]	0
Bit 0	R/W	PG0[0][0]	0

PG0[0-3][0-3]

The PG0[0-3][0-3] selects the STS-12/STM-4 SONET/SDH stream that is to be output on the STS-12/STM4 SONET/SDH stream #1 to #4Table 6default value being the STS-12/STM-4 stream itself.

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Register 0181H : DSSI Page 0 Source Selection for STS-12/STM-4 #5 to #8

Bit	Type	Function	Default
Bit 15	R/W	PG0[7][3]	0
Bit 14	R/W	PG0[7][2]	1
Bit 13	R/W	PG0[7][1]	1
Bit 12	R/W	PG0[7][0]	1
Bit 11	R/W	PG0[6][3]	0
Bit 10	R/W	PG0[6][2]	1
Bit 9	R/W	PG0[6][1]	1
Bit 8	R/W	PG0[6][0]	0
Bit 7	R/W	PG0[5][3]	0
Bit 6	R/W	PG0[5][2]	1
Bit 5	R/W	PG0[5][1]	0
Bit 4	R/W	PG0[5][0]	1
Bit 3	R/W	PG0[4][3]	0
Bit 2	R/W	PG0[4][2]	1
Bit 1	R/W	PG0[4][1]	0
Bit 0	R/W	PG0[4][0]	0

PG0[4-7][0-3]

The PG0[4-7][0-3] selects the STS-12/STM-4 SONET/SDH stream that is to be output on the STS-12/STM4 SONET/SDH stream #5 to #8, the default value being the STS-12/STM-4 stream itself.

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Register 0182H : DSSI Page 0 Source Selection for STS-12/STM-4 #9 to #12

Bit	Type	Function	Default
Bit 15	R/W	PG0[11][3]	1
Bit 14	R/W	PG0[11][2]	0
Bit 13	R/W	PG0[11][1]	1
Bit 12	R/W	PG0[11][0]	1
Bit 11	R/W	PG0[10][3]	1
Bit 10	R/W	PG0[10][2]	0
Bit 9	R/W	PG0[10][1]	1
Bit 8	R/W	PG0[10][0]	0
Bit 7	R/W	PG0[9][3]	1
Bit 6	R/W	PG0[9][2]	0
Bit 5	R/W	PG0[9][1]	0
Bit 4	R/W	PG0[9][0]	1
Bit 3	R/W	PG0[8][3]	1
Bit 2	R/W	PG0[8][2]	0
Bit 1	R/W	PG0[8][1]	0
Bit 0	R/W	PG0[8][0]	0

PG0[8-11][0-3]

The PG0[8-11][0-3] selects the STS-12/STM-4 SONET/SDH stream that is to be output on the STS-12/STM4 SONET/SDH stream #9 to #12, the default value being the STS-12/STM-4 stream itself.

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Register 0183H : DSSI Page 0 Source Selection for STS-12/STM-4 #13 to #16

Bit	Type	Function	Default
Bit 15	R/W	PG0[15][3]	1
Bit 14	R/W	PG0[15][2]	1
Bit 13	R/W	PG0[15][1]	1
Bit 12	R/W	PG0[15][0]	1
Bit 11	R/W	PG0[14][3]	1
Bit 10	R/W	PG0[14][2]	1
Bit 9	R/W	PG0[14][1]	1
Bit 8	R/W	PG0[14][0]	0
Bit 7	R/W	PG0[13][3]	1
Bit 6	R/W	PG0[13][2]	1
Bit 5	R/W	PG0[13][1]	0
Bit 4	R/W	PG0[13][0]	1
Bit 3	R/W	PG0[12][3]	1
Bit 2	R/W	PG0[12][2]	1
Bit 1	R/W	PG0[12][1]	0
Bit 0	R/W	PG0[12][0]	0

PG0[13-16][0-3]

The PG0[13-16][0-3] selects the STS-12/STM-4 SONET/SDH stream that is to be output on the STS-12/STM4 SONET/SDH stream #13 to #16, the default value being the STS-12/STM-4 stream itself.

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Register 0184H: DSSI Page 1 Source Selection for STS-12/STM-4 #1 to #4

Bit	Type	Function	Default
Bit 15	R/W	PG1[3][3]	0
Bit 14	R/W	PG1[3][2]	0
Bit 13	R/W	PG1[3][1]	1
Bit 12	R/W	PG1[3][0]	1
Bit 11	R/W	PG1[2][3]	0
Bit 10	R/W	PG1[2][2]	0
Bit 9	R/W	PG1[2][1]	1
Bit 8	R/W	PG1[2][0]	0
Bit 7	R/W	PG1[1][3]	0
Bit 6	R/W	PG1[1][2]	0
Bit 5	R/W	PG1[1][1]	0
Bit 4	R/W	PG1[1][0]	1
Bit 3	R/W	PG1[0][3]	0
Bit 2	R/W	PG1[0][2]	0
Bit 1	R/W	PG1[0][1]	0
Bit 0	R/W	PG1[0][0]	0

PG1[0-3][0-3]

The PG1[0-3][0-3] selects the STS-12/STM-4 SONET/SDH stream that is to be output on the STS-12/STM4 SONET/SDH stream #1 to #4, the default value being the STS-12/STM-4 stream itself.

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Register 0185H: DSSI Page 1 Source Selection for STS-12/STM-4 #5 to #8

Bit	Type	Function	Default
Bit 15	R/W	PG1[7][3]	0
Bit 14	R/W	PG1[7][2]	1
Bit 13	R/W	PG1[7][1]	1
Bit 12	R/W	PG1[7][0]	1
Bit 11	R/W	PG1[6][3]	0
Bit 10	R/W	PG1[6][2]	1
Bit 9	R/W	PG1[6][1]	1
Bit 8	R/W	PG1[6][0]	0
Bit 7	R/W	PG1[5][3]	0
Bit 6	R/W	PG1[5][2]	1
Bit 5	R/W	PG1[5][1]	0
Bit 4	R/W	PG1[5][0]	1
Bit 3	R/W	PG1[4][3]	0
Bit 2	R/W	PG1[4][2]	1
Bit 1	R/W	PG1[4][1]	0
Bit 0	R/W	PG1[4][0]	0

PG1[4-7][0-3]

The PG1[4-7][0-3] selects the STS-12/STM-4 SONET/SDH stream that is to be output on the STS-12/STM4 SONET/SDH stream #5 to #8, the default value being the STS-12/STM-4 stream itself.

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Register 0186H : DSSI Page 1 Source Selection for STS-12/STM-4 #9 to #12

Bit	Type	Function	Default
Bit 15	R/W	PG1[11][3]	1
Bit 14	R/W	PG1[11][2]	0
Bit 13	R/W	PG1[11][1]	1
Bit 12	R/W	PG1[11][0]	1
Bit 11	R/W	PG1[10][3]	1
Bit 10	R/W	PG1[10][2]	0
Bit 9	R/W	PG1[10][1]	1
Bit 8	R/W	PG1[10][0]	0
Bit 7	R/W	PG1[9][3]	1
Bit 6	R/W	PG1[9][2]	0
Bit 5	R/W	PG1[9][1]	0
Bit 4	R/W	PG1[9][0]	1
Bit 3	R/W	PG1[8][3]	1
Bit 2	R/W	PG1[8][2]	0
Bit 1	R/W	PG1[8][1]	0
Bit 0	R/W	PG1[8][0]	0

PG1[8-11][0-3]

The PG1[8-11][0-3] selects the STS-12/STM-4 SONET/SDH stream that is to be output on the STS-12/STM4 SONET/SDH stream #9 to #12, the default value being the STS-12/STM-4 stream itself.

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Register 0187H : DSSI Page 1 Source Selection for STS-12/STM-4 #13 to #16

Bit	Type	Function	Default
Bit 15	R/W	PG1[15][3]	1
Bit 14	R/W	PG1[15][2]	1
Bit 13	R/W	PG1[15][1]	1
Bit 12	R/W	PG1[15][0]	1
Bit 11	R/W	PG1[14][3]	1
Bit 10	R/W	PG1[14][2]	1
Bit 9	R/W	PG1[14][1]	1
Bit 8	R/W	PG1[14][0]	0
Bit 7	R/W	PG1[13][3]	1
Bit 6	R/W	PG1[13][2]	1
Bit 5	R/W	PG1[13][1]	0
Bit 4	R/W	PG1[13][0]	1
Bit 3	R/W	PG1[12][3]	1
Bit 2	R/W	PG1[12][2]	1
Bit 1	R/W	PG1[12][1]	0
Bit 0	R/W	PG1[12][0]	0

PG1[13-16][0-3]

The PG1[13-16][0-3] selects the STS-12/STM-4 SONET/SDH stream that is to be output on the STS-12/STM4 SONET/SDH stream #13 to #16, the default value being the STS-12/STM-4 stream itself.

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Register 0188H: DSSI Control Register

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6		Unused	
Bit 5		Unused	
Bit 4		Unused	
Bit 3		Unused	
Bit 2		Unused	
Bit 1		Unused	
Bit 0	R/W	IPS	0

The DSSI control register is provided at Read/Write Address 0188H. This register stores the internal page select (IPS), which is used for the selection of the control page. This internal bit allows the user to switch the page by changing the value in this register. In fact, either IPS or DCMP bits can be used independently for the page switching. This is implemented to provide both software and hardware control over the page selection, depending on the user preference.

IPS

The internal page select (IPS) bit is used in conjunction with the control page select (DCMP) input to select the active address page used by the DSSI. The IPS bit is XORed with the DCMP input signal and the logical result determines the page that will be used. When the result is logic 0, the page 0 is selected and, consequently, when the result is logic 1, the page 1 is selected. Reading this register bit provides the result of the XOR operation, thus providing the current page selected.

15.12 CSTRI Normal Registers

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Register 0190H: CSTRI Control

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W	Reserved	0
Bit 13	R/W	Reserved	0
Bit 12	R/W	Reserved	0
Bit 11	R/W	Reserved	0
Bit 10	R/W	Reserved	1
Bit 9	R/W	TXREF_CEN	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	CSU_ENB	0
Bit 3	R/W	CSU_RSTB	1
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R/W	Reserved	1

CSU_RSTB

The CSU_RSTB bit drives a software-reset signal that forces the CSU1250 into a reset. It is joined with the CSTRI ARB input signal (using an AND gate) and is then connected to the CSU_ARSTB output pin. For normal operation, it is held at logic '1'. To properly reset the CSU, the CSU_RSTB pin should be held low for at least 1 ms. Both the CSU_ENB bit and the CSU_IDDQ bit must be set to "0" during reset of the CSU.

CSU_ENB

The active low CSU enable control signal (CSU_ENB) bit can be used to force the CSU1250 into low power configuration if it is set to logic 1. For normal operation, it is set to logic 0. CSU_ENB (and CSU_IDDQ) must also be set to "0" while resetting the CSU. It is connected to the CSU_ENB pin.

TXREF_CEN

The TXLVREF chopper stabilization enable (TXREF_CEN) bit is connected to the TXREF_CEN output pin. It determines whether or not the offset correction circuitry (clocked by CCLK) is enabled in the TXLVREF_1250.

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Register 0191H: CSTRI Configuration and Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R	LOCKV	X
Bit 0	R/W	LOCKE	0

LOCKE

The CSU lock interrupt enable bit (LOCKE) controls the assertion of CSU lock state interrupts by the CSTRI. When LOCKE is high, an interrupt is generated on the interrupt output (INTB) when the CSU lock state changes. Interrupts due to changes in CSU lock state are masked when LOCKE is set low. Note that LOCKE only affects the INTB output; the LOCKI bit remains valid at all times.

LOCKV

The CSU lock status bit (LOCKV) indicates whether the clock synthesis unit is currently locked with the reference clock. LOCKV is set low when the CSU is not successfully locked with the reference clock. LOCKV is set high when the CSU is locked with the reference clock.

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Register 0192H: CSTRI Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R/W	LOCKI	0

LOCKI

The CSU lock interrupt status bit (LOCKI) responds to changes in the CSU lock state. Interrupts are to be generated as the CSU achieves lock with the reference clock or loses its lock to the reference clock. As a result, the LOCKI register bit is set high when any of these changes occurs. The LOCKI bit is cleared according to the value of WCIMODE. If WCIMODE is “0”, the LOCKI register bit will be cleared the next time it is read. If WCIMODE is “1”, the LOCKI register bit will be cleared when a ‘1’ is written to it. When LOCKE is set high, LOCKI is used to produce the interrupt output (INTB). Whether or not the interrupt is masked by the LOCKE bit, the LOCKI bit itself remains valid and may be polled to detect change of lock status events.

15.13 TRMP Normal Registers

There are 16 TRMP (#1 - #16) blocks in 16 STM-4 processing slices with independent register sets. When the SPECTRA-9953 is configured for quad STS-48/STM-16 mode, TRMP #1, #5, #9, #13 are configured as masters and the remaining TRMP blocks are configured as slaves. When configured for STS-192/STM-64 mode, only TRMP #1 is configured as master and the remaining blocks are configured as slaves.

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Register 2050H: TRMP Configuration

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11	R/W	LREIBLK	0
Bit 10	R/W	LREIEN	1
Bit 9	R/W	APSEN	1
Bit 8	R/W	TLDTS	1
Bit 7	R/W	TLDEN	0
Bit 6	R/W	TSLDSEL	0
Bit 5	R/W	TSLDTS	1
Bit 4	R/W	TSLDEN	0
Bit 3	R/W	TRACEEN	0
Bit 2	R/W	J0Z0INCEN	0
Bit 1	R/W	Z0DEF	0
Bit 0	R/W	A1A2EN	1

The TRMP Configuration register controls the transmit regenerator and Multiplexer functions.

These register bits are valid for both master and slave slices. Please refer to individual bit for details.

A1A2EN

The A1A2 framing enable (A1A2EN) bit controls the insertion of the framing bytes in the data stream. When A1A2EN is set to logic 1, F6h and 28h are inserted in the A1 and A2 bytes according to the priority of Table 10. When A1A2EN is set to logic 0, the framing bytes are not inserted.

This bit is valid for master and slave slices. For normal operation, this bit should be set to logic one for both master and slave slices.

Z0DEF

The Z0 definition (Z0DEF) bit defines the Z0 growth bytes. When Z0DEF is set to logic 0, the Z0 bytes are defined according to TELCORDIA. The Z0 bytes are located in STS-1/STM-0 #2 to #192 in STM64 mode and in STS-1/STM-0 # 2 to 48 in Quad STM-16 mode.

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When Z0DEF = 1, the bytes are defined according to ITU: Z0 bytes are STS-1/STM-0 #2 to #16 when in STM-16 interface mode and STS-1/STM-0 #2 to #64 when in STM-64 mode. When Z0DEF = 1, the user must ensure that remaining unused bytes (non-Z0 bytes) are inserted via TTOH ports to ensure proper transition density in these non-scrambled byte locations.

This bit is valid for master and slave slices. For normal operation, this bit should be set to the same value for both master and slave slices.

J0Z0INCEN

The J0 and Z0 increment enable (J0Z0INCEN) bit controls the insertion of an incremental pattern in the section trace and Z0 growth bytes. When J0ZOINCEN is set to logic 1, the corresponding STS-1/STM-0 path # is inserted in the J0 and Z0 bytes according to the priority of Table 10. When J0Z0INCEN is set to logic 0, no incremental pattern is inserted.

This bit is valid for master and slave slices. For normal operation, this bit should be set to the same value for both master and slave slices.

TRACEEN

The section trace enable (TRACEEN) bit controls the insertion of section trace in the data stream. When TRACEEN is set to logic 1, the section trace from the Section TTTP block is inserted in the J0 byte of STS-1/STM-0 #1 according to the priority of Table 10. When TRACEEN is set to logic 0, the section trace from the Section TTTP block is not inserted.

This bit is only valid for master slices.

TSLDEN

The TSLD enable (TSLDEN) bit controls the insertion of section or line DCC in the data stream. When TSLDEN is set to logic 1, the SPECTRA-9953 inserts all ones or all zeros as selected using the TSLD_VAL bit in the SPECTRA-9953 Transmit Control Register into the D1-D3 bytes or D4-D12 bytes of STS-1/STM-0 #1 according to the priority of Table 10. When TSLDEN is set to logic 0, the section or line DCC is not inserted.

This bit is only valid for master slices.

TSLDTS

The TSLD Tri-state control (TSLDTS) bit controls the TSLD output port. When TSLDTS is set to logic 1, the corresponding TSLDCLK output pin is tri-stated. When TSLDTS is set to logic 0, the corresponding TSLDCLK pin is driven.

This bit is only valid for master slices.

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TSLDSEL

The TSLD channel select (TSLDSEL) bit selects the contents of the TSLD port and the frequency of the TSLDCLK clock.

TSLDSEL	Contents	TOHCLK
0	Section DCC (D1-D3)	Nominal 192 kHz
1	Line DCC (D4-D12)	Nominal 576 kHz

TLDEN

The TLD enable (TLDEN) bit controls the insertion of line DCC in the data stream. When TLDEN is set to logic 1, the SPECTRA-9953 inserts all ones or all zeros as selected using the TLD_VAL bit in the SPECTRA-9953 Transmit Control Register into in the D4-D12 bytes of STS-1/STM-0 #1 according to the priority of Table 10. When TLDEN is set to logic 0, line DCC is not inserted.

This bit is only valid for master slices.

TLDTS

The TLDTS Tri-state control (TLDTS) bit controls the TLD output port. When TLDTS is set to logic 1, the corresponding TLDCLK output pin is tri-stated. When TLDTS is set to logic 0, the corresponding TLDCLK pin is driven.

This bit is only valid for master slices.

APSEN

The APS enable (APSEN) bit controls the insertion of automatic protection switching in the data stream. When APSEN is set to logic 1, the APS bytes from the RRMP are inserted in the K1/K2 bytes of STS-1/STM-0 #1 according to the priority of Table 10. When APSEN is set to logic 0, the APS bytes from the RRMP are not inserted.

This bit is only valid for master slices.

LREIEN

The line REI enable (LREIEN) bit controls the insertion of line remote error indication in the data stream. When LREIEN is set to logic 1, the line REI from the RRMP is inserted in the M1 byte of STS-1/STM-0 #3 according to the priority of Table 10. When LREIEN is set to logic 0, the line REI from the RRMP is not inserted.

This bit is only valid for master slices.

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LREIBLK

The line REI block error (LREIBLK) bit controls the generation of line remote error indication. When LREIBLK is set to logic 1, the line REI inserted in the M1 byte represents BIP-24 block errors (a maximum of 1 error per STS-3/STM-1 per frame). When LREIBLK is set to logic 0, the line REI inserted in the M1 byte represents BIP-8 errors (a maximum of 8 error per STS-1/STM-0 per frame up to a maximum of 255).

This bit is only valid for master slices.

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Register 2051H: TRMP Register Insertion

Bit	Type	Function	Default
Bit 15	R/W	UNUSEDV	0
Bit 14	R/W	UNUSEDEN	0
Bit 13	R/W	NATIONALV	0
Bit 12	R/W	NATIONALEN	0
Bit 11		Unused	X
Bit 10	R/W	E2REGEN	0
Bit 9	R/W	Z2REGEN	0
Bit 8	R/W	Z1REGEN	0
Bit 7	R/W	S1REGEN	0
Bit 6	R/W	D4D12REGEN	0
Bit 5	R/W	K1K2REGEN	0
Bit 4	R/W	D1D3REGEN	0
Bit 3	R/W	F1REGEN	0
Bit 2	R/W	E1REGEN	0
Bit 1	R/W	Z0REGEN	1
Bit 0	R/W	J0REGEN	1

The TRMP Register Insertion register controls the transmit regenerator and Multiplexer functions.

These register bits are only valid for master slices.

J0REGEN

The J0 register enable (J0REGEN) bit controls the insertion of section trace in the data stream. When J0REGEN is set to logic 1, the section trace from the TRMP Transmit J0 and Z0 register is inserted in the J0 byte of STS-1/STM-0 #1 according to the priority of Table 10. When J0REGEN is set to logic 0, the section trace from the TRMP Transmit J0 and Z0 register is not inserted.

Z0REGEN

The Z0 register enable (Z0REGEN) bit controls the insertion of Z0 growth bytes in the data stream. When Z0REGEN is set to logic 1, the Z0 growth byte from the TRMP Transmit J0 and Z0 register is inserted in the Z0 bytes according to the priority of Table 10. When Z0REGEN is set to logic 0, the Z0 growth byte from the TRMP Transmit J0 and Z0 register is not inserted. The Z0DEF bit in the TRMP Configuration register defines the Z0 bytes.

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E1REGEN

The E1 register enable (E1REGEN) bit controls the insertion of section order wire in the data stream. When E1REGEN is set to logic 1, the section order wire from the TRMP Transmit E1 and F1 register is inserted in the E1 byte of STS-1/STM-0 #1 according to the priority of Table 10. When E1REGEN is set to logic 0, the section order wire from the TRMP Transmit E1 and F1 register is not inserted.

F1REGEN

The F1 register enable (F1REGEN) bit controls the insertion of section user channel in the data stream. When F1REGEN is set to logic 1, the section user channel from the TRMP Transmit E1 and F1 register is inserted in the F1 byte of STS-1/STM-0 #1 according to the priority of Table 10. When F1REGEN is set to logic 0, the section user channel from the TRMP Transmit E1 and F1 register is not inserted.

D1D3REGEN

The D1 to D3 register enable (D1D3REGEN) bit controls the insertion of section data communication channel in the data stream. When D1D3REGEN is set to logic 1, the section DCC from the TRMP Transmit D1D3 and D4D12 register is inserted in the D1 to D3 bytes of STS-1/STM-0 #1 according to the priority of Table 10. When D1D3REGEN is set to logic 0, the section DCC from the TRMP Transmit D1D3 and D4D12 register is not inserted.

K1K2REGEN

The K1K2 register enable (K1K2REGEN) bit controls the insertion of automatic protection switching in the data stream. When K1K2REGEN is set to logic 1, the APS bytes from the TRMP Transmit K1 and K2 register are inserted in the K1, K2 bytes of STS-1/STM-0 #1 according to the priority of Table 10. When K1K2REGEN is set to logic 0, the APS bytes from the TRMP Transmit K1 and K2 register are not inserted.

D4D12REGEN

The D4 to D12 register enable (D4D12REGEN) bit controls the insertion of line data communication channel in the data stream. When D4D12REGEN is set to logic 1, the line DCC from the TRMP Transmit D1D3 and D4D12 register is inserted in the D4 to D12 bytes of STS-1/STM-0 #1 according to the priority of Table 10. When D4D12REGEN is set to logic 0, the line DCC from the TRMP Transmit D1D3 and D4D12 register is not inserted.

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S1REGEN

The S1 register enable (S1REGEN) bit controls the insertion of the synchronization status message in the data stream. When S1REGEN is set to logic 1, the SSM from the TRMP Transmit S1 and Z1 register is inserted in the S1 byte of STS-1/STM-0 #1 according to the priority of Table 10. When S1REGEN is set to logic 0, the SSM from the TRMP Transmit S1 and Z1 register is not inserted.

Z1REGEN

The Z1 register enable (Z1REGEN) bit controls the insertion of Z1 growth bytes in the data stream. When Z1REGEN is set to logic 1, the Z1 byte from the TRMP Transmit S1 and Z1 register is inserted in the Z1 bytes according to the priority of Table 10. When Z1REGEN is set to logic 0, the Z1 byte from the TRMP Transmit S1 and Z1 register is not inserted.

Z2REGEN

The Z2 register enable (Z2REGEN) bit controls the insertion of Z2 growth bytes in the data stream. When Z2REGEN is set to logic 1, the Z2 byte from the TRMP Transmit Z2 and E2 register is inserted in the Z2 bytes according to the priority of Table 10. When Z2REGEN is set to logic 0, the Z2 byte from the TRMP Transmit Z2 and E2 register is not inserted.

E2REGEN

The E2 register enable (E2REGEN) bit controls the insertion of line order wire in the data stream. When E2REGEN is set to logic 1, the line order wire from the TRMP Transmit Z2 and E2 register is inserted in the E2 byte of STS-1/STM-0 #1 according to the priority of Table 10. When E2REGEN is set to logic 0, the line order wire from the TRMP Transmit Z2 and E2 register is not inserted.

NATIONALEN

The national enable (NATIONALEN) bit controls the insertion of national bytes in the data stream. When NATIONALEN is set to logic 1, an all one or an all zero pattern is inserted in the national bytes according to the priority of Table 10. When NATIONALEN is set to logic 0, no pattern is inserted. The Z0DEF bit in the TRMP Configuration register defines the national bytes of ROW #1.

NATIONALV

The national value (NATIONALV) bit controls the value inserted in the national bytes. When NATIONALV is set to logic 1, an all one pattern is inserted in the national bytes if enabled via the NATIONALEN register bit. When NATIONALV is set to logic 0, an all zero pattern is inserted in the national bytes if enabled via the NATIONALEN register bit.

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UNUSEDEN

The unused enable (UNUSEDEN) bit controls the insertion of unused bytes in the data stream. When UNUSEDEN is set to logic 1, an all one or an all zero pattern is inserted in the unused bytes according to the priority of Table 10. When UNUSEDEN is set to logic 0, no pattern is inserted.

UNUSEDV

The unused value (UNUSEDV) bit controls the value inserted in the unused bytes. When UNUSEDV is set to logic 1, an all one pattern is inserted in the unused bytes if enabled via the UNUSEDEN register bit. When UNUSEDV is set to logic 0, an all zero pattern is inserted in the unused bytes if enabled via the UNUSEDEN register bit.

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Register 2052H: TRMP Error Insertion

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8	R/W	Reserved	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	LOSINS	0
Bit 5	R/W	LAISINS	0
Bit 4	R/W	LRDIINS	0
Bit 3	R/W	A1ERR	0
Bit 2	R/W	HMASKEN	1
Bit 1	R/W	B2MASKEN	1
Bit 0	R/W	B1MASKEN	1

The TRMP Error Insertion register controls the transmit regenerator and Multiplexer diagnostic features.

These register bits are valid for both master and slave slices. Please refer to individual bit for details.

B1MASKEN

The B1 mask enable (B1MASKEN) bit selects the use of the B1 byte extracted from the TTOH port. When B1MASKEN is set to logic 1, the B1 byte extracted from the TTOH port is used as a mask to toggle bits in the calculated B1 byte (the B1 byte extracted from the TTOH port is XOR with the calculated B1 byte). When B1MASKEN is set to logic 0, the B1 byte extracted from the TTOH port is inserted instead of the calculated B1 byte.

This bit is only valid for master slices.

B2MASKEN

The B2 mask enable (B2MASKEN) bit selects the use of the B2 bytes extracted from the TTOH port. When B2MASKEN is set to logic 1, the B2 bytes extracted from the TTOH port are used as a mask to toggle bits in the calculated B2 bytes (the B2 bytes extracted from the TTOH port are XOR with the calculated B2 bytes). When B2MASKEN is set to logic 0, the B2 bytes extracted from the TTOH port are inserted instead of the calculated B2 bytes.

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This bit is only valid for master slices.

HMASKEN

The H1/H2 mask enable (HMASKEN) bit selects the use of the H1/H2 bytes extracted from the TTOH port. When HMASKEN is set to logic 1, the H1/H2 bytes extracted from the TTOH port are used as a mask to toggle bits in the H1/H2 path payload pointer bytes (the H1/H2 bytes extracted from the TTOH port are XOR with the path payload pointer bytes). When HMASKEN is set to logic 0, the H1/H2 bytes extracted from the TTOH port are inserted instead of the internally generated path payload pointer bytes.

This bit is only valid for master slices.

A1ERR

The A1 error insertion (A1ERR) bit is used to introduce framing errors in the A1 bytes. When A1ERR is set to logic 1, 76h instead of F6h is inserted in all of the A1 bytes of the STS-12/STM-4 #1 according to the priority of Table 10. When A1ERR is set to logic 0, no framing errors are introduced.

This bit is only valid for master slices.

LRDIINS

The line RDI insertion (LRDIINS) bit is used to force a line remote defect indication in the data stream. When LRDIINS is set to logic 1, the 110 pattern is inserted in bits 6, 7 and 8 of the K2 byte of STS-1/STM-0 #1 to force a line RDI condition. When LRDIINS is set to logic 0, the line RDI condition is removed.

This bit is only valid for master slices.

LAISINS

The line AIS insertion (LAISINS) bit is used to force a line alarm indication signal in the data stream. When LAISINS is set to logic 1, all ones are inserted in the line overhead and in the payload (all the bytes of the frame except the section overhead bytes) to force a line AIS condition. When LAISINS is set to logic 0, the line AIS condition is removed. Line AIS is inserted/removed on frame boundary before scrambling.

This bit is valid for master and slave slices.

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LOSINS

The LOS insertion (LOSINS) bit is used to force a loss of signal condition in the data stream. When LOSINS is set to logic 1, the data steam is set to all zeros (after scrambling) to force a loss of signal condition. When LOSINS is set to logic 0, the loss of signal condition is removed.

This bit is valid for master and slave slices.

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Register 2053H: TRMP Transmit J0 and Z0

Bit	Type	Function	Default
Bit 15	R/W	J0V[7]	0
Bit 14	R/W	J0V[6]	0
Bit 13	R/W	J0V[5]	0
Bit 12	R/W	J0V[4]	0
Bit 11	R/W	J0V[3]	0
Bit 10	R/W	J0V[2]	0
Bit 9	R/W	J0V[1]	0
Bit 8	R/W	J0V[0]	1
Bit 7	R/W	Z0V[7]	1
Bit 6	R/W	Z0V[6]	1
Bit 5	R/W	Z0V[5]	0
Bit 4	R/W	Z0V[4]	0
Bit 3	R/W	Z0V[3]	1
Bit 2	R/W	Z0V[2]	1
Bit 1	R/W	Z0V[1]	0
Bit 0	R/W	Z0V[0]	0

These register bits are only valid for master slices.

Z0V[7:0]

The Z0 byte value (Z0V[7:0]) bits hold the Z0 growth byte to be inserted into the data stream. The Z0V[7:0] value is inserted in the Z0 bytes if the insertion is enabled via the Z0REGEN bit in the TRMP Register Insertion register. The Z0DEF bit in the TRMP Configuration register defines the Z0 bytes.

J0V[7:0]

The J0 byte value (J0V[7:0]) bits hold the section trace to be inserted into the data stream. The J0V[7:0] value is inserted in the J0 byte of STS-1/STM-0 #1 if the insertion is enabled via the J0REGEN bit in the TRMP Register Insertion register.

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Register 2054H: TRMP Transmit E1 and F1

Bit	Type	Function	Default
Bit 15	R/W	E1V[7]	0
Bit 14	R/W	E1V[6]	0
Bit 13	R/W	E1V[5]	0
Bit 12	R/W	E1V[4]	0
Bit 11	R/W	E1V[3]	0
Bit 10	R/W	E1V[2]	0
Bit 9	R/W	E1V[1]	0
Bit 8	R/W	E1V[0]	0
Bit 7	R/W	F1V[7]	0
Bit 6	R/W	F1V[6]	0
Bit 5	R/W	F1V[5]	0
Bit 4	R/W	F1V[4]	0
Bit 3	R/W	F1V[3]	0
Bit 2	R/W	F1V[2]	0
Bit 1	R/W	F1V[1]	0
Bit 0	R/W	F1V[0]	0

These register bits are only valid for master slices.

F1V[7:0]

The F1 byte value (F1V[7:0]) bits hold the section user channel to be inserted into the data stream. The F1V[7:0] value is inserted in the F1 byte of STS-1/STM-0 #1 if the insertion is enabled via the F1REGEN bit in the TRMP Register Insertion register.

E1V[7:0]

The E1 byte value (E1V[7:0]) bits hold the section order wire to be inserted into the data stream. The E1V[7:0] value is inserted in the E1 byte of STS-1/STM-0 #1 if the insertion is enabled via the E1REGEN bit in the TRMP Register Insertion register.

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Register 2055H: TRMP Transmit D1D3 and D4D12

Bit	Type	Function	Default
Bit 15	R/W	D1D3V[7]	0
Bit 14	R/W	D1D3V[6]	0
Bit 13	R/W	D1D3V[5]	0
Bit 12	R/W	D1D3V[4]	0
Bit 11	R/W	D1D3V[3]	0
Bit 10	R/W	D1D3V[2]	0
Bit 9	R/W	D1D3V[1]	0
Bit 8	R/W	D1D3V[0]	0
Bit 7	R/W	D4D12V[7]	0
Bit 6	R/W	D4D12V[6]	0
Bit 5	R/W	D4D12V[5]	0
Bit 4	R/W	D4D12V[4]	0
Bit 3	R/W	D4D12V[3]	0
Bit 2	R/W	D4D12V[2]	0
Bit 1	R/W	D4D12V[1]	0
Bit 0	R/W	D4D12V[0]	0

These register bits are only valid for master slices.

D4D12V[7:0]

The D4D12 byte value (D4D12V[7:0]) bits hold the line data communication channel to be inserted into the data stream. The D4D12V[7:0] value is inserted in the D4 to D12 bytes of STS-1/STM-0 #1 if the insertion is enabled via the D4D12REGEN bit in the TRMP Register Insertion register.

D1D3V[7:0]

The D1D3 byte value (D1D3V[7:0]) bits hold the section data communication channel to be inserted into the data stream. The D1D3V[7:0] value is inserted in the D1 to D3 bytes of STS-1/STM-0 #1 if the insertion is enabled via the D1D3REGEN bit in the TRMP Register Insertion register.

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Register 2056H: TRMP Transmit K1 and K2

Bit	Type	Function	Default
Bit 15	R/W	K1V[7]	0
Bit 14	R/W	K1V[6]	0
Bit 13	R/W	K1V[5]	0
Bit 12	R/W	K1V[4]	0
Bit 11	R/W	K1V[3]	0
Bit 10	R/W	K1V[2]	0
Bit 9	R/W	K1V[1]	0
Bit 8	R/W	K1V[0]	0
Bit 7	R/W	K2V[7]	0
Bit 6	R/W	K2V[6]	0
Bit 5	R/W	K2V[5]	0
Bit 4	R/W	K2V[4]	0
Bit 3	R/W	K2V[3]	0
Bit 2	R/W	K2V[2]	0
Bit 1	R/W	K2V[1]	0
Bit 0	R/W	K2V[0]	0

These register bits are only valid for master slices.

K1V[7:0], K2V[7:0]

The K1, K2 bytes value (K1V[7:0], K2V[7:0]) bits hold the APS bytes to be inserted into the data stream. The K1V[7:0], K2V[7:0] values are inserted in the K1, K2 bytes of STS-1/STM-0 #1 if the insertion is enabled via the K1K2REGEN bit in the TRMP Register Insertion register.

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Register 2057H: TRMP Transmit S1 and Z1

Bit	Type	Function	Default
Bit 15	R/W	S1V[7]	0
Bit 14	R/W	S1V[6]	0
Bit 13	R/W	S1V[5]	0
Bit 12	R/W	S1V[4]	0
Bit 11	R/W	S1V[3]	0
Bit 10	R/W	S1V[2]	0
Bit 9	R/W	S1V[1]	0
Bit 8	R/W	S1V[0]	0
Bit 7	R/W	Z1V[7]	0
Bit 6	R/W	Z1V[6]	0
Bit 5	R/W	Z1V[5]	0
Bit 4	R/W	Z1V[4]	0
Bit 3	R/W	Z1V[3]	0
Bit 2	R/W	Z1V[2]	0
Bit 1	R/W	Z1V[1]	0
Bit 0	R/W	Z1V[0]	0

These register bits are only valid for master slices.

Z1V[7:0]

The Z1 byte value (Z1V[7:0]) bits hold the Z1 growth byte to be inserted into the data stream. The Z1V[7:0] value is inserted in the Z1 byte if the insertion is enabled via the Z1REGEN bit in the TRMP Register Insertion register.

S1V[7:0]

The S1 byte value (S1V[7:0]) bits hold the synchronization status message to be inserted into the data stream. The S1V[7:0] value is inserted in the S1 byte of STS-1/STM-0 #1 if the insertion is enabled via the S1REGEN bit in the TRMP Register Insertion register.

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Register 2058H: TRMP Transmit Z2 and E2

Bit	Type	Function	Default
Bit 15	R/W	Z2V[7]	0
Bit 14	R/W	Z2V[6]	0
Bit 13	R/W	Z2V[5]	0
Bit 12	R/W	Z2V[4]	0
Bit 11	R/W	Z2V[3]	0
Bit 10	R/W	Z2V[2]	0
Bit 9	R/W	Z2V[1]	0
Bit 8	R/W	Z2V[0]	0
Bit 7	R/W	E2V[7]	0
Bit 6	R/W	E2V[6]	0
Bit 5	R/W	E2V[5]	0
Bit 4	R/W	E2V[4]	0
Bit 3	R/W	E2V[3]	0
Bit 2	R/W	E2V[2]	0
Bit 1	R/W	E2V[1]	0
Bit 0	R/W	E2V[0]	0

These register bits are only valid for master slices.

E2V[7:0]

The E2 byte value (E2[7:0]) bits hold the line order wire to be inserted into the data stream. The E2V[7:0] value is inserted in the E2 byte of STS-1/STM-0 #1 if the insertion is enabled via the E2REGEN bit in the TRMP Register Insertion register.

Z2V[7:0]

The Z2 byte value (Z2V[7:0]) bits hold the Z2 growth byte to be inserted into the data stream. The Z2V[7:0] value is inserted in the Z2 byte if the insertion is enabled via the Z2REGEN bit in the TRMP Register Insertion register.

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Register 2059H: TRMP Transmit H1 and H2 Mask

Bit	Type	Function	Default
Bit 15	R/W	H1MASK[7]	0
Bit 14	R/W	H1MASK[6]	0
Bit 13	R/W	H1MASK[5]	0
Bit 12	R/W	H1MASK[4]	0
Bit 11	R/W	H1MASK[3]	0
Bit 10	R/W	H1MASK[2]	0
Bit 9	R/W	H1MASK[1]	0
Bit 8	R/W	H1MASK[0]	0
Bit 7	R/W	H2MASK[7]	0
Bit 6	R/W	H2MASK[6]	0
Bit 5	R/W	H2MASK[5]	0
Bit 4	R/W	H2MASK[4]	0
Bit 3	R/W	H2MASK[3]	0
Bit 2	R/W	H2MASK[2]	0
Bit 1	R/W	H2MASK[1]	0
Bit 0	R/W	H2MASK[0]	0

These register bits are only valid for master slices.

H2MASK[7:0]

The H2 mask (H2MASK[7:0]) bits hold the H2 path payload pointer errors to be inserted into the data stream. The H2MASK[7:0] is XOR'ed with the path payload pointer already in the data stream.

H1MASK[7:0]

The H1 mask (H1MASK[7:0]) bits hold the H1 path payload pointer errors to be inserted into the data stream. The H1MASK[7:0] is XOR'ed with the path payload pointer already in the data stream.

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Register 205AH: TRMP Transmit B1 and B2 Mask

Bit	Type	Function	Default
Bit 15	R/W	B1MASK[7]	0
Bit 14	R/W	B1MASK[6]	0
Bit 13	R/W	B1MASK[5]	0
Bit 12	R/W	B1MASK[4]	0
Bit 11	R/W	B1MASK[3]	0
Bit 10	R/W	B1MASK[2]	0
Bit 9	R/W	B1MASK[1]	0
Bit 8	R/W	B1MASK[0]	0
Bit 7	R/W	B2MASK[7]	0
Bit 6	R/W	B2MASK[6]	0
Bit 5	R/W	B2MASK[5]	0
Bit 4	R/W	B2MASK[4]	0
Bit 3	R/W	B2MASK[3]	0
Bit 2	R/W	B2MASK[2]	0
Bit 1	R/W	B2MASK[1]	0
Bit 0	R/W	B2MASK[0]	0

These register bits are only valid for master slices.

B2MASK[7:0]

The B2 mask (B2MASK[7:0]) bits hold the B2 BIP-8 errors to be inserted into the data stream. The B2MASK[7:0] is XOR'ed with the calculated B2 before insertion in the B2 byte.

B1MASK[7:0]

The B1 mask (B1MASK[7:0]) bits hold the B1 BIP-8 errors to be inserted into the data stream. The B1MASK[7:0] is XOR'ed with the calculated B1 before insertion in the B1 byte.

15.14 STLI_192 Normal Registers

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Register 2060H: STLI Configuration

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R/W	Reserved	1
Bit 10	R/W	Reserved	1
Bit 9	R/W	Reserved	1
Bit 8	R/W	Reserved	1
Bit 7	R/W	PHASE_INIT[4]	0
Bit 6	R/W	PHASE_INIT[3]	0
Bit 5	R/W	PHASE_INIT[2]	0
Bit 4	R/W	PHASE_INIT[1]	0
Bit 3	R/W	INTERLEAVEEN4	1
Bit 2	R/W	INTERLEAVEEN3	1
Bit 1	R/W	INTERLEAVEEN2	1
Bit 0	R/W	INTERLEAVEEN1	1

INTERLEAVEEN[4:1]

The 4 byte interleave enable one (INTERLEAVEEN1) bit controls the 4 byte interleave rotation matrix in both STS-192/STM-64 and in quad STS-48/STM-16 modes. In STS-192/STM-64 mode, only INTERLEAVEEN1 is active and INTERLEAVEEN[4:3] has no effect. In quad STS-48/STM-16 mode, INTERLEAVEEN[n] bit controls the 4 byte interleave rotation matrix in the corresponding STS-48c (STM-16c) #n data stream. These bits should be set to there default values for normal operation.

PHASE_INIT[4:1]

The Phase Initialization register bits control the logic levels of the PHASE_INIT[N] outputs. If set to logic 0, the corresponding PHASE_INIT[N] output will be set low. If set to logic 1, the corresponding PHASE_INIT[N] output will be set high.

Reserved

The Reserved bits should be set to their default values for proper operation of the SPECTRA-9953.

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Register 2061H: STLI PGM Clock Configuration

Bit	Type	Function	Default
Bit 15	R/W	PGMTCLKSRC[1]	0
Bit 14	R/W	PGMTCLKSRC[0]	0
Bit 13	R/W	PGMTCLKSEL[1]	0
Bit 12	R/W	PGMTCLKSEL[0]	0
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7	R/W	RESERVED	0
Bit 6	R/W	RESERVED	0
Bit 5	R/W	RESERVED	0
Bit 4	R/W	RESERVED	0
Bit 3	R/W	RESERVED	0
Bit 2	R/W	RESERVED	0
Bit 1	R/W	RESERVED	0
Bit 0	R/W	RESERVED	0

The STLI Programmable Clock Configuration Register is used to configure the source and frequencies of the PGMTCLK output clock.

PGMTCLKSEL[1:0]

The programmable transmit clock frequency selection (PGMTCLKSEL) bits selects the frequency of the PGMTCLK output clock. When inactive,PGMTCLK is set to logic 0.

PGMTCLKSEL[1:0]	Source
00	Inactive
01	8KHz
10	19.44MHz
11	77.76MHz

PGMTCLKSRC[1:0]

The programmable transmit clock source (PGMTCLKSRC[1:0]) bits select the source of the PGMTCLK output clock

PGMTCLKSRC[1:0]	Source
00	TXCLK1
01	TXCLK2
10	TXCLK3
11	TXCLK4

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Register 2062H: STLI Interrupt Enable

Bit	Type	Function	Default
Bit 15	R	PH_ERR4	X
Bit 14	R	PH_ERR3	X
Bit 13	R	PH_ERR2	X
Bit 12	R	PH_ERR1	X
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7	R/W	PH_ERR_FE[4]	0
Bit 6	R/W	PH_ERR_FE[3]	0
Bit 5	R/W	PH_ERR_FE[2]	0
Bit 4	R/W	PH_ERR_FE[1]	0
Bit 3	R/W	PH_ERR_RE[4]	0
Bit 2	R/W	PH_ERR_RE[3]	0
Bit 1	R/W	PH_ERR_RE[2]	0
Bit 0	R/W	PH_ERR_RE[1]	0

PH_ERR_RE[4:1]

The phase error rising edge interrupt enable (PH_ERR_RE[4:1]) bits enable or disable PHASE_ERR[4:1] inputs as the source for a rising edge interrupt. When any PH_ERR_RE[4:1] bits are set to logic one, a rising edge on the corresponding PHASE_ERR[4:1] input will cause an interrupt. When any PH_ERR_RE[4:1] bits are set to logic 0, a rising edge on the corresponding PHASE_ERR[4:1] input can not cause an interrupt.

PH_ERR_FE[4:1]

The phase error falling edge interrupt enable (PH_ERR_FE[4:1] bits enable or disable PHASE_ERR[4:1] inputs as the source for a falling edge interrupt. When any PH_ERR_FE[4:1] bits are set to logic one, a falling edge on the corresponding PHASE_ERR[4:1] input will cause an interrupt. When any PH_ERR_FE[4:1] bits are set to logic 0, a falling edge on the corresponding PHASE_ERR[4:1] input can not cause an interrupt.

PH_ERR[4:1]

The phase error status (PH_ERR[4:1]) bits simply reflect the logic levels of the PHASE_ERR[4:1] inputs.

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Register 2063H: STLI Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7	R	PH_ERR4_FI	X
Bit 6	R	PH_ERR3_FI	X
Bit 5	R	PH_ERR2_FI	X
Bit 4	R	PH_ERR1_FI	X
Bit 3	R	PH_ERR4_RI	X
Bit 2	R	PH_ERR3_RI	X
Bit 1	R	PH_ERR2_RI	X
Bit 0	R	PH_ERR1_RI	X

If the WCIMODE bit in the SPECTRA-9953 Master Reset and Configuration Register (Register 0000H) is set high, these interrupt status bits are cleared on a write of logic one. Otherwise, these interrupt status bits are cleared on read.

PH_ERR[4:1]_RI

The phase error rising edge interrupt status (PH_ERR[N]_RI) bit is set to logic one if a rising edge has been detected on the corresponding PHASE_ERR[N] input. These interrupt sources can activate the INTB output if the corresponding interrupt bit, PH_ERR_RE[N] is set to logic one.

PH_ERR[4:1]_FI

The phase error falling edge interrupt status (PH_ERR[N]_FI) bit is set to logic one if a falling edge has been detected on the corresponding PHASE_ERR[N] input. These interrupt sources can activate the INTB output if the corresponding interrupt bit, PH_ERR_FE[N] is set to logic one.

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15.15 TTTP Section Normal Registers

There are 4 Section TTTP (#1 - #4) blocks in 4 STM-16 processing groups with independent register sets. When the SPECTRA-9953 is configured for quad STS-48/STM-16 mode, all four blocks are configured as masters to process the STS-48c/STM-16c data streams. When configured for STS-192/STM-64 mode, only TTTP #1 is configured as master and the other three (#2 - #4) blocks are inactive and may be considered as slaves.

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Register 20A0H: TTTP Section Indirect Address

Bit	Type	Function	Default
Bit 15	R	BUSY	X
Bit 14	R/W	RWB	0
Bit 13		Unused	
Bit 12	R/W	IADDR[6]	0
Bit 11	R/W	IADDR[5]	0
Bit 10	R/W	IADDR[4]	0
Bit 9	R/W	IADDR[3]	0
Bit 8	R/W	IADDR[2]	0
Bit 7	R/W	IADDR[1]	0
Bit 6	R/W	IADDR[0]	0
Bit 5		Unused	
Bit 4		Unused	
Bit 3	R/W	PATH[3]	0
Bit 2	R/W	PATH[2]	0
Bit 1	R/W	PATH[1]	0
Bit 0	R/W	PATH[0]	0

PATH[3:0]

PATH[3:0] must be set to “0001” for proper operation of the TTTP Section.

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IADDR[6:0]

The indirect address location (IADDR[6:0]) bits select which indirect address location is accessed by the current indirect transfer.

Indirect Address IADDR[6:0]	Indirect Data
000 0000	Configuration
000 0001 to 011 1111	Invalid address
100 0000	First byte of the 1/16/64 byte trace
100 0001 to 111 1111	Other bytes of the 16/64 byte trace

RWB

The active high read and active low write (RWB) bit selects if the current access to the internal RAM is an indirect read or an indirect write. Writing to the Indirect Address Register initiates an access to the internal RAM. When RWB is set to logic 1, an indirect read access to the RAM is initiated. The data from the addressed location in the internal RAM will be transferred to the Indirect Data Register. When RWB is set to logic 0, an indirect write access to the RAM is initiated. The data from the Indirect Data Register will be transferred to the addressed location in the internal RAM.

BUSY

The active high RAM busy (BUSY) bit reports if a previously initiated indirect access to the internal RAM has been completed. BUSY is set to logic 1 upon writing to the Indirect Address Register. BUSY is set to logic 0 upon completion of the RAM access. This register should be polled to determine when new data is available in the Indirect Data Register.

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Register 20A1H: TTTP Section Indirect Data

Bit	Type	Function	Default
Bit 15	R/W	DATA[15]	0
Bit 14	R/W	DATA[14]	0
Bit 13	R/W	DATA[13]	0
Bit 12	R/W	DATA[12]	0
Bit 11	R/W	DATA[11]	0
Bit 10	R/W	DATA[10]	0
Bit 9	R/W	DATA[9]	0
Bit 8	R/W	DATA[8]	0
Bit 7	R/W	DATA[7]	0
Bit 6	R/W	DATA[6]	0
Bit 5	R/W	DATA[5]	0
Bit 4	R/W	DATA[4]	0
Bit 3	R/W	DATA[3]	0
Bit 2	R/W	DATA[2]	0
Bit 1	R/W	DATA[1]	0
Bit 0	R/W	DATA[0]	0

DATA[15:0]

The indirect access data (DATA[15:0]) bits hold the data transfer to or from the internal RAM during indirect access. When RWB is set to logic 1 (indirect read), the data from the addressed location in the internal RAM will be transferred to DATA[15:0]. BUSY should be polled to determine when the new data is available in DATA[15:0]. When RWB is set to logic 0 (indirect write), the data from DATA[15:0] will be transferred to the addressed location in the internal RAM. The indirect Data register must contain valid data before the indirect write is initiated by writing to the Indirect Address Register.

DATA[15:0] has a different meaning depending on which address of the internal RAM is being accessed.

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Register 20A1H (Indirect Register 00H): TTTP Section Trace Configuration

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6		Unused	
Bit 5		Unused	
Bit 4		Unused	
Bit 3		Unused	
Bit 2	R/W	ZEROEN	0
Bit 1	R/W	BYTEEN	0
Bit 0	R/W	LENGTH16	0

LENGTH16

The message length (LENGTH16) bit selects the length of the trial trace message to be transmitted. When LENGTH16 is set to logic 1, the length of the trial trace message is 16 bytes. When LENGTH16 is set to logic 0, the length of the trial trace message is 64 bytes.

BYTEEN

The single byte message enable (BYTEEN) bit enables the single byte trial trace message. When BYTEEN is set to logic 1, the length of the trial trace message is 1 byte. When BYTEEN is set to logic 0, the length of the trial trace message is determined by LENGTH16. BYTEEN has precedence over LENGTH16.

ZEROEN

The all zero message enable (ZEROEN) bit enables the transmission of an all zero trial trace message. When ZEROEN is set to logic 1, an all zero message is transmitted. When ZEROEN is set to logic 0, the RAM message is transmitted. The enabling and disabling of the all zero trial trace message is not done on message boundary since the receiver is required to perform filtering on the message.

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Register 20A1H (Indirect Register 40H to 7FH): TTTP Section Indirect Register

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7	R/W	TRACE[7]	X
Bit 6	R/W	TRACE[6]	X
Bit 5	R/W	TRACE[5]	X
Bit 4	R/W	TRACE[4]	X
Bit 3	R/W	TRACE[3]	X
Bit 2	R/W	TRACE[2]	X
Bit 1	R/W	TRACE[1]	X
Bit 0	R/W	TRACE[0]	X

TRACE[7:0]

The trial trace message (TRACE[7:0]) bits contain the trial trace message to be transmitted. When BYTEEN is set to logic 1, the message is stored at indirect register address 40h. When BYTEEN is set to logic 0 and LENGTH16 is set to logic 1, the message is stored between indirect register address 40h and 4Fh. When BYTEEN is set to logic 0 and LENGTH16 is set to logic 0, the message is stored between indirect register address 40h and 7Fh.

15.16 TTTP Path Normal Registers

There are 16 Path TTTP (#1 - #16) blocks in 16 STM-4 processing groups with independent register sets. Depending on payload mapping, all paths of each Path TTTP blocks can be masters. Conversely, when processing an sts192c stream, only path #1 of TTTP #1 should be considered as a master.

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Register 20B0H: TTTP Path Indirect Address

Bit	Type	Function	Default
Bit 15	R	BUSY	X
Bit 14	R/W	RWB	0
Bit 13		Unused	
Bit 12	R/W	IADDR[6]	0
Bit 11	R/W	IADDR[5]	0
Bit 10	R/W	IADDR[4]	0
Bit 9	R/W	IADDR[3]	0
Bit 8	R/W	IADDR[2]	0
Bit 7	R/W	IADDR[1]	0
Bit 6	R/W	IADDR[0]	0
Bit 5		Unused	
Bit 4		Unused	
Bit 3	R/W	PATH[3]	0
Bit 2	R/W	PATH[2]	0
Bit 1	R/W	PATH[1]	0
Bit 0	R/W	PATH[0]	0

PATH[3:0]

The STS-1/STM-0 path (PATH[3:0]) bits select which STS-1/STM-0 path is accessed by the current indirect transfer. Only values “0001” to “1100” are valid. Paths #1 to #12 are valid when processing 12 STS-1/STM-0. Paths #1 to #4 are valid when processing 4 STS-3c/STM-1 and finally only path #1 is valid when processing an STS-12c/STM-4.

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IADDR[6:0]

The indirect address location (IADDR[6:0]) bits select which indirect address location is accessed by the current indirect transfer.

Indirect Address IADDR[6:0]	Indirect Data
000 0000	Configuration
000 0001 to 011 1111	Invalid address
100 0000	First byte of the 1/16/64 byte trace
100 0001 to 111 1111	Other bytes of the 16/64 byte trace

RWB

The active high read and active low write (RWB) bit selects if the current access to the internal RAM is an indirect read or an indirect write. Writing to the Indirect Address Register initiates an access to the internal RAM. When RWB is set to logic 1, an indirect read access to the RAM is initiated. The data from the addressed location in the internal RAM will be transferred to the Indirect Data Register. When RWB is set to logic 0, an indirect write access to the RAM is initiated. The data from the Indirect Data Register will be transferred to the addressed location in the internal RAM.

BUSY

The active high RAM busy (BUSY) bit reports if a previously initiated indirect access to the internal RAM has been completed. BUSY is set to logic 1 upon writing to the Indirect Address Register. BUSY is set to logic 0 upon completion of the RAM access. This register should be polled to determine when new data is available in the Indirect Data Register.

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Register 20B1H: TTTP Path Indirect Data

Bit	Type	Function	Default
Bit 15	R/W	DATA[15]	0
Bit 14	R/W	DATA[14]	0
Bit 13	R/W	DATA[13]	0
Bit 12	R/W	DATA[12]	0
Bit 11	R/W	DATA[11]	0
Bit 10	R/W	DATA[10]	0
Bit 9	R/W	DATA[9]	0
Bit 8	R/W	DATA[8]	0
Bit 7	R/W	DATA[7]	0
Bit 6	R/W	DATA[6]	0
Bit 5	R/W	DATA[5]	0
Bit 4	R/W	DATA[4]	0
Bit 3	R/W	DATA[3]	0
Bit 2	R/W	DATA[2]	0
Bit 1	R/W	DATA[1]	0
Bit 0	R/W	DATA[0]	0

DATA[15:0]

The indirect access data (DATA[15:0]) bits hold the data transfer to or from the internal RAM during indirect access. When RWB is set to logic 1 (indirect read), the data from the addressed location in the internal RAM will be transferred to DATA[15:0]. BUSY should be polled to determine when the new data is available in DATA[15:0]. When RWB is set to logic 0 (indirect write), the data from DATA[15:0] will be transferred to the addressed location in the internal RAM. The indirect Data register must contain valid data before the indirect write is initiated by writing to the Indirect Address Register.

DATA[15:0] has a different meaning depending on which address of the internal RAM is being accessed.

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Register 20B1H (Indirect Register 00H): TTTP Path Trace Configuration

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6		Unused	
Bit 5		Unused	
Bit 4		Unused	
Bit 3		Unused	
Bit 2	R/W	ZEROEN	0
Bit 1	R/W	BYTEEN	0
Bit 0	R/W	LENGTH16	0

LENGTH16

The message length (LENGTH16) bit selects the length of the trial trace message to be transmitted. When LENGTH16 is set to logic 1, the length of the trial trace message is 16 bytes. When LENGTH16 is set to logic 0, the length of the trial trace message is 64 bytes.

BYTEEN

The single byte message enable (BYTEEN) bit enables the single byte trial trace message. When BYTEEN is set to logic 1, the length of the trial trace message is 1 byte. When BYTEEN is set to logic 0, the length of the trial trace message is determined by LENGTH16. BYTEEN has precedence over LENGTH16.

ZEROEN

The all zero message enable (ZEROEN) bit enables the transmission of an all zero trial trace message. When ZEROEN is set to logic 1, an all zero message is transmitted. When ZEROEN is set to logic 0, the RAM message is transmitted. The enabling and disabling of the all zero trial trace message is not done on message boundary since the receiver is required to perform filtering on the message.

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Register 20B1H (Indirect Register 40H to 7FH): TTTP Path Indirect Register

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7	R/W	TRACE[7]	X
Bit 6	R/W	TRACE[6]	X
Bit 5	R/W	TRACE[5]	X
Bit 4	R/W	TRACE[4]	X
Bit 3	R/W	TRACE[3]	X
Bit 2	R/W	TRACE[2]	X
Bit 1	R/W	TRACE[1]	X
Bit 0	R/W	TRACE[0]	X

TRACE[7:0]

The trial trace message (TRACE[7:0]) bits contain the trial trace message to be transmitted. When BYTEEN is set to logic 1, the message is stored at indirect register address 40h. When BYTEEN is set to logic 0 and LENGTH16 is set to logic 1, the message is stored between indirect register address 40h and 4Fh. When BYTEEN is set to logic 0 and LENGTH16 is set to logic 0, the message is stored between indirect register address 40h and 7Fh.

15.17 TSVCA Normal Registers

There are 16 TSVCA (#1 - #16) blocks in 16 STM-4 processing slices with independent register sets.. The master/slave configuration for the TSVCAs depends on the payload mapping and is thus defined using top-level registers 0005H and 0006H as well as each TSVCA Payload Configuration register.

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Register 20C0H: TSVCA Indirect Address

Bit	Type	Function	Default
Bit 15	R	BUSY	X
Bit 14	R/W	RWB	0
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7	R/W	IADDR[1]	0
Bit 6	R/W	IADDR[0]	0
Bit 5		Unused	
Bit 4		Unused	
Bit 3	R/W	PATH[3]	0
Bit 2	R/W	PATH[2]	0
Bit 1	R/W	PATH[1]	0
Bit 0	R/W	PATH[0]	0

The Indirect Address Register is provided at SVCA Read/Write Address 00H.

RWB

The active high read and active low write (RWB) bit selects if the current access to the internal RAM is an indirect read or an indirect write. Writing to the Indirect Address Register initiates an access to the internal RAM. When RWB is set to logic 1, an indirect read access to the RAM is initiated. The data from the addressed location in the internal RAM will be transferred to the Indirect Data Register. When RWB is set to logic 0, an indirect write access to the RAM is initiated. The data from the Indirect Data Register will be transferred to the addressed location in the internal RAM.

BUSY

The active high RAM busy (BUSY) bit reports if a previously initiated indirect access to the internal RAM has been completed. BUSY is set to logic 1 upon writing to the Indirect Address Register. BUSY is set to logic 0, upon completion of the RAM access. This register should be polled to determine when new data is available in the Indirect Data Register.

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PATH[3:0]

The STS-1/STM-0 path (PATH[3:0]) bits select which STS-1/STM-0 path is accessed by the current indirect transfer. PATH[3:0] should only be written with master path locations. A read operation from an indirect register on a slave path returns the value from the master path. Also, slave path indirect registers are overwritten with the master path's indirect value. As such, when a TSVCA processes 12 x STS-1, all 12 indirect register paths are valid, while when a TSVCA processes an STS-12c, only the path #1 is valid. When a TSVCA is configured as a slave, path #1 is still valid.

PATH[3:0]	STS-1/STM-0 path #
0000	Invalid path
0001-1100	Path #1 to Path #12
1101-1111	Invalid path

IADDR[1:0]

The address location (ADDR[1:0]) bits select which address location is accessed by the current indirect transfer.

IADDR[1:0]	Indirect Register
00	SVCA Outgoing Positive Justification Performance Monitor
01	SVCA Outgoing Negative Justification Performance Monitor
10	SVCA Diagnostic/Configuration Register
11	Unused

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Register 20C1H: TSVCA Indirect Read/Write Data

Bit	Type	Function	Default
Bit 15	R/W	DATA[15]	0
Bit 14	R/W	DATA[14]	0
Bit 13	R/W	DATA[13]	0
Bit 12	R/W	DATA[12]	0
Bit 11	R/W	DATA[11]	0
Bit 10	R/W	DATA[10]	0
Bit 9	R/W	DATA[9]	0
Bit 8	R/W	DATA[8]	0
Bit 7	R/W	DATA[7]	0
Bit 6	R/W	DATA[6]	0
Bit 5	R/W	DATA[5]	0
Bit 4	R/W	DATA[4]	0
Bit 3	R/W	DATA[3]	0
Bit 2	R/W	DATA[2]	0
Bit 1	R/W	DATA[1]	0
Bit 0	R/W	DATA[0]	0

The Indirect Data Register is provided at SVCA Read/Write Address 01H.

DATA[15:0]

The indirect access data (DATA[15:0]) bits hold the data transfer to or from the internal RAM during indirect access. When RWB is set to logic 1 (indirect read), the data from the addressed location in the internal RAM will be transferred to DATA[15:0]. BUSY should be polled to determine when the new data is available in DATA[15:0]. When RWB is set to logic 0 (indirect write), the data from DATA[15:0] will be transferred to the addressed location in the internal RAM. The indirect Data register must contain valid data before the indirect write is initiated by writing to the Indirect Address Register.

DATA[15:0] has a different meaning depending on which address of the internal RAM is being accessed.

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Register 20C2H: TSVCA Payload Configuration Register[6]

Bit	Type	Function	Default
Bit 15	R/W	STS12CSL	0
Bit 14	R/W	STS12C	0
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	STS3C[4]	0
Bit 2	R/W	STS3C[3]	0
Bit 1	R/W	STS3C[2]	0
Bit 0	R/W	STS3C[1]	0

The Payload Configuration Register is provided at SVCA Read/Write Address 02H.

Note: there is a possibility that SVCA indirect registers can be corrupted upon path reconfiguration. Refer to section 14.13 for more explanation and how to avoid the problem.

STS3C[1]

The STS-3c (VC-4) payload configuration (STS3C[1]) bit selects the payload configuration. When STS3C[1] is set to logic 1, the STS-1/STM-0 paths #1, #5 and #9 are part of an STS-3c (VC-4) payload. When STS3C[1] is set to logic 0, the paths are STS-1 (VC-3) payloads. The STS12C register bit has precedence over the STS3C[1] register bit.

STS3C[2]

The STS-3c (VC-4) payload configuration (STS3C[2]) bit selects the payload configuration. When STS3C[2] is set to logic 1, the STS-1/STM-0 paths #2, #6 and #10 are part of an STS-3c (VC-4) payload. When STS3C[2] is set to logic 0, the paths are STS-1 (VC-3) payloads. The STS12C register bit has precedence over the STS3C[2] register bit.

[6] STS12CSL has precedence over all.

STS12C has precedence over STS3C configuration bits.

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STS3C[3]

The STS-3c (VC-4) payload configuration (STS3C[3]) bit selects the payload configuration. When STS3C[3] is set to logic 1, the STS-1/STM-0 paths #3, #7 and #11 are part of an STS-3c (VC-4) payload. When STS3C[3] is set to logic 0, the paths are STS-1 (VC-3) payloads. The STS12C register bit has precedence over the STS3C[3] register bit.

STS3C[4]

The STS-3c (VC-4) payload configuration (STS3C[4]) bit selects the payload configuration. When STS3C[4] is set to logic 1, the STS-1/STM-0 paths #4, #8 and #12 are part of an STS-3c (VC-4) payload. When STS3C[4] is set to logic 0, the paths are STS-1 (VC-3) payloads. The STS12C register bit has precedence over the STS3C[4] register bit.

STS12C

The STS-12c (VC-4-4c) payload configuration (STS12C) bit selects the payload configuration. When STS12C is set to logic 1, the STS-1/STM-0 paths #1 to #12 are part of an STS-12c (VC-4-4c) payload. When STS12C is set to logic 0, the STS-1/STM-0 paths are defined with the STS3C[1:4] register bit. The STS12C register bit is OR'ed with the STS12C SPECTRA-9953 transmit configuration register 2 (0005H) corresponding register bit. The STS12C register bit has precedence over the STS3C[1:4] register bit.

STS12CSL

The STS-12c/VC-4-4c slave concatenation (STS12CSL) signal enables the slave processing of an STS-12c/VC-4-4c payload. When STS12CSL is logic one, the SVCA process a slave STS-12c/VC-4-4c payload. When STS12CSL is logic zero, the SVCA process a master STS-12c/VC-4-4c payload. One master SVCA and three slaves SVCA can be used to process an STS-48c/VC-4-16c payload. One master SVCA and fifteen slaves SVCA can be used to process an STS-192c/VC-4-64c payload. The STS12CSL register bit is OR'ed with the device STS12CSL SPECTRA-9953 transmit configuration register 3 (0006H) corresponding register bit. The STS12CSL register bit has precedence over the STS3C[1:4] register bit.

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Register 20C3H: TSVCA Positive Pointer Justification Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R	PPJI[12]	0
Bit 10	R	PPJI[11]	0
Bit 9	R	PPJI[10]	0
Bit 8	R	PPJI[9]	0
Bit 7	R	PPJI[8]	0
Bit 6	R	PPJI[7]	0
Bit 5	R	PPJI[6]	0
Bit 4	R	PPJI[5]	0
Bit 3	R	PPJI[4]	0
Bit 2	R	PPJI[3]	0
Bit 1	R	PPJI[2]	0
Bit 0	R	PPJI[1]	0

The Positive Pointer Justification Interrupt Status Register is provided at SVCA Read/Write Address 03H.

PPJI[12:1]

The positive pointer justification interrupt status (PPJI[12:1]) bits are event indicators for STS-1/STM-0 paths #1 to #12. PPJI[12:1] are set to logic 1 to indicate a positive pointer justification event in the outgoing data stream. These interrupt status bits are independent of the interrupt enable bits. PPJI[12:1] are cleared to logic 0 when this register is read and WCIMODE input is logic 0. Each bit is independently cleared when WCIMODE is logic 1 and a write access with the corresponding bit is set to 1 is performed.

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Register 20C4H: TSVCA Negative Pointer Justification Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R	NPJI[12]	0
Bit 10	R	NPJI[11]	0
Bit 9	R	NPJI[10]	0
Bit 8	R	NPJI[9]	0
Bit 7	R	NPJI[8]	0
Bit 6	R	NPJI[7]	0
Bit 5	R	NPJI[6]	0
Bit 4	R	NPJI[5]	0
Bit 3	R	NPJI[4]	0
Bit 2	R	NPJI[3]	0
Bit 1	R	NPJI[2]	0
Bit 0	R	NPJI[1]	0

The Negative Pointer Justification Interrupt Status Register is provided at SVCA Read/Write Address 04H.

NPJI[12:1]

The negative pointer justification interrupt status (NPJI[12:1]) bits are event indicators for STS-1/STM-0 paths #1 to #12. NPJI[12:1] are set to logic 1 to indicate a negative pointer justification event in the outgoing data stream. These interrupt status bits are independent of the interrupt enable bits. NPJI[12:1] are cleared to logic 0 when this register is read and WCIMODE input is logic 0. Each bit is independently cleared when WCIMODE is logic 1 and a write access with the corresponding bit is set to 1 is performed.

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Register 20C5H: TSVCA FIFO Overflow Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R	FOVRI[12]	0
Bit 10	R	FOVRI[11]	0
Bit 9	R	FOVRI[10]	0
Bit 8	R	FOVRI[9]	0
Bit 7	R	FOVRI[8]	0
Bit 6	R	FOVRI[7]	0
Bit 5	R	FOVRI[6]	0
Bit 4	R	FOVRI[5]	0
Bit 3	R	FOVRI[4]	0
Bit 2	R	FOVRI[3]	0
Bit 1	R	FOVRI[2]	0
Bit 0	R	FOVRI[1]	0

The FIFO overflow Event Interrupt Status Register is provided at SVCA Read/Write Address 05H.

FOVRI[12:1]

The FIFO overflow event interrupt status (FOVRI[12:1]) bits are event indicators for STS-1/STM-0 paths #1 to #12. FOVRI[12:1] are set to logic 1 to indicate a FIFO overflow event. These interrupt status bits are independent of the interrupt enable bits. FOVRI[12:1] are cleared to logic 0 when this register is read and WCIMODE input is logic 0. Each bit is independently cleared when WCIMODE is logic 1 and a write access with the corresponding bit is set to 1 is performed.

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Register 20C6H: TSVCA FIFO Underflow Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R	FUDRI[12]	0
Bit 10	R	FUDRI[11]	0
Bit 9	R	FUDRI[10]	0
Bit 8	R	FUDRI[9]	0
Bit 7	R	FUDRI[8]	0
Bit 6	R	FUDRI[7]	0
Bit 5	R	FUDRI[6]	0
Bit 4	R	FUDRI[5]	0
Bit 3	R	FUDRI[4]	0
Bit 2	R	FUDRI[3]	0
Bit 1	R	FUDRI[2]	0
Bit 0	R	FUDRI[1]	0

The FIFO underflow Event Interrupt Status Register is provided at SVCA Read/Write Address 06H.

FUDRI[12:1]

The FIFO underflow event interrupt status (FUDR[12:1]) bits are event indicators for STS-1/STM-0 paths #1 to #12. FUDRI[12:1] are set to logic 1 to indicate a FIFO underflow event. These interrupt status bits are independent of the interrupt enable bits. FUDRI[12:1] are cleared to logic 0 when this register is read and WCIMODE input is logic 0. Each bit is independently cleared when WCIMODE is logic 1 and a write access with the corresponding bit is set to 1 is performed.

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Register 20C7H: TSVCA Pointer Justification Interrupt Enable

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R/W	PJIE[12]	0
Bit 10	R/W	PJIE[11]	0
Bit 9	R/W	PJIE[10]	0
Bit 8	R/W	PJIE[9]	0
Bit 7	R/W	PJIE[8]	0
Bit 6	R/W	PJIE[7]	0
Bit 5	R/W	PJIE[6]	0
Bit 4	R/W	PJIE[5]	0
Bit 3	R/W	PJIE[4]	0
Bit 2	R/W	PJIE[3]	0
Bit 1	R/W	PJIE[2]	0
Bit 0	R/W	PJIE[1]	0

The Pointer Justification Interrupt Enable Register is provided at SVCA direct Read/Write Address 07H.

PJIEN[12:1]

The pointer justification event interrupt enable (PJIE[12:1]) bits controls the activation of the interrupt (INTB) output for STS-1/STM-0 paths #1 to #12. When any of these bit locations is set to logic 1, the corresponding pending interrupt will assert the interrupt (INTB) output. When any of these bit locations is set to logic 0, the corresponding pending interrupt will not assert the interrupt (INTB) output.

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Register 20C8H: TSVCA FIFO Interrupt Enable

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11	R/W	FIE[12]	0
Bit 10	R/W	FIE[11]	0
Bit 9	R/W	FIE[10]	0
Bit 8	R/W	FIE[9]	0
Bit 7	R/W	FIE[8]	0
Bit 6	R/W	FIE[7]	0
Bit 5	R/W	FIE[6]	0
Bit 4	R/W	FIE[5]	0
Bit 3	R/W	FIE[4]	0
Bit 2	R/W	FIE[3]	0
Bit 1	R/W	FIE[2]	0
Bit 0	R/W	FIE[1]	0

The FIFO Event Interrupt Enable Register is provided at SVCA Read/Write Address 08H.

FIEN[12:1]

The FIFO event interrupt enable (FIE[12:1]) bits controls the activation of the interrupt (INTB) output for STS-1/STM-0 paths #1 to #12 caused by a FIFO overflow or a FIFO underflow. When any of these bit locations is set to logic 1, the corresponding pending interrupt will assert the interrupt (INTB) output. When any of these bit locations is set to logic 0, the corresponding pending interrupt will not assert the interrupt (INTB) output.

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Register 20C9H: TSVCA Pointer justification thresholds

Bit	Type	Function	Default
Bit 15	R/W	NTHRES[3]	0
Bit 14	R/W	NTHRES[2]	1
Bit 13	R/W	NTHRES[1]	1
Bit 12	R/W	NTHRES[0]	1
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6		Unused	
Bit 5		Unused	
Bit 4		Unused	
Bit 3	R/W	PTHRES[3]	0
Bit 2	R/W	PTHRES[2]	1
Bit 1	R/W	PTHRES[1]	1
Bit 0	R/W	PTHRES[0]	1

The SVCA pointer justification thresholds is provided at SVCA Read/Write Address 08H.

PTHRES[3:0]

The SVCA positive pointer justification thresholds determines the FIFO fill thresholds that triggers a positive pointer justification is requested. If the FIFO fill level is less than the PTHRES, than a positive justification is performed.

NTHRES[3:0]

The SVCA positive pointer justification thresholds determines the FIFO fill thresholds that triggers a negative pointer justification is requested. If the FIFO fill level is greater than the NTHRES, than a negative justification is performed.

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Register 20CAH: TSVCA Miscellaneous Register

Bit	Type	Function	Default
Bit 15	R/W	Reserved	0
Bit 14	R/W		0
Bit 13		Unused	
Bit 12		Unused	0
Bit 11	R/W	CLRFS[12]	0
Bit 10	R/W	CLRFS[11]	0
Bit 9	R/W	CLRFS[10]	0
Bit 8	R/W	CLRFS[9]	0
Bit 7	R/W	CLRFS[8]	0
Bit 6	R/W	CLRFS[7]	0
Bit 5	R/W	CLRFS[6]	0
Bit 4	R/W	CLRFS[5]	0
Bit 3	R/W	CLRFS[4]	0
Bit 2	R/W	CLRFS[3]	0
Bit 1	R/W	CLRFS[2]	0
Bit 0	R/W	CLRFS[1]	0

The FIFO MISC register provides miscellaneous control bits. It is provided at Read/Write Address 0AH.

CLRFS

The Clear Fixed Stuff (CLRFS) enables the regeneration of fixed stuff columns (#30, #59) of an STS-1/VC-3. When set to logic one, STS-1/VC-3 incoming fixed stuff columns (#30, #59) are discarded and regenerated (set to 00h) on the outgoing stream . When set to logic 0, these fixed stuff columns are relayed through the SVCA.

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Register 20CBH: TSVCA Performance Monitor Trigger

The Performance monitor transfer register is provided at Read/Write Address 20CBH. Any write to this register triggers a transfer of all performance monitor counters to holding registers that can be read by the ecbi interface.

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Indirect Register 00H: TSVCA Positive Justifications Performance Monitor

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12	R	PJPMON[12]	0
Bit 11	R	PJPMON[11]	0
Bit 10	R	PJPMON[10]	0
Bit 9	R	PJPMON[9]	0
Bit 8	R	PJPMON[8]	0
Bit 7	R	PJPMON[7]	0
Bit 6	R	PJPMON[6]	0
Bit 5	R	PJPMON[5]	0
Bit 4	R	PJPMON[4]	0
Bit 3	R	PJPMON[3]	0
Bit 2	R	PJPMON[2]	0
Bit 1	R	PJPMON[1]	0
Bit 0	R	PJPMON[0]	0

The Outgoing Positive justifications performance monitor is provided at SVCA indirect Read/Write Address 00H.

PJPMON[12:0][12:1]

This register reports the number of positive pointer justification events that occurred on the outgoing side in the previous accumulation interval. The content of this register becomes valid a maximum of 155ns (12 clock cycles) after a transfer is triggered by writing the SVCA performance monitor trigger direct register or a write to the SPECTRA-9953 master configuration register . The value of PJPMON is only valid for master slices. If PJPMON[12:0] is read for a slave slice, the master path's value will be returned.

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Indirect Register 01H: TSVCA Negative Justifications Performance Monitor

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12	R	NJPMON[12]	0
Bit 11	R	NJPMON[11]	0
Bit 10	R	NJPMON[10]	0
Bit 9	R	NJPMON[9]	0
Bit 8	R	NJPMON[8]	0
Bit 7	R	NJPMON[7]	0
Bit 6	R	NJPMON[6]	0
Bit 5	R	NJPMON[5]	0
Bit 4	R	NJPMON[4]	0
Bit 3	R	NJPMON[3]	0
Bit 2	R	NJPMON[2]	0
Bit 1	R	NJPMON[1]	0
Bit 0	R	NJPMON[0]	0

The outgoing Negative justifications performance monitor is provided at SVCA indirect Read/Write Address 01H.

NJPMON[12:0]

This register reports the number of negative pointer justification events that occurred on the outgoing side in the previous accumulation interval. The content of this register becomes valid a maximum of 155ns (12 clock cycles) after a transfer is triggered by writing the SVCA performance monitor trigger direct register or a write to the SPECTRA-9953 master configuration register . The value of NJPMON is only valid for master slices. If NJPMON[12:0] is read for a slave slice, the master path's value will be returned.

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Indirect Register 02H: TSVCA Diagnostic/Configuration

Bit	Type	Function	Default
Bit 15	R/W	PTRRST	0
Bit 14	R/W	PTRSS[1]	0
Bit 13	R/W	PTRSS[0]	0
Bit 12	R/W	JUS3DIS	0
Bit 11	R/W	PTRDD[1]	0
Bit 10	R/W	PTRDD[0]	0
Bit 9	R/W	Unused	0
Bit 8	R/W	Unused	0
Bit 7	R/W	unused	0
Bit 6	R/W	Diag_TOH_PAIS	0
Bit 5	R/W	Diag_NDFREQ	0
Bit 4	R/W	Diag_FifoAISDis	0
Bit 3	R/W	Diag_PAIS	0
Bit 2	R/W	Diag_LOP	0
Bit 1	R/W	Diag_NegJust	0
Bit 0	R/W	Diag_PosJust	0

The SVCA Diagnostic Register is provided at SVCA Read/Write Address 02H. These bits should be set to their default values during normal operation of the SVCA. The Diagnostic/Config register is only valid for master paths. Slave path Diagnostic/Config registers are overwritten with the master path's Diagnostic/Config register value.

Diag_PosJust

The Diag_PosJust bit forces the SVCA to generate outgoing positive justification events on the selected path(s). When set to 1, the SVCA generates positive justification events at the rate of one every four frames regardless of the current level of the internal FIFO. Prolonged application may cause the FIFO to overflow. However, the fifo monitor block has priority over the diagnostic justifications, so if the fifo level gets too high, then negative justifications will be performed, even if the Diag_PosJust bit is written high. As such, it is difficult to make the fifo overflow.

Diag_NegJust

When set high, The Diag_NegJust bit forces the SVCA to generate outgoing negative justification events on the selected path(s). When set to 1, the SVCA generates negative justification events at the rate of one every four frames regardless of the current level of the internal FIFO. Prolonged application may cause the FIFO to underflow. However, the fifo monitor block has priority over the diagnostic justifications, so if the fifo level gets too low, then positive justifications will be performed, even if the Diag_NegJust bit is written high. As such, it is difficult to make the fifo underflow.

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Note : Diag_PosJust and Diag_NegJust must not be set to one at the same time. If that occurs, their operation is disabled.

Diag_LOP

When set high, the Diag_LOP bit forces the SVCA to invert the outgoing NDF field of the payload (selected path(s)) pointer causing downstream pointer processing elements to enter a loss of pointer (LOP) state.

Diag_PAIS

When set high, the Diag_PAIS bit forces the SVCA to insert path AIS in the selected outgoing stream for at least three consecutive frames. AIS is inserted by writing an all ones pattern in the transport overhead bytes H1, H2, and H3, as well as in the entire STS synchronous payload envelope. The first frame after PAIS negates will contain a new data flag in the transport overhead H1 byte.

Diag_FifoAISDis

When set high, Diag_FifoAISDis bit forces the SVCA not to insert path AIS upon FIFO overflow/underflow detection. When set low (normal operation), detection of FIFO overflow/underflow causes path AIS to be inserted in the outgoing stream for at least three consecutive frames. Also, both overflow and underflow interrupts are triggered. (FOVR and FUDR)

Diag_NDFREQ

When set high, Diag_NDFREQ bit forces the SVCA to insert a NEW DATA FLAG indication in the frame regardless of the state of the pointer generation state machine. This register bit is not slef clearing.

Diag_TOH_PAIS

When set high, the Diag_TOH_PAIS bit allows path AIS to be inserted even during the section/line overhead. When Diag_TOH_PAIS is zero, path AIS output can only be inserted during the payload or during the H1, H2, and H3 bytes.

PTRDD[1:0]

The PTRDD[1:0] defines the STS-N/AU-N concatenation pointer bits DD. ITU requires that DD be set to 10 when processing AU-4, AU-3 or TU-3. On the other side, TELCORDIA does not specify these two bits.

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JUST3DIS

When set high, JUST3DIS allows the SVCA to perform 1 justification per frame when necessary. When set to zero, pointer justifications are allowed only every 4 frames.

PTRSS[1:0]

The PTRSS[1:0] defines the STS-N/AU-N pointer bits SS. ITU requires that SS be set to 10 when processing AU-4, AU-3 or TU-3. On the other side, TELCORDIA does not specify these two bits. The ss bits are set to 00 when processing a slave STS-1.

PTR_RST

When set high, Incoming and outgoing pointers are reset to their default values. This bit is level sensitive

15.18 R8TD Normal Registers

There are 16 R8TD (#1 - #16) blocks in 16 STM-4 processing slices with independent register sets

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Register 20D0H: R8TD Control and Status

Bit	Type	Function	Default
Bit 15	R/W	RESERVED	0
Bit 14	R/W	RESERVED	0
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9	R/W	PININV	0
Bit 8	R/W	OFAAIS	0
Bit 7	R/W	FUOE	0
Bit 6	R/W	LCVE	0
Bit 5	R/W	OFAE	0
Bit 4	R/W	OCAE	0
Bit 3	R	OFAV	X
Bit 2	R	OCAV	X
Bit 1	R/W	FOFA	0
Bit 0	R/W	FOCA	0

FOCA

The force out-of-character-alignment bit (FOCA) controls the operation of the character alignment circuit on a serial link. A transition from logic zero to logic one in this bit forces the receiver to the out-of-character-alignment state where it will search for the transport frame alignment character (K28.5). This bit must be manually set to logic zero before it can be used again.

FOFA

The force out-of-frame-alignment bit (FOFA) controls the operation of the frame alignment circuit. A transition from logic zero to logic one in this bit forces the receiver to the out-of-frame-alignment state where it will search for the transport frame alignment character (K28.5). This bit must be manually set to logic zero before it can be used again.

OCAV

The out-of-character-alignment status bit (OCAV) reports the state of the character alignment circuit. OCAV is set high when the receiver is in the out-of-character-alignment state. OCAV is set low when the receiver is in the in-character-alignment state.

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OFAV

The out-of-frame-alignment status bit (OFAV) reports the state of the frame alignment circuit. OFAV is set high when the receiver is in the out-of-frame-alignment state. OFAV is set low when the receiver is in the in-frame-alignment state.

OCAE

The out-of-character-alignment interrupt enable bit (OCAE) controls the change of character alignment state interrupts. Interrupts may be generated when the character alignment circuit changes state to the out-of-character-alignment state or to the in-character-alignment state. When OCAE is set high, an interrupt is generated when a change of state occurs. Interrupts due to changes of character alignment state are masked when OCAE is set low.

OFAE

The out-of-frame-alignment interrupt enable bit (OFAE) controls the change of frame alignment state interrupts. Interrupts may be generated when the frame alignment block changes state to the out-of-frame-alignment state or to the in-frame-alignment state. When OFAE is set high, an interrupt is generated when a change of state occurs. Interrupts due to changes of frame alignment state are masked when OFAE is set low.

LCVE

The line code violation interrupt enable bit (LCVE) controls the line code violation event interrupts. Interrupts may be generated when a line code violation is detected. When LCVE is set high, an interrupt is generated when an LCV is detected. Interrupts due to LCVs are masked when LCVE is set low.

FUOE

The FIFO underrun/overrun status interrupt enable (FUOE) controls the underrun/overrun event interrupts. Interrupts may be generated when the underrun/overrun event is detected. When FUOE is set high, an interrupt is generated when a FIFO underrun or overrun condition is detected. Interrupts due to FIFO underrun of overrun conditions are masked when FUEO is set low.

OFAAIS

The out of frame alignment alarm indication signal (OFAAIS) is set high to force high-order AIS signals in the R8TD egress data stream if the R8TD is in the out-of-frame-alignment state. The R8TD egress data stream is left unaffected in the out-of-frame alignment state when the OFFAIS is set low.

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PININV

The parallel incoming data invert bit (PININV) controls the active polarity of the incoming data stream. When PININV is set high, the incoming data stream is complemented before further processing by the R8TD. When PININV is set low, the incoming data stream is not complemented.

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Register 20D1H: R8TD Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R	FUOI	X
Bit 6	R	LCVI	X
Bit 5	R	OFAI	X
Bit 4	R	OCAI	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

If the WCIMODE bit in the SPECTRA-9953 Master Reset and Configuration Register (Register 0000H) is set high, these interrupt status bits are cleared on write. Otherwise, these interrupt status bits are cleared on read.

OCAI

The out-of-character-alignment interrupt status bit (OCAI) reports and acknowledges change of character alignment state interrupts. Interrupts are generated when the character alignment block changes state to the out-of-character-alignment state or to the in-character-alignment state. OCAI is set high when change of state occurs. When the interrupt is masked by the OCAE bit the OCAI remains valid and may be polled to detect change of frame alignment events.

OFAI

The out-of-frame-alignment interrupt status bit (OFAI) reports and acknowledges change of frame alignment state interrupts. Interrupts are generated when the frame alignment block changes state to the out-of-frame-alignment state or to the in-frame-alignment state. OFAI is set high when change of state occurs. When the interrupt is masked by the OFAE bit the OFAI remains valid and may be polled to detect change of frame alignment events.

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LCVI

The line code violation event interrupt status bit (LCVI) reports and acknowledges line code violation interrupts. Interrupts are generated when the character alignment block detects a line code violation in the incoming data stream. LCVI is set high when a line code violation event is detected. After being cleared, the LCVI bit will not return to 1 unless the R8TD leaves and re-enters the LCV state (i.e. when constant LCV are detected, the bit will not be re-written). When the interrupt is masked by the LCVE bit the LCVI remains valid and may be polled to detect change of frame alignment events.

FUOI

The FIFO underrun/overrun event interrupt status bit (FUOI) reports and acknowledges the FIFO underrun/overrun interrupts. Interrupts are generated when the character alignment block detects a that the read and write pointers are within one of each other. FUOI is set high when this event is detected. When the interrupt is masked by the FUOE bit the FUOI remains valid and may be polled to detect underrun/overrun events.

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Register 20D2H: R8TD Line Code Violation Count

Bit	Type	Function	Default
Bit 15	R	LCV[15]	X
Bit 14	R	LCV[14]	X
Bit 13	R	LCV[13]	X
Bit 12	R	LCV[12]	X
Bit 11	R	LCV[11]	X
Bit 10	R	LCV[10]	X
Bit 9	R	LCV[9]	X
Bit 8	R	LCV[8]	X
Bit 7	R	LCV[7]	X
Bit 6	R	LCV[6]	X
Bit 5	R	LCV[5]	X
Bit 4	R	LCV[4]	X
Bit 3	R	LCV[3]	X
Bit 2	R	LCV[2]	X
Bit 1	R	LCV[1]	X
Bit 0	R	LCV[0]	X

LCV[15:0]

The LCV[15:0] bits report the number of line code violations that have been detected since the last time the LCV registers were polled. The LCV registers are polled by writing to this register or to register 0000H, the SPECTRA-9953 Identity and Global Performance Monitor Update. This action transfers the internally accumulated error count to the LCV registers within 6 TCLK cycles and simultaneously resets the internal counter to begin a new cycle of error accumulation.

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Register 20D3H: R8TD Analog Control 1

Bit	Type	Function	Default
Bit 15	R/W	Reserved	1
Bit 14	R/W	Reserved	1
Bit 13	R/W	DRU_ENB	0
Bit 12	R/W	RX_ENB	0
Bit 11	R/W	Reserved	0
Bit 10	R/W	A_RSTB	1
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	DRU_CTRL[3]	0
Bit 4	R/W	DRU_CTRL[2]	0
Bit 3	R/W	DRU_CTRL[1]	0
Bit 2	R/W	DRU_CTRL[0]	0
Bit 1	R/W	DRU_IDDQ	0
Bit 0		Unused	X

This register controls internal analog functions.

DRU_IDDQ

The DRU_IDDQ controls the DRU_1250 operation. DRU_IDDQ is set high to force all DRU_1250 outputs and digital circuitry to be held static to enable the core digital circuitry IDDQ test.

DRU_CTRL[3:0]

The DRU_CTRL[3:0] bits control the DRU CTRL[3:0] inputs. DRU_CTRL[3:0] should be driven to 1101 For normal operation. This value differs from the default value of the bits (0000).

A_RSTB

The A_RSTB bit is a soft-reset for the Data Recovery Unit Analog block. Setting A_RSTB to logic 0 will reset the block.

RX_ENB

The RXLV enable bit (RX_ENB) bit controls the operation of RXLV block #X. Setting RX_ENB to logic 0 enables the block. Setting RX_ENB to logic 1 disables the block.

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DRU_ENB

The TXLV enable bit (DRU_ENB) bit controls the operation of Data Recovery Unit Analog block #X. Setting DRU_ENB to logic 0 enables the block. Setting DRU_ENB to logic 1 disables the block.

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Register 20D4H: R8TD Analog Control 2

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9	R	Reserved	X
Bit 8	R	Reserved	X
Bit 7	R	Reserved	X
Bit 6	R	Reserved	X
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

This register controls internal analog functions. This register should not be used.

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Register 20D5H: R8TD Analog Control 3

Bit	Type	Function	Default
Bit 15	R/W	Reserved	X
Bit 14	R/W	Reserved	X
Bit 13	R/W	Reserved	X
Bit 12	R/W	Reserved	X
Bit 11	R/W	Reserved	0
Bit 10	R/W	Reserved	0
Bit 9	R/W	Reserved	0
Bit 8	R/W	Reserved	0
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

15.19 THPP Normal Registers

There are 16 THPP (#1 - #16) blocks in 16 STM-4 processing slices with independent register sets. The master/slave configuration for the THPPs depends on the payload mapping and is thus defined using top-level registers 0005H and 0006H as well as each THPP Payload Config register (20E2H).

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Register 20E0H: THPP_R Indirect Addressing

Bit	Type	Function	Default
Bit 15	R	BUSY	X
Bit 14	R/W	RWB	0
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9	R/W	PAGE[3]	0
Bit 8	R/W	PAGE[2]	0
Bit 7	R/W	PAGE[1]	0
Bit 6	R/W	PAGE[0]	0
Bit 5		Unused	
Bit 4		Unused	
Bit 3	R/W	PATH[3]	0
Bit 2	R/W	PATH[2]	0
Bit 1	R/W	PATH[1]	0
Bit 0	R/W	PATH[0]	0

The Indirect Addressing Register is provided at THPP_R Read/Write Address 00H.

PATH[3:0]

The STS-1/STM-0 path (PATH[3:0]) bits select which STS-1/STM-0 path is accessed by the current indirect transfer.

PATH[3:0]	STS-1/STM-0 path #
0000	Invalid path
0001-1100	Path #1 to Path #12
1101-1111	Invalid path

PAGE[3:0]

The page (PAGE[3:0]) bits select which address location is accessed by the current indirect transfer.

PAGE[3:0]	Indirect Register
0000	THPP_R Control Register
0001	THPP_R Source & Pointer Control
0010	Unused
0011	Unused
0100	THPP_R Fixed stuff byte and B3MASK
0101	THPP_R J1 and C2 POH

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PAGE[3:0]	Indirect Register
0110	THPP_R G1 POH and H4MASK
0111	THPP_R F2 and Z3 POH
1000	THPP_R Z4 and Z5 POH
1001 to 1111	Unused

RWB

The active high read and active low write (RWB) bit selects if the current access to the internal RAM is an indirect read or an indirect write. Writing to the Indirect Address Register initiates an access to the internal RAM. When RWB is set to logic 1, an indirect read access to the RAM is initiated. The data from the addressed location in the internal RAM will be transferred to the Indirect Data Register. When RWB is set to logic 0, an indirect write access to the RAM is initiated. The data from the Indirect Data Register will be transferred to the addressed location in the internal RAM.

BUSY

The BUSY (BUSY) bit reports the status of an indirect read/write access to the time sliced ram. BUSY is set to logic 1 upon writing to the Indirect Addressing Register. BUSY is set to logic 0, upon completion of the RAM transfer. This register should be polled to determine when new data is available in the Indirect Data Register.

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Register 20E1H: THPP_R Indirect Data Register

Bit	Type	Function	Default
Bit 15	R/W	DATA[15]	0
Bit 14	R/W	DATA[14]	0
Bit 13	R/W	DATA[13]	0
Bit 12	R/W	DATA[12]	0
Bit 11	R/W	DATA[11]	0
Bit 10	R/W	DATA[10]	0
Bit 9	R/W	DATA[9]	0
Bit 8	R/W	DATA[8]	0
Bit 7	R/W	DATA[7]	0
Bit 6	R/W	DATA[6]	0
Bit 5	R/W	DATA[5]	0
Bit 4	R/W	DATA[4]	0
Bit 3	R/W	DATA[3]	0
Bit 2	R/W	DATA[2]	0
Bit 1	R/W	DATA[1]	0
Bit 0	R/W	DATA[0]	0

The Indirect Data Register is provided at THPP_R Read/Write Address 01H.

DATA[15:0]

The indirect access data (DATA[15:0]) bits hold the data transfer to or from the internal RAM during indirect access. When RWB is set to logic 1 (indirect read), the data from the addressed location in the internal RAM will be transferred to DATA[15:0]. BUSY should be polled to determine when the new data is available in DATA[15:0]. When RWB is set to logic 0 (indirect write), the data from DATA[15:0] will be transferred to the addressed location in the internal RAM. The indirect Data register must contain valid data before the indirect write is initiated by writing to the Indirect Address Register.

DATA[15:0] has a different meaning depending on which address of the internal RAM is being accessed.

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Register 20E2H: THPP_R Payload Configuration (TPC)

Bit	Type	Function	Default
Bit 15	R/W	STS12CSL	0
Bit 14	R/W	STS12C	0
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7	R/W	Unused	0
Bit 6	R/W	Unused	0
Bit 5	R/W	Unused	0
Bit 4	R/W	Unused	0
Bit 3	R/W	STS3C[4]	0
Bit 2	R/W	STS3C[3]	0
Bit 1	R/W	STS3C[2]	0
Bit 0	R/W	STS3C[1]	0

The Payload Configuration Register is provided at THPP_R Read/Write Address 02H.

STS3C[1]

The STS-3c (VC-4) payload configuration (STS3C[1]) bit selects the payload configuration. When STS3C[1] is set to logic 1, the STS-1/STM-0 paths #1, #5 and #9 are part of a STS-3c (VC-4) payload. When STS3C[1] is set to logic 0, the paths are STS-1 (VC-3) payloads. The STS12C register bit has precedence over the STS3C[1] register bit.

STS3C[2]

The STS-3c (VC-4) payload configuration (STS3C[2]) bit selects the payload configuration. When STS3C[2] is set to logic 1, the STS-1/STM-0 paths #2, #6 and #10 are part of a STS-3c (VC-4) payload. When STS3C[2] is set to logic 0, the paths are STS-1 (VC-3) payloads. The STS12C register bit has precedence over the STS3C[2] register bit.

STS3C[3]

The STS-3c (VC-4) payload configuration (STS3C[3]) bit selects the payload configuration. When STS3C[3] is set to logic 1, the STS-1/STM-0 paths #3, #7 and #11 are part of a STS-3c (VC-4) payload. When STS3C[3] is set to logic 0, the paths are STS-1 (VC-3) payloads. The STS12C register bit has precedence over the STS3C[3] register bit.

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STS3C[4]

The STS-3c (VC-4) payload configuration (STS3C[4]) bit selects the payload configuration. When STS3C[4] is set to logic 1, the STS-1/STM-0 paths #4, #8 and #12 are part of a STS-3c (VC-4) payload. When STS3C[4] is set to logic 0, the paths are STS-1 (VC-3) payloads. The STS12C register bit has precedence over the STS3C[4] register bit.

STS12C

The STS-12c (VC-4-4c) payload configuration (STS12C) bit selects the payload configuration. When STS12C is set to logic 1, the STS-1/STM-0 paths #1 to #12 are part of a STS-12c (VC-4-4c) payload. When STS12C is set to logic 0, the STS-1/STM-0 paths are defined with the STS3C[1:4] register bit. The STS12C register bit is OR'ed with the STS-12C SPECTRA-9953 transmit configuration register 2 corresponding bit . The STS12C register bit has precedence over the STS3C[1:4] register bit.

STS12CSL

The slave STS-12c (VC-4-4c) payload configuration (STS12CSL) bit selects the slave payload configuration. When STS12CSL is set to logic 1, the STS-1/STM-0 paths #1 to #12 are part of a STS-12c (VC-4-4c) slave payload. When STS12CSL is set to logic 0, the STS-1/STM-0 paths #1 to # 12 are part of a STS-12c (VC-4-4c) master payload. The STS12CSL register bit is OR'ed with the STS-12CSL SPECTRA-9953 transmit configuration register 3 corresponding bit. When STS12C is set to logic 0, the STS12CSL register bit has no effect.

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Indirect Register 00H: THPP_R Control Register (TCR)

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	TDIS	0
Bit 4		Unused	
Bit 3	R/W	FSBEN	0
Bit 2	R/W	PREIEBLK	0
Bit 1	R/W	EXCFS	0
Bit 0		Unused	

The THPP_R Control Indirect Register is provided at THPP_R r/w indirect address 00H.

EXCFS

When EXCFS is set to logic 1, the fixed stuff columns in the STS-1 SPE/VC-3 format are excluded from BIP calculations. When EXCFS is set to logic 0, the fixed stuff columns in the STS-1 SPE/VC-3 format are included in the BIP calculations.

PREIEBLK

When PREIEBLK is set to logic 1, the path REI value extracted on the PREI[3:0] input bus represents BIP-8 block errors, i.e. the REI-P value allowed in G1 is either 0 or 1. When PREIEBLK is set to logic 0, the path REI value extracted on the PREI[3:0] input bus represents BIP-8 errors, i.e.the REI-P value allowed in G1 is from 0 to 8.

FSBEN

When FSBEN is set logic one, THPP_R overwrites the fixed stuff byte on PIN[7:0] with the value found in TFSB. When FSBEN is set to logic zero, the fixed stuff byte value on PIN[7:0] is transparently passed through.

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TDIS

When TDIS is set to logic one, the path overhead byte value is passed through transparently without being overwritten by the THPP_R. When TDIS is set to logic zero, the THPP_R inserts a valid path overhead byte value .

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Indirect Register 01H: THPP_R Source & Pointer Control Register (TSPCR)

Bit	Type	Function	Default
Bit 15	R/W	UNEQV	0
Bit 14	R/W	UNEQ	0
Bit 13	R/W	Unused	0
Bit 12	R/W	Unused	0
Bit 11	R/W	ENG1REC	1
Bit 10	R/W	ENH4MASK	0
Bit 9	R/W	PTBJ1	0
Bit 8	R/W	SRCZ5	0
Bit 7	R/W	SRCZ4	0
Bit 6	R/W	SRCZ3	0
Bit 5	R/W	SRCF2	0
Bit 4	R/W	SRCG1	0
Bit 3	R/W	SRCH4	0
Bit 2	R/W	SRCC2	0
Bit 1	R/W	SRCJ1	0
Bit 0	R/W	IBER	0

The THPP_R Control Indirect Register is provided at THPP_R r/w indirect address 01H.

IBER

When the IBER register bit is set to logic one, the G1 byte received on the Add bus pass-through the THPP_R. When IBER is set to logic zero, the G1 byte is not pass-through and can be modified by one of the THPP_R POH sources.

SRCJ1, SRCC2, SRCH4, SRCG1, SRCF2, SRCZ3, SRCZ4, SRCZ5

The SRCxx bits are used to determine the source of the path overhead bytes inserted by the THPP_R For example, when a logic 1 is written to SRCJ1, the J1 byte inserted can be found in the internal register TPTSLO.

PTBJ1

The PTBJ1 register bit is used to determine the origin of the path trace byte to be inserted in by the THPP_R. When PTBJ1 is set high, the J1 byte source is the external path trace buffer. When PTBJ1 is set to logic low, The J1 byte source is other than the path trace buffer.

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ENH4MASK

When ENH4MASK is set to logic 1, the H4 value (H4V[7:0]) in the THPP Transmit Z3 and H4 Register is used as an error mask on the H4 byte passing through THPP. When ENH4MASK is set to logic 0, the H4 (H4V[7:0]) value from the THPP Transmit Z3 and H4 Register is inserted into the transmit stream.

ENG1REC

The valid high ENG1REC register bit enables the insertion of the RDI-P and REI-P extracted from a mate RHPP into the transmit stream. When ENG1REC is set to logic low, the G1 byte source is other than from the mate RHPP.

UNEQ

The unequiped bit (UNEQ) controls the insertion of an all one or an all zero pattern in the path overhead and in the payload, the fixed stuff bytes are excluded from insertion. When UNEQ is set to logic one, an all one or an all zero pattern is inserted in the path overhead and in the payload. When UNEQ is set logic 0, no pattern is inserted.

UNEQV

The unequiped value (UNEQV) bit controls the value inserted in the path overhead and in the payload. When UNEQV is set to logic 1, an all one pattern is inserted in the path overhead and in the payload if enable via the UNEQ register bit. When UNEQV is set to logic 0, an all zero pattern is inserted in the path overhead and in the payload if enable via the UNEQ register bit.

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Indirect Register 04H: THPP_R Fixed Stuff Byte and B3 Mask (TFSB)

Bit	Type	Function	Default
Bit 15	R/W	B3MASK[7]	0
Bit 14	R/W	B3MASK[6]	0
Bit 13	R/W	B3MASK[5]	0
Bit 12	R/W	B3MASK[4]	0
Bit 11	R/W	B3MASK[3]	0
Bit 10	R/W	B3MASK[2]	0
Bit 9	R/W	B3MASK[1]	0
Bit 8	R/W	B3MASK[0]	0
Bit 7	R/W	FSB[7]	0
Bit 6	R/W	FSB[6]	0
Bit 5	R/W	FSB[5]	0
Bit 4	R/W	FSB[4]	0
Bit 3	R/W	FSB[3]	0
Bit 2	R/W	FSB[2]	0
Bit 1	R/W	FSB[1]	0
Bit 0	R/W	FSB[0]	0

FSB[7:0]

When FSBEN is logic one, the THPP_R replaces the fixed stuff bytes with the byte from this register.

B3MASK[7:0]

The B3 parity byte to be inserted on the outgoing stream is XORed with this register byte to allow the user to insert errors in B3.

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Indirect Register 05H: THPP_R J1 and C2 (TJ1C2POH)

Bit	Type	Function	Default
Bit 15	R/W	C2[7]	0
Bit 14	R/W	C2[6]	0
Bit 13	R/W	C2[5]	0
Bit 12	R/W	C2[4]	0
Bit 11	R/W	C2[3]	0
Bit 10	R/W	C2[2]	0
Bit 9	R/W	C2[1]	0
Bit 8	R/W	C2[0]	0
Bit 7	R/W	J1[7]	0
Bit 6	R/W	J1[6]	0
Bit 5	R/W	J1[5]	0
Bit 4	R/W	J1[4]	0
Bit 3	R/W	J1[3]	0
Bit 2	R/W	J1[2]	0
Bit 1	R/W	J1[1]	0
Bit 0	R/W	J1[0]	0

J1[7:0]

When SRCJ1 is logic high, this byte is inserted in the J1 path overhead byte position

C2[7:0]

When SRCC2 is logic high, this byte is inserted in the C2 path overhead byte position .

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Indirect Register 06H: THPP_R G1 POH and H4 mask (TG1H4POH)

Bit	Type	Function	Default
Bit 15	R/W	H4[7]	0
Bit 14	R/W	H4[6]	0
Bit 13	R/W	H4[5]	0
Bit 12	R/W	H4[4]	0
Bit 11	R/W	H4[3]	0
Bit 10	R/W	H4[2]	0
Bit 9	R/W	H4[1]	0
Bit 8	R/W	H4[0]	0
Bit 7	R/W	G1[7]	0
Bit 6	R/W	G1[6]	0
Bit 5	R/W	G1[5]	0
Bit 4	R/W	G1[4]	0
Bit 3	R/W	G1[3]	0
Bit 2	R/W	G1[2]	0
Bit 1	R/W	G1[1]	0
Bit 0	R/W	G1[0]	0

G1[7:0]

When SRCG1 is logic high, this byte is inserted in the G1 path overhead byte position .

H4[7:0]

The logical value of the ENH4MASK register bit determines if this byte is to be inserted in transmit stream as the H4 path overhead byte value or is to be used as an error msak on the received H4 byte .

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Indirect Register 07H: THPP_R F2 and Z3 POH (TF2Z3POH)

Bit	Type	Function	Default
Bit 15	R/W	F2[7]	0
Bit 14	R/W	F2[6]	0
Bit 13	R/W	F2[5]	0
Bit 12	R/W	F2[4]	0
Bit 11	R/W	F2[3]	0
Bit 10	R/W	F2[2]	0
Bit 9	R/W	F2[1]	0
Bit 8	R/W	F2[0]	0
Bit 7	R/W	Z3[7]	0
Bit 6	R/W	Z3[6]	0
Bit 5	R/W	Z3[5]	0
Bit 4	R/W	Z3[4]	0
Bit 3	R/W	Z3[3]	0
Bit 2	R/W	Z3[2]	0
Bit 1	R/W	Z3[1]	0
Bit 0	R/W	Z3[0]	0

F2[7:0]

When SRCF2 is logic high, this byte is inserted in the F2 path overhead byte position .

Z3[7:0]

When SRCZ3 is logic high, this byte is inserted in the Z3 path overhead byte position .

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Indirect Register 08H: THPP_R Z4 & Z5 Ovhd. (TZ4Z5POH)

Bit	Type	Function	Default
Bit 15	R/W	Z4[7]	0
Bit 14	R/W	Z4[6]	0
Bit 13	R/W	Z4[5]	0
Bit 12	R/W	Z4[4]	0
Bit 11	R/W	Z4[3]	0
Bit 10	R/W	Z4[2]	0
Bit 9	R/W	Z4[1]	0
Bit 8	R/W	Z4[0]	0
Bit 7	R/W	Z5[7]	0
Bit 6	R/W	Z5[6]	0
Bit 5	R/W	Z5[5]	0
Bit 4	R/W	Z5[4]	0
Bit 3	R/W	Z5[3]	0
Bit 2	R/W	Z5[2]	0
Bit 1	R/W	Z5[1]	0
Bit 0	R/W	Z5[0]	0

Z4[7:0]

When SRCZ4 is logic high, this byte is inserted in the Z4 path overhead byte position .

Z5[7:0]

When SRCZ5 is logic high, this byte is inserted in the Z5 path overhead byte position .

15.20 SHPI Normal Registers

There are 16 SHPI (#1 - #16) blocks in 16 STM-4 processing slices with independent register sets. The master/slave configuration for the SHPIs depends on the payload mapping and is thus defined using top-level registers 0005H and 0006H as well as each SHPI Payload Config register (2102H).

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Register 2100H: SHPI Indirect Address

Bit	Type	Function	Default
Bit 15	R	BUSY	X
Bit 14	R/W	RWB	0
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9	R/W	ADDR[3]	0
Bit 8	R/W	ADDR[2]	0
Bit 7	R/W	ADDR[1]	0
Bit 6	R/W	ADDR[0]	0
Bit 5		Unused	
Bit 4		Unused	
Bit 3	R/W	PATH[3]	0
Bit 2	R/W	PATH[2]	0
Bit 1	R/W	PATH[1]	0
Bit 0	R/W	PATH[0]	0

The Indirect Address Register is provided at SHPI Read/Write Address 00H.

PATH[3:0]

The STS-1/STM-0 path (PATH[3:0]) bits select which STS-1/STM-0 path is accessed by the current indirect transfer.

PATH[3:0]	STS-1/STM-0 path #
0000	Invalid path
0001-1100	Path #1 to Path #12
1101-1111	Invalid path

ADDR[3:0]

The address location (ADDR[3:0]) bits select which address location is accessed by the current indirect transfer.

Indirect Address ADDR[3:0]	Indirect Data
0000	Pointer Interpreter Configuration
0001	Error Monitor Configuration
0010	Pointer Value
0011	Unused

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Indirect Address ADDR[3:0]	Indirect Data
0100	Unused
0101	Pointer Interpreter Status
0110	Unused
0111	Unused
1000	Path Negative Justification Event Counter
1001	Path Positive Justification Event Counter
1010to 1111	Unused

RWB

The active high read and active low write (RWB) bit selects if the current access to the internal RAM is an indirect read or an indirect write. Writing to the Indirect Address Register initiates an access to the internal RAM. When RWB is set to logic 1, an indirect read access to the RAM is initiated. The data from the addressed location in the internal RAM will be transferred to the Indirect Data Register. When RWB is set to logic 0, an indirect write access to the RAM is initiated. The data from the Indirect Data Register will be transferred to the addressed location in the internal RAM.

BUSY

The active high RAM busy (BUSY) bit reports if a previously initiated indirect access to the internal RAM has been completed. BUSY is set to logic 1 upon writing to the Indirect Address Register. BUSY is set to logic 0, upon completion of the RAM access. This register should be polled to determine when new data is available in the Indirect Data Register.

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Register 2101H: SHPI Indirect Data

Bit	Type	Function	Default
Bit 15	R/W	DATA[15]	0
Bit 14	R/W	DATA[14]	0
Bit 13	R/W	DATA[13]	0
Bit 12	R/W	DATA[12]	0
Bit 11	R/W	DATA[11]	0
Bit 10	R/W	DATA[10]	0
Bit 9	R/W	DATA[9]	0
Bit 8	R/W	DATA[8]	0
Bit 7	R/W	DATA[7]	0
Bit 6	R/W	DATA[6]	0
Bit 5	R/W	DATA[5]	0
Bit 4	R/W	DATA[4]	0
Bit 3	R/W	DATA[3]	0
Bit 2	R/W	DATA[2]	0
Bit 1	R/W	DATA[1]	0
Bit 0	R/W	DATA[0]	0

The Indirect Data Register is provided at SHPI Read/Write Address 01H.

DATA[15:0]

The indirect access data (DATA[15:0]) bits hold the data transfer to or from the internal RAM during indirect access. When RWB is set to logic 1 (indirect read), the data from the addressed location in the internal RAM will be transferred to DATA[15:0]. BUSY should be polled to determine when the new data is available in DATA[15:0]. When RWB is set to logic 0 (indirect write), the data from DATA[15:0] will be transferred to the addressed location in the internal RAM. The indirect Data register must contain valid data before the indirect write is initiated by writing to the Indirect Address Register.

DATA[15:0] has a different meaning depending on which address of the internal RAM is being accessed.

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Indirect Register 00H: SHPI Pointer Interpreter Configuration

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7	R/W	Unused	0
Bit 6	R/W	Unused	0
Bit 5	R/W	NDFCNT	0
Bit 4	R/W	Reserved	0*
Bit 3	R/W	RELAYPAIS	0
Bit 2	R/W	JUST3DIS	0
Bit 1	R/W	SSEN	0
Bit 0		Unused	X

The Pointer Interpreter Configuration Indirect Register is provided at SHPI r/w indirect address 00H.

*Bit #4 defaults to 0 but should be written to 1 in order to ensure compliant device operation. This is explained further in Section 14.2.2.

SSEN

The SS bits enable (SSEN) bit selects whether or not the SS bits are taking into account in the pointer interpreter state machine. When SSEN is set to logic 1, the SS bits must be set to 10 for a valid NORM_POINT, NDF_ENABLE, INC_IND, DEC_IND or NEW_POINT indication. When SSEN is set to logic 0, the SS bits are ignored.

JUST3DIS

The “justification more than 3 frames ago disable” (JUST3DIS) bit selects whether or not the INC_IND or DEC_IND pointer justifications must be more than 3 frames apart to be considered valid. When JUST3DIS is set to logic 0, the previous NDF_ENABLE, INC_IND or DEC_IND indication must be more than 3 frames ago or the present INC_IND or DEC_IND indication is considered an INV_POINT indication. NDF_ENABLE indications can be every frame regardless of the JUST3DIS bit. When JUST3DIS is set to logic 1, INC_IND or DEC_IND indication can be every frame.

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RELAYPAIS

The relay path AIS (RELAYPAIS) bit selects the condition to enter the path AIS state in the pointer interpreter state machine. When RELAYPAIS is set to logic 1, the path AIS state is entered with 1 X AIS_ind indication. When RELAYPAIS is set to logic 0, the path AIS state is entered with 3 X AIS_ind indications. This configuration bit also affects the concatenation pointer interpreter state machine.

NDFCNT

The new data flag counter (NDFCNT) bit selects the behavior of the consecutive NDF_ENABLE event counter in the pointer interpreter state machine. When NDFCNT is set to logic 1, the NDF_ENABLE definition is enabled NDF + ss. When NDFCNT is set to logic 0, the NDF_ENABLE definition is enabled NDF + ss + offset value in the range 0 to 782. This configuration bit only changes the NDF_ENABLE definition for the consecutive NDF_ENABLE even counter to count towards LOP-P defect when the pointer is out of range. This configuration bit has no bearing on pointer justification indication. It should be noted that this bit has no bearing on the INV_POINT counter, so an out of range NDF_ENABLE indication will always increment the INV_POINT counter irrespective of the NDFCNT bit setting.

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Indirect Register 01H: SHPI Error Monitor Configuration

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	FSBIPDIS	0
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

The Error Monitor Configuration Indirect Register is provided at SHPI r/w indirect address 01H.

FSBIPDIS

The disable fixed stuff columns during BIP-8 calculation (FSBIPDIS) bit controls the path BIP-8 calculation for an STS-1 (VC-3) payload. When FSBIPDIS is set to logic 1, the fixed stuff columns are not part of the BIP-8 calculation when processing an STS-1 (VC-3) payload. When FSBIPDIS is set to logic 0, the fixed stuff columns are part of the BIP-8 calculation when processing an STS-1 (VC-3) payload.

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Indirect Register 02H: SHPI Pointer Value

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11	R	SSV[1]	X
Bit 10	R	SSV[0]	X
Bit 9	R	PTRV[9]	X
Bit 8	R	PTRV[8]	X
Bit 7	R	PTRV[7]	X
Bit 6	R	PTRV[6]	X
Bit 5	R	PTRV[5]	X
Bit 4	R	PTRV[4]	X
Bit 3	R	PTRV[3]	X
Bit 2	R	PTRV[2]	X
Bit 1	R	PTRV[1]	X
Bit 0	R	PTRV[0]	X

The Pointer Value Indirect Register is provided at SHPI Read/Write Address 01H.

PTRV[9:0]

The path pointer value (PTRV[9:0]) bits represent the current STS (AU) pointer being processed by the pointer interpreter state machine or by the concatenation pointer interpreter state machine.

SSV[1:0]

The SS value (SSV[1:0]) bits represent the current SS (DD) bits being processed by the pointer interpreter state machine or by the concatenation pointer interpreter state machine.

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Indirect Register 05H: SHPI Pointer Interpreter Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6	R	NDF	X
Bit 5	R	ILLPTR	X
Bit 4	R	INVNDF	X
Bit 3	R	DISCOPA	X
Bit 2	R	CONCAT	X
Bit 1	R	ILLJREQ	X
Bit 0		Unused	X

The Pointer Interpreter Status Indirect Register is provided at SHPI r/w indirect address 02H.

Note: The Pointer Interpreter Status bits are don't care for slave time slots, except for the CONCAT bit, which is defined for slave timeslots. The other bits may be set high for slave timeslots, and should be ignored.

ILLJREQ

The illegal pointer justification request (ILLJREQ) signal is set high when a positive and/or negative pointer adjustment is received within three frames of a pointer justification event (inc_ind, dec_ind) or an NDF triggered active offset adjustment (NDF_enable). ILLJREQ is only declared when JUST3DIS is logic low.

CONCAT

The CONCAT bit is set high if the H1 and H2 pointer bytes received match the concatenation indication (one of the five NDF_enable patterns in the NDF field, don't care in the size field, and all-ones in the pointer offset field).

DISCOPA

The discontinuous change of pointer alignment (DISCOPA) signal is set high when there is a pointer adjustment due to receiving a pointer repeated three times.

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INVNDF

The invalid new data flag (INVNDF) signal is set high when an invalid NDF code is received.

ILLPTR

The illegal pointer offset (ILLPTR) signal is set high when the pointer received is out of the range. Legal values are from 0 to 782. Pointer justification requests (inc_req, dec_req) are not considered illegal. The ILLPTR bit is set high for AIS indication.

NDF

The new data flag (NDF) signal is set high when an enabled New Data Flag is received indicating a pointer adjustment (NDF_enabled indication).

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Indirect Register 08H: SHPI Path Negative Justification Event Counter

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12	R	PNJE[12]	X
Bit 11	R	PNJE[11]	X
Bit 10	R	PNJE[10]	X
Bit 9	R	PNJE[9]	X
Bit 8	R	PNJE[8]	X
Bit 7	R	PNJE[7]	X
Bit 6	R	PNJE[6]	X
Bit 5	R	PNJE[5]	X
Bit 4	R	PNJE[4]	X
Bit 3	R	PNJE[3]	X
Bit 2	R	PNJE[2]	X
Bit 1	R	PNJE[1]	X
Bit 0	R	PNJE[0]	X

The SHPI Path Negative Justification Event Counter register is provided at SHPI r/w indirect address 03H.

PNJE[12:0]

The Path Negative Justification Event (PNJE[12:0]) bits represent the number of Path Negative Justification Events that have occured since the last accumulation interval. The event counters are transferred to the holding registers by a microprocessor write to the SHPI Counters Update register (address 03H) or or a write to the SPECTRA-9953 master configuration register . The TIP output indicates the transfer status.

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Indirect Register 09H: SHPI Path Positive Justification Event Counter

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12	R	PPJE[12]	X
Bit 11	R	PPJE[11]	X
Bit 10	R	PPJE[10]	X
Bit 9	R	PPJE[9]	X
Bit 8	R	PPJE[8]	X
Bit 7	R	PPJE[7]	X
Bit 6	R	PPJE[6]	X
Bit 5	R	PPJE[5]	X
Bit 4	R	PPJE[4]	X
Bit 3	R	PPJE[3]	X
Bit 2	R	PPJE[2]	X
Bit 1	R	PPJE[1]	X
Bit 0	R	PPJE[0]	X

The SHPI Path Positive Justification Event Counter register is provided at SHPI r/w indirect address 04H.

PPJE[120]

The Path Positive Justification Event (PPJE[12:0]) bits represent the number of Path Positive Justification Events that have occured since the last accumulation interval. The event counters are transferred to the holding registers by a microprocessor write to the SHPI Counters Update register (address 03H) or a write to the SPECTRA-9953 master configuration register . The TIP output indicates the transfer status.

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Register 2102H: SHPI Payload Configuration

Bit	Type	Function	Default
Bit 15	R/W	STS12CSL	0
Bit 14	R/W	STS12C	0
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8	R/W	Unused	0
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	STS3C[4]	0
Bit 2	R/W	STS3C[3]	0
Bit 1	R/W	STS3C[2]	0
Bit 0	R/W	STS3C[1]	0

The Payload Configuration Register is provided at SHPI Read/Write Address 02H.

STS3C[1]

The STS-3c (VC-4) payload configuration (STS3C[1]) bit selects the payload configuration. When STS3C[1] is set to logic 1, the STS-1/STM-0 paths #1, #5 and #9 are part of a STS-3c (VC-4) payload. When STS3C[1] is set to logic 0, the paths are STS-1 (VC-3) payloads. The STS12C register bit has precedence over the STS3C[1] register bit.

STS3C[2]

The STS-3c (VC-4) payload configuration (STS3C[2]) bit selects the payload configuration. When STS3C[2] is set to logic 1, the STS-1/STM-0 paths #2, #6 and #10 are part of a STS-3c (VC-4) payload. When STS3C[2] is set to logic 0, the paths are STS-1 (VC-3) payloads. The STS12C register bit has precedence over the STS3C[2] register bit.

STS3C[3]

The STS-3c (VC-4) payload configuration (STS3C[3]) bit selects the payload configuration. When STS3C[3] is set to logic 1, the STS-1/STM-0 paths #3, #7 and #11 are part of a STS-3c (VC-4) payload. When STS3C[3] is set to logic 0, the paths are STS-1 (VC-3) payloads. The STS12C register bit has precedence over the STS3C[3] register bit.

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STS3C[4]

The STS-3c (VC-4) payload configuration (STS3C[4]) bit selects the payload configuration. When STS3C[4] is set to logic 1, the STS-1/STM-0 paths #4, #8 and #12 are part of a STS-3c (VC-4) payload. When STS3C[4] is set to logic 0, the paths are STS-1 (VC-3) payloads. The STS12C register bit has precedence over the STS3C[4] register bit.

STS12C

The STS-12c (VC-4-4c) payload configuration (STS12C) bit selects the payload configuration. When STS12C is set to logic 1, the STS-1/STM-0 paths #1 to #12 are part of a STS-12c (VC-4-4c) payload. When STS12C is set to logic 0, the STS-1/STM-0 paths are defined with the STS3C[1:4] register bit. The STS12C register bit is OR'ed with the SPECTRA-9953 transmit configuration 2 STS12C register bit . The STS12C register bit has precedence over the STS3C[1:4] register bit.

STS12CSL

The slave STS-12c (VC-4-4c) payload configuration (STS12CSL) bit selects the slave payload configuration. When STS12CSL is set to logic 1, the STS-1/STM-0 paths #1 to #12 are part of a STS-12c (VC-4-4c) slave payload. When STS12CSL is set to logic 0, the STS-1/STM-0 paths #1 to # 12 are part of a STS-12c (VC-4-4c) master payload. The STS12CSL register bit is OR'ed with the SPECTRA-9953 transmit configuration 3 STS12CSL register bit . When STS12C is set to logic 0, the STS12CSL register bit has no effect.

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Register 2103H: SHPI Counters Update

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

Any write to the SHPI Counters Update Register (address 03H) or a write to the SPECTRA-9953 master configuration register will trigger the transfer of all counter values to their holding registers. . The TIP output indicates the transfer status.

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Register 2104H: SHPI Path Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11	R	P_INT[12]	X
Bit 10	R	P_INT[11]	X
Bit 9	R	P_INT[10]	X
Bit 8	R	P_INT[9]	X
Bit 7	R	P_INT[8]	X
Bit 6	R	P_INT[7]	X
Bit 5	R	P_INT[6]	X
Bit 4	R	P_INT[5]	X
Bit 3	R	P_INT[4]	X
Bit 2	R	P_INT[3]	X
Bit 1	R	P_INT[2]	X
Bit 0	R	P_INT[1]	X

The SHPI Path Interrupt Status Register is provided at SHPI read address 04H.

P_INT[1:12]

The Path Interrupt Status bit (P_INT[1:12]) tells which path(s) have interrupts that are still active. Reading from this register will not clear any of the interrupts, it is simply added to reduce the average number of accesses required to service interrupts.

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Register 2105H: SHPI Pointer Concatenation Processing Disable

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11	R/W	PTRCDIS[12]	0
Bit 10	R/W	PTRCDIS[11]	0
Bit 9	R/W	PTRCDIS[10]	0
Bit 8	R/W	PTRCDIS[9]	0
Bit 7	R/W	PTRCDIS[8]	0
Bit 6	R/W	PTRCDIS[7]	0
Bit 5	R/W	PTRCDIS[6]	0
Bit 4	R/W	PTRCDIS[5]	0
Bit 3	R/W	PTRCDIS[4]	0
Bit 2	R/W	PTRCDIS[3]	0
Bit 1	R/W	PTRCDIS[2]	0
Bit 0	R/W	PTRCDIS[1]	0

The Pointer Concatenation processing Disable Register is provided at SHPI Read/Write Address 05H.

PTRCDIS[1:12]

The concatenation pointer processing disable (PTRCDIS[1:12]) bits disable the relaying of LOPC-P, AISC-P and ALLAISC-P to the SARC. When PTRCDIS[n] is set to logic 1, the path concatenation pointer interpreter state-machine (for the path n) is enabled and the Pointer interpreter Status can be read at their register locations, but the information is not relayed to the Alarm Controller (SARC). When PTRCDIS is set to logic 0, the above defects are relayed to the SARC.

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Register 2106H: SHPI PT_PATH Enable Register

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11	R/W	PT_PATH[12]	0
Bit 10	R/W	PT_PATH[11]	0
Bit 9	R/W	PT_PATH[10]	0
Bit 8	R/W	PT_PATH[9]	0
Bit 7	R/W	PT_PATH[8]	0
Bit 6	R/W	PT_PATH[7]	0
Bit 5	R/W	PT_PATH[6]	0
Bit 4	R/W	PT_PATH[5]	0
Bit 3	R/W	PT_PATH[4]	0
Bit 2	R/W	PT_PATH[3]	0
Bit 1	R/W	PT_PATH[2]	0
Bit 0	R/W	PT_PATH[1]	0

The SHPI Pass Through PATH Enable Register is provided at SHPI Read/Write Address 06H.

PT_PATH[12:1]

The PT_PATH[12:1] bits are active high and disable pointer interpretation on ADD bus data. When PT_PATH[x] is low, the H1/H2 bytes for STS-1/STM-0 path x are used by the SHPI to locate the SPE. When the PT_PATH[x] is high, a J1 K28.5 control character must be present for STS-1/STM-0 path x to mark the location of the SPE.

Notes:

1. The PT_PATH[12:1] bits must be set high when performing the System Side Line Loopback.

35. If the user wants to bypass the SHPI by using the PT_PATH[12:1] bits, then Section 14.12 (HPT mode Considerations) should be read.

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Register 2108H 2110H 2118H 2120H 2128H 2130H 2138H 2140H 2148H 2150H 2158H and 2160H: SHPI Pointer Interpreter Status

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6		Unused	
Bit 5	R	PAISCV	X
Bit 4	R	PLOPCV	X
Bit 3	R	PAISV	X
Bit 2	R	PLOPV	X
Bit 1		Unused	X
Bit 0		Unused	X

The Pointer Interpreter Status Register is provided at SHPI Read/Write Address 2108H 2110H 2118H 2120H 2128H 2130H 2138H 2140H 2148H 2150H 2158H and 2160H.

PLOPV

The path lost of pointer state (PLOPV) bit indicates the current status of the pointer interpreter state machine. PLOPV is set to logic 1 when the state machine is in the LOP_state. PLOPV is set to logic 0 when the state machine is not in the LOP_state.

PAISV

The path alarm indication signal state (PAISV) bit indicates the current status of the pointer interpreter state machine. PAISV is set to logic 1 when the state machine is in the AIS_state. PAISV is set to logic 0 when the state machine is not in the AIS_state.

PLOPCV

The path lost of pointer concatenation state (PLOPCV) bit indicates the current status of the concatenation pointer interpreter state machine. PLOPCV is set to logic 1 when the state machine is in the LOPC_state. PLOPCV is set to logic 0 when the state machine is not in the LOPC_state.

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PAISCV

The path concatenation alarm indication signal state (PAISCV) bit indicates the current status of the concatenation pointer interpreter state machine. PAISCV is set to logic 1 when the state machine is in the AISC_state. PAISCV is set to logic 0 when the state machine is not in the LOPC_state.

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Register 2109H 2111H 2119H 2121H 2129H 2131H 2139H 2141H 2149H 2151H 2159H and 2161H: SHPI Pointer Interpreter Interrupt Enable

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	PAISCE	0
Bit 4	R/W	PLOPCE	0
Bit 3	R/W	PAISE	0
Bit 2	R/W	PLOPE	0
Bit 1		Unused	X
Bit 0	R/W	PTRJEE	0

The Pointer Interpreter Interrupt Enable Register is provided at SHPI Read/Write Address 2109H 2111H 2119H 2121H 2129H 2131H 2139H 2141H 2149H 2151H 2159H and 2161H.

PTRJEE

The pointer justification event interrupt enable (PTRJEE) bit control the activation of the interrupt (INTB) output. When PTRJEE is set to logic 1, the NJEI and PJEI pending interrupt will assert the interrupt (INTB) output. When PTRJEE is set to logic 0, the NJEI and PJEI pending interrupt will not assert the interrupt (INTB) output.

PLOPE

The path loss of pointer interrupt enable (PLOPE) bit controls the activation of the interrupt (INTB) output. When PLOPE is set to logic 1, the PLOPI pending interrupt will assert the interrupt (INTB) output. When PLOPE is set to logic 0, the PLOPI pending interrupt will not assert the interrupt (INTB) output.

PAISE

The path alarm indication signal interrupt enable (PAISE) bit controls the activation of the interrupt (INTB) output. When PAISE is set to logic 1, the PAISI pending interrupt will assert the interrupt (INTB) output. When PAISE is set to logic 0, the PAISI pending interrupt will not assert the interrupt (INTB) output.

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PLOPCE

The path loss of pointer concatenation interrupt enable (PLOPCE) bit controls the activation of the interrupt (INTB) output. When PLOPCE is set to logic 1, the PLOPCI pending interrupt will assert the interrupt (INTB) output. When PLOPCE is set to logic 0, the PLOPCI pending interrupt will not assert the interrupt (INTB) output.

PAISCE

The path concatenation alarm indication signal interrupt enable (PAISCE) bit controls the activation of the interrupt (INTB) output. When PAISCE is set to logic 1, the PAISCI pending interrupt will assert the interrupt (INTB) output. When PAISCE is set to logic 0, the PAISCI pending interrupt will not assert the interrupt (INTB) output.

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Register 210AH 2112H 211AH 2122H 212AH 2132H 213AH 2142H 214AH 2152H 215AH and 2162H: SHPI Pointer Interpreter Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R	PAISCI	X
Bit 4	R	PLOPCI	X
Bit 3	R	PAISI	X
Bit 2	R	PLOPI	X
Bit 1	R	PJEI	X
Bit 0	R	NJEI	X

The Pointer Interpreter Interrupt Status Register is provided at SHPI Read/Write Address 210AH 2112H 211AH 2122H 212AH 2132H 213AH 2142H 214AH 2152H 215AH and 2162H.

NJEI

The negative pointer justification event interrupt status (NJEI) bit is an event indicator. NJEI is set to logic 1 to indicate a negative pointer justification event. The interrupt status bit is independent of the interrupt enable bit. NJEI is cleared to logic 0 when this register is read.

PJEI

The positive pointer justification event interrupt status (PJEI) bit is an event indicator. PJEI is set to logic 1 to indicate a positive pointer justification event. The interrupt status bit is independent of the interrupt enable bit. PJEI is cleared to logic 0 when this register is read.

PLOPI

The path loss of pointer interrupt status (PLOPI) bit is an event indicator. PLOPI is set to logic 1 to indicate any change in the status of PLOPV (entry to the LOP_state or exit from the LOP_state). The interrupt status bit is independent of the interrupt enable bit. PLOPI is cleared to logic 0 when this register is read.

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PAISI

The path alarm indication signal interrupt status (PAISI) bit is an event indicator. PAISI is set to logic 1 to indicate any change in the status of PAISV (entry to the AIS_state or exit from the AIS_state). The interrupt status bit is independent of the interrupt enable bit. PAISI is cleared to logic 0 when this register is read.

PLOPCI

The path loss of pointer concatenation interrupt status (PLOPCI) bit is an event indicator. PLOPCI is set to logic 1 to indicate any change in the status of PLOPCV (entry to the LOPC_state or exit from the LOPC_state). The interrupt status bit is independent of the interrupt enable bit. PLOPCI is cleared to logic 0 when this register is read.

PAISCI

The path concatenation alarm indication signal interrupt status (PAISCI) bit is an event indicator. PAISCI is set to logic 1 to indicate any change in the status of PAISCV (entry to the AISC_state or exit from the AISC_state). The interrupt status bit is independent of the interrupt enable bit. PAISCI is cleared to logic 0 when this register is read.

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Register 210CH 2114H 211CH 2124H 212CH 2134H 213CH 2144H 214CH 2154H 215CH and 2164H: SHPI Error Monitor Interrupt Enable

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8	R/W	PBIPEE	0
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

The Error Monitor Interrupt Enable Register is provided at SHPI Read/Write Address 0CH 2114H 211CH 2124H 212CH 2134H 213CH 2144H 214CH 2154H 215CH and 2164H.

PBIPEE

The path BIP-8 error interrupt enable (PBIPEE) bit controls the activation of the interrupt (INTB) output. When PBIPEE is set to logic 1, the PBIPEI pending interrupt will assert the interrupt (INTB) output. When PBIPEE is set to logic 0, the PBIPEI pending interrupt will not assert the interrupt (INTB) output.

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Register 210DH 2115H 211DH 2125H 212DH 2135H 213DH 2145H 214DH 2155H 215DH and 2165H: SHPI Error Monitor Interrupt Status

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8	R	PBIPEI	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

The Error Monitor Interrupt Status Register is provided at SHPI Read/Write Address 210DH 2115H 211DH 2125H 212DH 2135H 213DH 2145H 214DH 2155H 215DH and 2165H.

PBIPEI

The path BIP-8 error interrupt status (PBIPEI) bit is an event indicator. PBIPEI is set to logic 1 to indicate a path BIP-8 error. The interrupt status bit is independent of the interrupt enable bit. PBIPEI is cleared to logic 0 when this register is read.

15.21 ASSI Normal Registers

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Register 2180H : ASSI Page 0 Source Selection for STS-12/STM-4 #1 to #4

Bit	Type	Function	Default
Bit 15	R/W	PG0[3][3]	0
Bit 14	R/W	PG0[3][2]	0
Bit 13	R/W	PG0[3][1]	1
Bit 12	R/W	PG0[3][0]	1
Bit 11	R/W	PG0[2][3]	0
Bit 10	R/W	PG0[2][2]	0
Bit 9	R/W	PG0[2][1]	1
Bit 8	R/W	PG0[2][0]	0
Bit 7	R/W	PG0[1][3]	0
Bit 6	R/W	PG0[1][2]	0
Bit 5	R/W	PG0[1][1]	0
Bit 4	R/W	PG0[1][0]	1
Bit 3	R/W	PG0[0][3]	0
Bit 2	R/W	PG0[0][2]	0
Bit 1	R/W	PG0[0][1]	0
Bit 0	R/W	PG0[0][0]	0

The ASSI Page 0 source selection for STS-12/STM-4 #1 to #4 is provided at ASSI Read/Write Address 0180.

PG0[0-3][0-3]

The PG0[0-3][0-3] selects the STS-12/STM-4 SONET/SDH stream that is to be output on the STS-12/STM4 SONET/SDH stream #1 to #4, the default value being the STS-12/STM-4 stream itself.

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Register 2181H: ASSI Page 0 Source Selection for STS-12/STM-4 #5 to #8

Bit	Type	Function	Default
Bit 15	R/W	PG0[7][3]	0
Bit 14	R/W	PG0[7][2]	1
Bit 13	R/W	PG0[7][1]	1
Bit 12	R/W	PG0[7][0]	1
Bit 11	R/W	PG0[6][3]	0
Bit 10	R/W	PG0[6][2]	1
Bit 9	R/W	PG0[6][1]	1
Bit 8	R/W	PG0[6][0]	0
Bit 7	R/W	PG0[5][3]	0
Bit 6	R/W	PG0[5][2]	1
Bit 5	R/W	PG0[5][1]	0
Bit 4	R/W	PG0[5][0]	1
Bit 3	R/W	PG0[4][3]	0
Bit 2	R/W	PG0[4][2]	1
Bit 1	R/W	PG0[4][1]	0
Bit 0	R/W	PG0[4][0]	0

The ASSI Page 0 source selection for STS-12/STM-4 #5 to #8 is provided at ASSI Read/Write Address 0181.

PG0[4-7][0-3]

The PG0[4-7][0-3] selects the STS-12/STM-4 SONET/SDH stream that is to be output on the STS-12/STM4 SONET/SDH stream #5 to #8, the default value being the STS-12/STM-4 stream itself.

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Register 2182H: ASSI Page 0 Source Selection for STS-12/STM-4 #9 to #12

Bit	Type	Function	Default
Bit 15	R/W	PG0[11][3]	1
Bit 14	R/W	PG0[11][2]	0
Bit 13	R/W	PG0[11][1]	1
Bit 12	R/W	PG0[11][0]	1
Bit 11	R/W	PG0[10][3]	1
Bit 10	R/W	PG0[10][2]	0
Bit 9	R/W	PG0[10][1]	1
Bit 8	R/W	PG0[10][0]	0
Bit 7	R/W	PG0[9][3]	1
Bit 6	R/W	PG0[9][2]	0
Bit 5	R/W	PG0[9][1]	0
Bit 4	R/W	PG0[9][0]	1
Bit 3	R/W	PG0[8][3]	1
Bit 2	R/W	PG0[8][2]	0
Bit 1	R/W	PG0[8][1]	0
Bit 0	R/W	PG0[8][0]	0

The ASSI Page 0 source selection for STS-12/STM-4 #8 to #11 is provided at ASSI Read/Write Address 0180.

PG0[8-11][0-3]

The PG0[8-11][0-3] selects the STS-12/STM-4 SONET/SDH stream that is to be output on the STS-12/STM4 SONET/SDH stream #9 to #12, the default value being the STS-12/STM-4 stream itself.

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Register 2183H: ASSI Page 0 Source Selection for STS-12/STM-4 #13 to #16

Bit	Type	Function	Default
Bit 15	R/W	PG0[15][3]	1
Bit 14	R/W	PG0[15][2]	1
Bit 13	R/W	PG0[15][1]	1
Bit 12	R/W	PG0[15][0]	1
Bit 11	R/W	PG0[14][3]	1
Bit 10	R/W	PG0[14][2]	1
Bit 9	R/W	PG0[14][1]	1
Bit 8	R/W	PG0[14][0]	0
Bit 7	R/W	PG0[13][3]	1
Bit 6	R/W	PG0[13][2]	1
Bit 5	R/W	PG0[13][1]	0
Bit 4	R/W	PG0[13][0]	1
Bit 3	R/W	PG0[12][3]	1
Bit 2	R/W	PG0[12][2]	1
Bit 1	R/W	PG0[12][1]	0
Bit 0	R/W	PG0[12][0]	0

The ASSI Page 0 source selection for STS-12/STM-4 #12 to #15 is provided at ASSI Read/Write Address 0183.

PG0[13-16][0-3]

The PG0[13-16][0-3] selects the STS-12/STM-4 SONET/SDH stream that is to be output on the STS-12/STM4 SONET/SDH stream #13 to #16, the default value being the STS-12/STM-4 stream itself.

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Register 2184H: ASSI Page 1 Source Selection for STS-12/STM-4 #1 to #4

Bit	Type	Function	Default
Bit 15	R/W	PG1[3][3]	0
Bit 14	R/W	PG1[3][2]	0
Bit 13	R/W	PG1[3][1]	1
Bit 12	R/W	PG1[3][0]	1
Bit 11	R/W	PG1[2][3]	0
Bit 10	R/W	PG1[2][2]	0
Bit 9	R/W	PG1[2][1]	1
Bit 8	R/W	PG1[2][0]	0
Bit 7	R/W	PG1[1][3]	0
Bit 6	R/W	PG1[1][2]	0
Bit 5	R/W	PG1[1][1]	0
Bit 4	R/W	PG1[1][0]	1
Bit 3	R/W	PG1[0][3]	0
Bit 2	R/W	PG1[0][2]	0
Bit 1	R/W	PG1[0][1]	0
Bit 0	R/W	PG1[0][0]	0

The ASSI Page 1 source selection for STS-12/STM-4 #1 to #4 is provided at ASSI Read/Write Address 0180.

PG1[0-3][0-3]

The PG1[0-3][0-3] selects the STS-12/STM-4 SONET/SDH stream that is to be output on the STS-12/STM4 SONET/SDH stream #1 to #4, the default value being the STS-12/STM-4 stream itself.

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Register 2185H: ASSI Page 1 Source Selection for STS-12/STM-4 #5 to #8

Bit	Type	Function	Default
Bit 15	R/W	PG1[7][3]	0
Bit 14	R/W	PG1[7][2]	1
Bit 13	R/W	PG1[7][1]	1
Bit 12	R/W	PG1[7][0]	1
Bit 11	R/W	PG1[6][3]	0
Bit 10	R/W	PG1[6][2]	1
Bit 9	R/W	PG1[6][1]	1
Bit 8	R/W	PG1[6][0]	0
Bit 7	R/W	PG1[5][3]	0
Bit 6	R/W	PG1[5][2]	1
Bit 5	R/W	PG1[5][1]	0
Bit 4	R/W	PG1[5][0]	1
Bit 3	R/W	PG1[4][3]	0
Bit 2	R/W	PG1[4][2]	1
Bit 1	R/W	PG1[4][1]	0
Bit 0	R/W	PG1[4][0]	0

The ASSI Page 1 source selection for STS-12/STM-4 #5 to #8 is provided at ASSI Read/Write Address 0181.

PG1[4-7][0-3]

The PG1[4-7][0-3] selects the STS-12/STM-4 SONET/SDH stream that is to be output on the STS-12/STM4 SONET/SDH stream #5 to #8, the default value being the STS-12/STM-4 stream itself.

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Register 2186H: ASSI Page 1 Source Selection for STS-12/STM-4 #9 to #12

Bit	Type	Function	Default
Bit 15	R/W	PG1[11][3]	1
Bit 14	R/W	PG1[11][2]	0
Bit 13	R/W	PG1[11][1]	1
Bit 12	R/W	PG1[11][0]	1
Bit 11	R/W	PG1[10][3]	1
Bit 10	R/W	PG1[10][2]	0
Bit 9	R/W	PG1[10][1]	1
Bit 8	R/W	PG1[10][0]	0
Bit 7	R/W	PG1[9][3]	1
Bit 6	R/W	PG1[9][2]	0
Bit 5	R/W	PG1[9][1]	0
Bit 4	R/W	PG1[9][0]	1
Bit 3	R/W	PG1[8][3]	1
Bit 2	R/W	PG1[8][2]	0
Bit 1	R/W	PG1[8][1]	0
Bit 0	R/W	PG1[8][0]	0

The ASSI Page 1 source selection for STS-12/STM-4 #8 to #11 is provided at ASSI Read/Write Address 0180.

PG1[8-11][0-3]

The PG1[8-11][0-3] selects the STS-12/STM-4 SONET/SDH stream that is to be output on the STS-12/STM4 SONET/SDH stream #9 to #12, the default value being the STS-12/STM-4 stream itself.

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Register 2187H: ASSI Page 1 Source Selection for STS-12/STM-4 #13 to #16

Bit	Type	Function	Default
Bit 15	R/W	PG1[15][3]	1
Bit 14	R/W	PG1[15][2]	1
Bit 13	R/W	PG1[15][1]	1
Bit 12	R/W	PG1[15][0]	1
Bit 11	R/W	PG1[14][3]	1
Bit 10	R/W	PG1[14][2]	1
Bit 9	R/W	PG1[14][1]	1
Bit 8	R/W	PG1[14][0]	0
Bit 7	R/W	PG1[13][3]	1
Bit 6	R/W	PG1[13][2]	1
Bit 5	R/W	PG1[13][1]	0
Bit 4	R/W	PG1[13][0]	1
Bit 3	R/W	PG1[12][3]	1
Bit 2	R/W	PG1[12][2]	1
Bit 1	R/W	PG1[12][1]	0
Bit 0	R/W	PG1[12][0]	0

The ASSI Page 1 source selection for STS-12/STM-4 #12 to #15 is provided at ASSI Read/Write Address 0183.

PG1[13-16][0-3]

The PG1[13-16][0-3] selects the STS-12/STM-4 SONET/SDH stream that is to be output on the STS-12/STM4 SONET/SDH stream #13 to #16, the default value being the STS-12/STM-4 stream itself.

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Register 2188H: ASSI Control Register

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		Unused	
Bit 9		Unused	
Bit 8		Unused	
Bit 7		Unused	
Bit 6		Unused	
Bit 5		Unused	
Bit 4		Unused	
Bit 3		Unused	
Bit 2		Unused	
Bit 1		Unused	
Bit 0	R/W	IPS	0

The ASSI control register is provided at Read/Write Address 0188H. This register stores the internal page select (IPS), which is used for the selection of the control page. This internal bit allows the user to switch the page by changing the value in this register. In fact, either IPS or DCMP bits can be used independently for the page switching. This is implemented to provide both software and hardware control over the page selection, depending on the user preference.

IPS

The internal page select (IPS) bit is used in conjunction with the control page select (DCMP) input to select the active address page used by the ASSI. The IPS bit is XORed with the DCMP input signal and the logical result determines the page that will be used. When the result is logic 0, the page 0 is selected and, consequently, when the result is logic 1, the page 1 is selected. Reading this register bit provides the result of the XOR operation, thus providing the current page selected.

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16 Test Features Description

The test mode registers are used for production and board testing.

During production testing, the test mode registers are used to apply test vectors. In this case, the test mode registers (as opposed to the normal mode registers) are selected when A[14] is high.

During board testing, the digital output pins and the data bus are held in a high-impedance state by simultaneously asserting (low) the CSB, RDB, and WRB inputs. All of the functional blocks (TSBs) for SPECTRA-9953 device are placed in test mode 0 so that device inputs may be read and device outputs may be forced through the microprocessor interface. Refer to the section "Test Mode "0" for details.

Note: The SPECTRA-9953 device supports a standard IEEE 1149.1 five-signal JTAG boundary scan test port that can be used for board testing. All digital device inputs may be read and all digital device outputs may be forced through this JTAG test port.

Table 16 Test Mode Register Memory Map

Address	Register
0000H-3FFFH	Normal Mode Registers
4000	Master Test Register
4001	Test Mode Address Force Enable
4002	Test Mode Address Force Value
4003	System Side Control
4004	Line side analog test regsiter
4005	Sysctl control test points
4006	Sysctl observation test points
4007	Rohi control test points
4008	Rohi observation test points
4009	Tohi control test points
400A	tohi observation test points
400B-4FFF	Reserved For Test

16.1 Master Test and Test Configuration Registers

Notes on Test Mode Register Bits:

1. Writing values into unused register bits has no effect. However, to ensure software compatibility with future, feature-enhanced versions of the product, unused register bits must be written with logic zero. Reading back unused bits can produce either a logic one or a logic zero; hence, unused register bits should be masked off by software when read.

36. Writable test mode register bits are not initialized upon reset unless otherwise noted.

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Register 4000H: SPECTRA-9953 Master Test

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8	R/W	Test_tclk_mux_en[7]	X
Bit 7	R/W	Test_rclk_mux_en	X
Bit 6		Unused	
Bit 5	R/W	PMCATST	X
Bit 4	R/W	PMCTST	X
Bit 3	R/W	Reserved	0
Bit 2	R/W	IOTST	0
Bit 1	R/W	HIZDATA	0
Bit 0	R/W	HIZIO	0

This register is used to enable SPECTRA-9953 test features. HIZIO, HIZDATA, IOTST and DBCTRL are reset to zero by a reset of the SPECTRA-9953 using the RSTB input. PMCTST , PMCATST, test_rclk_mux_en and test_tclk_mux_en are reset when CSB is logic 1. PMCTST and PMCATST can also be reset by writing a logic 0 to the corresponding register bit.

Access to this register is not affected by the Test Mode Address Force functions in registers 4001H and 4002H.

HIZIO, HIZDATA

The HIZIO and HIZDATA bits control the tri-state modes of the SPECTRA-9953. While the HIZIO bit is a logic one, all output pins of the SPECTRA-9953 except the data bus and output TDO are held tri-state. The microprocessor interface is still active. While the HIZDATA bit is a logic one, the data bus is also held in a high-impedance state which inhibits microprocessor read cycles. The HIZDATA bit is overridden by the DBCTRL bit.

[7] For proper normal mode operation of the device, CSB must be high during a reset.

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IOTST

The IOTST bit is used to allow normal microprocessor access to the top-level test registers and control or observe the top-level device input/outputs for board level testing. When IOTST is a logic 1, all inputs/outputs can be observed/controlled via test registers.

PMCTST

The PMCTST bit is used to configure the SPECTRA-9953 for PMC's manufacturing tests. When PMCTST is set to logic one, the SPECTRA-9953 microprocessor port becomes the test access port used to run the PMC "canned" manufacturing test vectors. The PMCTST can be cleared by setting CSB to logic one or by writing logic zero to the bit.

PMCATST

The PMCATST bit is used to configure the analog portion of the SPECTRA-9953 for PMC's manufacturing tests. The PMCATST can be cleared by setting CSB to logic one or by writing logic zero to the bit.

Test_rclk_mux_en

The test_rclk_mux_en is used during test mode to force the test_rclk input clock on the internal line receive clock (77MHz and 155MHz). The test_rclk_mux_en can be cleared by setting CSB to logic one or by writing logic zero to the bit.

Test_tclk_mux_en

The test_tclk_mux_en is used during test mode to force the test_tclk input clock on the internal line receive clock (77MHz and 155MHz). The test_tclk_mux_en can be cleared by setting CSB to logic one or by writing logic zero to the bit.

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Register 4001H: SPECTRA-9953 Test Mode Address Force Enable

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R/W	TM_A_EN	X

This register is used to force the address pins to a certain value. These bits are valid when either PMCTST or IOTST is set to logic 1. The TM_A[X] bit is forced when TM_A_EN is logic 1. Otherwise, the A[X] pin is used.

Access to this register is not affected by the Test Mode Address Force functions in registers 4001H and 4002H.

TM_A_EN

When TM_A_EN is logic 1 and either PMCTST or IOTST is logic 1, the TM_A[X] register bit replaces the input pin A[X]. Like PMCTST and PMCATST, TM_A_EN bits are cleared only when CSB is logic 1 or when they are written to logic 0.

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Register 4002H: SPECTRA-9953 Test Mode Address Force Value

Bit	Type	Function	Default
Bit 15		Unused	X
Bit 14		Unused	X
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	TM_A[13]	X
Bit 2	R/W	TM_A[12]	X
Bit 1	R/W	TM_A[11]	X
Bit 0	R/W	TM_A[10]	X

This register is used to force the address pins to a certain value. These bits are valid when either PMCTST or IOTST is set to logic 1. The TM_A[X] bit is forced when TM_A_EN is logic 1. Otherwise, the A[X] pin is used.

Access to this register is not affected by the Test Mode Address Force functions in registers 4001H and 4002H.

TM_A[13:10]

When TM_A_EN is logic 1 and either PMCTST or IOTST is logic 1, the TM_A[X] bit replaces the input pin A[X]. Like PMCTST and PMCATST, TM_A[X] bits are cleared only when CSB is logic 1 or when they are written to logic 0.

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Register 4003H: System Side Control

Bit	Type	Function	Default
Bit 15	R/W	UNUSED	X
Bit 14	R/W	UNUSED	X
Bit 13	R/W	UNUSED	X
Bit 12	R/W	UNUSED	X
Bit 11	R/W	UNUSED	X
Bit 10	R/W	UNUSED	X
Bit 9	R/W	UNUSED	X
Bit 8	R/W	UNUSED	X
Bit 7	R/W	UNUSED	X
Bit 6	R/W	UNUSED	X
Bit 5	R/W	UNUSED	X
Bit 4	R/W	UNUSED	X
Bit 3	R/W	UNUSED	X
Bit 2	R/W	SYS_ATMSB	X
Bit 1	R/W	R8TD_SCLKE	X
Bit 0	R/W	T8TE_SCLKE	X

This register is used to enable test mode in the analog blocks. These bits are valid when PMCATST is set to logic 1.

Access to this register is not affected by the Test Mode Address Force functions in registers 4001H and 4002H.

SYS_ATMSB

Global System side analog MABC test mode select. This signal is to be driven to logic ‘0’ whenever an individual ABC ATMSB is at logic ‘0’. SYS_ATMSB bits are cleared only when CSB is logic 1 or when they are written to logic 0.

R8TD_SCLKE

When enabled, this register bit muxes the system clock on the R8TD piclk in order to apply scan vectors. R8TD_SCLKE bits are cleared only when CSB is logic 1 or when they are written to logic 0.

T8TE_SCLKE

When enabled, this register bit muxes the system clock on the T8TD poclk in order to apply scan vectors. T8TE_SCLKE bits are cleared only when CSB is logic 1 or when they are written to logic 0.

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Register 4004H: SPECTRA-9953 Line Side Analog Test Register

Bit	Type	Function	Default
Bit 15		Unused	
Bit 14		Unused	
Bit 13		Unused	
Bit 12		Unused	
Bit 11		Unused	
Bit 10		LINE_ANALOG_TMS	
Bit 9		LINE_ANALOG_ATMS[5]	
Bit 8		LINE_ANALOG_ATMS[4]	
Bit 7		LINE_ANALOG_ATMS[3]	
Bit 6		LINE_ANALOG_ATMS[2]	
Bit 5		LINE_ANALOG_ATMS[1]	
Bit 4		LINE_ANALOG_ATMS[0]	
Bit 3	R/W	LINE_ANALOG_TIN[3]	X
Bit 2	R/W	LINE_ANALOG_TIN[2]	X
Bit 1	R/W	LINE_ANALOG_TIN[1]	X
Bit 0	R/W	LINE_ANALOG_TIN[0]	X

This register is used to enable test mode in the line side analog blocks. These bits are valid when PMCATST is set to logic 1.

Access to this register is not affected by the Test Mode Address Force functions in registers 4001H and 4002H.

LINE_ANALOG_TMS

When LINE_ANALOG_TMS and PMCATST are logic 1, the line side analog mega ABC is configured for its manufacturing test mode. Like PMCTST and PMCATST, LINE_ANALOG_TMS bits are cleared only when CSB is logic 1 or when they are written to logic 0.

LINE_ANALOG_ATMS[5:0]

LINE_ANALOG_ATMS[5:0] is used to select the block to be tested when the OIFs is in analog test mode. Like PMCTST and PMCATST, LINE_ANALOG_TMS bits are cleared only when CSB is logic 1 or when they are written to logic 0.

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LINE_ANALOG_TIN[3:0]

LINE_ANALOG_TIN[3:0] is used to select the test points in the OIF mega ABC block selected by LINE_ANALOG_ATMS[5:0]. Like PMCTST and PMCATST, LINE_ANALOG_TMS bits are cleared only when CSB is logic 1 or when they are written to logic 0.

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Register 4005H: SPECTRA-9953 SYSCTL Control Test Points

Bit	Type	Function	Default
Bit 15	R/W	Unused	X
Bit 14	R/W	Unused	X
Bit 13	R/W	Unused	X
Bit 12	R/W	STS_CNTR_FORCE	X
Bit 11	R/W	ASTS[3]	X
Bit 10	R/W	ASTS[2]	X
Bit 9	R/W	ASTS[1]	X
Bit 8	R/W	ASTS[0]	X
Bit 7	R/W	DSTS[3]	X
Bit 6	R/W	DSTS[2]	X
Bit 5	R/W	DSTS[1]	X
Bit 4	R/W	DSTS[0]	X
Bit 3	R/W	J0_FORCE	X
Bit 2	R/W	AJ0_FE	X
Bit 1	R/W	DJ0_FE	X
Bit 0	R/W	DFPO	X

This register is used to enable sysctl control test points. DFPO control point is active when IOTST is set to logic 1. Other control signals are active when J0_FORCE is set to logic 1.

Access to this register is not affected by the Test Mode Address Force functions in registers 4001H and 4002H.

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Register 4006H: SPECTRA-9953 SYSCTL Observation Test Points

Bit	Type	Function	Default
Bit 15	R/W	Unused	X
Bit 14	R/W	Unused	X
Bit 13	R/W	Unused	X
Bit 12	R/W	UNUSED	X
Bit 11	R/W	UNUSED	X
Bit 10	R/W	AJ0_FE	X
Bit 9	R/W	DJ0_FE	X
Bit 8	R/W	TPAIS[4]	X
Bit 7	R/W	TPAIS[3]	X
Bit 6	R/W	TPAIS[2]	X
Bit 5	R/W	TPAIS[1]	X
Bit 4	R/W	TPAIS_FP	X
Bit 3	R/W	ACMP	X
Bit 2	R/W	AFP	X
Bit 1	R/W	DCMP	X
Bit 0	R/W	DFP	X

This register is used to enable sysctl observation test points.

Access to this register is not affected by the Test Mode Address Force functions in registers 4001H and 4002H.

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Register 4007H: SPECTRA-9953 ROHI Control Test Points

Bit	Type	Function	Default
Bit 15	R/W	Unused	X
Bit 14	R/W	STM16_CLKCTRL4	X
Bit 13	R/W	STM16_CLKCTRL3	X
Bit 12	R/W	STM16_CLKCTRL2	X
Bit 11	R/W	STM16_CLKCTRL1	X
Bit 10	R/W	STM16_IOTST4	X
Bit 9	R/W	STM16_IOTST3	X
Bit 8	R/W	STM16_IOTST2	X
Bit 7	R/W	STM16_IOTST1	X
Bit 6	R/W	STM16CLK_MUX	X
Bit 5	R/W	B3E	X
Bit 4	R/W	RTOH	X
Bit 3	R/W	ROHCLK	X
Bit 2	R/W	ROHFP	X
Bit 1	R/W	RLDCLK	X
Bit 0	R/W	RSLDCLK	X

This register is used to enable ROHI control test points. RSLDCLK, RLDCLK, ROHFP, ROHCLK, RTOH and B3E control points are active when IOTST is set to logic 1. STM16_IOTST[4:1] is used to independently control the four ROHI blocks. STM16CLK_MUX is used to force test_rclk on the internal ROHI block 103MHz clock. STM16_CLKCTRL[4:1] are used to independently control the ROHI blocks.

Access to this register is not affected by the Test Mode Address Force functions in registers 4001H and 4002H.

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Register 4008H: SPECTRA-9953 ROHI Observation Test Points

Bit	Type	Function	Default
Bit 15	R/W		X
Bit 14	R/W		X
Bit 13	R/W		X
Bit 12	R/W		X
Bit 11	R/W		X
Bit 10	R/W		X
Bit 9	R/W		X
Bit 8	R/W		X
Bit 7	R/W		X
Bit 6	R/W		X
Bit 5	R/W		X
Bit 4	R/W		X
Bit 3	R/W	STM16CLK4	X
Bit 2	R/W	STM16CLK3	X
Bit 1	R/W	STM16CLK2	X
Bit 0	R/W	STM16CLK1	X

This register is used to enable ROHI observation test points.

Access to this register is not affected by the Test Mode Address Force functions in registers 4001H and 4002H.

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Register 4009H: SPECTRA-9953 TOHI Control Test Points

Bit	Type	Function	Default
Bit 15	R/W	UNUSED	X
Bit 14	R/W	UNUSED	X
Bit 13	R/W	UNUSED	X
Bit 12	R/W	STM16_CLKCTRL4	X
Bit 11	R/W	STM16_CLKCTRL3	X
Bit 10	R/W	STM16_CLKCTRL2	X
Bit 9	R/W	STM16_CLKCTRL1	X
Bit 8	R/W	STM16_IOTST4	X
Bit 7	R/W	STM16_IOTST3	X
Bit 6	R/W	STM16_IOTST2	X
Bit 5	R/W	STM16_IOTST1	X
Bit 4	R/W	STM16CLK_MUX	X
Bit 3	R/W	TOHCLK	X
Bit 2	R/W	TOHFP	X
Bit 1	R/W	TLDCLK	X
Bit 0	R/W	TSLDCLK	X

This register is used to enable TOHI control test points. TSLDCLK, TLDCLK, TOHFP, TOHCLK control points are active when IOTST is set to logic 1. STM16_IOTST[4:1] is used to independently control the four ROHI blocks. STM16CLK_MUX is used to force test_tclk on the internal TOHI block 103MHz clock. STM16_CLKCTRL[4:1] are used to independently control the ROHI blocks.

Access to this register is not affected by the Test Mode Address Force functions in registers 4001H and 4002H.

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Register 400AH: SPECTRA-9953 TOHI Observation Test Points

Bit	Type	Function	Default
Bit 15	R/W	UNUSED	X
Bit 14	R/W	UNUSED	X
Bit 13	R/W	UNUSED	X
Bit 12	R/W	UNUSED	X
Bit 11	R/W	TTOHEN4	X
Bit 10	R/W	TTOHEN3	X
Bit 9	R/W	TTOHEN2	X
Bit 8	R/W	TTOHEN1	X
Bit 7	R/W	TTOH4	X
Bit 6	R/W	TTOH3	X
Bit 5	R/W	TTOH2	X
Bit 4	R/W	TTOH1	X
Bit 3	R/W	STM16_CLK4	X
Bit 2	R/W	STM16_CLK3	X
Bit 1	R/W	STM16_CLK2	X
Bit 0	R/W	STM16_CLK1	X

This register is used to enable ROHI observation test points.

Access to this register is not affected by the Test Mode Address Force functions in registers 4001H and 4002H.

16.2 JTAG Test Port

The SPECTRA-9953 device supports the IEEE Boundary Scan Specification as described in the IEEE 1149.1 standards. The Test Access Port (TAP) consists of the five standard pins, TRSTB, TCK, TMS, TDI and TDO used to control the TAP controller and the boundary scan registers. The TRSTB input is the active-low reset signal used to reset the TAP controller. TCK is the test clock used to sample data on input, TDI and to output data on output, TDO. The TMS input is used to direct the TAP controller through its states.

The SPECTRA-9953 JTAG Test Access Port (TAP) allows access to the TAP controller and the four TAP registers: instruction, bypass, device identification, and boundary scan. Using the TAP, device input logic levels can be read, device outputs can be forced, the device can be identified and the device scan path can be bypassed. For more details on the JTAG port, please refer to the Operations section.

Table 17 Instruction Register (Length - 3 bits)

Instructions	Selected Register	Instruction Codes, IR[2:0]
EXTEST	Boundary Scan	000

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Instructions	Selected Register	Instruction Codes, IR[2:0]
IDCODE	Identification	001
SAMPLE	Boundary Scan	010
BYPASS	Bypass	011
BYPASS	Bypass	100
STCTEST	Boundary Scan	101
BYPASS	Bypass	110
BYPASS	Bypass	111

Table 18 Identification Register

Length	32 bits
Version Number	2H
Part Number	5317H
Manufacturer's Identification Code	0CDH
Device Identification	053170CDH

Table 19 Boundary Scan Register

Pin/ Enable	Register Bit	Cell Type	I.D. Bit	Pin/ Enable	Register Bit	Cell Type	I.D. Bit
hiz	270	IN_CELL		oeb_rld[4]	135	IN_CELL	
rstb	269	IN_CELL		rld[4]	134	OUT_CELL	
ale	268	IN_CELL		oeb_rld[3]	133	IN_CELL	
Oeb_intb	267	IN_CELL		rld[3]	132	OUT_CELL	
intb	266	OUT_CELL		oeb_rld[2]	131	IN_CELL	
csb	265	IN_CELL		rld[2]	130	OUT_CELL	
rdb	264	IN_CELL		oeb_rld[1]	129	IN_CELL	
wrb	263	IN_CELL		rld[1]	128	OUT_CELL	
a[14]	262	IN_CELL		oeb_rldclk[4]	127	IN_CELL	
a[13]	261	IN_CELL		rldclk[4]	126	OUT_CELL	
a[12]	260	IN_CELL		oeb_rldclk[3]	125	IN_CELL	
a[11]	259	IN_CELL		rldclk[3]	124	OUT_CELL	
a[10]	258	IN_CELL		oeb_rldclk[2]	123	IN_CELL	
a[9]	257	IN_CELL		rldclk[2]	122	OUT_CELL	
a[8]	256	IN_CELL		oeb_rldclk[1]	121	IN_CELL	
a[7]	255	IN_CELL		rldclk[1]	120	OUT_CELL	
a[6]	254	IN_CELL		oeb_rsld[4]	119	IN_CELL	
a[5]	253	IN_CELL		rsld[4]	118	OUT_CELL	
a[4]	252	IN_CELL		oeb_rsld[3]	117	IN_CELL	
a[3]	251	IN_CELL		rsld[3]	116	OUT_CELL	
a[2]	250	IN_CELL		oeb_rsld[2]	115	IN_CELL	

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Pin/ Enable	Register Bit	Cell Type	I.D. Bit	Pin/ Enable	Registe r Bit	Cell Type	I.D. Bit
a[1]	249	IN_CELL		rsld[2]	114	OUT_CELL	
a[0]	248	IN_CELL		oeb_rsld[1]	113	IN_CELL	
Oeb_d[15]	247	IN_CELL		rsld[1]	112	OUT_CELL	
d[15]	246	IO_CELL		oeb_rsldclk[4]	111	IN_CELL	
Oeb_d[14]	245	IN_CELL		rsldclk[4]	110	OUT_CELL	
d[14]	244	IO_CELL		oeb_rsldclk[3]	109	IN_CELL	
Oeb_d[13]	243	IN_CELL		rsldclk[3]	108	OUT_CELL	
d[13]	242	IO_CELL		oeb_rsldclk[2]	107	IN_CELL	
oeb_d[12]	241	IN_CELL		rsldclk[2]	106	OUT_CELL	
d[12]	240	IO_CELL		oeb_rsldclk[1]	105	IN_CELL	
oeb_d[11]	239	IN_CELL		rsldclk[1]	104	OUT_CELL	
d[11]	238	IO_CELL		pgmrclk	103	OUT_CELL	
oeb_d[10]	237	IN_CELL		sync_err4	102	IN_CELL	
d[10]	236	IO_CELL		sync_err3	101	IN_CELL	
oeb_d[9]	235	IN_CELL		sync_err2	100	IN_CELL	
d[9]	234	IO_CELL		sync_err1	99	IN_CELL	
oeb_d[8]	233	IN_CELL		rxclk1_p	98	IN_CELL	
d[8]	232	IO_CELL		rxdata1_p[0]	97	IN_CELL	
oeb_d[7]	231	IN_CELL		rxdata1_p[1]	96	IN_CELL	
d[7]	230	IO_CELL		rxdata1_p[2]	95	IN_CELL	
oeb_d[6]	229	IN_CELL		rxdata1_p[3]	94	IN_CELL	
d[6]	228	IO_CELL		rxclk2_p	93	IN_CELL	
oeb_d[5]	227	IN_CELL		rxdata2_p[0]	92	IN_CELL	
d[5]	226	IO_CELL		rxdata2_p[1]	91	IN_CELL	
oeb_d[4]	225	IN_CELL		rxdata2_p[2]	90	IN_CELL	
d[4]	224	IO_CELL		rxdata2_p[3]	89	IN_CELL	
oeb_d[3]	223	IN_CELL		rxclk3_p	88	IN_CELL	
d[3]	222	IO_CELL		rxdata3_p[0]	87	IN_CELL	
oeb_d[2]	221	IN_CELL		rxdata3_p[1]	86	IN_CELL	
d[2]	220	IO_CELL		rxdata3_p[2]	85	IN_CELL	
oeb_d[1]	219	IN_CELL		rxdata3_p[3]	84	IN_CELL	
d[1]	218	IO_CELL		rxclk4_p	83	IN_CELL	
oeb_d[0]	217	IN_CELL		rxdata4_p[0]	82	IN_CELL	
d[0]	216	IO_CELL		rxdata4_p[1]	81	IN_CELL	
tpais[4]	215	IN_CELL		rxdata4_p[2]	80	IN_CELL	
tpais[3]	214	IN_CELL		rxdata4_p[3]	79	IN_CELL	
tpais[2]	213	IN_CELL		txclk1_src_p	78	IN_CELL	
tpais[1]	212	IN_CELL		txclk1_p	77	OUT_CELL	
afp	211	IN_CELL		txdata1_p[0]	76	OUT_CELL	

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Pin/ Enable	Register Bit	Cell Type	I.D. Bit	Pin/ Enable	Register Bit	Cell Type	I.D. Bit
acmp	210	IN_CELL		txdata1_p[1]	75	OUT_CELL	
tpaisfp	209	IN_CELL		txdata1_p[2]	74	OUT_CELL	
dfp	208	IN_CELL		txdata1_p[3]	73	OUT_CELL	
dfpo	207	OUT_CELL		txclk2_src_p	72	IN_CELL	
dcmp	206	IN_CELL		txclk2_p	71	OUT_CELL	
sysclk	205	IN_CELL		txdata2_p[0]	70	OUT_CELL	
quad2488	204	IN_CELL		txdata2_p[1]	69	OUT_CELL	
trcpdat[4]	203	IN_CELL		txdata2_p[2]	68	OUT_CELL	
trcpdat[3]	202	IN_CELL		txdata2_p[3]	67	OUT_CELL	
trcpdat[2]	201	IN_CELL		txclk3_src_p	66	IN_CELL	
trcpdat[1]	200	IN_CELL		txclk3_p	65	OUT_CELL	
rrcpdat[4]	199	OUT_CELL		txdata3_p[0]	64	OUT_CELL	
rrcpdat[3]	198	OUT_CELL		txdata3_p[1]	63	OUT_CELL	
rrcpdat[2]	197	OUT_CELL		txdata3_p[2]	62	OUT_CELL	
rrcpdat[1]	196	OUT_CELL		txdata3_p[3]	61	OUT_CELL	
trcpfp	195	IN_CELL		txclk4_src_p	60	IN_CELL	
rrcpclk	194	OUT_CELL		txclk4_p	59	OUT_CELL	
rrcpfp	193	OUT_CELL		txdata4_p[0]	58	OUT_CELL	
trcpclk	192	IN_CELL		txdata4_p[1]	57	OUT_CELL	
ralm[4]	191	OUT_CELL		txdata4_p[2]	56	OUT_CELL	
ralm[3]	190	OUT_CELL		txdata4_p[3]	55	OUT_CELL	
ralm[2]	189	OUT_CELL		phase_init4	54	OUT_CELL	
ralm[1]	188	OUT_CELL		phase_init3	53	OUT_CELL	
rsalm[4]	187	OUT_CELL		phase_init2	52	OUT_CELL	
rsalm[3]	186	OUT_CELL		phase_init1	51	OUT_CELL	
rsalm[2]	185	OUT_CELL		phase_err4	50	IN_CELL	
rsalm[1]	184	OUT_CELL		phase_err3	49	IN_CELL	
ad1_p[0]	183	IN_CELL		phase_err2	48	IN_CELL	
ad1_p[1]	182	IN_CELL		phase_err1	47	IN_CELL	
ad1_p[2]	181	IN_CELL		txfpo4	46	OUT_CELL	
ad1_p[3]	180	IN_CELL		txfpo3	45	OUT_CELL	
dd1_p[0]	179	OUT_CELL		txfpo2	44	OUT_CELL	
dd1_p[1]	178	OUT_CELL		txfpo1	43	OUT_CELL	
dd1_p[2]	177	OUT_CELL		txfpi	42	IN_CELL	
dd1_p[3]	176	OUT_CELL		pgmtclk	41	OUT_CELL	
ad2_p[0]	175	IN_CELL		oeb_tsldclk[4]	40	IN_CELL	
ad2_p[1]	174	IN_CELL		tsldclk[4]	39	OUT_CELL	
ad2_p[2]	173	IN_CELL		oeb_tsldclk[3]	38	IN_CELL	
ad2_p[3]	172	IN_CELL		tsldclk[3]	37	OUT_CELL	

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Pin/ Enable	Register Bit	Cell Type	I.D. Bit	Pin/ Enable	Register Bit	Cell Type	I.D. Bit
dd2_p[0]	171	OUT_CELL		oeb_tsldclk[2]	36	IN_CELL	
dd2_p[1]	170	OUT_CELL		tsldclk[2]	35	OUT_CELL	
dd2_p[2]	169	OUT_CELL		oeb_tsldclk[1]	34	IN_CELL	
dd2_p[3]	168	OUT_CELL		tsldclk[1]	33	OUT_CELL	
ad3_p[0]	167	IN_CELL		tsld[4]	32	IN_CELL	
ad3_p[1]	166	IN_CELL		tsld[3]	31	IN_CELL	
ad3_p[2]	165	IN_CELL		tsld[2]	30	IN_CELL	
ad3_p[3]	164	IN_CELL		tsld[1]	29	IN_CELL	
dd3_p[0]	163	OUT_CELL		oeb_tldclk[4]	28	IN_CELL	
dd3_p[1]	162	OUT_CELL		tldclk[4]	27	OUT_CELL	
dd3_p[2]	161	OUT_CELL		oeb_tldclk[3]	26	IN_CELL	
dd3_p[3]	160	OUT_CELL		tldclk[3]	25	OUT_CELL	
ad4_p[0]	159	IN_CELL		oeb_tldclk[2]	24	IN_CELL	
ad4_p[1]	158	IN_CELL		tldclk[2]	23	OUT_CELL	
ad4_p[2]	157	IN_CELL		oeb_tldclk[1]	22	IN_CELL	
ad4_p[3]	156	IN_CELL		tldclk[1]	21	OUT_CELL	
dd4_p[0]	155	OUT_CELL		tld[4]	20	IN_CELL	
dd4_p[1]	154	OUT_CELL		tld[3]	19	IN_CELL	
dd4_p[2]	153	OUT_CELL		tld[2]	18	IN_CELL	
dd4_p[3]	152	OUT_CELL		tld[1]	17	IN_CELL	
b3e[4]	151	OUT_CELL		tohclk[4]	16	OUT_CELL	
b3e[3]	150	OUT_CELL		tohclk[3]	15	OUT_CELL	
b3e[2]	149	OUT_CELL		tohclk[2]	14	OUT_CELL	
b3e[1]	148	OUT_CELL		tohclk[1]	13	OUT_CELL	
rtoh[4]	147	OUT_CELL		tohfp[4]	12	OUT_CELL	
rtoh[3]	146	OUT_CELL		tohfp[3]	11	OUT_CELL	
rtoh[2]	145	OUT_CELL		tohfp[2]	10	OUT_CELL	
rtoh[1]	144	OUT_CELL		tohfp[1]	9	OUT_CELL	
rohfp[4]	143	OUT_CELL		ttoh[4]	8	IN_CELL	
rohfp[3]	142	OUT_CELL		ttoh[3]	7	IN_CELL	
rohfp[2]	141	OUT_CELL		ttoh[2]	6	IN_CELL	
rohfp[1]	140	OUT_CELL		ttoh[1]	5	IN_CELL	
rohclk[4]	139	OUT_CELL		ttohen[4]	4	IN_CELL	
rohclk[3]	138	OUT_CELL		ttohen[3]	3	IN_CELL	
rohclk[2]	137	OUT_CELL		ttohen[2]	2	IN_CELL	
rohclk[1]	136	OUT_CELL		ttohen[1]	1	IN_CELL	

Note

1. All oeb_ signals are active low enables for the respective signal names.

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16.2.1 Boundary Scan Cells

In the following diagrams, CLOCK-DR is equal to TCK when the current controller state is SHIFT-DR or CAPTURE-DR, and otherwise is unchanged. The multiplexer in the center of the diagram selects one of four inputs, depending on the status of select lines G1 and G2. The ID Code bit is as listed in the Boundary Scan Register table, Table 19.

Figure 19 Input Observation Cell (IN_CELL)

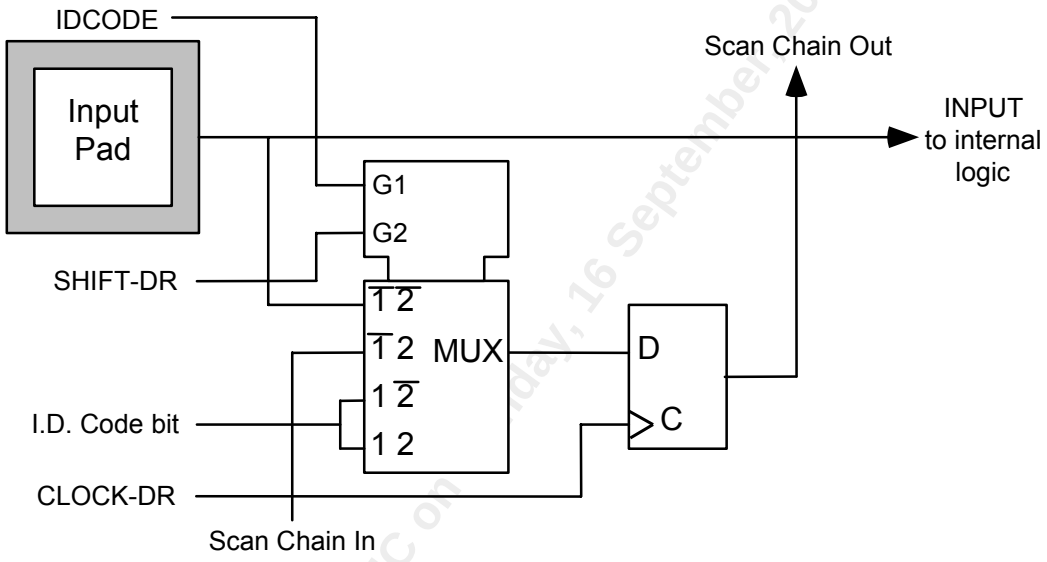

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Figure 20 Output Cell (OUT_CELL)

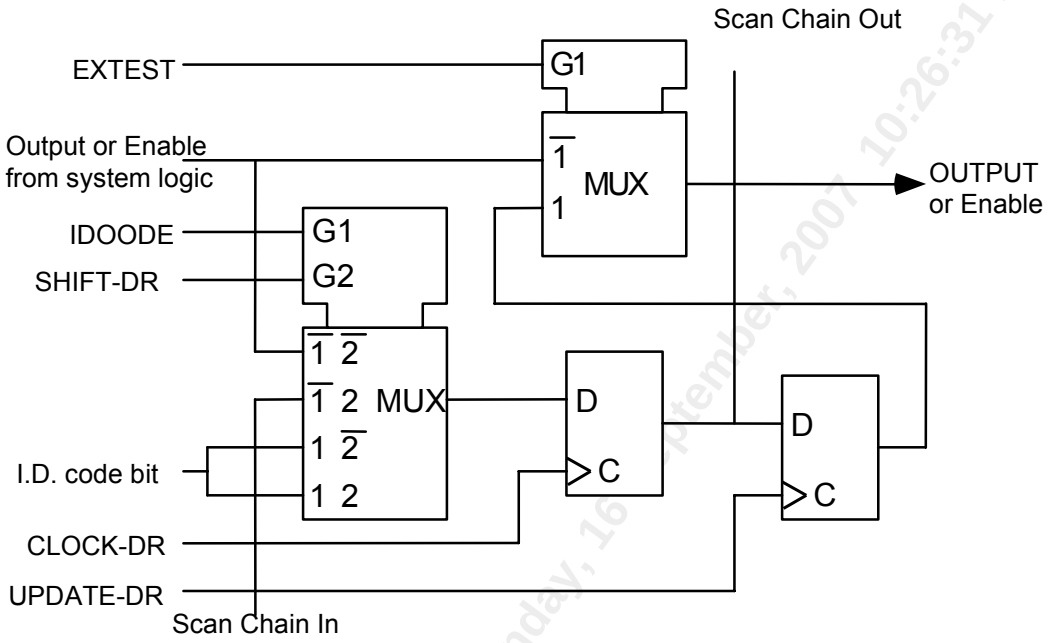

Figure 21 Bidirectional Cell (IO_CELL)

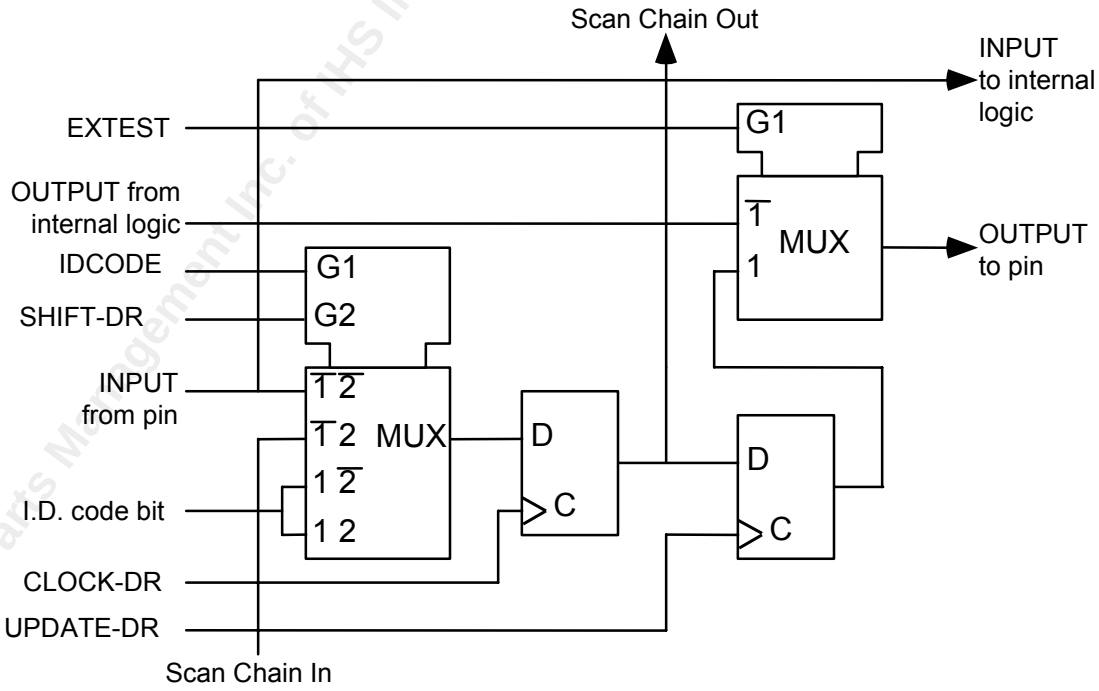

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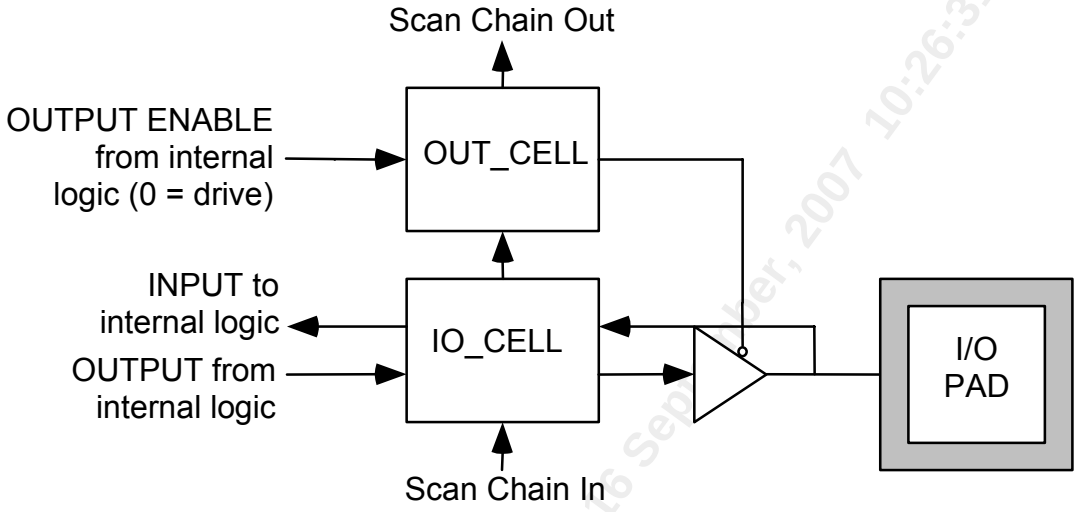
Figure 22 Layout of Output Enable and Bidirectional Cells



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17 Operations

The SPECTRA-9953 device is a SONET/SDH Payload Extractor and Aligner. It processes the section, line, path overhead of an STS-192/192c stream (STM-64/AU4-64c/AU4-16c/AU4-12c/AU4-8c/ AU4-4c/AU4/AU3/TU3) or quad STS-48/48c (STM-16/AU4-16c/AU4-12c/AU4-16c/AU4-8c/AU4-4c/AU4/AU3/TU3) streams. The SPECTRA-9953 supports a rich set of line, path, and system configuration options. This section provides details about operating the device.

17.1 Power Sequencing

The SPECTRA-9953 device uses four separate main power sources: VDDO, VDDI, AVDH, and AVDL. The device has one main set of analog and digital ground pins: VSS. Moreover, some analog blocks (CSU, DRU) have their own quiet power and ground pins (AVDH, AVDL, AVSH, AVSL, QAVD, QAVS).

The analog high power, AVDH, must be connected to a properly de-coupled +3.3 V supply. The analog low power, AVDL, must be connected to a properly de-coupled +1.8 V supply. The digital I/O power pins, VDDO, must be connected to a properly de-coupled +3.3 V supply. The digital core power, VDDI, must be connected to a properly de-coupled +1.8 V supply. The digital and analog power pins that are of the same supply voltage can be sourced from the same physical power supply source.

The ground pins can be connected to a common uninterrupted physical ground plane. All analog and digital power pins are to be de-coupled to the VSS ground. Each analog power pin is to be independently de-coupled to the ground plane.

The power-on sequence is as follows:

1. The 1.8 V supplies (VDDI, AVDL) can be brought up at the same time or after the 3.3 V supplies (VDDO, AVDH, CSU_AVDH) as long as the 1.8V supplies never exceed the 3.3V supplies by more than 0.3V.

20. Analog supplies must not exceed digital supplies of the same nominal voltage by more than 0.3V.

21. Data applied to I/O pins must not exceed VDDO by more than 0.3V unless the data is current-limited to 20 mA.

22. There are no power-up ramp rate restrictions.

23. The device must be powered down according to the same restrictions above.

1.

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17.2 Device Initialization

17.2.1 Device Reset

The reset pin of the SPECTRA-9953 device (RSTB – active low) should be asserted for at least 1 ms to initiate a complete initialization, or re-initialization, of the device. While RSTB is held low (logic 0) both the digital and the analog portions of the chip are being reset. During active hardware reset, the CSB input pin must be high.

Users may elect to reset the SPECTRA-9953 device using the register bits. This is accomplished by writing to the SPECTRA-9953 Master Configuration register, the SPECTRA-9953 Line Side Analog Control register, and the SPECTRA-9953 System side Analog Control register. For a global software reset, the Master configuration RESET bit should be set to 1 for at least 1 ms. To reset the digital core only, the master configuration RESET_CORE and RESETSL[4-1] should be set to 1. To reset the system side analog blocks, the system side analog control register SYS_ARB, R8TD_ARSTB and T8TE_ARSTB should be set to 0 for at least 1 ms. Finally to reset the line side analog blocks, the line side analog control register Line_ARST should be set to 1.

17.2.2 Register Initialization

There are several registers in the SPECTRA-9953 whose initial values must be overwritten for proper device functioning:

In the R8TD Analog Control 1 Register (20D3), the DRU_CTL[3:0] bits have a default value of 0000. However, for the DRUs to work properly, they must be written with 1101. This must be performed at all 16 R8TDs.

In the RHPPs and SHPIs, the Indirect Register 00 bit 4 should be written to 1 in order to be completely SONET compliant. This should be performed for all 12 indirent register loactions at each RHPP and SHPI.

17.2.3 Line-Side Re-Initialization

Several operations can lead to a floating or discontinuous clock coming from the Line Side Analog Interface (OIFs) to the digital core. These operations include Resetting the OIFs (Register 001DH bit 0), Disabling the OIFs (Register 001DH bit 5), toggling the quad2488 pin, or initiating the Line Side System Loopback (LSSLB). When any of these operations occur, the imperfect clock feeding the digital core may lead to ram corruption

After such operations, the user must rewrite all indirect registers in the rclk and tclk domains, i.e. all indirect registers in the TSVCA, THPP and RHPP. After this is done, the device is guaranteed to operate normally.

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17.2.4 DLL Reset

While the DLL should be transparent to the user in normal mode, if the sysclk input glitches, there is a possibility that the DLL will seize, and that the system side of the Spectra-9953 will not have the proper timings. For this reason, the DLL can be programmed to issue an interrupt in the event of errors (Register 004CH, bit 2). When such an interrupt occurs, DLL should be reset by writing to Register 004EH, after which the system side will operate normally.

17.3 Programming the SPECTRA-9953 Configuration Registers

The SPECTRA-9953 Receive and Transmit configuration registers are used to set each STS-12/STM-4 slice in one of the following modes:

- Mode 1: Master Slice Processing a Concatenated or Channelized STS-12/STM-4 SONET/SDH Stream. When processing a concatenated STS-12c/STM-4c, all TSB level payload configuration registers are ignored. When channelized STS-12/STM-4 streams are being processed, the functional block (TSB) level configuration registers are used to define the payload type that constitutes the STS-12/STM-4. Each TSB must be configured in this case.
- Mode 2: Slave Slice Processing Part of a Concatenated STS-N*12c. In this case, all TSB-level configuration registers are ignored.

17.4 Interrupt Service Routine

The SPECTRA-9953 device will assert INTB to logic 0 when a condition that is configured to produce an interrupt occurs. To find which condition caused this interrupt to occur, use the following procedure:

1. Read the registers 0020-002F to find the functional block(s) that caused the interrupt.

24. Find the register address of the corresponding block that caused the interrupt and read its Interrupt Status registers. The interrupt functional block and interrupt source identification register bits from step 1 are cleared once these register(s) have been read and the interrupt(s) identified.

25. Service the interrupt(s).

26. If the INTB pin is still logic 0, then there are still interrupts to be serviced and steps 1 to 3 need to be repeated. Otherwise, all interrupts have been serviced. Wait for the next assertion of INTB.

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17.5 Accessing Indirect Registers

Indirect registers are used to conserve address space in the SPECTRA-9953 device. Writing the indirect address register accesses indirect registers.For indirect register access, the clock for the TSB in question has to be running. The following is a summary of which clock needs to be running for each TSB's indirect register access.:

Table 20 Clocks for TSB Indirect Register Access

MODE	CLOCK	TSBs
OC-192	SYSCLK	SHPI, RSVCA, SARC
	RXCLK2	All: RHPP, RTTP_PATH, RTTP_SECTION
	TXCLK_SRC2	All TSVCA, THPP, TTTP_PATH, TTTP_SECTION
QUAD OC-48	SYSCLK	SHPI, RSVCA, SARC
	RXCLK1	STM16 #1: RHPP, RTTP_PATH, RTTP_SECTION
	RXCLK2	STM16 #2: RHPP, RTTP_PATH, RTTP_SECTION
	RXCLK3	STM16 #3: RHPP, RTTP_PATH, RTTP_SECTION
	RXCLK4	STM16 #4: RHPP, RTTP_PATH, RTTP_SECTION
	TX_CLK_SRC1	STM16 #1 TSVCA, THPP, TTTP_PATH, TTTP_SECTION
	TX_CLK_SRC2	STM16 #2 TSVCA, THPP, TTTP_PATH, TTTP_SECTION
	TX_CLK_SRC3	STM16 #3 TSVCA, THPP, TTTP_PATH, TTTP_SECTION
	TX_CLK_SRC4	STM16 #4 TSVCA, THPP, TTTP_PATH, TTTP_SECTION

The following steps should be followed for writing to indirect registers:

1. Read the BUSY bit. If it is equal to logic 0, continue to step 2. Otherwise, continue polling the BUSY bit.

27. Write the desired configurations for the channel into the indirect data registers.

28. Write the channel number (indirect address) to the indirect address register with RWB set to logic 0.

29. Read BUSY. Once it equals 0, the indirect write has been completed.

The following steps should be followed for reading indirect registers:

1. Read the BUSY bit. If it is equal to logic 0, continue to step 2. Otherwise, continue polling the BUSY bit.

30. Write the channel number (indirect address) to the indirect address register with RWB set to logic 1.

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31. Read the BUSY bit. If it is equal to logic 0, continue to 4. Otherwise, continue polling the BUSY bit.

32. Read the indirect data registers to find the state of the register bits for the selected channel number.

17.6 Using the Performance Monitoring Features

The performance monitor counters within the different blocks are provided for performance monitoring purposes. All performance monitor counters have been sized to not saturate if polled every second. The counters will saturate and not roll over if they reach their maximum value.

Writing can do a device update of all the counters to the SPECTRA-9953 Master Input Signal Activity, Accumulation Trigger register (002H). If this register is written to, the TIP bit in the SPECTRA-9953 Master Accumulation Transfer and Parity Error Interrupt Status register can be polled to determine when all the counter values have been transferred and are ready to be read.

17.7 Using The Section/Line Bit Error Rate Monitoring Features

The Bit Error Rate Monitor (SBER) block counts and monitors line BIP errors over programmable periods of time (window size). It can monitor to declare an alarm or to clear it if the alarm is already set. A different threshold must be used to declare or clear the alarm, whether or not those two operations are performed at the same BER. The following tables list the recommended content of the SBER registers for different speeds (STS-N) and error rates (BER). Both SBERs in the TSB are equivalent and are programmed similarly. In a normal application, they will be set to monitor different BER.

When the SF/SD CMODE bit is 1, this indicates that the clearing monitoring is recommended to be performed using a window size that is eight times longer than the declaration window size. When the SF/SD CMODE bit is 0 this indicates that the clearing monitoring is recommended to be performed using a window size equal to the declaration window size. In all cases the clearing threshold is calculated for a BER that is 10 times lower than the declaration BER, as required in the references. The tables indicate the declare BER, the evaluation period and the recommended CMODE and associated thresholds.

The saturation threshold is not listed in the table. It is programmed with the value 0xFFFFFF by default, deactivating saturation. Saturation capabilities are provided to allow the user to address issues associated with error bursts. It enables the user to determine a ceiling value at which the error counters will saturate, letting error bursts pass through within a frame or sub window period.

Since the monitoring algorithm is based on a pseudo-sliding window containing eight sub intervals, the time required to declare or clear an alarm can take up to nine sub-accumulation periods (SAP). The following tables thus consider that each SAP must take a value lower or equal to $1/9^{th}$ of the timing constraint, in frames.

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Table 21 Recommended SBER Settings for Different Data and BER Rates Using Telcordia Objectives

STS	Monitored Declare BER	Objective met for Switching Time (s)	SF/SD CMODE	SF/SD SAP (hex)	SF/SD DECTH (hex)	SF/SD CLRTH (hex)
48	10^{-3}	0.008	0	00000007	002116	000677
48	10^{-4}	0.008	0	00000007	0005F8	0000C1
48	10^{-5}	0.008	0	00000007	000095	000019
48	10^{-6}	0.063	0	00000037	000074	000014
48	10^{-7}	0.625	0	0000022B	000075	000014
48	10^{-8}	5.200	0	0000120E	000060	000011
48	10^{-9}	42.000	0	000091D5	00004C	00000F
192	10^{-3}	0.008	0	00000007	008547	00195E
192	10^{-4}	0.008	0	00000007	001860	0002D7
192	10^{-5}	0.008	0	00000007	000280	000053
192	10^{-6}	0.016	0	0000000E	000076	000014
192	10^{-7}	0.156	0	0000008A	000074	000014
192	10^{-8}	1.300	0	00000483	000060	000011
192	10^{-9}	10.400	0	0000241C	00004B	00000F

Table 22 Recommended SBER Settings for Different Data and BER Rates Using Telcordia and ITU Requirements

STS	Monitored Declare BER	Requirement met for Switching Time (s)	SF/SD CMODE	SF/SD SAP (hex)	SF/SD DECTH (hex)	SF/SD CLRTH (hex)
48	10^{-3}	0.01	0	00000008	0025A5	00077B
48	10^{-4}	0.10	0	0000002B	002554	000465
48	10^{-5}	1.00	0	00000192	00256F	000426
48	10^{-6}	10.00	0	00000F98	002570	000420
48	10^{-7}	100.00	0	00009BD6	002571	00041F
48	10^{-8}	1,000.00	0	00061647	002571	00041F
48	10^{-9}	10,000.00	0	003CDEAD	002571	00041F
192	10^{-3}	0.01	0	00000008	0097FA	001D2C
192	10^{-4}	0.10	0	0000002B	00970C	0010FD

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192	10^{-5}	1.00	0	00000192	009789	001004
192	10^{-6}	10.00	0	00000F98	00978F	000FEB
192	10^{-7}	100.00	0	00009BD6	009792	000FE9
192	10^{-8}	1,000.00	0	00061647	009793	000FE9
192	10^{-9}	10,000.00	0	003CDEAD	009793	000FE9

Important Note:

The **user should NOT** use CMODE = 1 mode when working with Telcordia or ITU requirements for the evaluation periods. In that case, the clearing time (eight times declare time) would not be conform to the requirements (where clearing time requirement = declare time requirement). For the same reason, the user should also avoid using CMODE = 1 with Telcordia objectives when dealing with STS-1 or any detection threshold = 10^{-3}.

The user should note that a probability of 99% was assumed as the probability that the switch initiation time (declaring) is below the Telcordia requirement. Since the Telcordia specification is vague regarding this issue (“must be very close to 1.0”), the approximation with 0.99 is sufficient and lets the Telcordia requirements be identical to the ITU requirements.

The user should also note that the Telcordia objectives are stricter than Telcordia and ITU requirements upon detection and clearing times. But Telcordia and ITU requirements are stricter than Telcordia objectives upon detection and clearing probability for a given BER (99% vs 95% for Telcordia objectives).

17.8 Using The Receive Trail trace Processor Features

The RTTP monitors a one-byte, 16-byte, or 64-byte trail trace message. To monitor a one-byte message, the ALGO register bits must be set to 11 (algo3). The trail trace byte is captured at address 40H. To monitor a 16-byte message, the ALGO register bits must be set to 01/10 (algo1/2) and the LENGTH16 register bit must be set to logic one. The trail trace message is captured between the 40H and 4FH addresses. To monitor a 64-byte message, the ALGO register bits must be set to 01/10 (algo1/2) and LENGTH16 register bit must be set to logic zero. The trail trace message is captured between the 40H and 7FH addresses.

When SYNC_CRLF is low, the synchronization is based on the MSB of the trail trace byte. Only one of the bytes has its MSB set high. The byte with its MSB set high is the first byte of the message. When SYNC_CRLF is high, the synchronization is based on the CR/LF (CR = 0Dh, LF = 0Ah) characters of the trail trace message. The byte following the CR/LF bytes is the first byte of the message.

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Figure 23 Layout of Output Enable and Bidirectional Cells

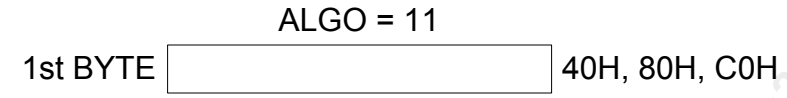

Figure 24 16-Byte Trail Trace Message, sync on MSB

Figure 25 16-byte Trail Trace Message, sync on CR/LF

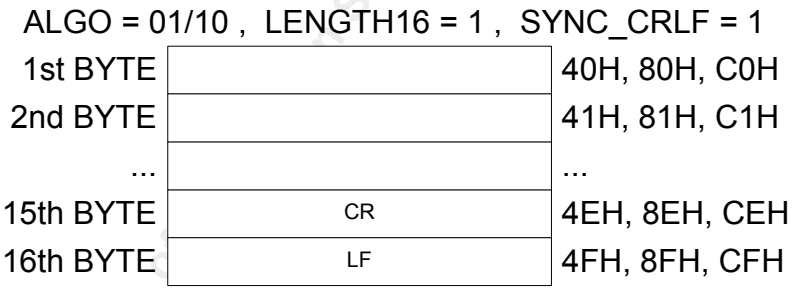

Figure 26 64-Byte Trail Trace Message, sync on MSB

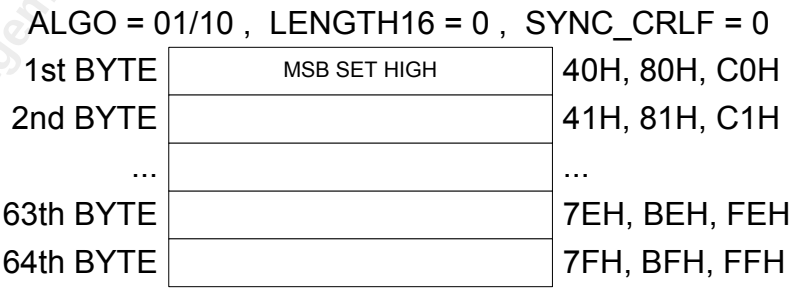

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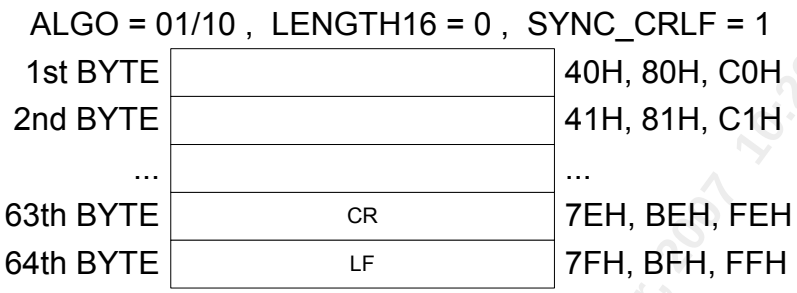
Figure 27 64-Byte Trail Trace Message, sync on CR/LF



To avoid declaring an unstable/mismatch defect when the transmitter updates the trail trace message, the RTTP considers an all zeros message to be matched. An all-zeros captured message in algorithm 1 and an all-zeros accepted message in algorithm 2 are not validated against the expected message but are considered match. That is, a match is declared when the captured or accepted message is all zeros regardless of the expected message. This feature can be turned off by setting the ZEROEN register bit to logic one.

Note: The transmitter is required to force an all zeros trail trace message when the trail trace message is updated.

17.9 Using the Transmit Trail trace Processor

The TTTP generates a one-byte, 16-byte, or 64-byte trail trace message. To generate a one-byte message, the BYTEEN register bit must be set to logic one. The trail trace byte is placed at address 40H. To generate a 16-byte message, the BYTEEN register bit must be set to logic zero and the LENGTH16 register bit must be set to logic one. The trail trace message is placed between the 40H and 4FH addresses. To generate a 64-byte message, both the BYTEEN and the LENGTH16 register bits must be set to logic zero. The trail trace message is placed between the 40H and 7FH addresses.

The trail trace message must include synchronization because the TTTP does not add synchronization to the message. The synchronization mechanism is different for a 16-byte message and for a 64-byte message. When the message is 16 bytes, the synchronization is based on the MSB of the trail trace byte. Only one of the 16 bytes has is MSB set high. The byte with its MSB set high is the first byte of the message. When the message is 64 bytes, the synchronization is based on the CR/LF (CR = 0Dh, LF = 0Ah) characters of the trail trace message. The byte following the CR/LF bytes is the first byte of the message.

Figure 28 64-Byte Trail Trace Message, sync on CR/LF

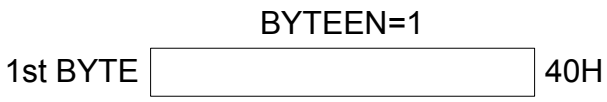


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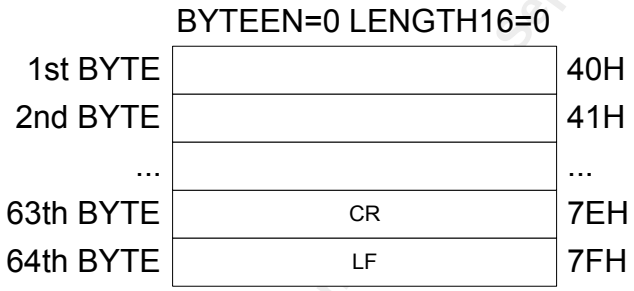
Figure 29 16-Byte Trail Trace Message

Figure 30 64-Bytes Trail Trace Message



To avoid generating an unstable/mismatch message, the TTTP can be configured (with the ZEROEN register bit) to generate an all-zeros trail trace message while the microprocessor updates the internal message. The enabling and disabling of the all-zeros message is not done on message boundary since the receiver is required to perform filtering on the message.

17.10 Using the SONET/SDH Alarm Controller Block

17.10.1 Received Section/Line Alarms

The Received Section/Line Alarm Block processes all the section and line defects detected by the overhead processor and generates the consequent action indications.

Three consequent action indications are defined:

- The receive section alarm (RSALM),
- The receive line AIS insertion (RLAISINS) and
- The transmit line RDI insertion (TLRDIINS) indications.

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Equation 1:

```
Alarm =   (OOF   AND  OOFEN          ) OR
          (LOF   AND  LOFEN          ) OR
          (LOS   AND  LOSEN          ) OR
          (LAIS  AND  LAISEN         ) OR
          (LRDI  AND  LRDIEN         ) OR
          (APSBF       AND  APSBFEN                ) OR
          (STIU  AND  STIUEN         ) OR
          (STIM  AND  STIMEN         ) OR
          (SDBER       AND  SDBEREN                ) OR
          (SFBER       AND  SFBEREN                )
```

RSALM: The RSALM indication is defined by Equation 1. The bits from and including OOFEN to SFBEREN in Register 00E3H: SARC Section RSALM Enable are register configuration bits that individually enable or disable each defect.

RLAISINS: The RLAISINS indication is defined by Equation 1. The bits from and including OOFEN to SFBEREN in Register 00E4H: SARC Section Receive AIS-L Insert Enable are register configuration bits that individually enable or disable each defect. The RLAISINS inserts L-AIS on the received transport overhead to be output on the RTOH port.

TLRDIINS: The TLRDIINS indication is defined by Equation 1. The bits from and including OOFEN to SFBEREN in Register 00E5H: SARC Section Transmit RDI-L Insert Enable are register configuration bits that individually enable or disable each defect. The TLRDIINS is the L-RDI returned to the far end device.

APS and BIP-L, TAPSINS and TLREIINS: The received filtered APS (K1,K2) bytes and the L-BIP are output on the receive ring control port (RRCP) and sent to the transmit side to optionally return the APS bytes and the L-REI to the far end device.

17.10.2 Received Path Alarm Block

The Received Path Alarm Block processes all path defects detected by the overhead processor and prepares the consequent action indications. Three consequent action indications are defined: the receive path alarm (RPALM, which is connected to chip output RALM), the receive path AIS insertion (RPAISINS), and the transmit path ERDI insertion (TPERDIINS[2:0]) indications.

The first step for generating consequent action indications is to monitor the ALLPAISC, PAIS, PAISC, PLOP, and PLOPC signals in order to generate PAISPTR and PLOPTR defects. With the PAISPTR and PLOPTR defects, the Receive Path Alarm Block can prepare the receive path alarm (RPALM), the receive path AIS insertion (RPAISINS), and the transmit path ERDI insertion (TPERDIINS[2:0]) indications.

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PAISPTR alarms are declared according to Equation 2. PAISPTRCFG[1:0] bits exist for each path. A path AIS defect is declared when the selected Equation 2 is true. A path AIS defect is removed when the selected Equation 2 is false. An interrupt is generated when a PAISPTR defect is declared and also when a PAISPTR defect is removed. For slave slices in concatenated payloads, the PAISPTRCFG[1:0] should be left at 00b.

Equation 2:

PAISPTRCFG[1:0]	PAISPTR
"00"	PAIS
"01"	PAIS or PAISC
"10"	PAIS and ALLPAISC
Others	'0'

PLOPTR alarms are declared according to Equations 3 and 4. A path LOP defect is declared when the selected Equation 4 is true. A path LOP defect is removed when the selected Equation 4 is false. An interrupt is generated when a PLOPTR defect is declared and also when a PLOPTR defect is removed. PLOPPTRCFG[1:0] bits exist for each path. Optionally, a PLOPTR defect can be terminated by a PAISPTR defect. The PLOPTREND bit is a register configuration bit that defines if PLOPTR is terminated by PAISPTR or not. A PLOPTREND bit exists for each path. When the PLOPTR is terminated by PAISPTR and this PAISPTR is true the PLOPTR is forced false, in any others case it takes PLOPTR_NOEND value. For slave slices in concatenated payloads, the PLOPTRCFG[1:0] should be left at 00b.

Equation 3:

PLOPTRCFG[1:0]	PLOPTR_NOEND
"00"	PLOP
"01"	PLOP or PLOPC
"10"	PLOP or PLOPC or PAIS or PAISC
Others	'0'

Equation 4:

PLOPTREND	PAISPTR	PLOPTR
'0'	Don't care	PLOPTR_NOEND
'1'	'0'	PLOPTR_NOEND
	'1'	'0'

The receive RPALM indication is defined by Equation 5. The bits from and including RSALMEN to PTIMEN in the Indirect Register 1H: SARC Path RPALM Enable Indirect Data (48 path) are register configuration bits that individually enable or disable each defect. The bits exist for each path. The RPALM is indicated on chip output RALM.

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Equation 5:

```
Alarm =   (RSALM      AND  RSALMEN              ) OR
          (MSRSALM    AND  MSRSALMEN    ) OR
          (PLOPTR     AND  PLOPTREN             ) OR
          (PAISPTR    AND  PAISPTREN            ) OR
          (PPLU  AND  PPLUEN        ) OR
          (PPLM AND  PPLMEN                 ) OR
          (PUNEQ      AND  PUNEQEN              ) OR
          (PPDI  AND  PPDIEN        ) OR
          (PRDI  AND  PRDIEN        ) OR
          (PERDIAND  PERDIEN                ) OR
          (PTIU  AND  PTIUEN        ) OR
          (PTIM  AND  PTIMEN        )
```

The RPAISINS indication is defined by Equation 6. The bits from and including RLAISINSEN to PTIMEN in the Indirect Register 2H: SARC Path Receive AIS-P Insert Enable Indirect Data (48 path) are register configuration bits that individually enable or disable each defect. The bits exist for each path. The RPAISINS is used to insert P-AIS on the receive SONET/SDH stream. PAIS is inserted by inserting an all-ones pattern on the H1-H2 and the SPE bytes. Optionally, it can be inserted on the transport overhead bytes.

Equation 6:

```
Alarm =   (RLAISINS     AND  RLAISINSEN    ) OR
          (MSRLAISINS AND  MSRLAISINSEN         ) OR
          (PLOPTR     AND  PLOPTREN             ) OR
          (PAISPTR    AND  PAISPTREN            ) OR
          (PPLU  AND  PPLUEN        ) OR
          (PPLM AND  PPLMEN                 ) OR
          (PUNEQ      AND  PUNEQEN              ) OR
          (PPDI  AND  PPDIEN        ) OR
          (PRDI  AND  PRDIEN        ) OR
          (PERDIAND  PERDIEN                ) OR
          (PTIU  AND  PTIUEN        ) OR
          (PTIM  AND  PTIMEN        )
```

The Path ERDI[2:0] insertion indication (PERDIINS) is defined in Table 23. A RDIEN bit exists for each path. P-ERDI alarms are used to generate the receive in-band P-RDI alarm. They are also used to return P-RDI to the far-end device.

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Table 23 Functional Description of Path ERDI (PERDIINS) Encoding

RDIEN	PLOPTR or PAISPTR	PUNEQ or PTIU or PTIM	PPLU or PPLM	Path ERDI[2:0] (PERDIINS)
0	1	Don't care	Don't care	101
	0	1	Don't care	110
		0	1	010
			0	001
1	1	Don't care	Don't care	100
	0	Don't care	Don't care	000

The Received Path Alarm Block individually detects each BIP-P when different of zero. The P-BIP is sent out on the RRCP port and fed back to the transmit side to be returned as REI-P to the far-end device.

17.10.3 Multiplexer Block

The Multiplexer Block determines the source of the APS, line RDI insertion indication (LRDIINS), line REI, path ERDI insertion indication (PERDIINS), and path REI defect indications to be inserted in the remote data stream.

When the ring control port is enabled (by setting the TLRCPEN register configuration for line signals and the TPRCPEN register configuration bit for path signals to one), the defect indications are sourced from the transmit ring control port. When the ring control port is disabled (by setting the the configuration bit to zero), the defect indications are sourced from the defects detected in receive data stream. The line and each path are controlled independently.

The Multiplexer Block also controls the persistency of the LRDI insertion indication (LRDIINS) and PERDI insertion indication (PERDIINS) in the transmit data stream.

When LRDI22 is set to one, a new line RDI insertion indication (LRDIINS) value must be persistent for at least 22 frames. When LRDI22 is set to zero, a new line RDI insertion indication (LRDIINS) value must be persistent for at least 12 frames.

When PERDI22 is set to one, a new path ERDI insertion indication (PERDIINS) value must be persistent for at least 22 frames. When PERDI22 is set to zero, a new path ERDI insertion indication (PERDIINS) value must be persistent for at least 12 frames.

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17.10.4 Add Transmit PAIS Block

The Add Transmit PAIS block processes the external Add bus alarms (TPAIS port) and the internal alarms declared by the either the 8B/10B decoder or the add pointer interpreter (TLOPTR, TPAISPTR). A consequent action is a transmitted path AIS insertion (TPAISINS). The first step to the generation of the consequent action indications is to monitor the TALLPAISC, TPAIS, TPAISC, TPLOP, and TPLOPC signals generated by the Add bus pointer interpreter and to generate TPAISPTR and TPLOPTR defects. With the TPAISPTR and TPLOPTR defects and the external TPAIS information, the Add Transmit PAIS Block can prepare the transmit path AIS insertion (TPAISINS).

In Register 00E7H: SARC Transmit Path Configuration, the TPAISPTRCFG[1:0] bit is the register configuration bit that defines the TPAISPTR defect. Only one TPAISPTRCFG[1:0] bit exists for 48 transmit paths. A transmit path alarm indication signal defect is declared when the selected Equation 7 is true. A transmit path alarm indication signal defect is removed when the selected Equation 7 is false. No interrupt is generated with this defect.

Equation 7:

TPAISPTRCFG[1:0]	TPAISPTR
“00”	TPAIS
“01”	TPAIS or TPAISC
“10”	TPAIS and TALLPAISC
Others	‘0’

Also in Register 00E7H: SARC Transmit Path Configuration, the TPLOPTRCFG[1:0] bit is the register configuration bit that defines the TPLOPTR_NOEND defect. Only one TPLOPPTRCFG[1:0] bit exists for 48 transmit paths. The TPLOPTR defect can be optionally terminated by a TPAISPTR defect.

The TPLOPTREND bit is the register configuration bit that defines if TPLOPTR is terminated by TPAISPTR or not. Only one TPLOPTREND bit exists for 48 transmit paths. When the TPLOPTR is terminated by TPAISPTR and this TPAISPTR is true the TPLOPTR is forced to false, in any others case it takes TPLOPTR_NOEND value. A transmit path loss of pointer defect is declared when the selected Equation 9 is true. A transmit path loss of pointer defect is removed when the selected Equation 9 is false. No interrupt is generated with this defect.

Equation 8:

TPLOPTRCFG[1:0]	TPLOPTR_NOEND
“00”	TPLOP
“01”	TPLOP or TPLOPC
“10”	TPLOP or TPLOPC or TPAIS or TPAISC
Others	‘0’

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Equation 9:

TPLOPTREND	TPAISPTR	TPLOPTR
'0'	Don't care	PLOPTR_NOEND
'1'	'0'	PLOPTR_NOEND
	'1'	'0'

The transmit path AIS TPAISINS insertion is defined by Equation 10. ADDPAISEN to TPAISPTREN "Indirect Register 3H: SARC Path Transmit AIS-P Insert Enable Indirect Data (48 path)" are register configuration bits that individually enable or disable each defect. The bits from and including ADDPAISEN to TPAISPTREN exist for each path.

Equation 10:

```
Alarm =     (TPAIS AND  ADDPAISEN          ) OR
            (TPLOPTR    AND  TPLOPTREN     ) OR

            (TPAISPTR   AND  TPAISPTREN    )
```

17.11 System Add bus "AFP" Synchronization.

Any CHESS™ chip set TSE/TBS/SPECTRA fabric can be viewed as a collection of "columns" of devices. A TST switch (see Figure 31) has five columns: one column consisting of the ingress flow from the load devices (e.g., a SPECTRA-9953 device); one column consisting of the ingress flow through the TBS devices; a column consisting of the TSE devices; and one column consisting of the egress flow through the load devices (e.g. a SPECTRA-9953 device). Note that the devices in columns 0 and 4 (1 and 3) are the same devices and the dual column references refer to their two separate simplex flows. STS-12 frames are pipelined through this structure in a regular fashion, under control of a single clock frequency (77.76 MHz). There are latencies between these columns, and these latencies may vary from path to path. The following design is used to accommodate these latencies.

A timing pulse for SONET frames (8 kHz, 125 µs) is generated and fed to each member of the CHESS™ chip set. Each CHESS™ chip has a *FrameDelay* register (AFPDLY), which contains the count of 77.76 MHz clock ticks that device should delay from the timing pulse before expecting the framing character of the STS-12 frame. The base timing pulse is called t. The delays from t based on the settings of the AFPDLY registers in the successive columns of CHESS™ chips are called $t_0, \ldots t_4$. The first signal, t_0, determines the start of an STS-12 frame. This signal is used to instruct the ingress load devices to start emitting an STS-12 frame (with its special "J0" control character) at that time. t_i is determined by the customer, based on device and wiring delays to be approximately the earliest time that all "J0" characters will have arrived in the ingress FIFOs of the t_i column of devices. t_i is selected to provide assurance that all "J0" characters have arrived. The i^{th} column of devices use the t_i signal to synchronize emission of the STS-12 frames.

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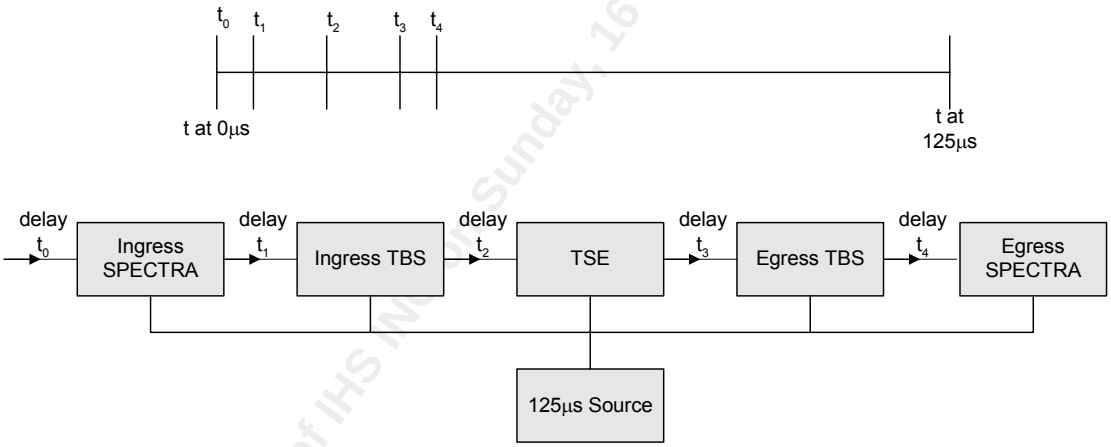
The ingress FIFOs permit a variable latency in AFP arrival of up to 16 clock cycles. That is, the largest tolerable delay between the slowest and fastest LVDS is 16 bytes. Consequently, the external system must ensure that the relative delays between all the 16 receive LVDS links be less than 16 bytes. The minimum value for the internal programmable delay (AFPDLY[13:0]) is the delay to the last (slowest) J0 character plus 20 bytes. The maximum value is the delay to the first (fastest) J0 character plus 36 bytes. The actual programmed delay should be based on the delay of the "slowest" of the 16 links – the link in which J0 arrives last plus a small safety margin of 1 or 2 words. The magnitude of the clock cycle delay is bounded by two parameters. First, the programmed delay register AFPDLY is 14 bits. This implies that a clock cycle delay of 2^{14}–1 or 16,383 clock cycles can be programmed. However, the second parameter, the frame rate (125 µs), bounds the delay to nearly one STS-12 frame or 9718 (9719 unique values but 0 is the value for no delay) clock cycles (125 µs x 77.76 MHz), after which the next SONET frame begins.

Figure 31 "AFP" Synchronization Control



17.12 HPT Mode Considerations

When the SHPI is set to bypass mode (does not interpret the incoming H1/H2/H3) there are several performance considerations with respect to the SHPI and PAIS relaying:

1. When the System Diagnostic Loopback (SDLB) is enabled, the PAIS characters are not relayed to the Drop Bus, but the all-ones pattern is still present in the H1/H2/H3 bytes and the SPE bytes. In order to reliably detect PAIS on the system side of a downstream SPECTRA-9953 or other PMC-Sierra framer device, the pointer interpreter blocks (SHPI) must be enabled.

33. Add bus PAIS characters are not relayed consistently to the transmit line. However, this is only an issue if the SHPI is disabled, as an enabled pointer processor can detect the all-ones patterns in the H1/H2 bytes and relay the PAIS reliably.

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34. Similarly, when the SSLLB is enabled, PAIS characters are not consistently relayed to the Transmit line. In this case, the SHPI can be disabled as long as the RSVCA DiagTOHAIS (Indirect Register 02H bit 6) is set to Logic 1 to correctly assert the PAIS Telecom bus signal throughout the TOH. Otherwise, PAIS may be incorrectly removed for a single frame at the TSVCA.

35. When an Out of Frame Alignment (OFA) condition occurs in the R8TD, the block can optionally set the payload to all 1s. However, the PAIS Telecombus signal is not set. Therefore, if the SHPI is disabled, PAIS will not be relayed to the Transmit Line. Again, enabling the SHPI prevents this condition. Alternately, an interrupt can be generated from the R8TD and AIS can be manually inserted at the TSVCA Using the Diag_PAIS bit.

36. The R8TD also shows the H3 byte as being part of the payload when in PAIS. When the SHPI is disabled, the payload indication signal passes through the SHPI to the TSVCA, whose FIFO will overflow due to what it perceives as constant incoming negative pointer justifications. Also, the TSVCA will insert PAIS due to this overflow, meaning that PAIS will be inserted in the Transmit Line even if its insertion is not enabled in the SARC with TPAISPRTEN. Enabling the SHPI prevents this condition as the payload signal will be regenerated, and no “negative justifications” will be seen at the TSVCA. Alternately, the Diag_FifoAisDis in TSVCA Indirect register 02H can disable the insertion of AIS due to FIFO overflows/underflows.

17.13 SVCA Reconfiguration Considerations

When an SVCA (TSVCA or RSVCA) undergoes a reconfiguration, (from top-level registers or via SVCA Normal Register 02H) there is a possibility that its indirect registers will be corrupted and consequently that data integrity will be lost. To avoid such a situation, before the reconfiguration, the contents of Indirect Register 02H should be read and stored, and after the reconfigureation, the contents should be written back to Indirect Register 02H. This way, data corruption can be avoided.

17.14 JTAG Support

The SPECTRA-9953 device supports the IEEE Boundary Scan specification as described in the IEEE 1149.1 standards. The Test Access Port (TAP) consists of the five standard pins: TRSTB, TCK, TMS, TDI and TDO. These are used to control the TAP controller and the boundary scan registers. The TRSTB input is the active-low reset signal used to reset the TAP controller. TCK is the test clock used to sample data on input, TDI and to output data on output, TDO. The TMS input is used to direct the TAP controller through its states. The basic boundary scan architecture is shown in .

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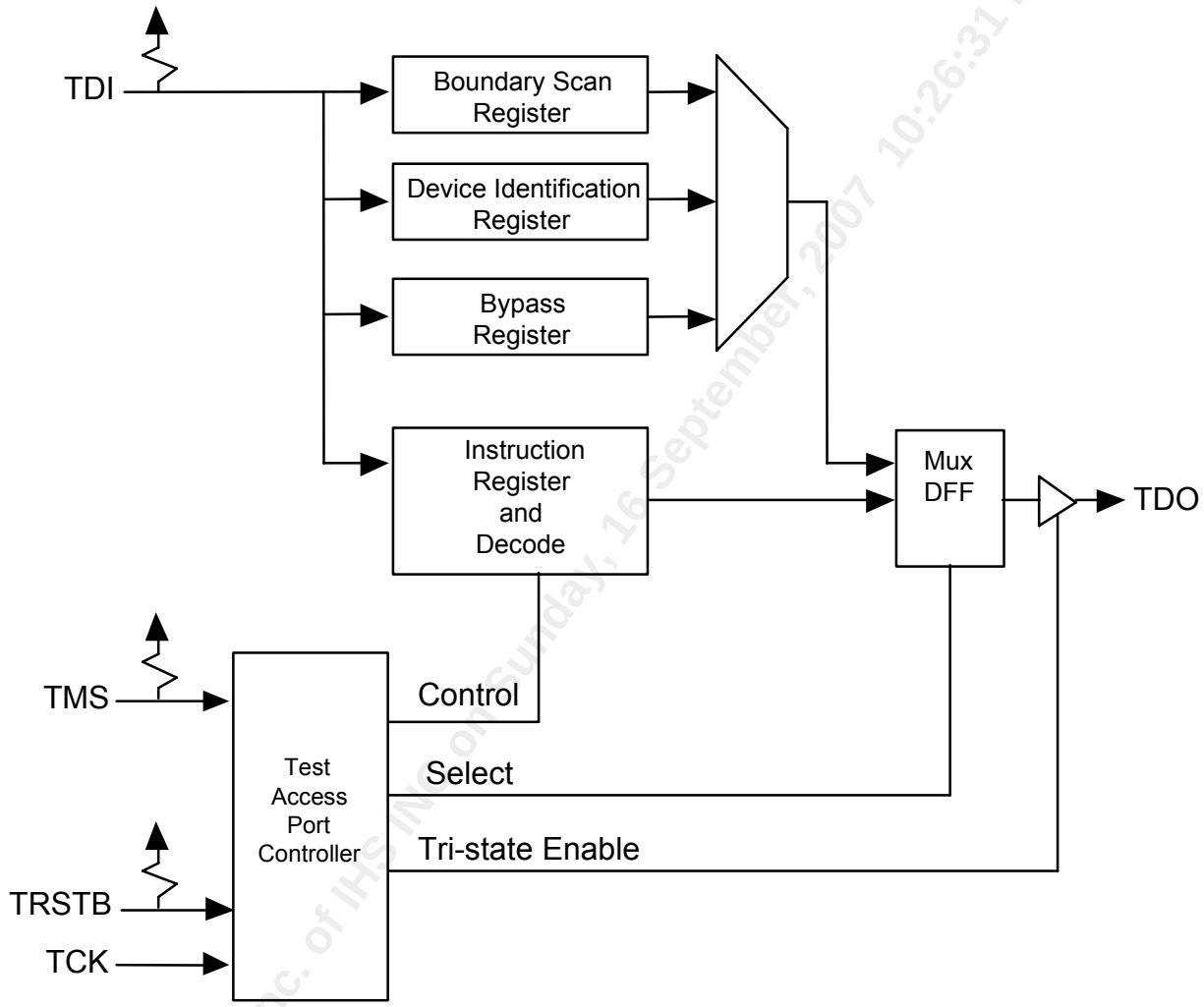
Figure 32 Boundary Scan Architecture



The boundary scan architecture consists of a TAP controller, an instruction register with instruction decode, a bypass register, a device identification register, and a boundary scan register. The TAP controller interprets the TMS input and generates control signals to load the instruction and data registers. The instruction register with instruction decode block is used to select the test to be executed and/or the register to be accessed. The bypass register offers a single-bit delay from primary input, TDI to primary output, TDO. The device identification register contains the device identification code.

The boundary scan register allows testing of board inter-connectivity. The boundary scan register consists of a shift register place in series with device inputs and outputs. Using the boundary scan register, all digital inputs can be sampled and shifted out on primary output, TDO. In addition, patterns can be shifted in on primary input, TDI and forced onto all digital outputs.

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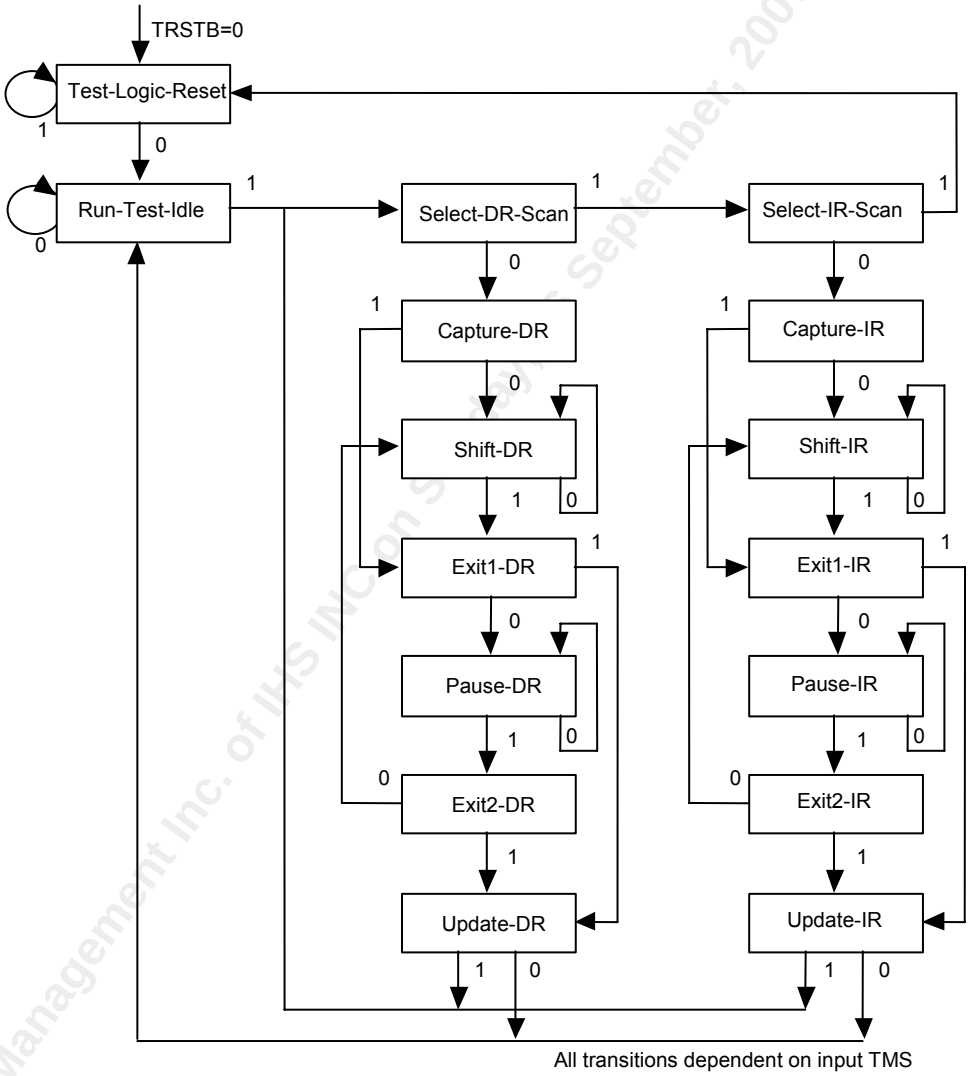
17.14.1 TAP Controller

The TAP controller is a synchronous finite state machine clocked by the rising edge of primary input, TCK. All state transitions are controlled using primary input, TMS. The finite state machine is described below.

Figure 33 TAP Controller Finite State Machine



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17.14.2 States

Test-Logic-Reset

The test logic reset state is used to disable the TAP logic when the device is in normal mode operation. The state is entered asynchronously by asserting input, TRSTB. The state is entered synchronously regardless of the current TAP controller state by forcing input, TMS high for five TCK clock cycles. While in this state, the instruction register is set to the IDCODE instruction.

Run-Test-Idle

The run test/idle state is used to execute tests.

Capture-DR

The capture data register state is used to load parallel data into the test data registers selected by the current instruction. If the selected register does not allow parallel loads or no loading is required by the current instruction, the test register maintains its value. Loading occurs on the rising edge of TCK.

Shift-DR

The shift data register state is used to shift the selected test data registers by one stage. Shifting is from MSB to LSB and occurs on the rising edge of TCK.

Update-DR

The update data register state is used to load a test register's parallel output latch. In general, the output latches are used to control the device. For example, for the EXTEST instruction, the boundary scan test register's parallel output latches are used to control the device's outputs. The parallel output latches are updated on the falling edge of TCK.

Capture-IR

The capture instruction register state is used to load the instruction register with a fixed instruction. The load occurs on the rising edge of TCK.

Shift-IR

The shift instruction register state is used to shift both the instruction register and the selected test data registers by one stage. Shifting is from MSB to LSB and occurs on the rising edge of TCK.

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Update-IR

The update instruction register state is used to load a new instruction into the instruction register. The new instruction must be scanned in using the Shift-IR state. The load occurs on the falling edge of TCK.

The Pause-DR and Pause-IR states are provided to allow shifting through the test data and/or instruction registers to be momentarily paused.

Boundary Scan Instructions

The following is a description of the standard instructions. Each instruction selects a serial test data register path between input, TDI and output, TDO.

17.14.3 Instructions

BYPASS

The bypass instruction shifts data from input, TDI to output, TDO with one TCK clock period delay. The instruction is used to bypass the device.

EXTEST

The external test instruction allows testing of the interconnection to other devices. When the current instruction is the EXTEST instruction, the boundary scan register is place between input, TDI and output, TDO. Primary device inputs can be sampled by loading the boundary scan register using the Capture-DR state. The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state. Primary device outputs can be controlled by loading patterns shifted in through input TDI into the boundary scan register using the Update-DR state.

SAMPLE

The sample instruction samples all the device inputs and outputs. For this instruction, the boundary scan register is placed between TDI and TDO. Primary device inputs and outputs can be sampled by loading the boundary scan register using the Capture-DR state. The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state.

IDCODE

The identification instruction is used to connect the identification register between TDI and TDO. The device's identification code can then be shifted out using the Shift-DR state.

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STCTEST

The single transport chain instruction is used to test out the TAP controller and the boundary scan register during production test. When this instruction is the current instruction, the boundary scan register is connected between TDI and TDO. During the Capture-DR state, the device identification code is loaded into the boundary scan register. The code can then be shifted out output, TDO using the Shift-DR state.

17.15 Board Design Recommendations

17.15.1 Power Supply Filtering

1.8V and 3.3V supplies for the SPECTRA-9953 device require 5% tolerance. RC filtering is required for all analog power pins as shown in Figure 1 below.

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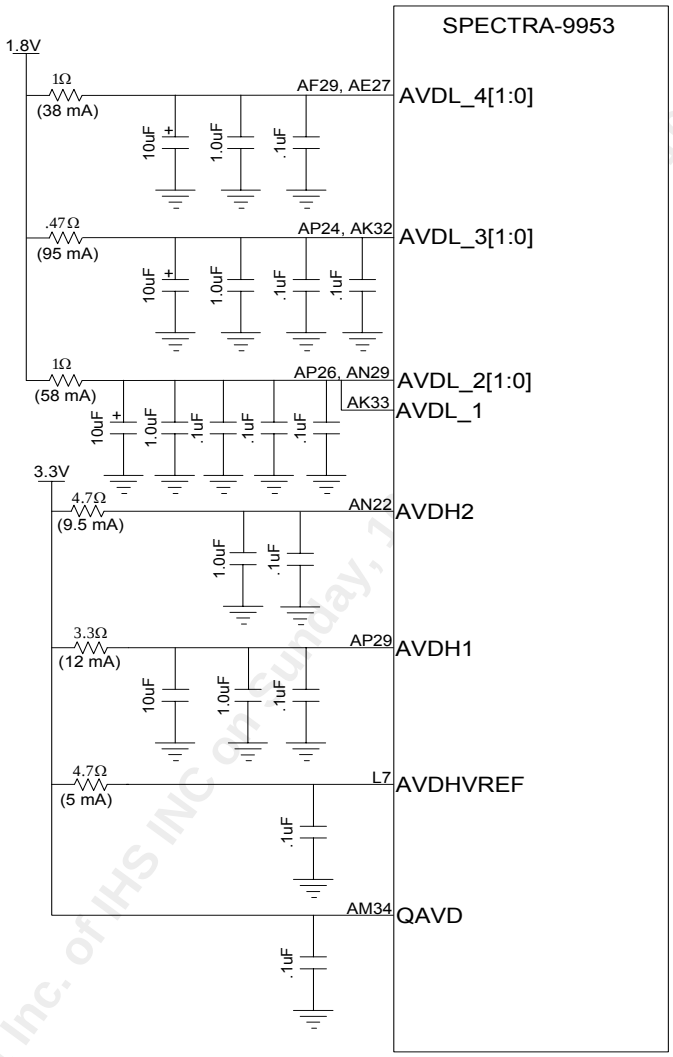
Figure 34 SPECTRA-9953 Analog Power Filtering



RC filtering is used for all analog power pins. Ideally, each physical cluster of power pins should have a 0.1uF high-frequency capacitor as close as possible to it. For example, on AVDL4, a 0.1uF capacitor should be used for [AF29, AE27] cluster while another 0.1uF capacitor should be used for AVDL3 [AP24, AK32]. Larger tantalum caps can be located conveniently close to the SPECTRA-9953 chip.

The analog ground pins, QAVS, AVSL and AVSH, and digital ground pins, VSS[299..0], should be connected to the common ground plane.

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Decoupling recommendations for VDDO and VDDI are as follows: 0.1µF capacitors for every four VDDI power pins as layout allows and eight 22 µF low ESR tantalum capacitors for bulk decoupling. 0.1µF capacitors for every three VDDO power pins as layout allows and four 22 µF low ESR tantalum capacitors for bulk decoupling. All 0.1µF decoupling capacitors should be positioned as close to the pins as possible to reduce the series inductance connecting the capacitor to the pin. Tantalum capacitors can be conveniently located around the device.

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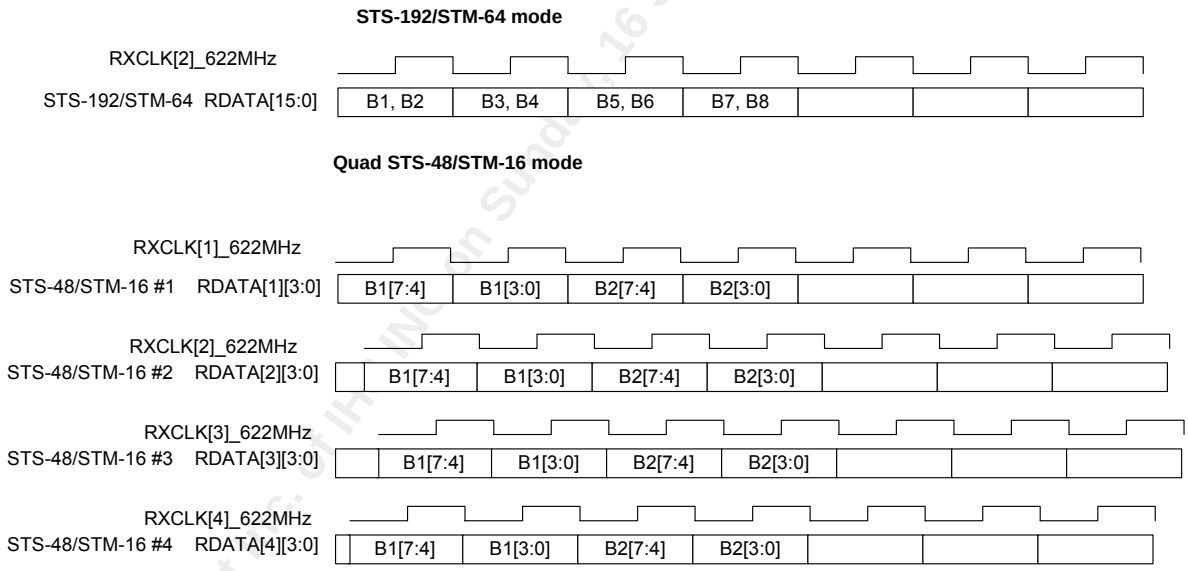
18 Functional Timing

18.1 Line Interface Functional Timing

The SPECTRA-9953 device complies with the OIF STS-192/STM-64 SERDES Interface Revision 3.1. When the SPECTRA-9953 is used to process an STS-192/STM-64 SONET/SDH stream, the RXDATA/TXDATA bus carries two bytes and is sampled/updated on the rising edge of the RXCLK[2]/TXCLK[2]. When four STS-48/STM-16 are processed, each RXDATA[N][3:0]/TXDATA[N][3:0] carries a nibble and is sampled/updated on the rising edge of the RXCLK[N]/TXCLK[N]. Figure 35 shows as an example the functional timings of the receive line side.

Figure 35 SPECTRA-9953 Line Interface Functional Timing



Transmit line interface input and output framing pulses are considered asynchronous. An internal low speed clock (77.76 MHz) is used to detect a rising edge on TXFPI[N] and to update TXFPO[N]. TXFPI[N] rising edge is detected and used to force an outgoing framing pulse on the corresponding Aligner (SVCA). TXFPO[N] is driven high for one internal 77.76 MHz clock to indicate the approximate position of the first framing byte (A1). As shown in Figure 36, TXFPO is asserted high for approximately eight TXCLK clock cycles when processing an STS-192/STM-64 stream to indicate the first 16 bytes of the SONET/SDH frame (A1 bytes).

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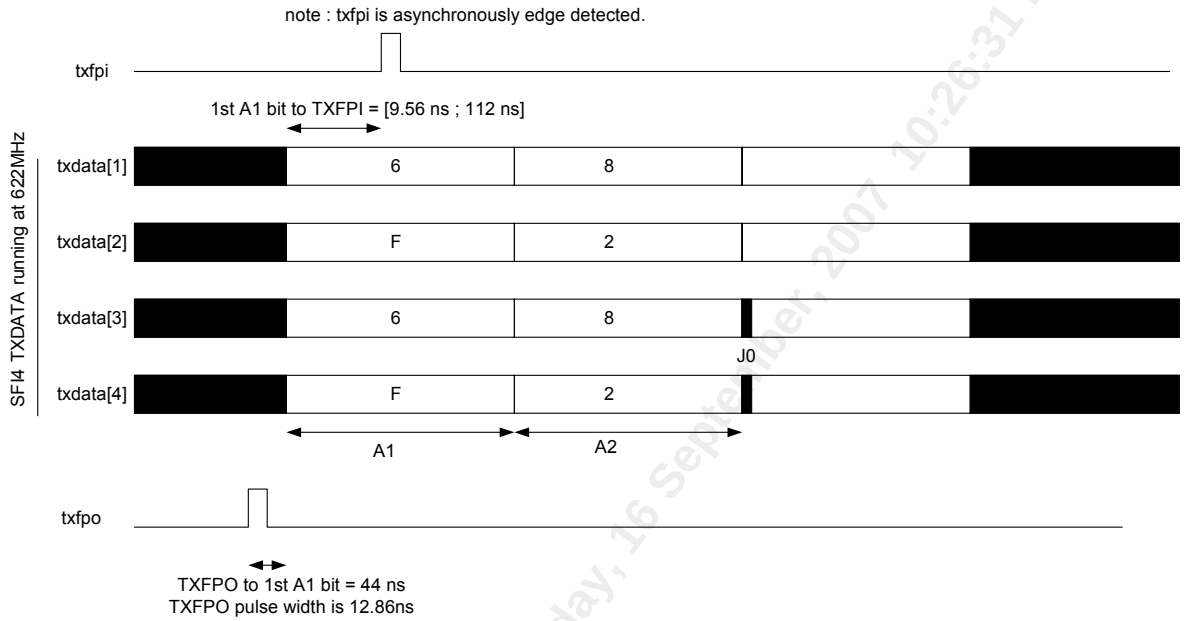
Figure 36 TXFPI/TXFPO Functional Timing



18.2 System Add Interface

Figure 30 shows the relative timing of the add system interface. The LVDS links carry SONET/SDH frame octets that are encoded in 8B/10B characters. Frame boundaries, justification events, and alarm conditions are encoded in special control characters. The upstream devices sourcing the links share a common clock and have a common transport frame alignment that is synchronized by the Add Serial Interface Frame Pulse signal (AFP). Due to phase noise from clock multiplication circuits and backplane routing discrepancies, the links will not phase aligned to each other will be frequency locked The delay from AFP being sampled high to the first and last J0 character is shown in Figure 37. In this example, the first J0 is delivered on link ADX[N]. The delay to the last J0 represents the time when the all the links have delivered their J0 character. In the example below, link ADY[M] is shown to be the slowest. The minimum value for the internal programmable delay (AFPDLY[13:0]) is the delay to the last J0 character plus 20. The maximum value is the delay to the first J0 character plus 36. Consequently, the external system must ensure that the relative delays between all the add LVDS links be less than 16 bytes. The relative phases of the links in Figure 37 are shown for illustrative purposes only. Links may have different delays relative to other links than what is shown.

Also note that changes to AFPDLY[13:0] will only take effect after an AFP pulse has been received, (and while AFP_DISABLE is not set to 1).

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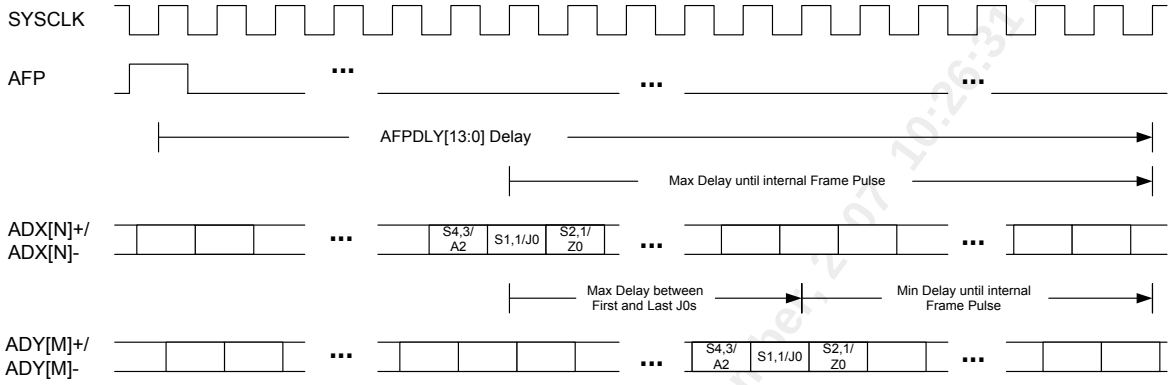
Figure 37 Add System Bus Functional Timing

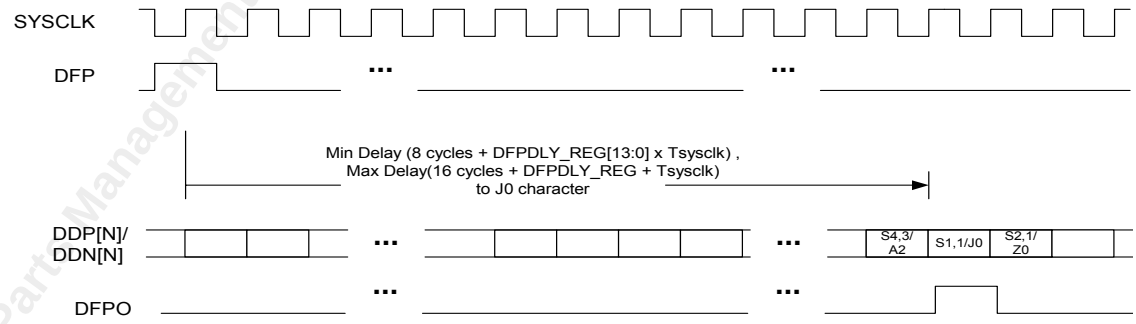


18.3 System Drop Interface Timing

Figure 38 shows the delay from assertion of DFP to the drop serial data links. Due to the presence of FIFOs in the data path, the maximum delay to the J0 character being output on the serial drop lines is 16 SYSCLK cycles. The minimum delay is eight SYSCLK cycles. DFPO is asserted high to indicate the J0 character emission on the Drop bus. DFPO may pulse more than once if the delay between J0s emission is more than two bytes. In order to align the 16 links, the T8TE center bit may be used upon system startup. An internal software delay register (DFPDLY_REG[13:0]) is used to internally delay the external DFP pulse, thus delaying the emission of the J0 characters on the serial Drop bus.

Also note that changes to DFPDLY[13:0] will only take effect after a DFP pulse has been received, (and while DFP_DISABLE is not set to 1).

Figure 38 Drop System Interface Timing



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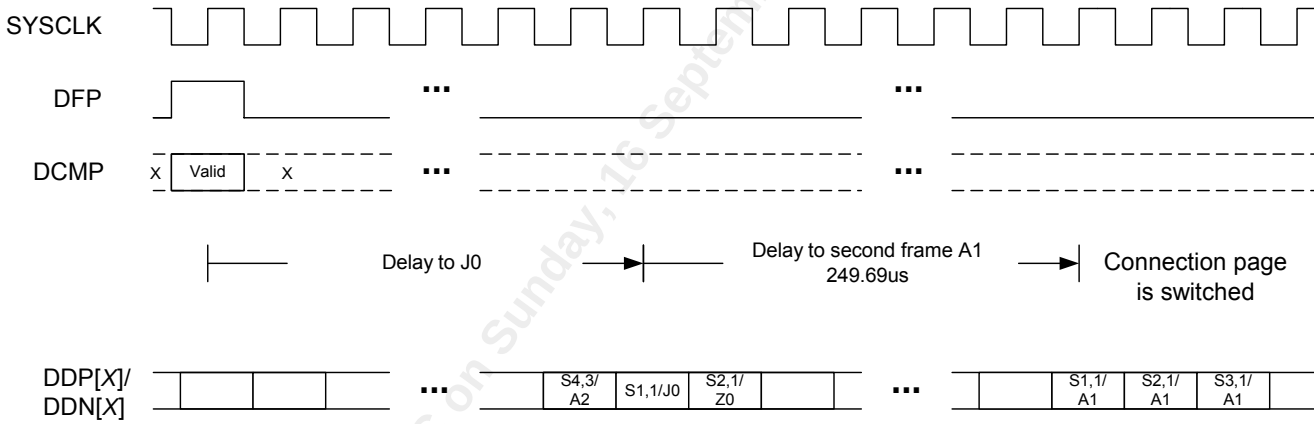
18.4 System ACMP/DCMP Timing

Figure 39 shows the delay from DCMP/ACMP to the drop/add serial data links. DCMP/ACMP is valid only at the DFP/AFP pulse time and are ignored at all other locations in the transport frame. A change in value to the connection memory page signal (CMP) results in changing the active space slot interchange settings. Given that CMP is sampled on the DFP/AFP pulse time 0, the first data that is switched according to the newly selected connection memory page are the A1 bytes of the second frame following the first J0 byte dropped/added by/to the SPECTRA-9953. The time to the ASSI/DSSI page change is therefore afp/dfp_delay + 249.69µs.

Figure 39 CMP Functional Timing



18.5 Receive Transport Overhead Port Timing (RTOH)

The SPECTRA-9953 extracts and serially outputs all the transport overhead bytes (defined and undefined) on the RTOH ports. 10368 bits (9x3x48 bytes) are output on each RTOH[N] between two ROHFP assertion. Figure 40 shows the receive transport overhead (RTOH) functional timings. ROHCLK[1:4] is a nominal 82.94MHz clock generated by gapping a 103.68MHz clock. The gapping occurs after the fourth bit 7 has been serialized out on the RTOH port for each group of 4 bytes. This gap is eight 103.68 MHz clock periods wide. All RTOH outputs (RTOH[N], ROHFP[N]) are updated on the rising edge of ROHCLK[N]. The rising edge of ROHCLK[N] should be used to sample RTOH[N] and ROHFP[N]. Sampling ROHFP[N] high identifies the MSB of the first A1 Byte on RTOH. It should be noted that Figure 40 uses STS-1 ordering that is internal to SPECTRA-9953 and does not correspond exactly to the Bellcore STS-1 ordering found in Figure 7.

When processing an STS-192/STM-64 or a quad STS-48/STM-16 data stream, the following multiplexing structure is used :

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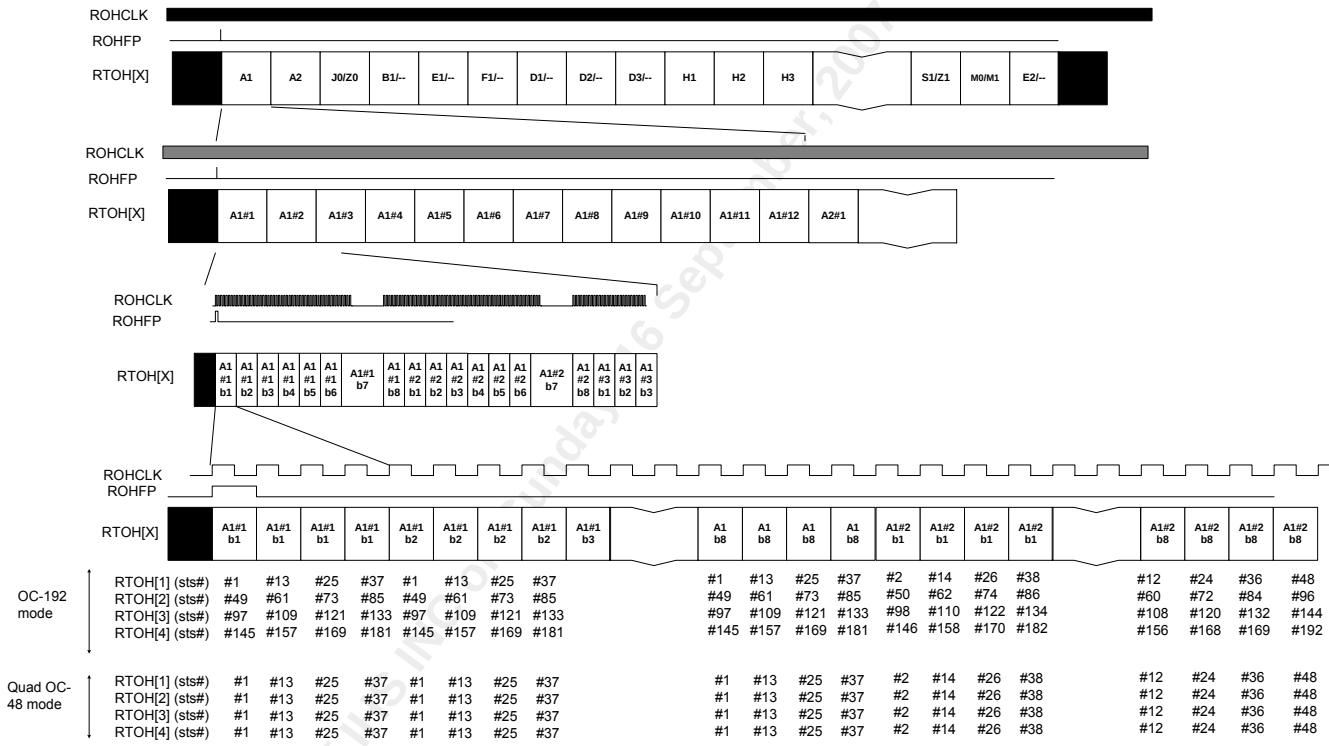
RTOH[1] bit-wise multiplexes the transport overhead bytes from slices [1,1] [1,2] [1,3] [1,4].
RTOH[2] bit-wise multiplexes the transport overhead bytes from slices [2,1] [2,2] [2,3] [2,4].
RTOH[3] bit-wise multiplexes the transport overhead bytes from slices [3,1] [3,2] [3,3] [3,4].
RTOH[4] bit-wise multiplexes the transport overhead bytes from slices [4,1] [1,2] [1,3] [4,4].

Figure 40 Receive Transport Overhead Description



18.6 Transmit Transport Overhead Port Timing (TTOH)

The function of the transmit transport overhead S/P block is to serially input from the TTOH port all the transport overhead (TOH) bytes to be inserted in the current transmit frame. The TOH bytes must be input from TTOH in the same order that they are transmitted (A1, A2, J0/Z0, B1, E1, F1, D1-D3, H1-H3, B2, K1, K2, D4-D12, S1/Z1, M1/Z2 and E2). The multiplexing structure is the same as the RTOH port (refer to Figure 40).

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TOHCLK[4:1] are the generated output clocks used to provide timing for the TTOH[4:1] input, the TTOHEN[4:1] inputs, and the TOHFP[4:1] output. TTOHCLK is a nominal 82.94 MHz clock generated by gapping a 103.68 MHz clock. As opposed to ROHCLK[4:1], the TOHCLK[4:1] clocks are gapped between the 8th and 1st bits of the TTOH bytes. This gap is eight 103.68 MHz clock periods wide. Sampling TOHFP high with the rising edge of TOHCLK identifies the MSB of the first A1 byte on TTOH. TTOH and TTOHEN data should be externally aligned with the falling edge of TOHCLK. TTOHEN is used to validate, on a byte per byte basis, the byte insertion from the TTOH port. When TTOHEN is sampled high on the serial byte, the serial byte is to be inserted. When TTOHEN is sampled high on the MSB of the TTOH serial byte (i.e. the first serial bit), the byte is inserted in the transport overhead. When TTOHEN is sampled low on the MSB of the TTOH serial byte, the byte is discarded.

18.7 Receive DCC Port Timing (RDCC)

The function of the receive section and line RDCC block is to serially output the DCC bytes onto RLD and RSLD. The line DCC bytes (D1-D3) are output serially onto RLD. RSLD is selectable to output either the section DCC bytes (D4-D12) or the line DCC bytes (D1-D3). The RRMP RSLDSEL register bit selects which of the two sources is multiplexed onto RSLD.

Figure 33 shows the RDCC port functional timings. RLDCLK is the generated output clock used to provide timing for the RLD output. RLDCLK is a nominal 576 kHz clock. RSLDCLK is the generated output clock used to provide timing for the RSLD output. If RSLD carries the line DCC, RSLDCLK is a nominal 576 kHz clock or if RSLD carries the section DCC, RSLDCLK is a nominal 192 kHz clock. Sampling ROHFP high identifies the MSB of the first DCC byte on RLD (D4) and RSLD (D1 or D4). RLD and RSLD are aligned with the falling edge of RLDCLK and RSLDCLK and should be sampled on the rising edge of RLDCLK and RSLDCLK. Note that when TST-192/STM-64 mode is enabled RDCC ports 2-4 should be ignored.

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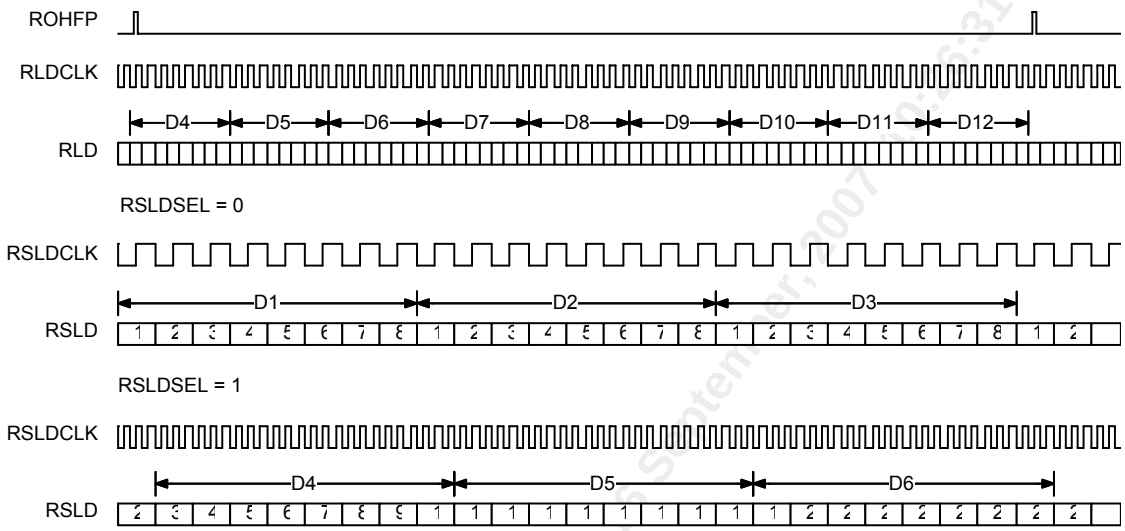
Figure 41 RDCC Port Functional Timing



18.8 Transmit DCC Port Timing (TDCC)

The function of the transmit section and line TDCC block is to serially input from the TLD and the TSLD ports the DCC bytes to be inserted in the next transmit frame. The line DCC bytes (D4-D12) are input from TLD. TSLD is selectable to input either the section DCC bytes (D4-D12) or the line DCC bytes (D1-D3). The TRMP TSLDSEL register bit selects which of the two inputs is multiplexed onto TSLD.

Figure 29 shows the TDCC functional timings. TLDCLK is the generated output clock used to provide timing for the TLD input. TLDCLK is a nominal 576 KHz clock. TSLDCLK is the generated output clock used to provide timing for the TSLD input. If TSLD carries the line DCC, TSLDCLK is a nominal 576 KHz clock or if TSLD carries the section DCC, TSLDCLK is a nominal 192 KHz clock. Sampling TOHFP high identifies the MSB of the first DCC byte on TLD (D4) and TSLD (D1 or D4). TLD and TSLD data should be externally aligned with the falling edge of TLDCLK and TSLDCLK. When STS-192/STM-64 mode active, TDCC ports 2-4 are ignored.

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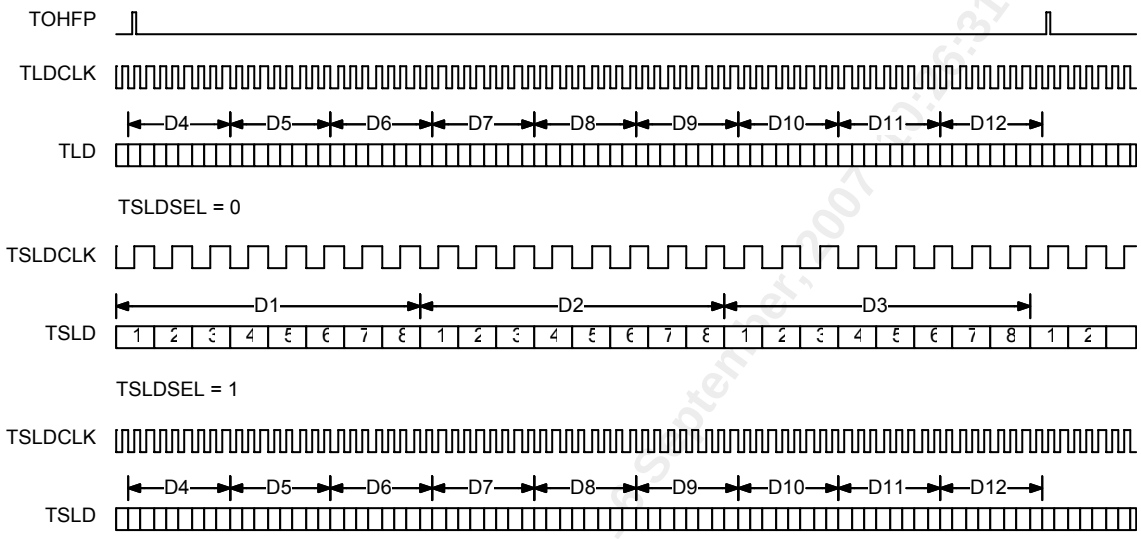
Figure 42 TDCC Functional Timing



18.9 B3E Port Functional Timing

The path bit interleaved parity error (B3E) is asserted high for each path BIP-8 error detected in the received payload. B3E[4:1] multiplexes the 192 paths BIP-8 errors according the multiplexing format shown in Figure 43. Up to eight B3E errors can be generated per STS-1 per frame when the configuration register bit B3EBLK=0. When B3EBLK=1, only one B3E is generated per STS-1 per frame. Each processing slice generates the B3E errors for 12 paths. Four processing slices are bit-wise multiplexed to generate the stream shown in Figure 43. For each STS-1, there are 3 opportunities within each frame where the B3E count can be generated. Any one error can never appear at more than one opportunity, thus eliminating the possibility of counting the error twice.

B3E[4:1] is updated on the rising edge of ROHCLK[4:1]. Sampling ROHFP[N] high identifies the B3E of the first path in the group.

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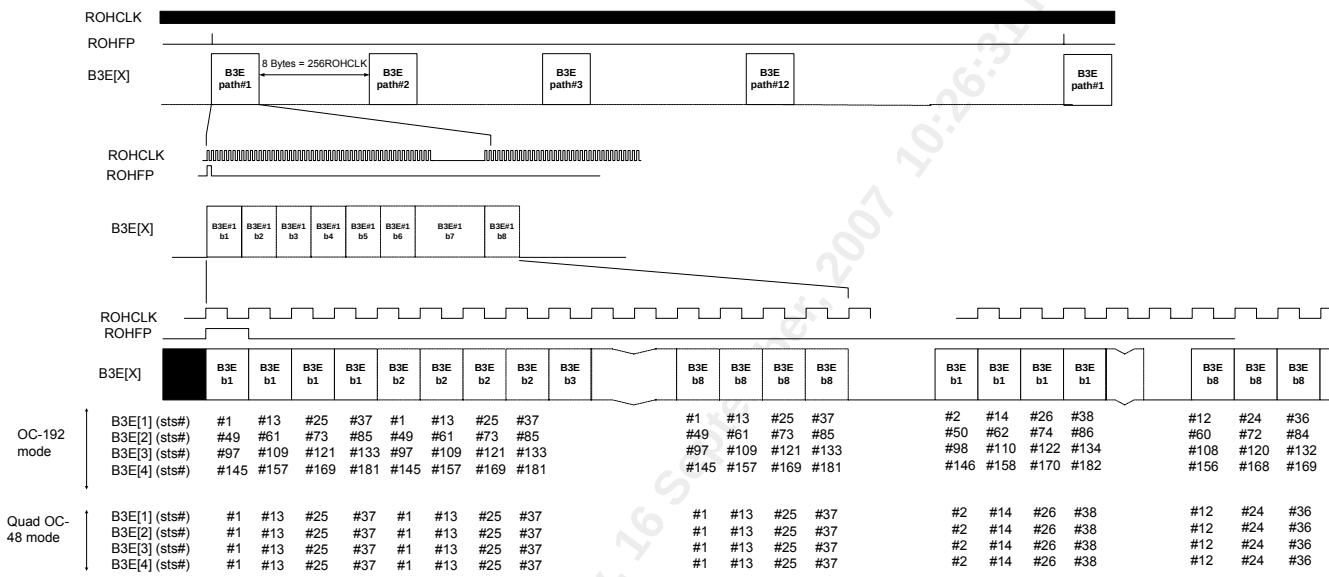
Figure 43 B3E Port Functional Timing



18.10 Receive Ring Control Port Timing (RRCP)

RRCP serially outputs all the section, line, and path defects detected in the receive data stream. Sampling RRCPFP high with RRCPCLK, identifies the OOF defect on RRCPDAT. Path information is updated two times during a single frame period of 125 µs as shown in Figure 44. Four RRCPDAT are used to carry the section/line and path alarms for the 192 paths when processing an STS-192/STM-64 stream or for the four groups of 48 paths when processing four STS-48/STM-16 streams. In both modes, RRCPDAT[N] extracts the 12 path alarms from slice#N,1 followed by the 12 path alarms from slice#N,2, then slice#N,3 and finally the 12 path alarms from slice#N,4.

Also shown is the receive path alarm (RALM) functional timings. RALM serially outputs the "ORing" of the enabled path defects. The same figure shows the STS-1/STM-0 time slots assignment on RALM. Each STS-1/STM-0 time slot is either high or low for 54 consecutive RRCPCLK clock cycles.

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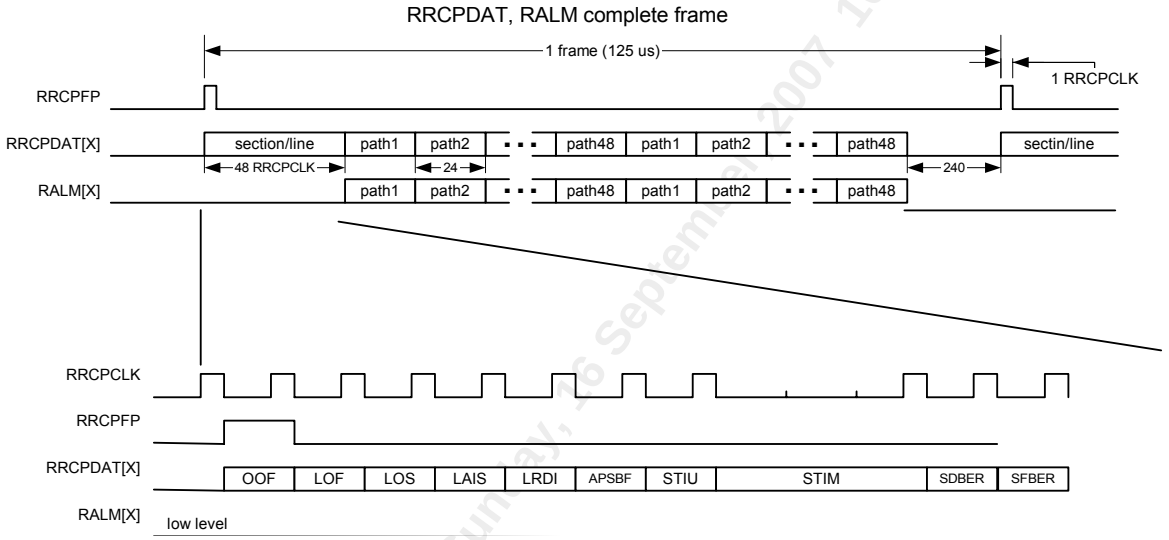
Figure 44 RRCP Port Functional Timing



18.11 Transmit Ring Control Port Timing (TRCP)

The functional timing of the transmit Ring Control Port is identical to that of the receive ring control port. The TRCP port serially inputs the section, line, and path defects to be sent on the transmit direction. The TRCP port is usually connected to the RRCP port of a mate SPECTRA-9953 device. TRCP port is not restricted to RRCP port as long as the format and the timings between TRCPCLK, TRCPFP and TRCPDAT[4:1] are respected. Sampling TRCPFP high with TRCPCLK identifies the OOF defect on TRCPDAT. TRCPFP must be asserted to initiate TRCPDAT capture. Only the first 2352 bits after TRCPFP assertion are considered valid and part of the ring control port.

18.12 Add bus Transmit AIS Timing

The Add bus path AIS port allows the user to insert path AIS. Sampling TPAISFP high with SYSCLK identifies STS-1/STM-0 path #1 on TPAIS[4:1]. TPAISFP must be asserted to initiate TPAIS capture. Each TPAIS[N] carries path AIS for a group of 48 paths. TPAIS[N] carries path AIS for slice#N,1twelve paths, followed by slice#N,2, then slice#N,3, and finally the twelfth path AIS for slice#N,4. The following figure shows the functional timing of the Add AIS port.

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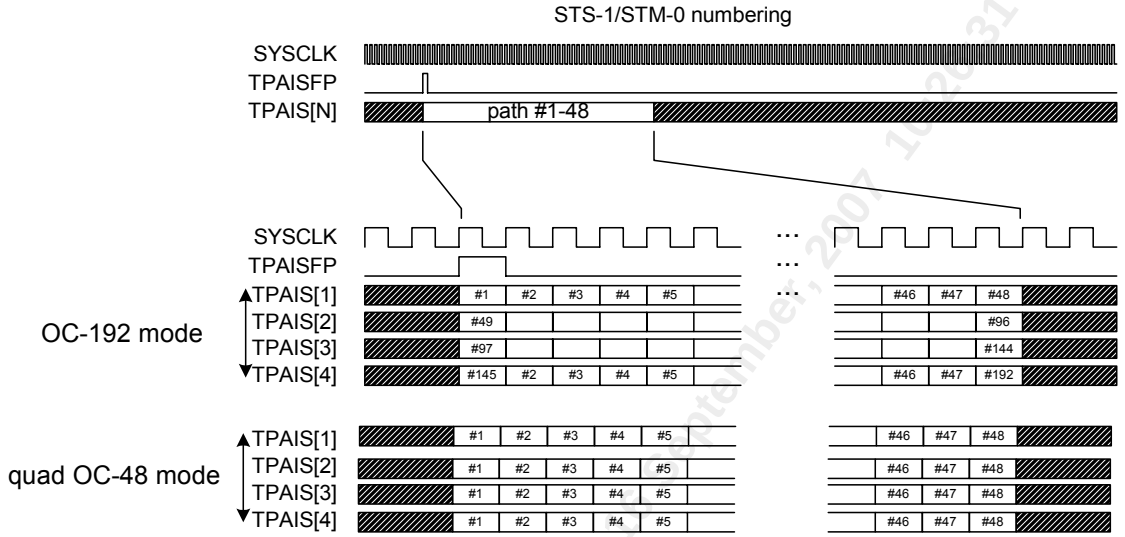
Figure 45 Add_PAIS Functional Timing



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19 Absolute Maximum Ratings

Maximum rating are the worst case limits that the device can withstand without sustaining permanent damage. They are not indicative of normal mode operation conditions.

Table 24 Absolute Maximum Ratings

Storage Temperature	-40°C to +125°C
1.8V Supply Voltage (VDDI, AVDL)	-0.3V to 2.5V
3.3V Supply Voltage (VDDO, AVDH, CSU_AVDH)	-0.3V to 4.6V
Voltage on Any Digital Pin	-0.3V to VDDO+0.3V
Voltage on Any LVDS Pin	-0.3V to AVDH + 0.3V
Static Discharge Voltage	±1000 V
Latch-Up Current (digital I/O)	±100 mA
Latch-Up Current (LVDS)	±90
Latch-Up Current (RESK)	±50
DC Input Current	±20 mA
Reflow Temperature	+230°C
Absolute Maximum Junction Temperature	+125°C
input pad tolerance	-2V < VDDO < +2V for 10ns, 100mA max
output pad overshoot limits	-2V < VDDO < +2V for 10ns, 20mA max

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20 D.C. Characteristics

T_A = -40°C to T_J = +125°C, V_{VDDI} = $V_{VDDItypical}$ ± 5%, V_{VDDO} = $V_{DDOtypical}$ ± 5% (Typical Conditions: T_C = 25°C, V_{VDDI} = 1.8V, V_{VDDO} = 3.3V, V_{AVDL} = 1.8V, V_{AVDH} = 3.3V)

Table 25 D.C. Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Conditions
VDDI	Power Supply at 1.8V	1.71	1.8	1.89	Volts	
VDDO	Power Supply at 3.3V	3.135	3.3	3.465	Volts	
V_{IL}	Input Low Voltage	0		0.8	Volts	Guaranteed Input Low voltage.
V_{IH}	Input High Voltage	2.0			Volts	Guaranteed Input High voltage.
V_{OL}	Output or Bi-directional Low Voltage		0.1	0.4	Volts	Guaranteed output Low voltage at VDDO=2.97V and I_{OL}=maximum rated for pad.
V_{OH}	Output or Bi-directional High Voltage	2.4	2.7		Volts	Guaranteed output High voltage at VDDO=2.97V and I_{OH}=maximum rated current for pad.
V_{T+}	Reset Input High Voltage	2.2			Volts	Applies to RSTB and TRSTB only.
V_{T-}	Reset Input Low Voltage			0.8	Volts	Applies to RSTB and TRSTB only.
V_{TH}	Reset Input Hysteresis Voltage		0.5		Volts	Applies to RSTB and TRSTB only.
I_{ILPU}	Input Low Current	-200	-50	-4	µA	V_{IL} = GND. Notes 1 and 3.
I_{IHPU}	Input High Current	-10	0	+10	µA	V_{IH} = V_{DD}. Notes 1 and 3.
I_{IL}	Input Low Current	-10	0	+10	µA	V_{IL} = GND. Notes 2 and 3.
I_{IH}	Input High Current	-10	0	+10	µA	V_{IH} = V_{DD}. Notes 2 and 3.
C_{IN}	Input Capacitance		5		PF	t_A=25°C, f = 1 MHz
C_{OUT}	Output Capacitance		5		PF	t_A=25°C, f = 1 MHz
C_{IO}	Bi-directional Capacitance		5		PF	t_A=25°C, f = 1 MHz

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Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{IV}	LVDS Input Voltage Range	0		2.4	V	
$\|V_{IDM}\|$	LVDS Minimum Input Differential Voltage	100			mV	Vidm/2 +Vcm < 2.4 V and Vcm - Vidm/2 > 0 V
R_{IN}	LVDS Differential Input Impedance	80	100	120	Ω	
V_{LOH}	LVDS Output voltage high	1350	1375	1425	mV	R_{LOAD}=100Ω ±1%
V_{LOL}	LVDS Output voltage low	900	1025	1125	mV	R_{LOAD}=100Ω ±1%
$\|V_{ODM}\|$	LVDS Output Differential Voltage	300	350	450	mV	R_{LOAD}=100Ω ±1%
V_{OCM}	LVDS Output Common-Mode Voltage	1125	1200	1275	mV	R_{LOAD}=100Ω ±1%
R_O	LVDS Output Impedance, Differential	80	100	120	Ω	
$\|\Delta V_{ODM}\|$	Change in $\|V_{ODM}\|$ between “0” and “1”			25	mV	R_{LOAD}=100Ω ±1%
ΔV_{OCM}	Change in V_{OCM} between “0” and “1”			25	mV	R_{LOAD}=100Ω ±1%
I_{SP}, I_{SN}	LVDS Short-Circuit Output Current			10	mA	Drivers shorted to ground
I_{SPN}	LVDS Short-Circuit Output Current			10	mA	Drivers shorted together

Notes on D.C. Characteristics:

1. Input pin or bi-directional pin with internal pull-up resistor.

37. Input pin or bi-directional pin without internal pull-up resistor

38. Negative currents flow into the device (sinking), positive currents flow out of the device (sourcing.)

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21 Power Information

21.1 Power Requirements

Table 26 Power Requirements

Conditions	Parameter	Typ[1,3]	High[4]	Max[2]	Units
OC192 All serial links, parallel buses, PRBS generators and PRBS monitors running.	IDDOP (AVDH1)	0.015	-	0.019	A
	IDDOP (AVDH2)	0.010	-	0.013	A
	IDDOP (AVDHREF)	0.009	-	0.011	A
	IDDOP (AVDL123)	0.103	-	0.13	A
	IDDOP (AVDL4)	0.023	-	0.035	A
	IDDOP (QAVD)	0.005	-	0.007	A
	IDDOP (VDDI)	5.104	-	6.2	A
	IDDOP (VDDO)	0.643	-	0.8	A
	Total Power	12.2485	12.979	-	W
4 x OC-48	IDDOP (AVDH1)	0.015	-	0.020	A
	IDDOP (AVDH2)	0.009	-	0.015	A
	IDDOP (AVDHREF)	0.009	-	0.014	A
	IDDOP (AVDL123)	0.101	-	0.14	A
	IDDOP (AVDL4)	0.025	-	0.033	A
	IDDOP (QAVD)	0.004	-	0.010	A
	IDDOP (VDDI)	5.322	-	6.3	A
	IDDOP (VDDO)	0.640	-	0.8	A
	Total Power	12.640	13.616	-	W

Notes:

1. Typical IDD values are calculated as the mean value of current under the following conditions: typically processed silicon, nominal supply voltage, Tj=60 °C, outputs loaded with 30 pF, and a normal amount of traffic or signal activity. These values are suitable for evaluating typical device performance in a system.
2. Max IDD values are currents guaranteed by the production test program and/or characterization over process for operating currents at the maximum operating voltage and operating temperature that yields the highest current (including outputs loaded to 30pF).
3. Typical power values are calculated using the formula:

   $$\text{Power} = \sum i(\text{VDDNomi} \times \text{IDDTypi})$$

   Where i denotes all the various power supplies on the device, VDDNomi is the nominal voltage for supply i, and IDDTypi is the typical current for supply i (as defined in note 1 above). These values are suitable for evaluating typical device performance in a system.

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4. High power values are a “normal high power” estimate, calculated using the formula:

   Power = ∑i(VDDMaxi x IDDHighi)

   Where i denotes all the various power supplies on the device, VDDMaxi is the maximum operating voltage for supply i, and IDDHighi is the current for supply i. IDDHigh values are calculated as the mean value plus two sigmas (2σ) of measured current under the following conditions: Tj=105° C, outputs loaded with 30 pF. These values are suitable for evaluating board and device thermal characteristics.

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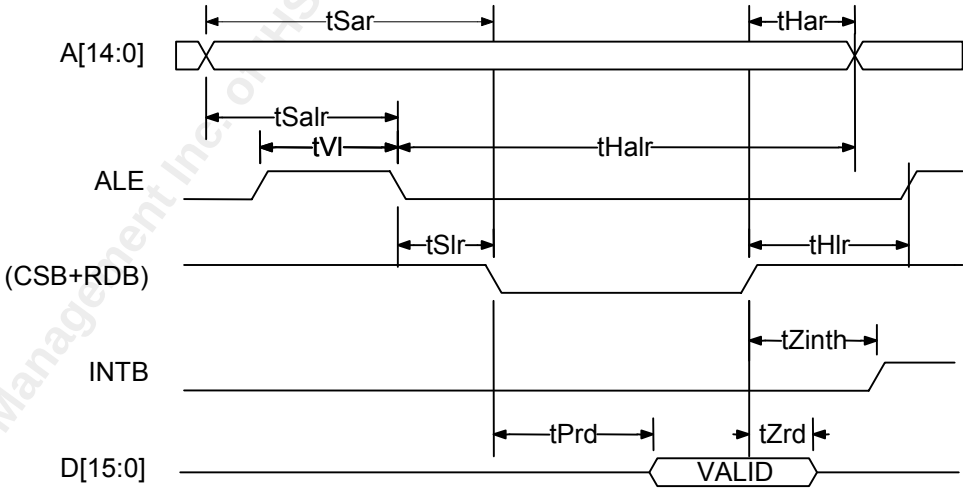
22 Microprocessor Interface Timing Characteristics

T_A = -40°C to T_J = +125°C, V_{VDDI} = $V_{VDDItypical}$ ± 5%, V_{VDDO} = $V_{DDOtypical}$ ± 5% (Typical Conditions: T_C = 25°C, V_{VDDI} = 1.8V, V_{VDDO} = 3.3V, V_{AVDL} = 1.8V, V_{AVDH} = 3.3V))

Table 27 Microprocessor Interface Read Access

Symbol	Parameter	Min	Max	Units
tS_{AR}	Address to Valid Read Set-up Time	10		ns
tH_{AR}	Address to Valid Read Hold Time	5		ns
tS_{ALR}	Address to Latch Set-up Time	10		ns
tH_{ALR}	Address to Latch Hold Time	10		ns
tV_{L}	Valid Latch Pulse Width	5		ns
tS_{LR}	Latch to Read Set-up	0		ns
tH_{LR}	Latch to Read Hold	5		ns
tP_{RD}	Valid Read to Valid Data Propagation Delay		70	ns
tZ_{RD}	Valid Read Negated to Output Tri-state		20	ns
tZ_{INTH}	Valid Read Negated to INTB High (WCIMODE = 0)		50	ns

Figure 46 Intel Microprocessor Interface Read Timing



Notes on Microprocessor Interface Read Timing:

1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.

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39. Output propagation delays are measured with a 100 pF load on the Microprocessor Interface data bus, (D[15:0]).

40. A valid read cycle is defined as a logical OR of the CSB and the RDB signals.

41. In non-multiplexed address/data bus architectures, ALE should be held high so parameters tS_{ALR}, tH_{ALR}, tV_L, tS_{LR}, and tH_{LR} are not applicable.

42. Parameter tH_{AR} is not applicable if address latching is used.

43. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

44. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

Table 28 Microprocessor Interface Write Access

Symbol	Parameter	Min	Max	Units
tS_{AW}	Address to Valid Write Set-up Time	10		ns
tS_{DW}	Data to Valid Write Set-up Time	20		ns
tS_{ALW}	Address to Latch Set-up Time	10		ns
tH_{ALW}	Address to Latch Hold Time	10		ns
tV_L	Valid Latch Pulse Width	5		ns
tS_{LW}	Latch to Write Set-up	0		ns
tH_{LW}	Latch to Write Hold	5		ns
tH_{DW}	Data to Valid Write Hold Time	5		ns
tH_{AW}	Address to Valid Write Hold Time	5		ns
tV_{WR}	Valid Write Pulse Width	40		ns
tZ_{INTH}	Valid Write Negated to INTB High (WCIMODE = 1)		50	ns

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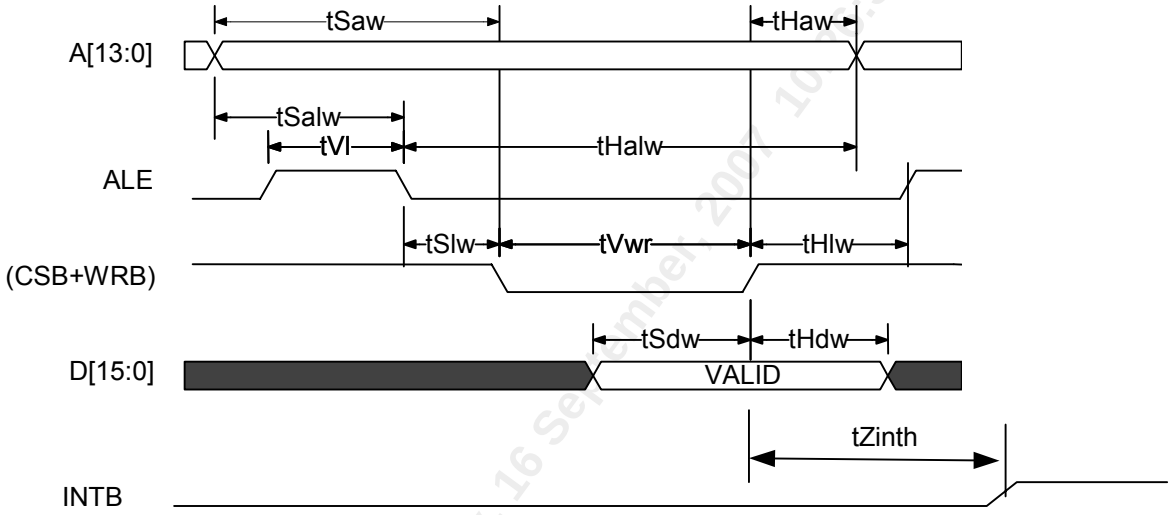
Figure 47 Intel Microprocessor Interface Write Timing



Notes on Microprocessor Interface Write Timing:

1. A valid write cycle is defined as a logical OR of the CSB and the WRB signals.

45. In non-multiplexed address/data bus architectures, ALE should be held high so parameters tS_{ALW}, tH_{ALW}, tV_L, tS_{LW}, and tH_{LW} are not applicable.

46. Parameter tH_{AW} is not applicable if address latching is used.

47. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

48. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

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23 A.C. Timing Characteristics

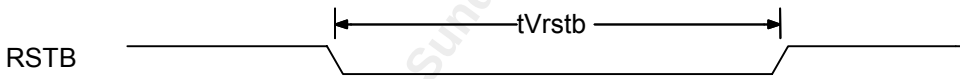
T_A = -40°C to T_J = +125°C, V_{VDDI} = $V_{VDDItypical}$ ± 5%, V_{VDDO} = $V_{DDOtypical}$ ± 5% (Typical Conditions: T_C = 25°C, V_{VDDI} = 1.8V, V_{VDDO} **= 3.3V, V_{AVDL} = 1.8V, V_{AVDH}** = 3.3V)

23.1 Reset Timing

Table 29 System Miscellaneous Timing

Symbol	Description	Min	Max	Units
TVRSTB	RSTB input pulse width	100		ns

Figure 48 System Miscellaneous Timing Diagram Timing



23.2 Line Interface Timing

Table 30 Line Interface Timing

Symbol	Description	Min	Max	Units
FRXCLK	RXCLK Frequency (nominally 622.08MHz)	622.07	622.09	MHz
T_RXCLK	RXCLK period (nominally 1.608 ns)	1.607	1.61	ns
TW_RXCLK	RXCLK duty cycle (TH_RXCLK/TL_RXCLK)	45	55	%
TR_RXCLK	RXCLK rise time (20%-80%)	100	300	ps
TF_RXCLK	RXCLK fall time (20%-80%)	100	300	ps
TS_RXCLK	RXDATA Setup time	300		ps

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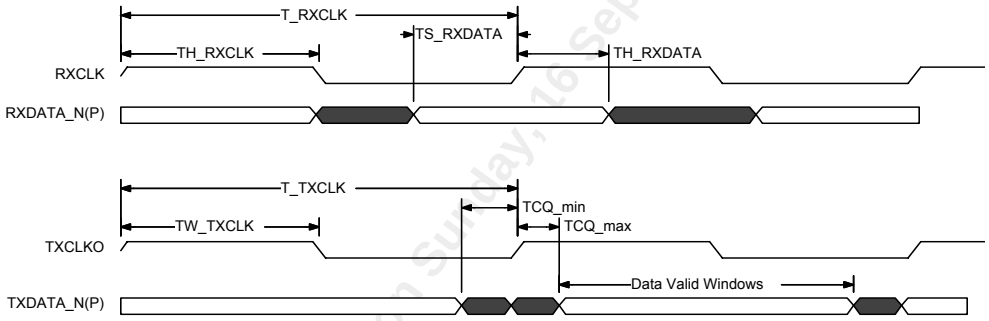
TH_RXCLK	RXDATA hold time	300		ps
FTXCLK	TXCLK Frequency (nominally 622.08MHz)	622.07	622.09	MHz
T_TXCLK	TXCLK period (nominally 1.608 ns)	1.607	1.61	ns
TW_TXCLK	TXCLK duty cycle (TH_TXCLK/TL_TLCLK)	40	60	%
TR_TXCLK	TXCLK rise time (20%-80%)	100	250[1]	ps
TF_TXCLK	TXCLK fall time (20%-80%)	100	250[1]	ps
TCQ_min, TCQ_max	TXDATA propagation delay	-200	200	ps

Notes on Line Interface Timing:

1. TXCLK Rise/fall times specified with a load capacitance of 1pF.

Figure 49 Line Interface Timing



PMC-Sierra's LVDS I/Os operate according to the IEEE 1596.3-1996 specification. The transmitter drives a differential signal through a pair of 50 Ω characteristic interconnects, such as board traces, backplane traces, or short lengths of cable. The receiver presents a 100 Ω differential termination impedance to terminate the lines. Included in the standard is sufficient common-mode range for the receiver to accommodate as much as 925 mV of common-mode ground difference.

23.3 System (777 MHz) Interface Timing

Table 31 System Interface Timing

Symbol	Description	Min	Typical	Max	Units
F_{SYSCLK}	SYSCLK Frequency (nominally 77.76 MHz)	77		78	MHz
THI_{SYSCLK}	SYSCLK High Pulse Width	5.8			ns
TLO_{SYSCLK}	SYSCLK Low Pulse Width	5.8			ns

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Symbol	Description	Min	Typical	Max	Units
F_{SYSCLK}	SYSCLK Frequency (nominally 77.76 MHz)	77		78	MHz
THI_{SYSCLK}	SYSCLK High Pulse Width	5.8			ns
TLO_{SYSCLK}	SYSCLK Low Pulse Width	5.8			ns
F_{ADLVDS}	ADP/N[X] , DDP/N[X] bit rate	10 F_{SYSCLK} – 100 ppm	10 F_{SYSCLK}	10 F_{SYSCLK} – 100 ppm	Mbit/s
T_{fall}	V_{ODM} fall time, 80%-20%, (RLOAD=100Ω ±1%	200	300	400	ps
T_{rise}	V_{ODM} rise time, 80%-20%, (RLOAD=100Ω ±1%	200	300	400	ps
T_{skew}	Differential skew			50	ps

The min and max f_{ADLVDS} specification is to accommodate transients between generated clocks. The mean data rate on the add and drop interfaces must be exactly $10f_{SYSCLK}$. FIFO overrun/underrun in the R8TD and T8TE will result if the mean data rate differs from $10f_{SYSCLK}$. A common system clock needs to be used for all devices with serial TelecomBus interfaces.

PMC-Sierra's LVDS I/Os operate according to IEEE 1596.3-1996. The transmitter drives a differential signal through a pair of 50 Ω characteristic interconnects, such as board traces, backplane traces, or short lengths of cable. The receiver presents a 100 Ω differential termination impedance to terminate the lines. Included in the standard is sufficient common-mode range for the receiver to accommodate as much as 925 mV of common-mode ground difference.

23.4 System Interface Control Pin Timing

Table 32 System Interface Control Pin Timing

Symbol	Description	Min	Max	Units
F_{SYSCLK}	SYSCLK Frequency (nominally 77.76 MHz)	77	78	MHz
THI_{SYSCLK}	SYSCLK High Pulse Width	5.8		ns
TLO_{SYSCLK}	SYSCLK Low Pulse Width	5.8		ns
TS_{CMP}	DCMP/ACMP Set-Up Time	3		ns
TH_{CMP}	DCMP/ACMP Hold Time	0		ns
TS_{fp}	DFP/AFP Set-Up Time	3		ns

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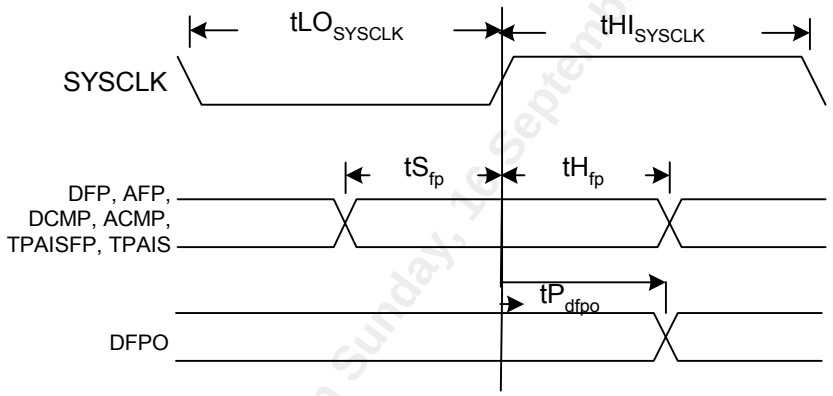
Symbol	Description	Min	Max	Units
TH_{fp}	DFP/AFP Hold Time	0		ns
TS_{AIS}	TPAISFP/TPAIS Set-Up Time	3		ns
TH_{AIS}	TPAISFP/TPAIS Hold Time	0		ns
TP_{DFPO}	DFPO Propagation delay	0	6	ns

Figure 50 SPECTRA-9953 System Side Input/Output Timing



Notes on Input Timing:

1. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

49. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

Notes on Output Timing:

1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.

50. Output propagation delays are measured with a 30 pF load on the outputs except when otherwise specified.

23.5 Receive Transport Overhead Port and B3E Timing

Table 33 ROHCLK1-4/B3E Output Timing

Symbol	Description	Min	Max	Units
F_{ROHCLK}	ROHCLK1-4 Frequency : (ROHCLK is nominally 82.94 MHz and is generated by gapping an internal 103.68 MHz receive line clock)	103.51	103.68	MHz
TPROHFP	ROHCLK1-4 rising edge to ROHFP1-4 valid	1	6	ns

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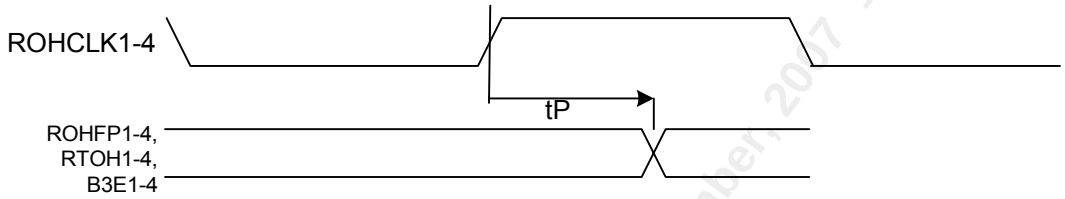
TPRTOH	ROHCLK1-4 rising edge to RTOH1-4 valid	1	6	ns
tPB3E	ROHCLK1-4 rising edge to B3E1-4 valid	1	6	ns

Figure 51 Receive RTOH Output Timing



Notes on Output Timing:

1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.

51. Output propagation delays are measured with a 30 pF load on the outputs except when otherwise specified.

23.6 Receive DCC Port Timing

Table 34 Receive DCC Output Timing

Symbol	Description	Min	Max	Units
$F_{RSLDCLK}$	RSLDCLK Frequency	192 or 576		khZ
TPRSLD	RSLDCLK falling edge to RSLD valid	-250	0	ns
TS_{ROHFP}[8]	ROHFP output setup time to RSLDCLK rising edge	4		ns
TH_{ROHFP}	ROHFP output hold time to RSLDCLK rising edge	1		ns
F_{RLDCLK}	RLDCLK Frequency	576		KHz
TP_{RLD}	RLDCLK falling edge to RLD valid	-250	0	ns
TS_{ROHFP}	ROHFP output setup time to RLDCLK rising edge	4		ns
TH_{ROHFP}	ROHFP output hold time to RLDCLK rising edge	1		ns

[8] ROHFP is an output. Because it is used to synchronize the DCC ports, it is characterized with-respect to RLDCLK and RSLDCLK. Set-up and hold times are used to provide the window where the pulse is valid around a rising edge of RLDCLK and RSLDCLK.

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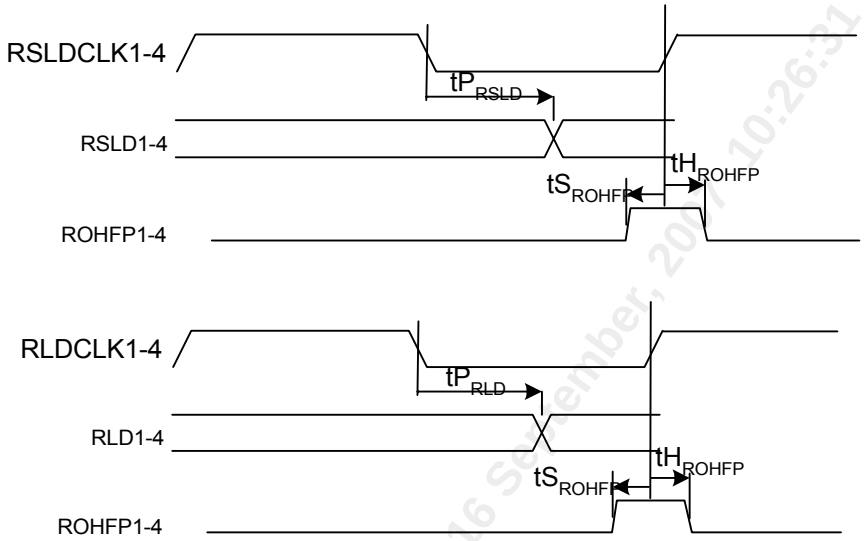
Figure 52 Receive DCC Output Timing



Notes on Output Timing:

1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.

52. Output propagation delays are measured with a 30 pF load on the outputs except when otherwise specified.

23.7 Transmit Overhead Port Timing

Table 35 TOH Port Input/Output Timing

Symbol	Description	Min	Max	Units
F_{TOHCLK}	TOHCLK1-4 Frequency : (ROHCLK is nominally 82.94 MHz and is generated by gapping an internal 103.68 MHz receive line clock)	103.51	103.68	MHz
TS_{TTOH}	TTOH1-4 Set-up time to TOHCLK1-4 rising edge	3		ns
TH_{TTOH}	TTOH1-4 Hold time to TOHCLK1-4 rising edge	0		ns
TS_{TTOHEN}	TTOHEN1-4 Set-up time to TOHCLK1-4 rising edge	3		ns
TH_{TTOHEN}	TTOHEN1-4 Hold time to TOHCLK1-4 rising edge	0		ns
TPTOHFP	TOHCLK1-4 rising edge to TOHFP1-4 valid	1	6	ns

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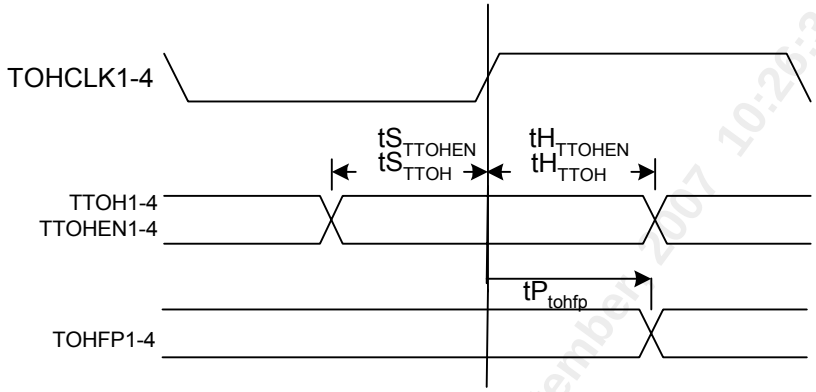
Figure 53 Transmit Transport Overhead Port Timing



Notes on Input Timing:

1. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

53. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

Notes on Output Timing:

1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.

54. Output propagation delays are measured with a 30 pF load on the outputs except when otherwise specified.

23.8 Transmit DCC Port Timing

Table 36 Transmit DCC Input/Output Timing

Symbol	Description	Min	Max	Units
FTSLDCLK	TSLDCLK Frequency	192 or 576		KhZ
TS_{TSLD}	TSLD Set-up time to TSLDCLK rising edge	50		ns
TH_{TSLD}	TSLD Hold time to TSLDCLK rising edge	250		ns
TS_{TOHFP}[9]	TOHFP output setup time to TSLDCLK rising edge	4		ns

[9] TOHFP is an output. Because it is used to synchronize the transmit DCC ports, it is characterized with-respect to TLDCLK and TSLDCLK. Set-up and hold times are used to provide the window the pulse is valid around a rising edge of TLDCLK and TSLDCLK.

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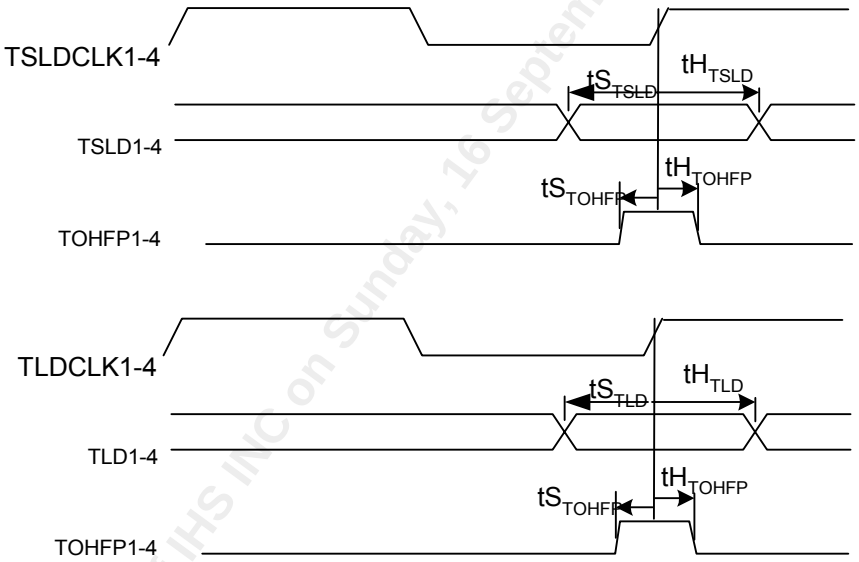
Symbol	Description	Min	Max	Units
TH_{TOHFP}	TOHFP output hold time to TSLDCLK rising edge	1		ns
FTLDCLK	TLDCLK Frequency	576		KHz
TS_{TLD}	TLD Set-up time to TLDCLK rising edge	50		ns
TH_{TLD}	TLD Hold time to TLDCLK rising edge	250		ns
TS_{TOHFP}	TOHFP output setup time to TLDCLK rising edge	4		ns
TH_{TOHFP}	TOHFP output hold time to TLDCLK rising edge	1		ns

Figure 54 Transmit DCC Input/Output Timing



Notes on Input Timing:

1. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

55. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

23.9 Receive Ring Control Port Timing

Table 37 RRCP Timing

Symbol	Description	Min	Max	Units
FRRCPCLK	RRCPCLK Frequency : RRCPCLK is nominally 20.736 MHz and is generated by gapping an internal 25.92 MHz transmit line clock	20.736		MHz
$TP_{RRCPDAT}$	RRCPCK falling edge to RRCPDAT1-4 valid	-3	8	ns

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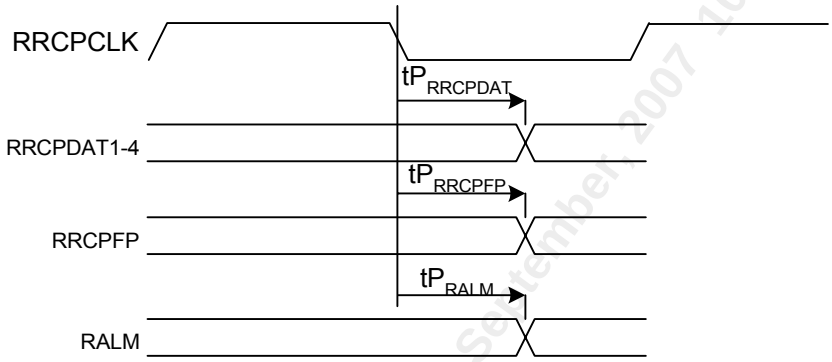
TP_{RRCPFP}	RRCPCK falling edge to RRCPFP valid	-3	8	ns
TP_{RALM}	RRCPCK falling edge to RALM1-4 valid	-3	8	ns

Figure 55 RRCP Timing



Notes on Output Timing:

1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.

56. Output propagation delays are measured with a 30 pF load on the outputs except when otherwise specified.

23.10 Transmit Ring Control Port Timing

Table 38 TRCP Timing

Symbol	Description	Min	Max	Units
FTRCPCLK	TRCPCLK Frequency : TRCPCLK is nominally 20.736 MHz and is generated by gapping an internal 25.92 MHz transmit line clock	20.736		MHz
$TLO_{TRCPCLK}$				
$THI_{TRCPCLK}$				
TS_{TRCPFP}	TRCPFP Set-up time to TRCPCK rising edge	5		ns
TH_{TRCPFP}	TRCPFP Hold time to TRCPCK rising edge	5		ns
$TS_{TRCPDAT}$	TRCPDAT1-4 Set-up time to TRCPCLK rising edge	5		ns
$TH_{TRCPDAT}$	TRCPDAT1-4 Hold time to TRCPCLK rising edge	5		ns

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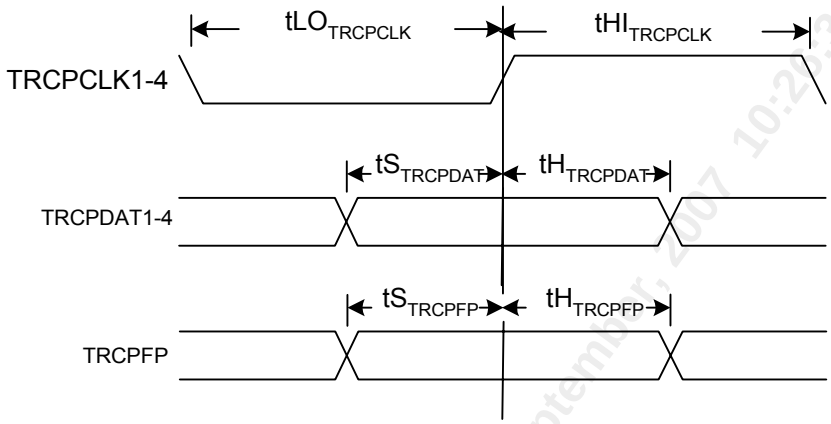
Figure 56 TRCP Port Timing



Notes on Input Timing:

1. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

57. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

23.11 JTAG Test Port Timing

Table 39 JTAG Port Interface

Symbol	Description	Min	Max	Units
F_{TCK}	TCK Frequency		4	MHz
THI_{TCK}	TCK HI Pulse Width	100		ns
THI_{TCK}	TCK LO Pulse Width	100		ns
TS_{TMS}	TMS Set-up time to TCK	25		ns
tH_{TMS}	TMS Hold time to TCK	25		ns
tS_{TDI}	TDI Set-up time to TCK	25		ns
tH_{TDI}	TDI Hold time to TCK	25		ns
tP_{TDO}	TCK Low to TDO Valid	2	25	ns
tV_{TRSTB}	TRSTB Pulse Width	100		ns

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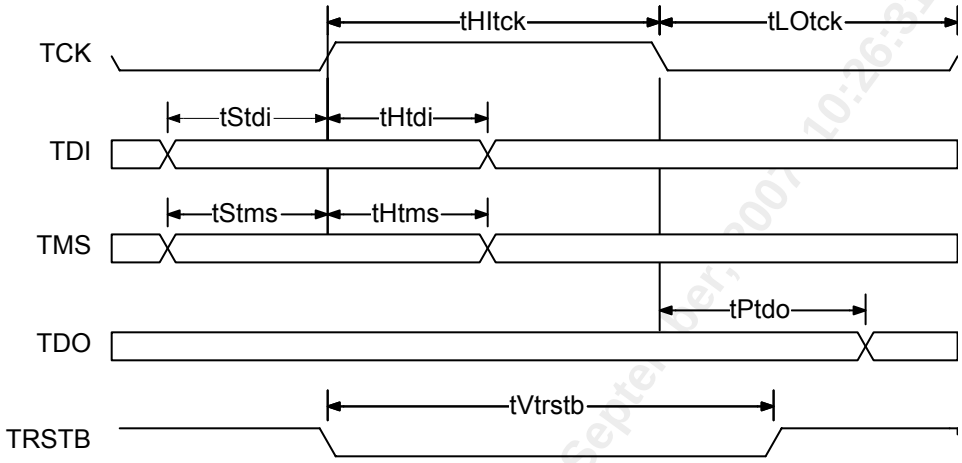
Figure 57 JTAG Port Interface Timing



Notes on Input Timing:

1. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

58. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

Notes on Output Timing:

1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.

59. Output propagation delays are measured with a 30 pF load on the outputs except when otherwise specified.

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24 Thermal Information

This product is designed to operate over a wide temperature range when used with a heat sink and is suited for outside plant equipment[1].

Table 40 Outside Plant Thermal Information

Maximum long-term operating junction temperature (T_J) to ensure adequate long-term life.	**105^{0}C**
Maximum junction temperature (T_J) for short-term excursions with guaranteed continued functional performance[2]. This condition will typically be reached when the local ambient temperature reaches 85 °C.	**125 ^{0}C**
Minimum ambient temperature (T_A)	**-40 ^{0}C**

Table 41 Device Compact Model[3]

Junction-to-Case Thermal Resistance, θ_{JC}	0.16 °C/W
Junction-to-Board Thermal Resistance, θ_{JB}	3.95 °C/W

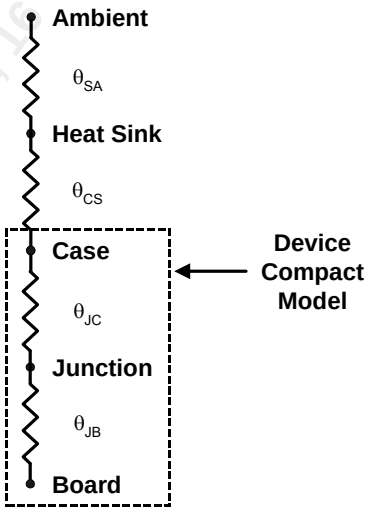

Table 42 Heat Sink Requirements

$\theta_{SA}+\theta_{CS}$[4]	The sum of θ_{SA} + θ_{CS} must be less than or equal to: $[(105 - T_A) / P_D] - \theta_{JC}$] °C/W where: T_A is the ambient temperature at the heat sink location P_D is the operating power dissipated in the package
	θ_{SA} and θ_{CS} are required for long-term operation

Power depends upon the operating mode. To obtain power information, refer to 'High' power values in section 18.1 Power Requirements.Notes

1. The minimum ambient temperature requirement for Outside Plant Equipment meets the minimum ambient temperature requirement for Industrial Equipment.

60. Short-term is used as defined in Telcordia Technologies Generic Requirements GR-63-Core Core.

61. θ_{JC}, the junction-to-case thermal resistance, is a measured nominal value plus two sigma. θ_{JB}, the junction-to-board thermal resistance, is obtained by simulating conditions described in JEDEC Standard JESD 51-8.

62. θ_{SA} is the thermal resistance of the heat sink to ambient. θ_{CS} is the thermal resistance of the heat sink attached material. The maximum θ_{SA} required for the airspeed at the location of the device in the system with all components in place.

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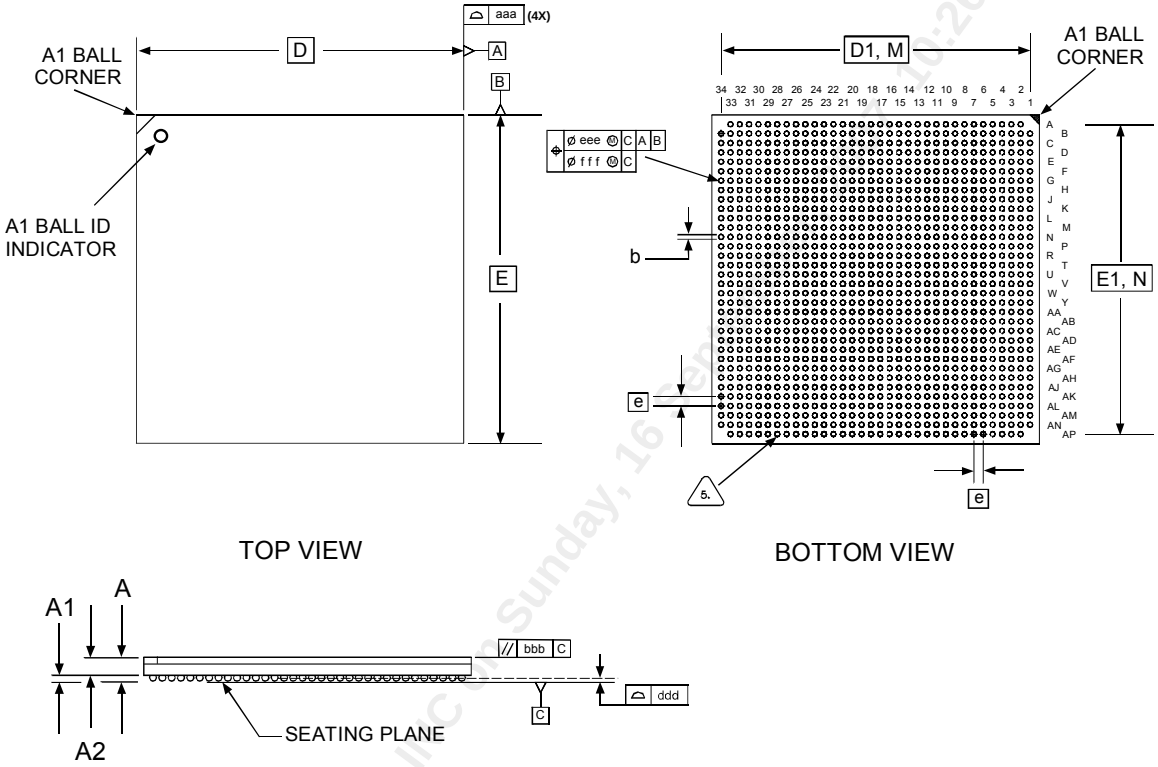
25 Mechanical Information

Figure 58 1152-Pin 35x35mm FCBGA (3M Substrate)



NOTES: 1) ALL DIMENSIONS IN MILLIMETER.
2) DIMENSION aaa DENOTES PACKAGE BODY PROFILE.
3) DIMENSION bbb DENOTES PARALLEL.
4) DIMENSION ddd DENOTES COPLANARITY.
5) DIAMETER OF SOLDER MASK OPENING IS 0.530 MM (SMD).
6) PACKAGE COMPLIANT TO JEDEC REGISTERED OUTLINE MS-034, VARIATION AAR-1.

PACKAGE TYPE : 1152 FLIP CHIP BALL GRID ARRAY - FCBGA															
BODY SIZE : 35 x 35 x 2.39 MM (7 LAYERS)															
Dim.	A	A_1	A_2	D	D_1	E	E_1	M,N	b	e	aaa	bbb	ddd	eee	f f f
Min.	2.11	0.40	1.71	-	-	-	-	-	0.50	-	-	-	-	-	-
Nom.	2.39	0.50	1.89	35.00 BSC	33.00 BSC	35.00 BSC	33.00 BSC	34x34	0.64	1.00 BSC	-	-	-	-	-
Max.	2.67	0.60	2.07	-	-	-	-	-	0.70	-	0.20	0.25	0.20	0.25	0.10

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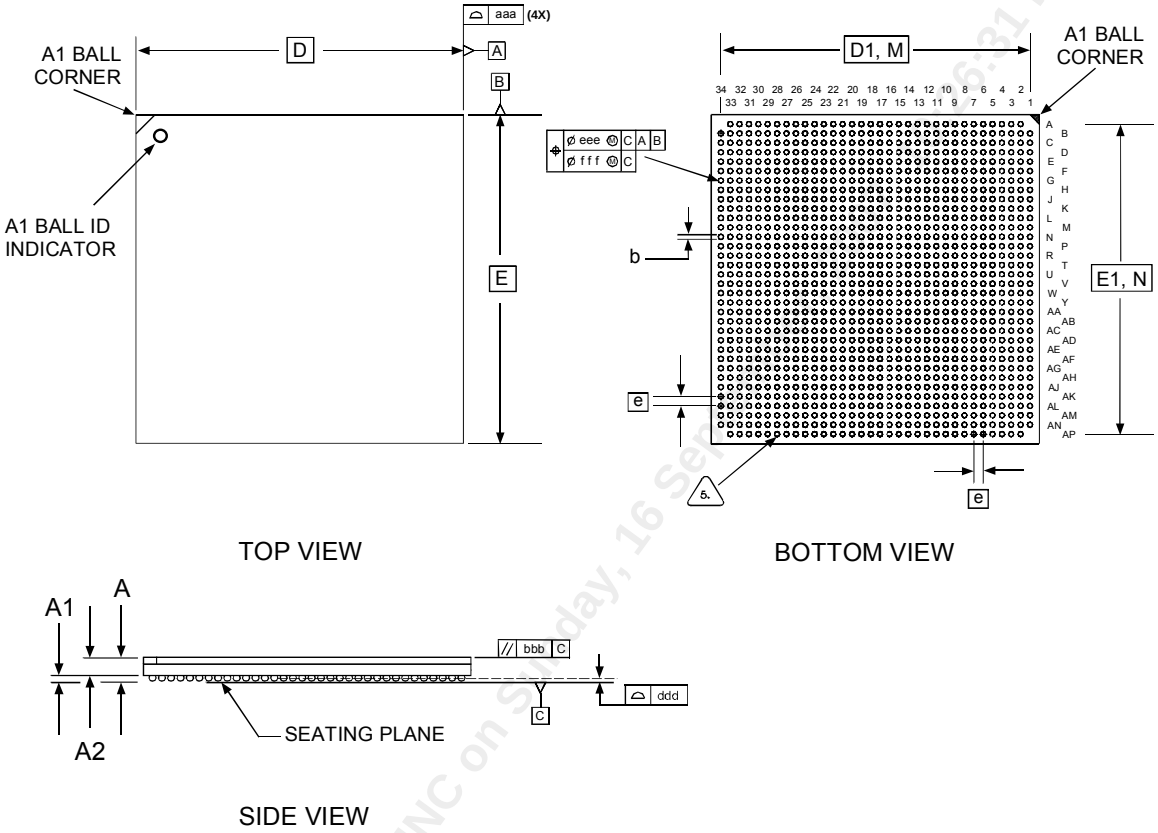
Figure 59 1152-Pin 35x35mm FCBGA (HDBU Substrate)



NOTES: 1) ALL DIMENSIONS IN MILLIMETER.
2) DIMENSION aaa DENOTES PACKAGE BODY PROFILE.
3) DIMENSION bbb DENOTES PARALLEL.
4) DIMENSION ddd DENOTES COPLANARITY.
5) DIAMETER OF SOLDER MASK OPENING IS 0.530 MM (SMD).
6) PACKAGE COMPLIANT TO JEDEC REGISTERED OUTLINE MS-034, VARIATION AAR-1.

PACKAGE TYPE : 1152 FLIP CHIP BALL GRID ARRAY - FCBGA (HDBU 3_2_3)															
BODY SIZE : 35 x 35 x 3.04 MM															
Dim.	A	A_1	A_2	D	D_1	E	E_1	M,N	b	e	aaa	bbb	ddd	eee	f f f
Min.	2.76	0.40	2.36	-	-	-	-	-	0.50	-	-	-	-	-	-
Nom.	3.04	0.50	2.54	35.00 BSC	33.00 BSC	35.00 BSC	33.00 BSC	34x34	0.64	1.00 BSC	-	-	-	-	-
Max.	3.32	0.60	2.72	-	-	-	-	-	0.70	-	0.20	0.25	0.20	0.25	0.10

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26 Ordering Information

Table 43 Ordering Information

PART NO.	Description
PM5317-FI	SPECTRA-9953 1152-Pin FCBGA (3M Substrate)
PM5317H-FI	SPECTRA-9953 1152-Pin FCBGA (HDBU Substrate)
PM5317-FGI	SPECTRA-9953 1152-Pin FCBGA (HDBU Substrate, RoHS-compliant)

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Notes

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