National Semiconductor

ADVANCED INFORMATION

54F/74F710
400 MHz Single Supply TTL-ECL Shift Register

General Description

The 'F710 Shift Register is comprised of an 8-bit transparent holding register with TTL inputs for data and load enable which is translated internally to ECL levels. The holding register is the loading stage for the 8-bit shift register. The shift register is a single direction, two output shift register with a cascade input that is functional during serial shift operations.

The shift register also features a mode input (MODE) and differential ECL clock inputs (SC and $\overline{SC}$) for synchronous shifting and loading of data, both of which are done on the rising edge of the clock. The mode input is provided for selection of shifting or loading of data. Two outputs are available, one for every fourth bit of the shift register. Parallel loading will take place at speeds up to 100 MHz. Shifting will take place at speeds up to 400 MHz. The 'F710 was designed to be used in systems where both TTL and ECL logic are operating from a common voltage supply.

The 'F710 can be used in applications of high speed TTL-ECL translation such as high resolution color graphics, instrumentation, and communication systems.

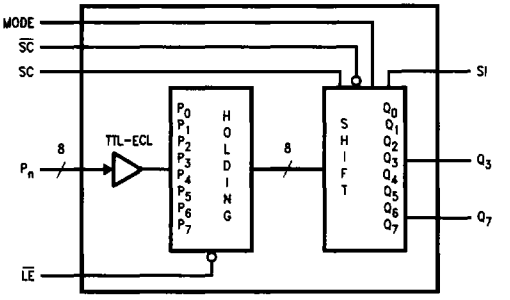
Features

- 400 MHz shift speed
- 100 MHz parallel load speed
- TTL parallel inputs
- ECL serial input
- 10K and 10KH ECL compatible (referenced to V_{CC})
- Transparent data holding register
- Available in 20-lead DIP

Applications

- High resolution color graphics
- CAE/CAD/CAM applications
- Radar Processing
- Instrumentation

Functional Block Diagram



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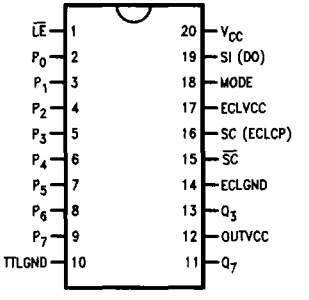
Connection Diagram

Pin Assignment for DIP



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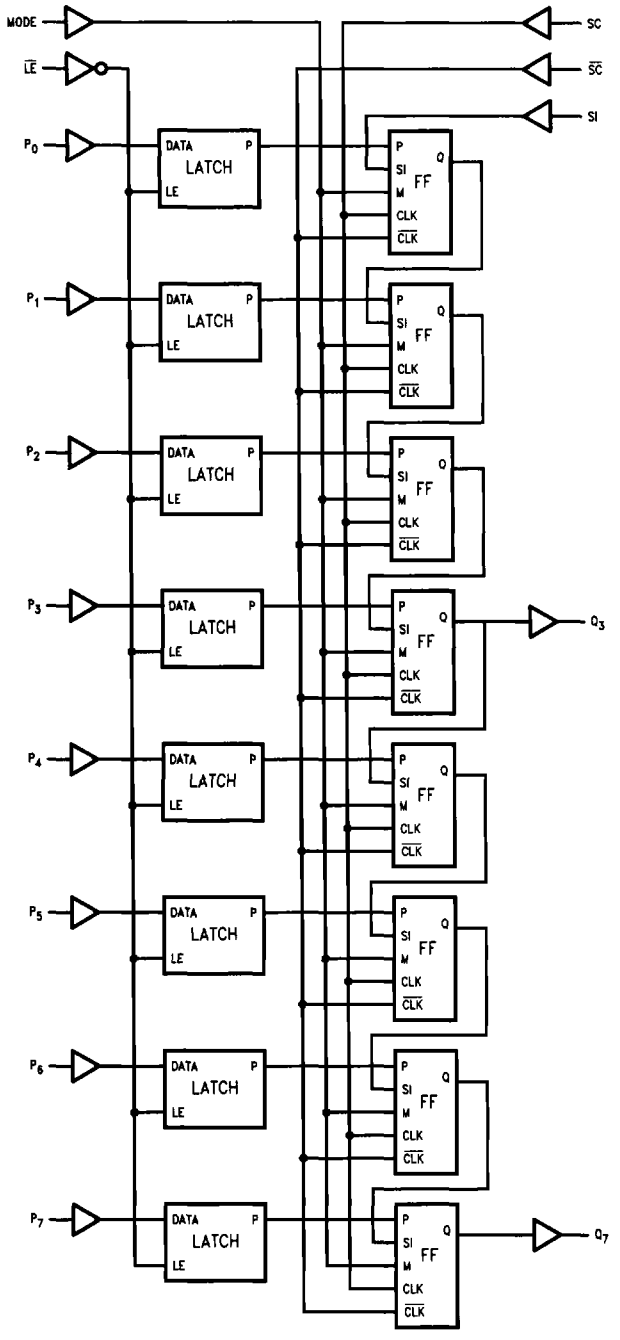
'F710 Logic Diagram



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