
HD74HC83

4-bit Binary Full Adder (with Fast Carry)

HITACHI

ADE-205-426 (Z)
1st. Edition
Sep. 2000

Description

This improved full adder performs the addition of two 4-bit binary numbers. The sum () output are provided for each bit and the resultant carry (C_4) is obtained from the fourth bit.

This adder features full internal look ahead across all four bit generating the carry term in ten nanoseconds typically.

This provides the system designer with partial look-ahead performance at the economy and reduced package count of a ripple-carry implementation.

Features

- High Speed Operation: t_{pd} (A_i or B_i to Z_i) = 16 ns typ ($C_L = 50$ pF)
- High Output Current: Fanout of 10 LSTTL Loads
- Wide Operating Voltage: $V_{CC} = 2$ to 6 V
- Low Input Current: 1 μ A max
- Low Quiescent Supply Current: I_{CC} (static) = 4 μ A max ($T_a = 25^\circ\text{C}$)

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Function Table

Inputs				Outputs					
				When $C_0 = L$ /When $C_2 = L$			When $C_0 = H$ /When $C_2 = H$		
A_1/A_3	B_1/B_3	A_2/A_4	B_2/B_4	Σ_1/Σ_3	Σ_2/Σ_4	C_2/C_4	Σ_1/Σ_3	Σ_2/Σ_4	C_2/C_4
L	L	L	L	L	L	L	H	L	L
H	L	L	L	H	L	L	L	H	L
L	H	L	L	H	L	L	L	H	L
H	H	L	L	L	H	L	H	H	L
L	L	H	L	L	H	L	H	H	L
H	L	H	L	H	H	L	L	L	H
L	H	H	L	H	H	L	L	L	H
H	H	H	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H	H	L
H	L	L	H	H	H	L	L	L	H
L	H	L	H	H	H	L	L	L	H
H	H	L	H	L	L	H	H	L	H
L	L	H	H	L	L	H	H	L	H
H	L	H	H	H	L	H	L	H	H
L	H	H	H	H	L	H	L	H	H
H	H	H	H	L	H	H	H	H	H

H : High level

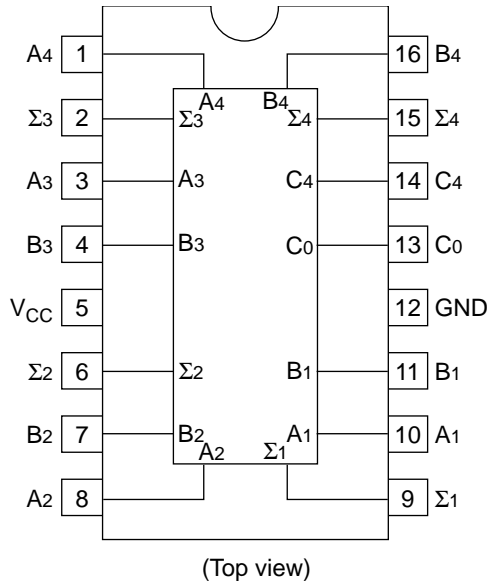
L : Low level

X : Irrelevant

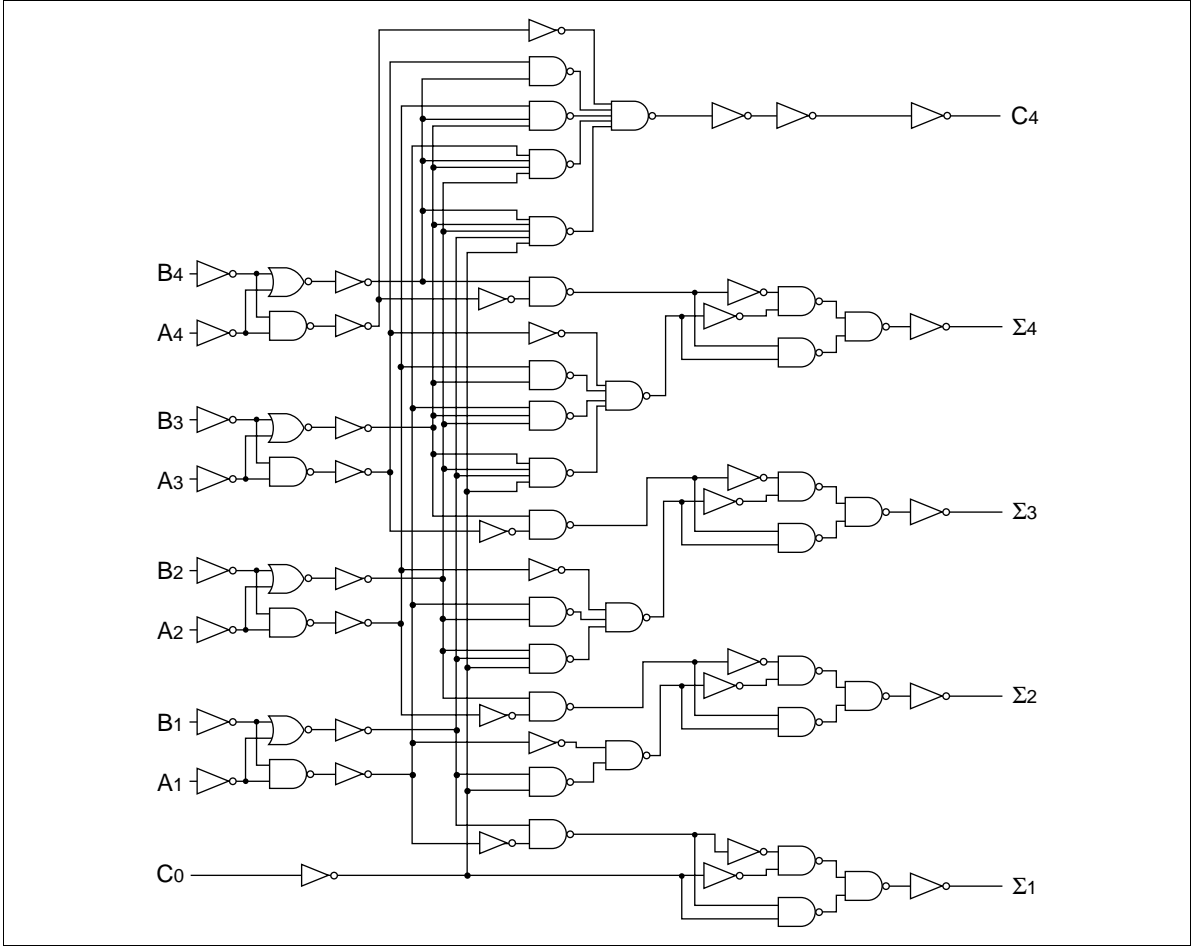
Note: Input conditions at A_1 , B_1 , A_2 , B_2 and C_0 are used to determine outputs Σ_1 and Σ_2 and the value of the internal carry C_2 .

The value at C_2 , A_3 , B_3 , A_4 and B_4 are then used to determine outputs Σ_3 , Σ_4 and C_4 .

Pin Arrangement



Block Diagram (1/2)



DC Characteristics

Item	Symbol	V _{CC} (V)	Ta = 25°C			Ta = -40 to +85°C		Unit	Test Conditions	
			Min	Typ	Max	Min	Max			
Input voltage	V _{IH}	2.0	1.5	—	—	1.5	—	V		
		4.5	3.15	—	—	3.15	—			
		6.0	4.2	—	—	4.2	—			
	V _{IL}	2.0	—	—	0.5	—	0.5			V
		4.5	—	—	1.35	—	1.35			
		6.0	—	—	1.8	—	1.8			
Output voltage	V _{OH}	2.0	1.9	2.0	—	1.9	—	V	Vin = V _{IH} or V _{IL} I _{OH} = -20 μA	
		4.5	4.4	4.5	—	4.4	—			
		6.0	5.9	6.0	—	5.9	—			
		4.5	4.18	—	—	4.13	—			I _{OH} = -4 mA
		6.0	5.68	—	—	5.63	—			I _{OH} = -5.2 mA
	V _{OL}	2.0	—	0.0	0.1	—	0.1	V	Vin = V _{IH} or V _{IL} I _{OL} = 20 μA	
		4.5	—	0.0	0.1	—	0.1			
		6.0	—	0.0	0.1	—	0.1			
		4.5	—	—	0.26	—	0.33			I _{OL} = 4 mA
		6.0	—	—	0.26	—	0.33			I _{OL} = 5.2 mA
Input current	I _{in}	6.0	—	—	±0.1	—	±1.0	μA	Vin = V _{CC} or GND	
Quiescent supply current	I _{CC}	6.0	—	—	4.0	—	40	μA	Vin = V _{CC} or GND, I _{out} = 0 μA	

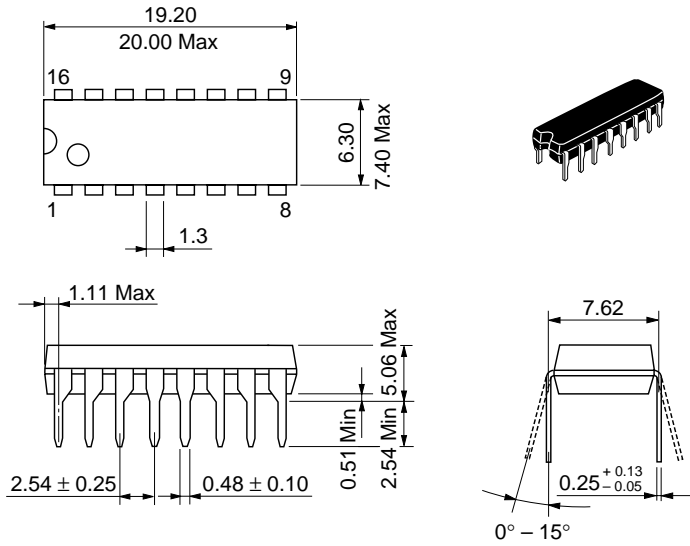
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AC Characteristics ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Item	Symbol	V_{CC} (V)	Ta = 25°C		Ta = -40 to +85°C		Unit	Test Conditions				
			Min	Typ	Max	Min			Max			
Propagation delay time	t_{PLH}	2.0	—	—	150	—	190	ns	C_0 to Σ_i			
			t_{PHL}	4.5	—	19				30	—	38
				6.0	—	—				26	—	33
	t_{PLH}	2.0	—	—	150	—	190	ns	A_i or B_i to Σ_i			
			t_{PHL}	4.5	—	16				30	—	38
				6.0	—	—				26	—	33
	t_{PLH}	2.0	—	—	150	—	190	ns	C_0 to C_4			
			t_{PHL}	4.5	—	17				30	—	38
				6.0	—	—				26	—	33
t_{PLH}	2.0	—	—	150	—	190	ns	A_i or B_i to C_4				
		t_{PHL}	4.5	—	18				30	—	38	
			6.0	—	—				26	—	33	
Output rise/fall time	t_{TLH}	2.0	—	—	75	—	95	ns				
	t_{THL}	4.5	—	5	15	—	19					
		6.0	—	—	13	—	16					
Input capacitance	C_{in}	—	—	5	10	—	10	pF				

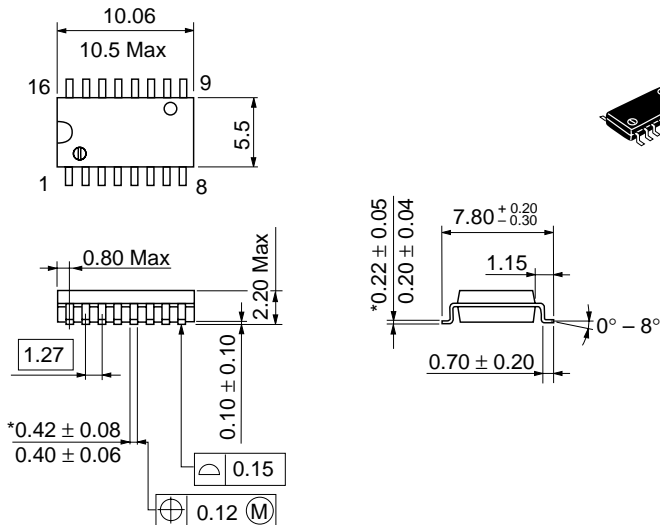
Package Dimensions

Unit: mm



Hitachi Code	DP-16
JEDEC	Conforms
EIAJ	Conforms
Mass (reference value)	1.07 g

Unit: mm

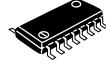
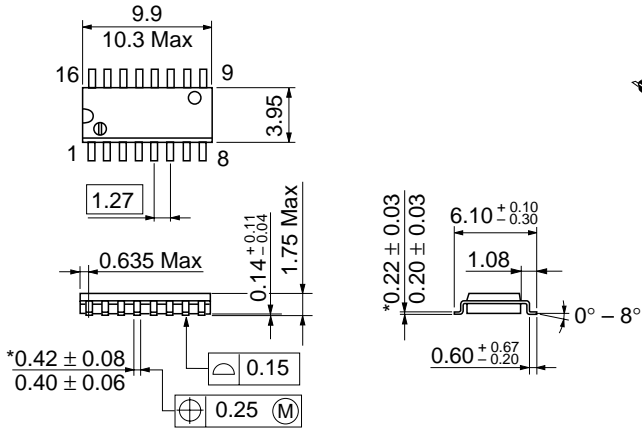


*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-16DA
JEDEC	—
EIAJ	Conforms
Mass (reference value)	0.24 g

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Unit: mm



*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-16DN
JEDEC	Conforms
EIAJ	Conforms
Mass (reference value)	0.15 g

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