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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

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HM62W16258BI Series

4 M SRAM (256-kword × 16-bit)

ADE-203-1072A (Z)
Rev. 1.0
Jun. 10, 1999

Description

The Hitachi HM62W16258BI Series is 4-Mbit static RAM organized 262,144-word × 16-bit. HM62W16258BI Series has realized higher density, higher performance and low power consumption by employing Hi-CMOS process technology. It offers low power standby power dissipation; therefore, it is suitable for battery backup systems. It is packaged in standard 44-pin plastic TSOPII.

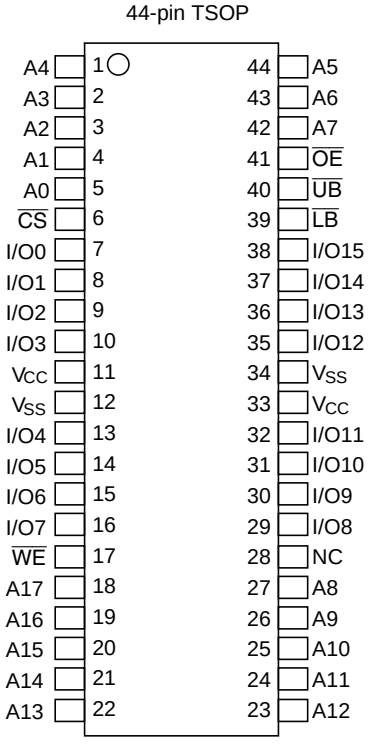
Features

- Single 3.3 V supply: 3.3 V ± 0.3 V
- Fast access time: 70 ns (max)
- Power dissipation:
  - Active: 9.9 mW (typ)
  - Standby: 3.3 µW (typ)
- Completely static memory.
  - No clock or timing strobe required
- Equal access and cycle times
- Common data input and output.
  - Three state output
- Battery backup operation.
- Temperature range: –40 to 85°C

Ordering Information

Type No.	Access time	Package
HM62W16258BLTTI-7	70 ns	400-mil 44-pin plastic TSOPII (normal-bend type) (TTP-44DB)

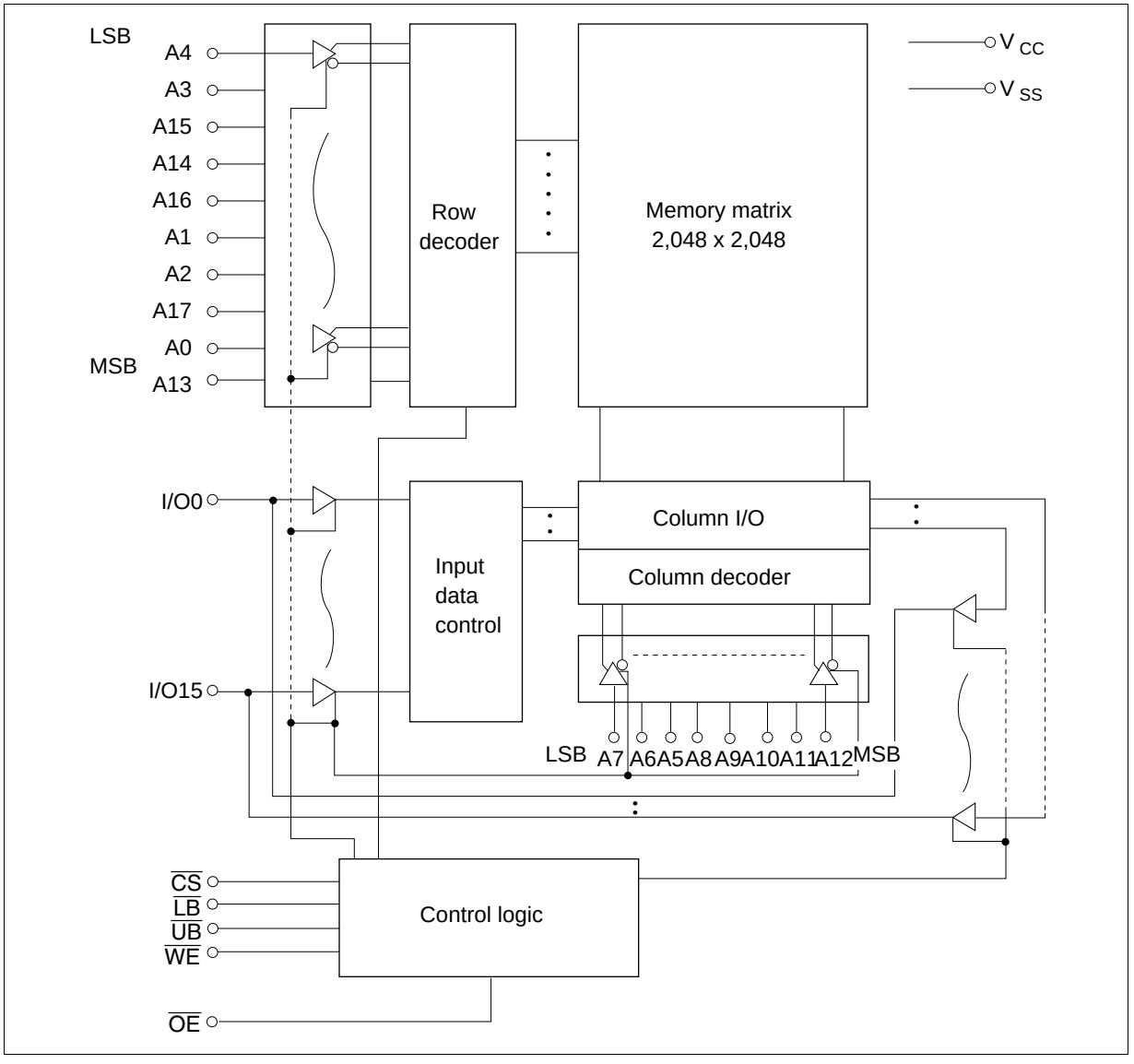
Pin Arrangement



Pin Description

Pin name	Function
A0 to A17	Address input
I/O0 to I/O15	Data input/output
$\overline{CS}$	Chip select
$\overline{WE}$	Write enable
$\overline{OE}$	Output enable
$\overline{LB}$	Lower byte select
$\overline{UB}$	Upper byte select
V_{CC}	Power supply
V_{SS}	Ground
NC	No connection

Block Diagram



Operation Table

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	$\overline{UB}$	$\overline{LB}$	I/O0 to I/O7	I/O8 to I/O15	Operation
H	×	×	×	×	High-Z	High-Z	Standby
×	×	×	H	H	High-Z	High-Z	Standby
L	H	L	L	L	Dout	Dout	Read
L	H	L	H	L	Dout	High-Z	Lower byte read
L	H	L	L	H	High-Z	Dout	Upper byte read
L	L	×	L	L	Din	Din	write
L	L	×	H	L	Din	High-Z	Lower byte write
L	L	×	L	H	High-Z	Din	Upper byte write
L	H	H	×	×	High-Z	High-Z	Output disable

Note: H: V_{IH}, L: V_{IL}, ×: V_{IH} or V_{IL}

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Power supply voltage relative to V_{SS}	V_{CC}	–0.5 to + 4.6	V
Terminal voltage on any pin relative to V_{SS}	V_T	–0.5*[1] to V_{CC} + 0.3*[2]	V
Power dissipation	P_T	1.0	W
Storage temperature range	Tstg	–55 to +125	°C
Storage temperature range under bias	Tbias	–40 to +85	°C

Notes: 1. V_T min: –3.0 V for pulse half-width ≤ 30 ns.
2. Maximum voltage is +4.6 V.

DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{CC}	3.0	3.3	3.6	V	
	V_{SS}	0	0	0	V	
Input high voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V	
Input low voltage	V_{IL}	–0.3	—	0.6	V	1
Ambient temperature range	Ta	–40	—	85	°C	

Note: 1. V_{IL} min: –3.0 V for pulse half-width ≤ 30 ns.

DC Characteristics

Parameter		Symbol	Min	Typ*[1]	Max	Unit	Test conditions
Input leakage current		$\|I_{LI}\|$	—	—	1	µA	Vin = V_{SS} to V_{CC}
Output leakage current		$\|I_{LO}\|$	—	—	1	µA	$\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}, or $\overline{LB}$ = $\overline{UB}$ = V_{IH}, $V_{I/O}$ = V_{SS} to V_{CC}
Operating current		I_{CC}	—	—	20	mA	$\overline{CS}$ = V_{IL}, Others = V_{IH}/V_{IL}, $I_{I/O}$ = 0 mA
Average operating current	HM62W16258BI-7	I_{CC1}	—	—	70	mA	Min. cycle, duty = 100%, $I_{I/O}$ = 0 mA, $\overline{CS}$ = V_{IL}, Others = V_{IH}/V_{IL}
		I_{CC2}	—	3	15	mA	Cycle time = 1 µs, duty = 100%, $I_{I/O}$ = 0 mA, $\overline{CS}$ ≤ 0.2 V, V_{IH} ≥ V_{CC} – 0.2 V, V_{IL} ≤ 0.2 V
Standby current		I_{SB}	—	—	0.3	mA	$\overline{CS}$ = V_{IH}
Standby current		I_{SB1}	—	1	40	µA	0 V ≤ Vin ≤ $\overline{CS}$ ≥ V_{CC} – 0.2 V
Output high voltage		V_{OH}	2.4	—	—	V	I_{OH} = –1 mA
			V_{CC} – 0.2	—	—	V	I_{OH} = –100 µA
Output low voltage		V_{OL}	—	—	0.4	V	I_{OL} = 2 mA
			—	—	0.2	V	I_{OL} = 100 µA

Notes: 1. Typical values are at V_{CC} = 3.0 V, Ta = +25°C and not guaranteed.

Capacitance (Ta = +25°C, f = 1.0 MHz)

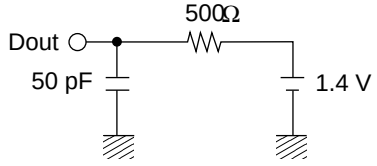
Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	Note
Input capacitance	Cin	—	—	8	pF	Vin = 0 V	1
Input/output capacitance	$C_{I/O}$	—	—	10	pF	$V_{I/O}$ = 0 V	1

Note: 1. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = –40 to +85°C, V_{CC} = 3.3 V ± 0.3 V, unless otherwise noted.)

Test Conditions

- Input pulse levels: V_{IL} = 0.4 V, V_{IH} = 2.4 V
- Input rise and fall time: 5 ns
- Input timing reference levels: 1.4 V
- Output timing reference levels: 1.4 V
- Output load (Including scope and jig)



Read Cycle

		HM62W16258BI			
		-7			
Parameter	**Symbol**	**Min**	**Max**	**Unit**	**Notes**
Read cycle time	t_{RC}	70	—	ns	
Address access time	t_{AA}	—	70	ns	
Chip select access time	t_{ACS}	—	70	ns	
Output enable to output valid	t_{OE}	—	40	ns	
Output hold from address change	t_{OH}	10	—	ns	
$\overline{LB}$, $\overline{UB}$ access time	t_{BA}	—	70	ns	
Chip select to output in low-Z	t_{CLZ}	10	—	ns	2, 3
$\overline{LB}$, $\overline{UB}$ enable to low-z	t_{BLZ}	5	—	ns	2, 3
Output enable to output in low-Z	t_{OLZ}	5	—	ns	2, 3
Chip deselect to output in high-Z	t_{CHZ}	0	25	ns	1, 2, 3
$\overline{LB}$, $\overline{UB}$ disable to high-Z	t_{BHZ}	0	25	ns	1, 2, 3
Output disable to output in high-Z	t_{OHZ}	0	25	ns	1, 2, 3

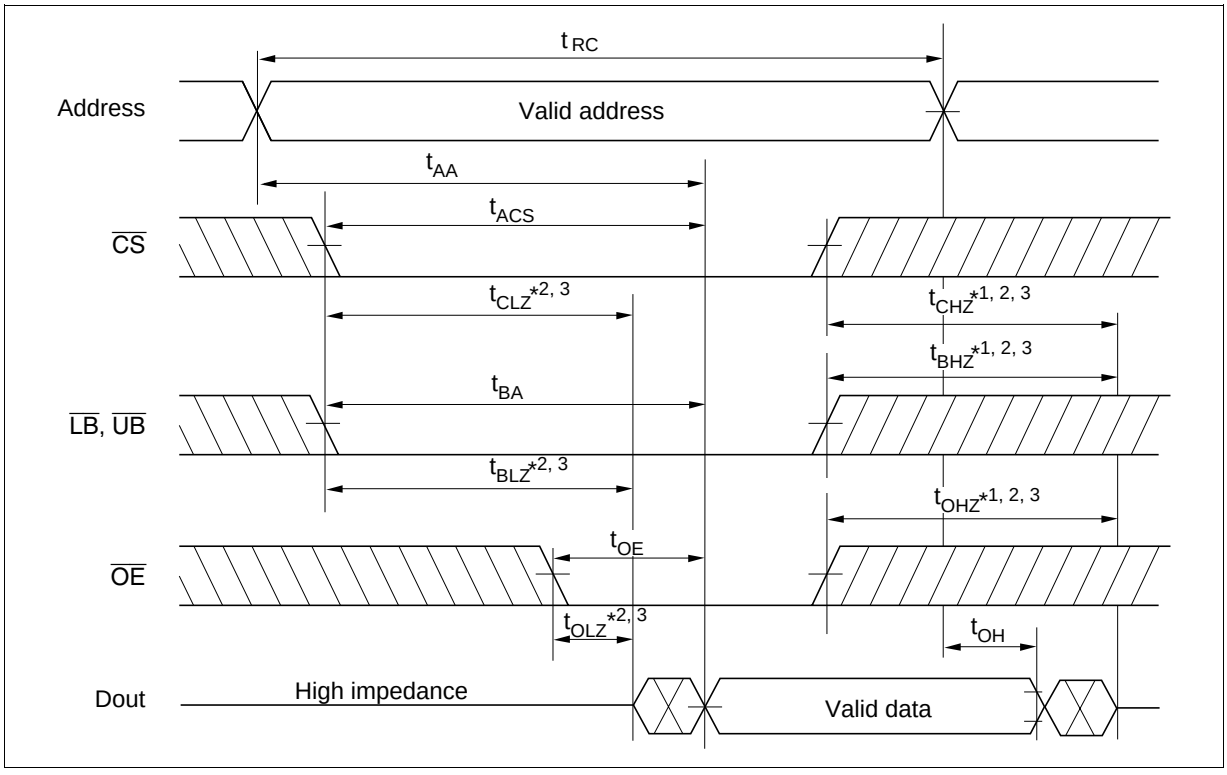
Write Cycle

		HM62W16258BI			
		-7			
Parameter	**Symbol**	**Min**	**Max**	**Unit**	**Notes**
Write cycle time	t_{WC}	70	—	ns	
Address valid to end of write	t_{AW}	60	—	ns	
Chip selection to end of write	t_{CW}	60	—	ns	5
Write pulse width	t_{WP}	50	—	ns	4
$\overline{LB}$, $\overline{UB}$ valid to end of write	t_{BW}	55	—	ns	
Address setup time	t_{AS}	0	—	ns	6
Write recovery time	t_{WR}	0	—	ns	7
Data to write time overlap	t_{DW}	30	—	ns	
Data hold from write time	t_{DH}	0	—	ns	
Output active from end of write	t_{OW}	5	—	ns	2
Output disable to output in High-Z	t_{OHZ}	0	25	ns	1, 2
Write to output in high-Z	t_{WHZ}	0	25	ns	1, 2

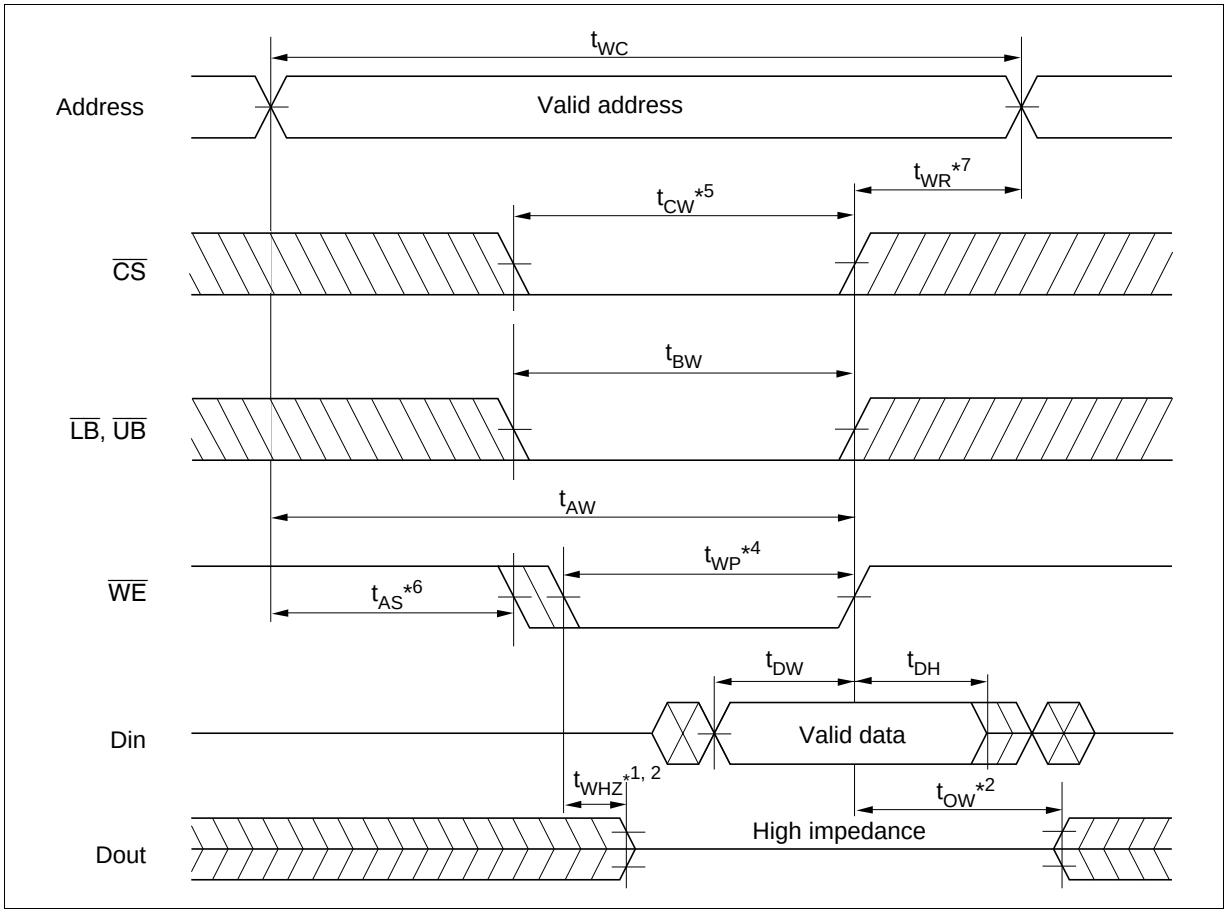
Notes:
1. t_{CHZ}, t_{OHZ}, t_{WHZ} and t_{BHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.
2. This parameter is sampled and not 100% tested.
3. At any given temperature and voltage condition, t_{HZ} max is less than t_{LZ} min both for a given device and from device to device.
4. A write occures during the overlap of a low $\overline{CS}$, a low $\overline{WE}$ and a low $\overline{LB}$ or a low $\overline{UB}$. A write begins at the latest transition among $\overline{CS}$ going low, $\overline{WE}$ going low and $\overline{LB}$ going low or $\overline{UB}$ going low. A write ends at the earliest transition among $\overline{CS}$ going high, $\overline{WE}$ going high and $\overline{LB}$ going high or $\overline{UB}$ going high. t_{WP} is measured from the beginning of write to the end of write.
5. t_{CW} is measured from the later of $\overline{CS}$ going low to the end of write.
6. t_{AS} is measured from the address valid to the beginning of write.
7. t_{WR} is measured from the earliest of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.

Timing Waveform

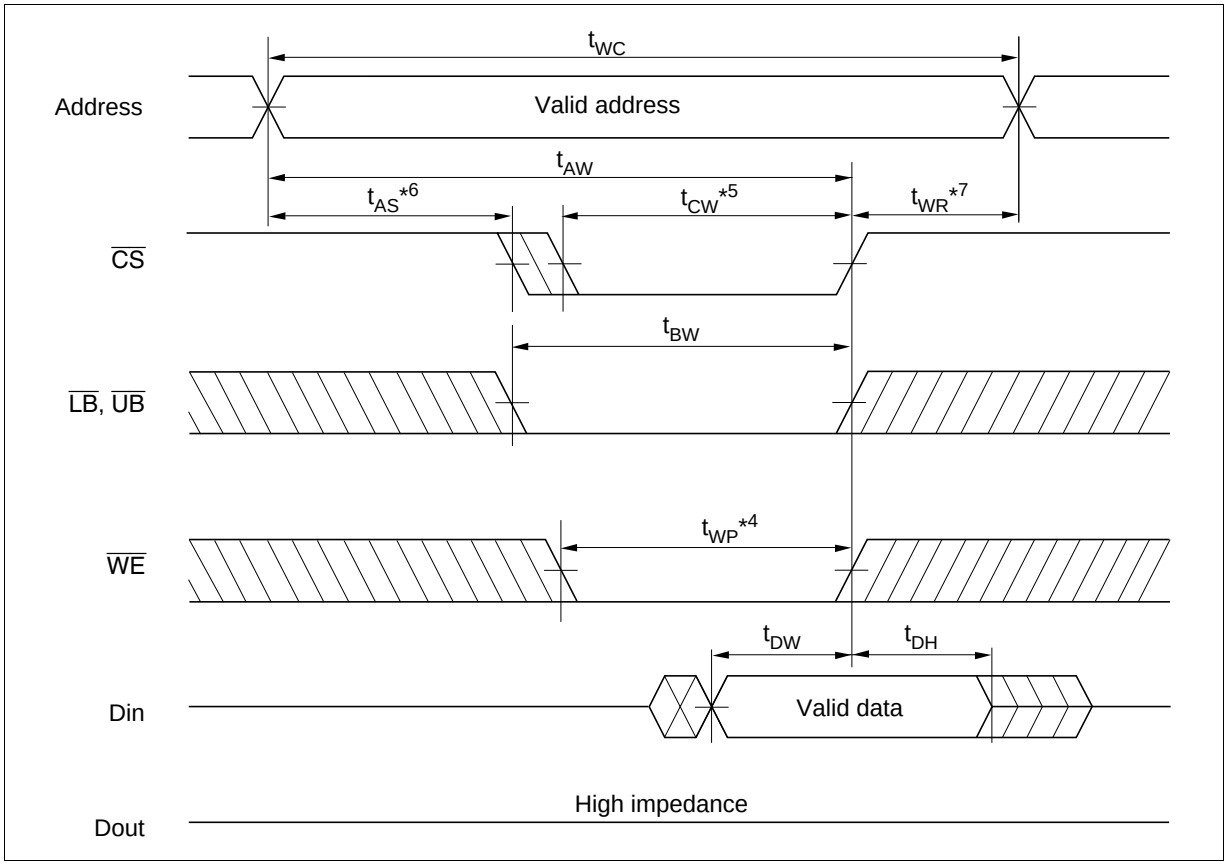
Read Cycle



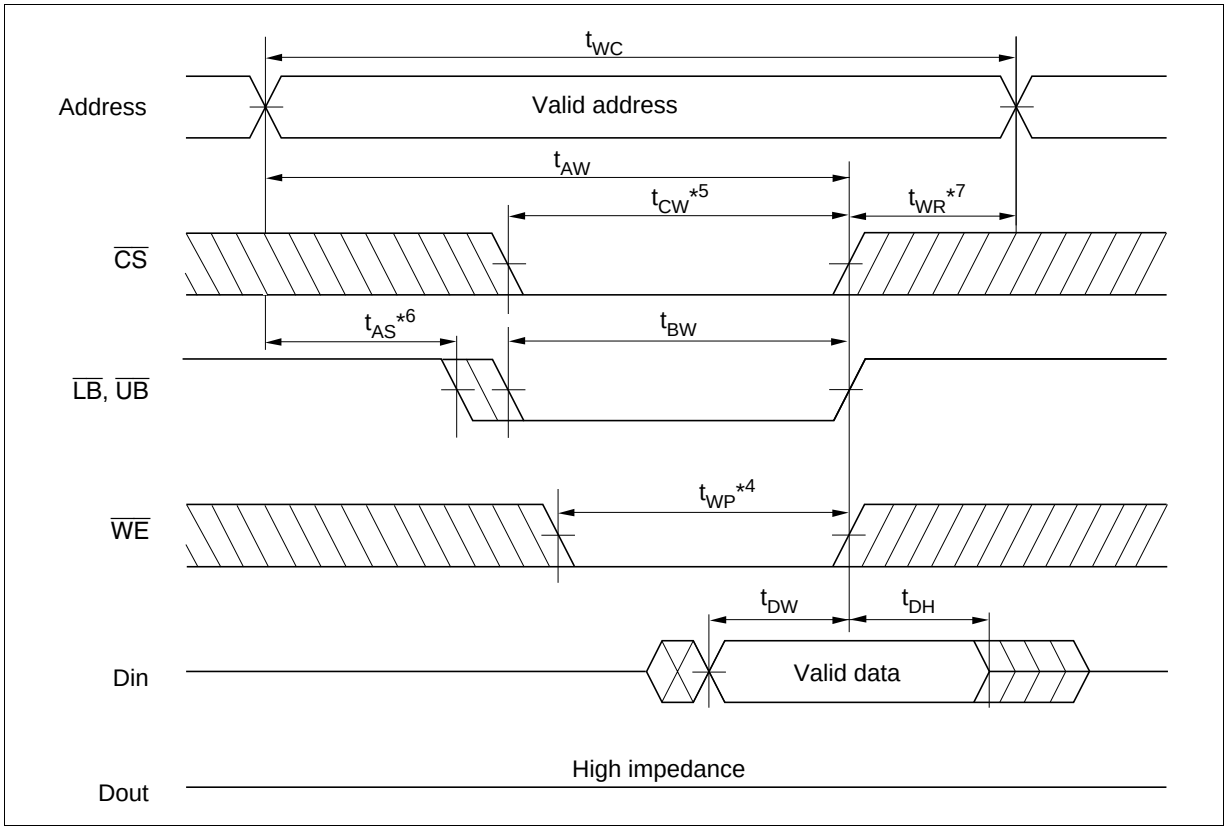
Write Cycle (1) ($\overline{WE}$ Clock)



Write Cycle (2) ($\overline{CS}$ Clock, $\overline{OE}$ = V_{IH})



Write Cycle (3) ($\overline{LB}$, $\overline{UB}$ Clock, $\overline{OE}$ = V_{IH})



Low V_{CC} Data Retention Characteristics (Ta = –40 to +85°C)

Parameter	Symbol	Min	Typ*3	Max	Unit	Test conditions*2
V_{CC} for data retention	V_{DR}	2.0	—	—	V	Vin ≥ 0V (1) $\overline{CS} \geq V_{CC} - 0.2$ V or (2) $\overline{LB} = \overline{UB} \geq V_{CC} - 0.2$ V $\overline{CS} \leq 0.2$ V
Data retention current	I_{CCDR}*1	—	0.8	20	µA	V_{CC} = 3.0 V, Vin ≥ 0V (1) $\overline{CS} \geq V_{CC} - 0.2$ V or (2) $\overline{LB} = \overline{UB} \geq V_{CC} - 0.2$ V $\overline{CS} \leq 0.2$ V
Chip deselect to data retention time	t_{CDR}	0	—	—	ns	See retention waveform
Operation recovery time	t_R	t_{RC}*4	—	—	ns	

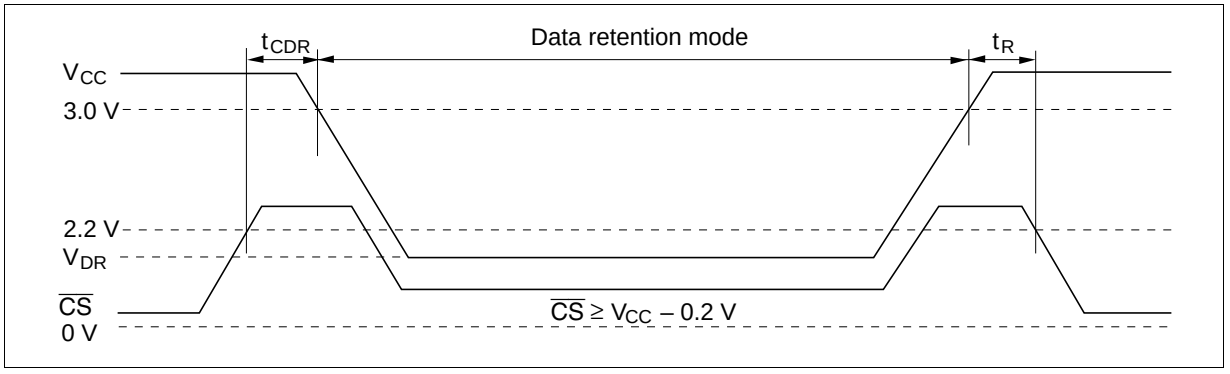
Notes: 1. 10 µA max. at Ta = 0 to +40°C.

2. $\overline{CS}$ controls address buffer, $\overline{WE}$ buffer, $\overline{OE}$ buffer, $\overline{LB}$, $\overline{UB}$ buffer and Din buffer. If $\overline{CS}$ controls data retention mode, Vin levels (address, $\overline{WE}$, $\overline{OE}$, $\overline{LB}$, $\overline{UB}$, I/O) can be in the high impedance state. If $\overline{LB}$, $\overline{UB}$ controls data retention mode, $\overline{LB}$, $\overline{UB}$ must be $\overline{LB} = \overline{UB} \geq V_{CC} - 0.2$ V, $\overline{CS}$ must be $\overline{CS} \leq 0.2$ V. The other input levels (address, $\overline{WE}$, $\overline{OE}$, I/O) can be in the high impedance state.

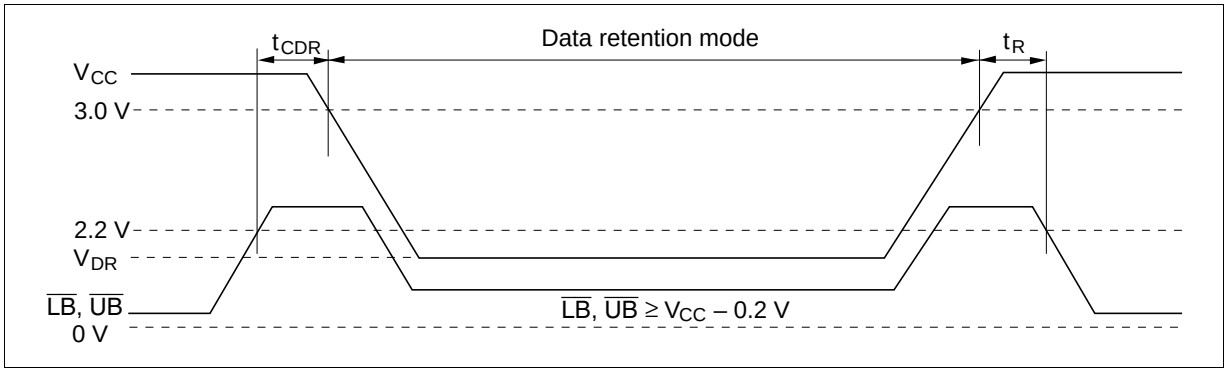
3. Typical values are at V_{CC} = 3.0 V, Ta = +25˚C and not guaranteed.

4. t_{RC} = read cycle time.

Low V_{CC} Data Retention Timing Waveform (1) ($\overline{CS}$ Controlled)



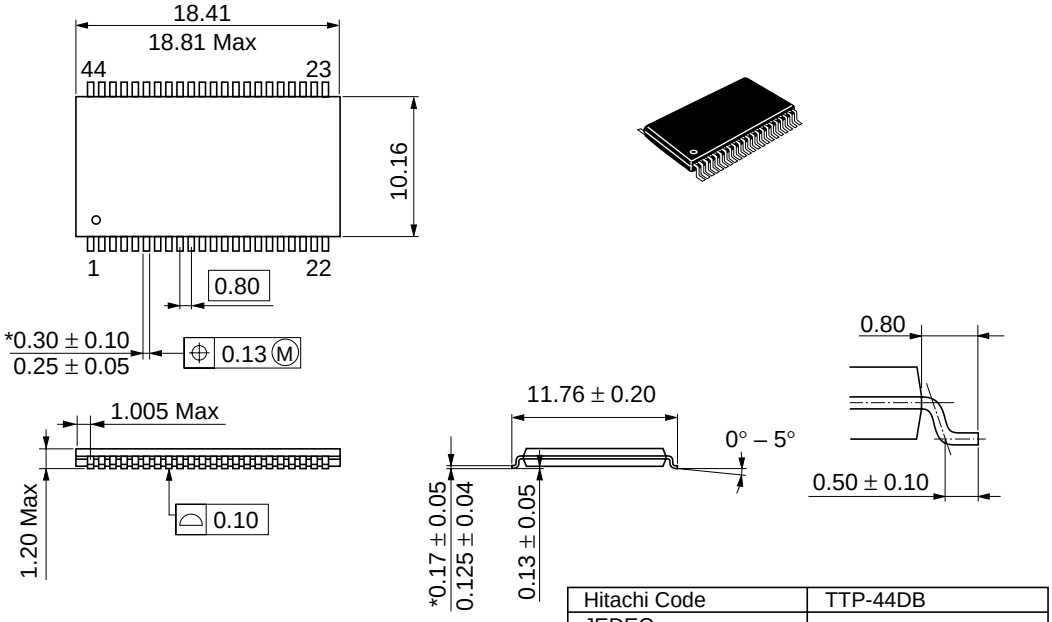
Low V_{CC} Data Retention Timing Waveform (2) ($\overline{LB}$, $\overline{UB}$ Controlled)



Package Dimensions

HM62W16258BLTTI Series (TTP-44DB)

Unit: mm



*Dimension including the plating thickness
Base material dimension

Hitachi Code	TTP-44DB
JEDEC	—
EIAJ	—
Weight (reference value)	0.43 g

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HITACHI

Hitachi, Ltd.
Semiconductor & Integrated Circuits.
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan
Tel: Tokyo (03) 3270-2111 Fax: (03) 3270-5109

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For further information write to:

Hitachi Semiconductor
(America) Inc.
179 East Tasman Drive,
San Jose,CA 95134
Tel: <1> (408) 433-1990
Fax: <1>(408) 433-0223

Hitachi Europe GmbH
Electronic components Group
Dornacher Straße 3
D-85622 Feldkirchen, Munich
Germany
Tel: <49> (89) 9 9180-0
Fax: <49> (89) 9 29 30 00

Hitachi Europe Ltd.
Electronic Components Group.
Whitebrook Park
Lower Cookham Road
Maidenhead
Berkshire SL6 8YA, United Kingdom
Tel: <44> (1628) 585000
Fax: <44> (1628) 778322

Hitachi Asia Pte. Ltd.
16 Collyer Quay #20-00
Hitachi Tower
Singapore 049318
Tel: 535-2100
Fax: 535-1533

Hitachi Asia Ltd.
Taipei Branch Office
3F, Hung Kuo Building. No.167,
Tun-Hwa North Road, Taipei (105)
Tel: <886> (2) 2718-3666
Fax: <886> (2) 2718-8180

Hitachi Asia (Hong Kong) Ltd.
Group III (Electronic Components)
7/F., North Tower, World Finance Centre,
Harbour City, Canton Road, Tsim Sha Tsui,
Kowloon, Hong Kong
Tel: <852> (2) 735 9218
Fax: <852> (2) 730 0281
Telex: 40815 HITEC HX

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