The Analog Mixed Signal Company

ZMD31150

Fast Automotive Sensor Signal Conditioner

Data Sheet

Rev. 1.04 / November 2009

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ZMD31150

Brief Description

The ZMD31150 is a CMOS integrated circuit for highly-accurate amplification and sensor-specific correction of bridge sensor signals. Digital compensation of sensor offset, sensitivity, temperature drift, and non-linearity is accomplished via a 16-bit RISC microcontroller running a correction algorithm, with calibration coefficients stored in an EEPROM.

The ZMD31150 is adjustable to nearly all bridge sensor types. Measured values are provided at the analog voltage output or at the digital ZACwire™ and I²C interface. The digital interface can be used for a simple PC-controlled calibration procedure, in order to program a set of calibration coefficients into an on-chip EEPROM. Thus, a specific sensor and a ZMD31150 are mated digitally: fast, precise, and without the cost overhead associated with trimming by external devices or a laser.

Benefits

- No external trimming components required
- Only a few external protection devices needed
- PC-controlled configuration and One-Shot calibration via I²C or ZACwire™ interface: Simple, cost efficient, quick, and precise
- End-of-Line calibration via I²C or ZACwire™ interface
- High accuracy (0.25% FSO @ -25 to 85° C; 0.5% FSO @ -40 to 125° C)
- The ZMD31150 is optimized for automotive environments by its special protection circuitry and excellent electromagnetic compatibility

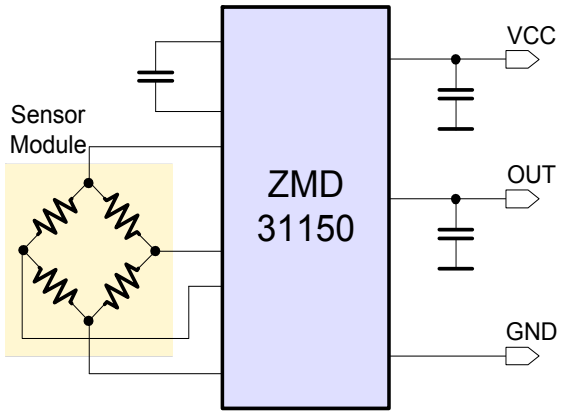
Features

- Digital compensation of sensor offset, sensitivity, temperature drift, and non-linearity
- Adjustable to nearly all bridge sensor types, analog gain of 420, overall gain up to 2000
- Output options: ratiometric analog voltage output (5 - 95% in maximum, 12.4 bit resolution) or ZACwire™ (digital one-wire-interface)
- Temperature compensation: internal or external diode, bridge resistance, thermistor
- Sensor biasing by voltage or constant current
- Sample rate up to 7.8 kHz
- High voltage protection up to 33 V
- Reverse polarity and short circuit protection
- Wide operation temperature -40 to +150 °C
- Supply voltage 4.5 to 5.5 V
- Traceability by user-defined EEPROM entries
- Several safety and diagnostic functions

Available Support

- Evaluation Kit
- Application Notes
- Mass calibration solution

ZMD31150 Overview



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1 Electrical Characteristics

1.1. Absolute Maximum Ratings

Parameters apply in operation temperature range and without time limitations.

Table 1.1 Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Conditions
V_{DDE_AMR}	Supply Voltage [1]	-33	33	V_{DC}	To V_{SSE}, refer to chapter 3 for application circuits
V_{OUT}	Potential at pin AOUT [1]	-33	33	V_{DC}	Related to V_{SSE}
V_{DDA_AMR}	Analog Supply Voltage [1]	-0.3	6.5	V_{DC}	Related to V_{SSA}, V_{DDE} - V_{DDA} < 0.35 V
V_{A_IO} V_{D_IO}	Voltage at all analog and digital IO – Pins	-0.3	V_{DDA} + 0.3	V_{DC}	Related to V_{SSA}
T_{STG}	Storage temperature	-55	150	°C	

1.2. Operating Conditions

All voltages are related to V_{SSA}.

Table 1.2 Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
T_{AMB}	Ambient temperature [2]	-40		150	°C	TQE
T_{AMB_TQA}	Ambient temperature advanced performance [4]	-40		125	°C	TQA
T_{AMB_TQI}	Ambient temperature advanced performance [4]	-25		85	°C	TQI
V_{DDE}	Supply Voltage	4.5	5.0	5.5	V_{DC}	
R_{BR_V}	Bridge Resistance [3, 4]	2		25	kΩ	Bridge Voltage Mode
R_{BR_C}	Bridge Resistance [3, 4]			10	kΩ	Bridge Current Excitation, note I_{BR_MAX}
R_{IBR}	Resistor R_{IBR} [4]	0.07 * R_{BR}			kΩ	$I_{BR} = V_{DDA} / (16 * R_{IBR})$
I_{BR_MAX}	Maximum Bridge Current			2	mA	
V_{BR_TOP}	Maximum Bridge Top Voltage			15/16 * V_{DDA} - 0.3	V	
TC R_{IBR}	TC Current Reference Resistor [4]		50		ppm/K	Behavior influences generated current

[1] Refer to the 'ZMD31150 High Voltage Protection Description' for specification and detailed conditions
[2] Notice temperature profile description in the 'ZMD31150 Dice Package Document' for operation in temperature range > 125 °C
[3] Symmetric behavior and identical electrical properties (especially with regard to the low pass characteristic) of both sensor inputs of the ZMD31150 are required. Unsymmetrical conditions of the sensor and/or external components connected to the sensor input pins of ZMD31150 can generate a failure in signal operation
[4] No measurement in mass production, parameter is guaranteed by design and/or quality observation

1.3. Electrical Parameters

All parameter values are valid on behalf on in chapter 1.2 specified operating conditions (special definitions excluded). All Voltages related to VSSA.

1.3.1. Supply Current and System Operation Conditions

Table 1.3 Parameters for Supply Current and System Operation Conditions

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
I_{VDDE}	Supply current			5.5	mA	Without bridge and load current, $f_{CLK} \leq 3$ MHz
f_{CLK}	Clock frequency	2 [5]	3	4 [5]	MHz	Guaranteed adjustment range

1.3.2. Analog Front-End (AFE) Characteristics

Table 1.4 Parameters for AFE

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
V_{IN_SP}	Input Span	1		275	mV/V	Analog gain: 420 to 2.8
	Analog Offset Compensation Range	-300		300	% V_{IN_SP}	Depends on gain adjust, refer to chapter 2.3.1.1
I_{IN_OFF}	Parasitic differential input offset current [5]	-10 -2		10 2	nA nA	Within T_{AMB}; Within T_{AMB_TQI}
V_{IN_CM}	Common mode input range	0.29 * V_{DDA}		0.65 * V_{DDA}	V	Depends on gain adjust, no XZC, refer to chapter 2.3.1

1.3.3. Temperature Measurement (refer chapter 0)

Table 1.5 Parameters for Temperature Measurement

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
A_{TSED}	External temperature diode channel gain	300		1300	ppm FS / mV	
I_{TSE}	External temperature diode bias current	6	10	20	µA	
	External temperature diode input range *	0		1.5	V	
A_{TSER}	External temperature resistor channel gain	1200		3500	ppm FS / (mV/V)	
V_{TSER}	External temperature resistor input range *	0		600	mV/V	
ST_{TSI}	Internal temperature diode sensitivity	700		2700	ppm FS /K	raw values – without conditioning

[5] No measurement in mass production, parameter is guaranteed by design and/or quality observation

1.3.4. Sensor Connection Check

Table 1.6 Parameters for Sensor Connection Check

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
RSCC_min	Sensor connection loss	100			kΩ	detection threshold
RSSC_short	Sensor input short	0		50	Ω	short detection guaranteed
RSSC_pass	Sensor input no short	1000			Ω	short is never detected

1.3.5. AD-Conversion

Table 1.7 Parameters for AD-Conversion

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
r_{ADC}	A/D Resolution *	13		16	Bit	
DNL_{ADC}	DNL *			0.95	LSB	r_{ADC} =13Bit, f_{CLK}=3MHz, best fit, 2nd order, complete AFE, 5.3.5.5
INL_{ADC}	INL TQA *			4	LSB	
INL_{ADC}	INL TQE			5	LSB	
Range	ADC Input Range	10		90	%VDDA	

1.3.6. DAC & Analog Output (Pin AOUT)

Table 1.8 Parameters for DAC & Analog Output

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
r_{DAC}	D/A Resolution		12		Bit	analog output, 10-90%
$I_{SRC/SINK\_OUT}$	Output current sink and source for VDDE=5V			2.5 5	mA	Vout: 5-95%, RLOAD>=2k□ Vout: 10-90%, RLOAD>=1k□
I_{OUT_max}	Short circuit current	-25		25	mA	to VSSE/VDDE[6]
V_{SR_OUT95} V_{SR_OUT90}	Addressable output signal range	0.05 0.1		0.95 0.9	VDDE	@ RLOAD>=2k□ @ RLOAD>=1k□
SR_{OUT}	Output slew rate *	0.1			V/□s	CLOAD < 50nF
R_{OUT_DIA}	Output resistance in diagnostic mode			82	Ω	Diagnostic Range: <4|96>%, RLOAD>=2k□ <8|92>%, RLOAD>=1k□
C_{LOAD}	Load capacitance *			150	nF	C3 + CL (refer chapter 3)
DNL_{OUT}	DNL	-1.5		1.5	LSB	
INL_{OUT}	INL TQA *	-5		5	LSB	best fit, rDAC =12Bit
INL_{OUT}	INL TQE	-8		8	LSB	best fit, rDAC =12Bit
I_{LEAK_OUT}	Output Leakage current @ 150grd	-25		25	µA	in case of power or ground loss

[6] minimum output voltage to VDDE or maximum output voltage to VSSE

1.3.7. System Response

Table 1.9 Parameters for System Response

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
t_{STA}	Startup time [2]			5	ms	to 1st output, fclk=3MHz, no ROM check, ADC: 14bit & 2nd order
t_{RESP}	Response time (100% jump) *	256		512	µs	f_{CLK}=4MHz, 13Bit, 2nd order, refer chapter 0
	Bandwidth *		5		kHz	comparable to analog SSCs
$V_{NOISE,PP}$	Analog Output Noise Peak-to-Peak *			10	mV	shorted inputs, gain= bandwidth ≤ 10kHz
$V_{NOISE,RMS}$	Analog Output Noise RMS *			3	mV	shorted inputs, gain= bandwidth ≤ 10kHz
RE_{OUT_5}	Ratiometricity Error			1000	ppm	maximum error of VDDE=5V to 4.5/5.5V
F_{ALL} TQI F_{ALL} TQA F_{ALL} TQE	Overall failure (deviation from ideal line including INL, gain, offset & temp errors)		0.25 (0.1) 0.5 (0.25) 1.0 (0.5)		% FS	13Bit 2nd order ADC, fclk<=3MHz, XZC=0 1, no sensor caused effects; inside of parenthesis: digital readout

1.4. Interface Characteristics & EEPROM

1.4.1. I²C Interface (refer ZMD31150_FD_Rev_*.pdf for timing details)

Table 1.10 Parameters for I²C Interface

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
$V_{I2C\_IN\_H}$	Input-High-Level *	0.8			VDDA	
$V_{I2C\_IN\_L}$	Input-Low-Level *			0.2	VDDA	
$V_{I2C\_OUT\_L}$	Output-Low-Level *			0.15	VDDA	Open Drain, I_{OL}<2mA
C_{SDA}	SDA load capacitance *			400	pF	
f_{SCL}	SCL clock frequency *			400	kHz	
R_{I2C}	Internal pullup resistor *	25		100	kΩ	

[2] Depends on resolution and configuration - start routine begins approximately 0.8ms after power on

* no measurement in mass production, parameter is guarantied by design and/or quality observation
1 XZC is active: additional overall failure of 25ppm/K for XZC=31 in maximum, failure decreases linear for XZC adjusts lower than 31

1.4.2. ZACwire™ One Wire Interface (OWI)

Table 1.11 Parameters for ZACwire™

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
$V_{OWI\_IN\_L}$	Input-Low-Level *			0.2	VDDA	
$V_{OWI\_IN\_H}$	Input-High-Level *	0.75			VDDA	
$V_{OWI\_OUT\_L}$	Output-Low-Level *			t.b.d.	VDDA	Open Drain, I_{OL}<?mA
	Start Window *	96	175	455	ms	typ: @ fclk=3MHz

1.4.3. EEPROM

Table 1.12 Parameters for EEPROM

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
T_{AMB_EEP}	Ambient temperature EEPROM programming *	-40		150	°C	
n_{WRI_EEP}	Write cycles *			100k 100		@write <= 85°C @write up to 150°C
n_{READ_EEP}	Read cycles *			$8 * 10^8$		<=175°C[2]
t_{RET_EEP}	Data retention *			15	a	1300h @ 175°C [3] (=100000h@55°C & 27000h@125°C & 3000h@150°C)
t_{WRI_EEP}	Programming time *		12		ms	per written word, fclk=3MHz

* no measurement in mass production, parameter is guarantied by design and/or quality observation
[2] valid for the dice, notice additional package and temperature version caused restrictions
[3] over lifetime and valid for the dice, use calculation sheet “ZMD_TempProfile_Rev_*.xls” for temperature stress calculation, notice additional package and temperature version caused restrictions

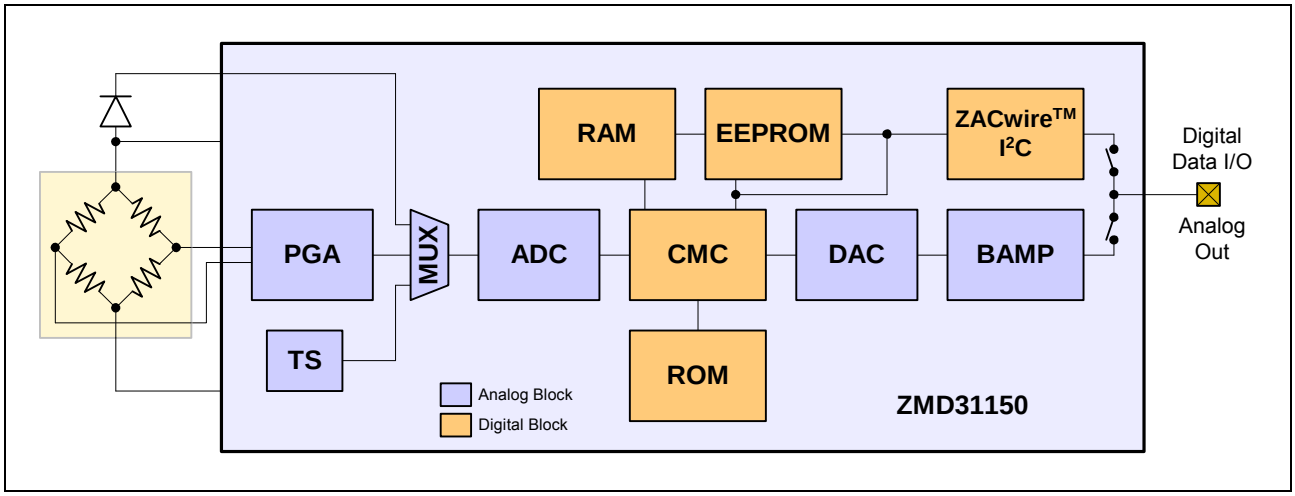
2 Circuit Description

2.1. Signal Flow

The ZMD31150's signal path is partly analog and partly digital. The analog part is realized differentially – this means, the differential bridge sensor signal is internally handled via two signal lines, which are rejected symmetrically around an internal common mode potential (analog ground = $V_{DDA}/2$).

Consequently, it is possible to amplify positive and negative input signals, which are located within the common mode range of the signal input.

Figure 2.1 Block Diagram of the ZMD31150



The differential signal from the bridge sensor is pre-amplified by the Programmable Gain Amplifier (PGA). The Multiplexer (MUX) transmits the signals from either the bridge sensor, the external diode, or the separate temperature sensor, to the Analog-to-Digital Converter (ADC) in a certain sequence (instead of the temperature diode, the internal pn-junction (TS) can be used optionally). Afterwards, the ADC converts these signals into digital values.

The digital signal correction takes place in the calibration microcontroller (CMC). It is based on a correction formula located in the ROM, and on sensor-specific coefficients stored in the EEPROM during calibration. Dependent on the programmed output configuration, the corrected sensor signal is output as an analog value or in a digital format (I^2C^{TM}, ZACwire™). The configuration data and the correction parameters can be programmed into the EEPROM via the digital interfaces.

2.2. Application Modes

For each application, a configuration set has to be established (generally prior to calibration) by programming the on-chip EEPROM regarding to the following modes:

- Sensor Channel
  - Sensor Mode: Ratiometric bridge excitation in voltage or current supply mode.
  - Input Range: The gain adjustment of the AFE with respect to the maximum sensor signal span and the zero point of the ADC has to be chosen.

- Additional Offset Compensation (XZC): The extended analog offset compensation has to be enabled, if required; e.g., if the sensor offset voltage is near to or larger than the sensor span.
- Resolution/Response Time: The A/D converter has to be configured for resolution and converting scheme, or ADC order (first or second order). These settings influence the sampling rate and the signal integration time, and thus, the noise immunity.

- Temperature
  - Temperature Measurement: The source for the temperature correction has to be chosen.

2.3. Analog Front End (AFE)

The Analog Front End (AFE) consists of the Programmable Gain Amplifier (PGA), the Multiplexer (MUX), and the Analog-to-Digital Converter (ADC).

2.3.1. Programmable Gain Amplifier (PGA)

The following table shows the adjustable gains, the sensor signal spans, and the allowed common mode range.

Table 2.1 Adjustable gains, resulting sensor signal spans, and common mode ranges

No.	Overall Gain a_{IN}	Max. Span V_{IN_SP} [mV/V] [1)]	Gain Amp1	Gain Amp2	Gain Amp3	Input common mode range V_{IN_CM} as % of VDDA [2)]	
						XZC = Off	XZC = On
1	420	1.8	30	7	2	29 to 65	45 to 55
2	280	2.7	30	4.66	2	29 to 65	45 to 55
3	210	3.6	15	7	2	29 to 65	45 to 55
4	140	5.4	15	4.66	2	29 to 65	45 to 55
5	105	7.1	7.5	7	2	29 to 65	45 to 55
6	70	10.7	7.5	4.66	2	29 to 65	45 to 55
7	52.5	14.3	3.75	7	2	29 to 65	45 to 55
8	35	21.4	3.75	4.66	2	29 to 65	45 to 55
9	26.3	28.5	3.75	3.5	2	29 to 65	45 to 55
10	14	53.75	1	7	2	29 to 65	45 to 55
11	9.3	80	1	4.66	2	29 to 65	45 to 55
12	7	107	1	3.5	2	29 to 65	45 to 55
13	2.8	267	1	1.4	2	32 to 57	not applicable

1) Recommended internal signal range is 75% of supply voltage in maximum.
Span is calculated by the following formula: Span = 75% / gain

1) Bridge in voltage mode, containing maximum input signal (with XZC: +300% Offset), 14-bit accuracy. Refer to the 'ZMD31150 Functional Description' for usable input signal/common mode range at bridge in current mode.

2.3.1.1. Offset Compensation

The ZMD31150 supports two methods of sensor offset compensation (zero shift):

- Digital offset correction
- XZC - Analog compensation for large offset values (up to in maximum approximately 300% of span, depending on gain adjustment)

Digital sensor offset correction will be processed during the digital signal correction/conditioning by the calibration microcontroller (CMC). Analog sensor offset pre-compensation will be needed for compensation of large offset values, which would overdrive the analog signal path by uncompensated gaining. For analog sensor offset pre-compensation, a compensation voltage will be added in the analog pre-gaining signal path (coarse offset removal). The analog offset compensation in the AFE can be adjusted by 6 EEPROM bits.

Table 2.2 Analog Zero Point Shift Ranges (XZC)

PGA gain a_{IN}	Max. Span V_{IN_SP} [mV/V]	Offset shift per step in % of full span	Approx. maximum offset shift [mV/V]	Approx. maximum shift in [% V_{IN_SP}] (@ ± 31)
420	1.8	12.5 %	7.8	388 %
280	2.7	7.6 %	7.1	237 %
210	3.6	12.5 %	15.5	388 %
140	5.4	7.6 %	14.2	237 %
105	7.1	5.2 %	13	388 %
70	10.7	7.6 %	28	237 %
52.5	14.3	5.2 %	26	388 %
35	21.4	7.6 %	57	237 %
26.3	28.5	5.2 %	52	161 %
14	53.75	12.5 %	194	388 %
9.3	80	7.6 %	189	237 %
7	107	5.2 %	161	161 %
2.8	267	0.83 %	72	26 %

2.3.2. Measurement Cycle

The Multiplexer selects, depending on EEPROM settings, the following inputs in a certain sequence.

- Temperature measured by external diode or thermistor, internal pn-junction or bridge
- Internal offset of the input channel (V_{OFF})
- Pre-amplified bridge sensor signal

The complete measurement cycle is controlled by the CMC. The cycle diagram at the right shows its principle structure.

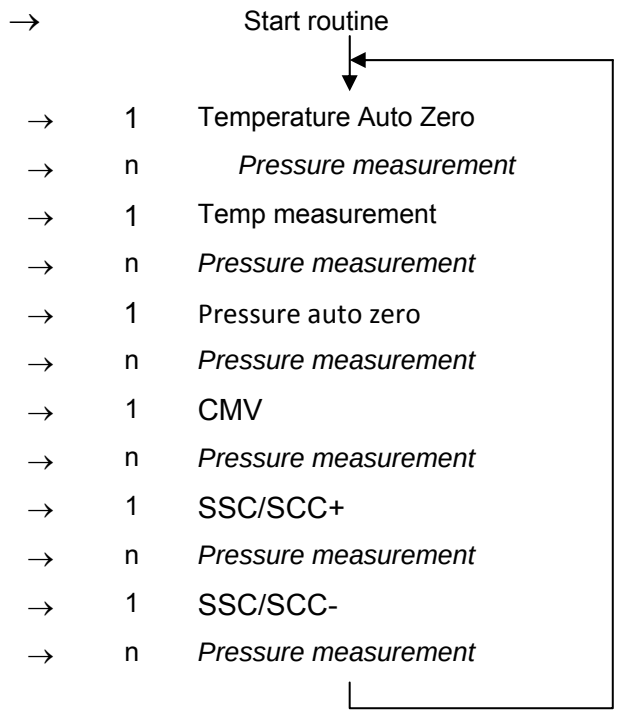
The EEPROM adjustable parameters are:

- n=<1,31>: Pressure measurement count

After power on the start routine is called, which contains all needed measurements once.

Remark: The tasks “CMV”, “SSC/SCC+” and “SSC/SCC-“ are contained independent from EEPROM configuration always in cycle.

Figure 2.2 Measurement Cycle



2.3.3. Analog-to-Digital Converter

The ADC is an integrating AD-Converter in full differential switched capacitor technique.

Programmable ADC-resolutions are r_{ADC}=<13,14> and with segmentation <15,16> bit.

It can be used as first or second order converter. In the **first order** mode it is inherently monotone and insensitive against short and long term instability of the clock frequency. The conversion cycle time depends on the desired resolution and can be roughly calculated by:

$$t_{CYC\_1} = 2^{r}\ \mu s / 2 / f_{CLK}$$

In the **second order** mode two conversions are stacked with the advantage of much shorter conversion cycle time and the drawback of a lower noise immunity caused by the shorter signal integration period. The conversion cycle time at this mode is roughly calculated by:

$$t_{CYC\_2} = 2^{(r+3)/2} / 2 / f_{CLK}$$

The calculation formulas give a overview about conversion time for one AD-conversion. Refer Calculation sheet “ZMD31150_Bandwidth_Calculation_Rev*.xls” for detailed calculation of sampling time and bandwidth.

The result of the AD conversion is a relative counter result corresponding to the following equation:

$$Z_{ADC} = 2^{r} * (V_{ADC\_DIFF} / V_{ADC\_REF} - RS_{ADC})$$

Z_{ADC}: number of counts (result of the conversion)

r: adjusted resolution in bit

V_{ADC/REF_DIFF}: differential input/reference voltage of ADC

RS_{ADC}: digital ADC Range Shift (RS_{ADC} = $^1/_{16}$, $^1/_8$, $^1/_4$, $^1/_2$, controlled by the EEPROM content)

With the RS_{ADC} value a sensor input signal can be shifted in the optimal input range of the ADC.

Table 2.3 Analog Output resolution versus sample rat

ADC Adjustment		approx. Output Resolution *1)		Sample Rate f_{CON} *2)		Averaged Bandwidth @	
Order	r_{ADC}	Digital	Analog	f_{CLK}=3MHz	f_{CLK}=4MHz	f_{CLK}=3MHz	f_{CLK}=4MHz
O_{ADC}	Bit	Bit	Bit	Hz	Hz	Hz	Hz
1	13	13	12	345	460	130	172
1	14	14	12	178	237	67	89
1	15	14	12	90	120	34	45
1	16	14	12	45	61	17	23
2	13	13	12	5859	7813	2203	2937
2	14	14	12	3906	5208	1469	1958
2	15	14	12	2930	3906	1101	1468
2	16	14	12	1953	2604	734	979

**1) ADC resolution should be one bit higher then applied output resolution, if AFE gain is adjusted in such manner, that input range is used more than 50%. Otherwise ADC resolution should be more than one bit higher than applied output resolution.*

**2) The sampling rate (AD conversion time) is only a part of the whole cycle, refer "ZMD31150 bandwidth calculation sheet" for detailed information*

Remark: ADCs reference voltage ADC_{VREF} is defined by the potential between <VBR_T> and <VBR_B> (or <VDDA> to <VSSA>, if CFGAPP:BREF=1). The theoretically input range ADC_{RANGE_INP} of the ADC is equivalent to ADCs reference voltage.

In practice ADCs input range should be used in maximum from 10% to 90% of ADC_{RANGE_INP} - a necessary condition for abiding specified accuracy, stability and nonlinearity parameters of AFE. These condition is also valid for whole temperature range and all applicable sensor tolerances. Inside of ZMD31150 is no failsafe task implemented, which verifies abiding of these condition.

2.4. Temperature Measurement

The ZMD31150 supports four different methods for temperature data acquiring needed for calibration of the sensor signal in temperature range. Temperature data can be acquired using:

- an internal pn-junction temperature sensor,
- an external pn-junction temperature sensor connected to sensor top potential (VBRTOP),
- an external resistive half bridge temperature sensor and
- the temperature coefficient of the sensor bridge at bridge current excitation.

Refer “ZMD31150 Functional Description” for a detailed explanation of temperature sensor adaptation and adjustment.

2.5. System Control and Conditioning Calculation

The system control supports the following tasks/features:

- control the measurement cycle regarding to the EEPROM-stored configuration data
- 16 bit correction calculation for each measurement signal using the EEPROM stored calibration coefficients and ROM-based algorithms = signal conditioning
- manage start up sequence and start signal conditioning
- handle communication requests received by the serial interface
- failsafe tasks for the functions of ZMD31150 and message detected errors with diagnostic states

Refer “ZMD31150_FunctionalDescription_Rev_*.PDF” for a detailed description.

2.5.1. Operation Modes

The internal state machine represents three main states:

- the continuous running signal conditioning mode – called **N**ormal **O**peration **M**ode: NOM
- the calibration mode with access to all internal registers and states – called **C**ommand **M**ode: CM
- the failure messaging mode – called **D**iagnostic **M**ode: DM

2.5.2. Start Up Phase[7]

The start up phase consist of following parts:

1 internal supply voltage settling phase (=potential VDDA-VSSA) – finished by disabling the reset signal through the power on clear block (POC). Refer “ZMD31150_HighVoltageProt_Rev_*.PDF”, chapter 4 for power on/off thresholds.
Time (for beginning with VDDA-VSSA=0V): 500□s to 2000□s, AOUT: tristate

2 system start, EEPROM read out and signature check (and ROM-check, if CFGAPP:CHKROM=1).
Time: ~200□s (~9000□s with ROM-check – 28180clocks), AOUT: LOW (DM)

3 processing the start routine of signal conditioning (all measures & conditioning calculation).
Time: 5x AD conversion time, AOUT behavior depending on adjusted OWI mode (2.6):
- OWIANA & OWIDIS => AOUT: LOW (DM)
- OWIWIN & OWIENA => AOUT: tristate

The analog output AOUT will be activated at the end of start up phase depending on adjusted output and communication mode (2.6). In case of detected errors Diagnostic Mode (DM) is activated and diagnostic output signal is driven at the output.

After the start up phase the continuous running measurement and calibration cycle is started. Refer “ZMD31150_BandwidthCalculation_Rev_*.xls” for detailed information about output update rate.

[7] All described timings are roughly estimated values and correlates with internal clock frequency. Timings estimated for fclk=3MHz.

2.5.3. Conditioning Calculation

The digitalized value for pressure (acquired raw data) is processed with the correction formula to remove offset and temperature dependency and to compensate non-linearity up to 3rd order. The result of the correction calculation is a non-negative 15 Bit value for pressure (P) in the range [0; 1). This value P is clipped with programmed limitation coefficients and continuously written to the output register of the digital serial interface and the output DAC.

Note: The conditioning includes up to third order nonlinearity sensor input correction. The available adjustment ranges depend on the specific calibration parameters, for a detailed description refer to "ZMD31150 Functional Description". To give a rough idea: Offset compensation and linear correction are only limited by the loose of resolution it will cause, the second order correction is possible up to about 30% full scale difference to straight line, third order up to about 20% (ADC resolution = 13bit). The used calibration principle is able to reduce present nonlinearity errors of the sensor up to 90%. The temperature calibration includes first and second order correction and should be fairly sufficient in all relevant cases. ADC resolution influences also calibration possibilities – 1 bit more resolution reduces calibration range by approximately 50%. Calculation input data width is in maximum 14bit. 15 & 16bit ADC resolution mode uses only a 14 bit segment of ADC range.

2.6. Analog Output AOUT

The analog output is used for output the analog signal conditioning result and for "End of Line" communication via the ZACwire™ interface (one wire communication interface - OWI). The ZMD31150 supports four different modes of the analog output in combination with OWI behavior:

- OWIENA: analog output is deactivated, OWI communication is enabled
- OWIDIS: analog output is active (~2ms after power on), OWI communication is disabled
- OWIWIN: analog output will be activated after time window,
  OWI communication is enabled in time window of ~500ms in maximum,
  transmission of "START_CM" command has to be finished during time window

- OWIANA: analog output will be activated after ~2ms power on time,
  OWI communication is enabled in time window of ~500ms in maximum,
  transmission of "START_CM" command has to be finished during time window,
  to communicate the internal driven potential at AOUT has to be overwritten
  by the external communication master (AOUT drive capability is current limited)

The analog output potential is driven by an unity gain output buffer, those input signal is generated by an 12.4bit resistor string DAC. The output buffer (BAMP) – a rail-to-rail OPAMP - is offset compensated and current limited. So a short circuit of analog output to ground or power supply does not damage the ZMD31150.

2.7. Serial Digital Interface

The ZMD31150 includes a serial digital interface (SIF), which is used for communication with the circuit to realize calibration of the sensor module. The serial interface is able to communicate with two communication protocols – I^2C™ and ZACwire™ (an one wire communication interface – also called OWI). The OWI can be used to realize a "End of Line" calibration via the analog output AOUT of the complete assembled sensor module.

Refer "ZMD31150 Functional Description" for a detailed description of the serial interfaces and communication protocols.

2.8. Failsafe Features, Watchdog and Error Detection

The ZMD31150 detects various possible errors. A detected error is signalized by changing the interal status in diagnostic mode (DM). In this case the analog output is set to LOW (minimum possible output value = lower diagnostic range – LDR) and the output registers of the digital serial interface are set to a significant error code.

A watchdog oversees the continuous working of the CMC and the running measurement loop. The operation of the internal clock oscillator is verified continuously by oscillator fail detection.

A check of the sensor bridge for broken wires is done permanently by two comparators watching the input voltage of each input (sensor connection and short check). Additionally the common mode voltage of the sensor and sensor input short is watched permanently (sensor aging).

Different functions and blocks in digital part - like RAM-, ROM-, EEPROM- and register content - are watched continuously. Refer “ZMD31150 Functional Description” for a detailed description of safety features and methods of error messaging.

2.9. High Voltage, Reverse Polarity and Short Circuit Protection

The ZMD31150 is designed for 5V power supply operation.

The ZMD31150 and the connected sensor is protected from overvoltage and reverse polarity damage by an internal supply voltage limiter. The analog output AOUT can be connected (short circuit, overvoltage and reverse) with all potentials in protection range under all potential conditions at the pins VDDE and VSSE.

All external components – explained in application circuit in chapter 3 – are required to guarantee these operation, the protection is no time limited. Refer “ZMD31150 High Voltage Protection Description” for a detailed description of protection cases and conditions.

3 Application Circuit Examples

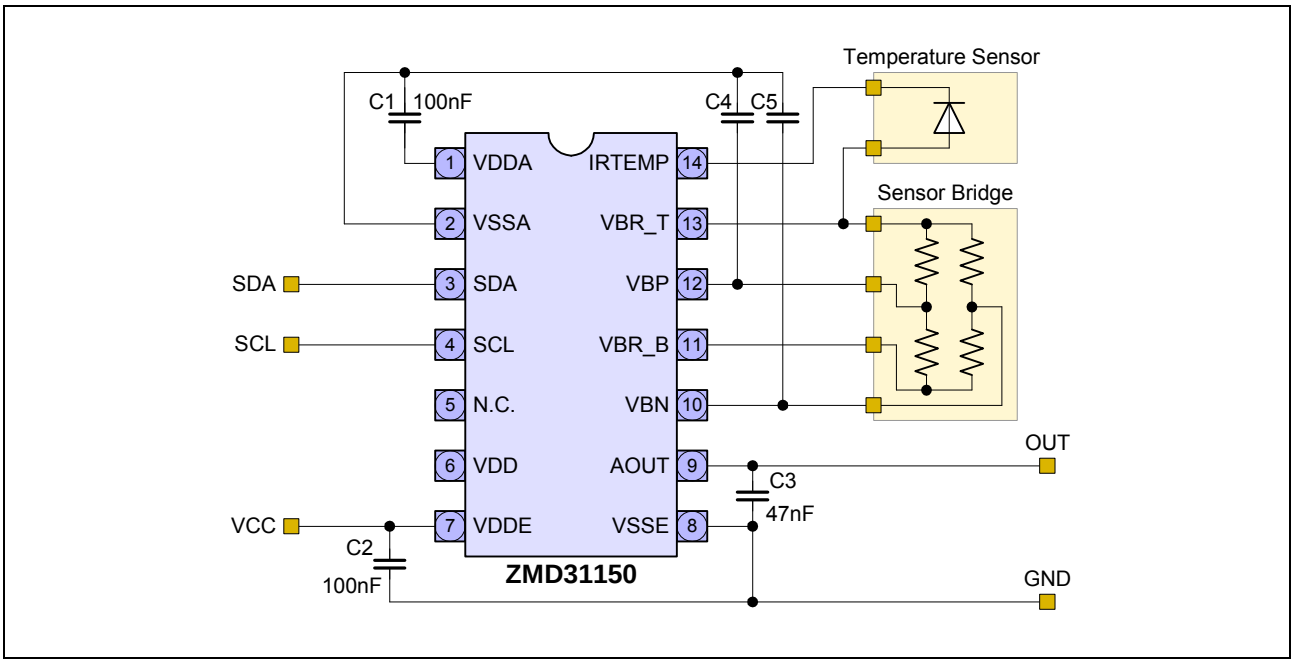
The application circuits contain external components, which are needed for overvoltage, reverse polarity, and short circuit protection.

Note: Check also the available 'ZMD31150 Application Notes' for application examples and board layout.

Table 3.1 Application Circuit Parameters

Symbol	Parameter	Min	Typ	Max	Unit	Notes
C1	C	100		470	nF	
C2	C	100			nF	
C3 [8) 9)]	C	4	47	160	nF	The value of C3 is the sum of the load capacitor and the cable capacitance
C4, C5 [9)]	C	0		10	nF	Recommended to increase EMC immunity. The value of C4, C5 is the sum of the load capacitor and the cable capacitance
R1			10		kΩ	
R_{IBR}	R	Refer to chapter 1.2			Ω	

Figure 3.1 Bridge in Voltage Mode, External Diode Temperature Sensor



[8] value of C3 summarizes load capacitor and cable capacity
[9] higher values for C3, C4 and C5 increase EMC immunity

Figure 3.2 Bridge in Voltage Mode, External Thermistor

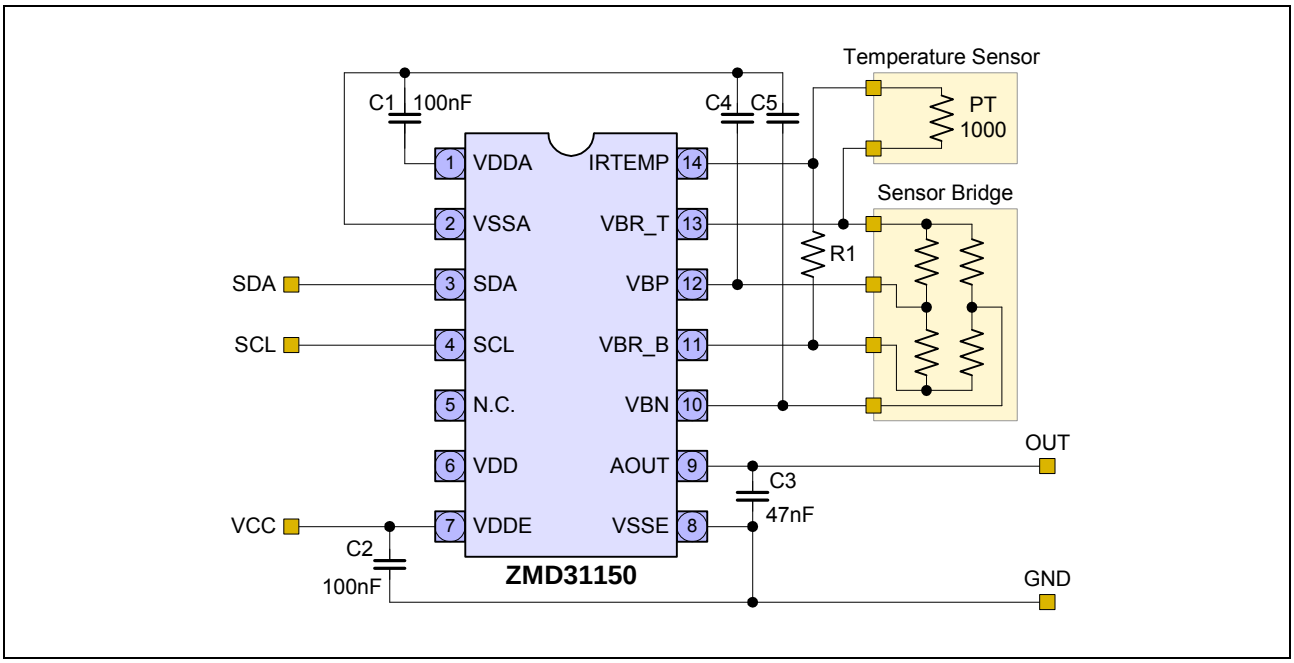
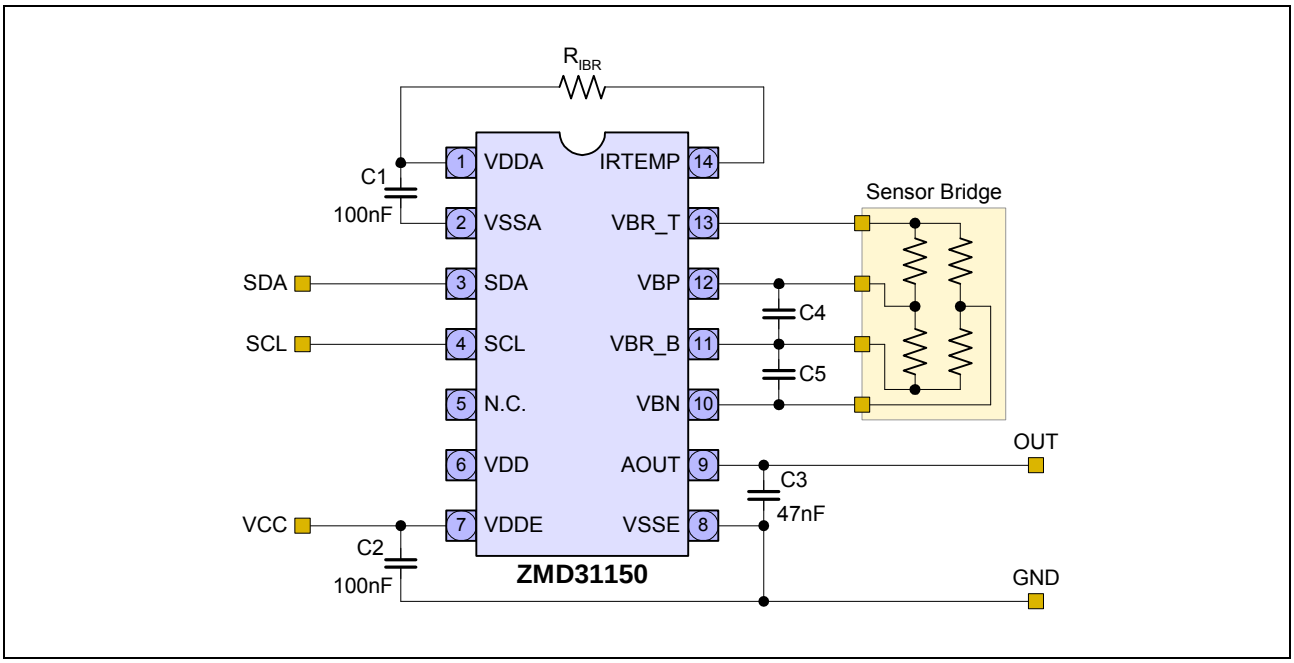


Figure 3.3 Bridge in Current Mode, Temperature Measurement via Bridge TC



4 Pin Configuration, Latch-Up and ESD Protection

4.1. Pin Configuration and Latch-up Conditions

Table 4.1 Pin Configuration and Latch-Up Conditions

Pin	Name	Description	Remarks	Usage/ Connection	Latch-up related Application Circuit Restrictions and/or Remarks
9	AOUT	Analog output & one wire IF IO	IO	Required/-	Trigger Current/Voltage: -100mA/33V
7	VDDE	Positive external supply voltage	Supply	Required/-	Trigger Current/Voltage: -100mA/33V
6	VDD	Positive digital supply voltage	Analog IO	Required or open/-	only capacitor to VSSA is allowed, otherwise no application access
8	VSSE	Negative external supply voltage	Ground	Required/-	
4	SCL	I²C clock	Digital IN, pullup	-/VDDA	Trigger Current/Voltage to VDDA/VSSA: +/-100mA or 8/-4V
3	SDA	I²C data IO	Digital IO, pullup	-/VDDA	
2	VSSA	Negative analogue supply voltage	Analog IO	Required/-	
1	VDDA	Positive analogue supply voltage	Analog IO	Required/-	
13	VBR_T	Bridge top potential	Analog IO	Required/VDDA	Depending on application circuit, short to VDDA/VSSA possible
11	VBR_B	Bridge bottom potential	Analog IO	Required/VSSA	
14	IRTEMP	Temp sensor & current source resistor	Analog IO	-/VDDA, VSSA	Depending on application circuit
12	VBP	Positive input sensor bridge	Analog IN	Required/-	
10	VBN	Negative input sensor bridge	Analog IN	Required/-	

[1] Usage: If “Required” is specified, an electrical connection is necessary – refer to the application circuits
Connection: To be connected to this potential, if not used or no application/configuration related constraints are given

4.2. ESD-Protection

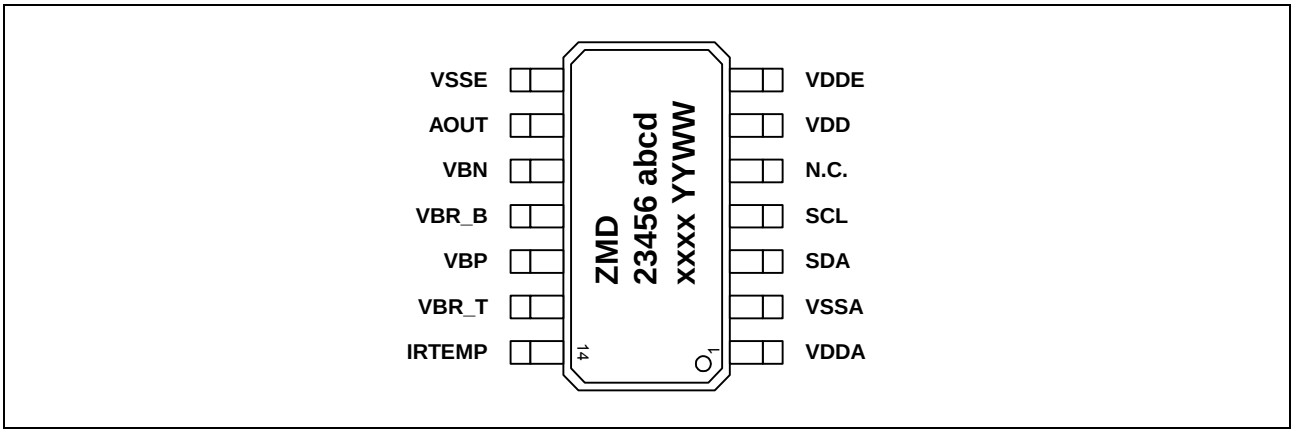
All pins have an ESD Protection of >2000V. Additionally the pins VDDE, VSSE and AOUT have an ESD Protection of >4000V.

ESD Protection referred to the human body model is tested with devices in SSOP14 packages during product qualification. The ESD test follows the human body model with 1.5kOhm/100pF based on MIL 883, Method 3015.7.

5 Package

The standard package of the ZMD31150 is an SSOP14 green package (5.3mm body width) with a lead pitch of 0.65 mm.

Figure 5.1 ZMD31150 Pin Diagram



6 Quality and Reliability

The ZMD31150 is qualified according to the AEC-Q100 standard, operating temperature grade 0. A fit rate <5fit (temp=55°C, S=60%) is guaranteed. A typical fit rate of the C7D-technologie, which is used for ZMD31150, is 2.5fit.

7 Customization

For high-volume applications, which require an up- or downgraded functionality compared to the ZM31150, ZMDI can customize the circuit design by adding or removing certain functional blocks.

For it ZMDI has a considerable library of sensor-dedicated circuitry blocks.

Thus ZMDI can provide a custom solution quickly. Please contact ZMDI for further information.

8 Additional Documents

Table 8.1 Additional Documents

Document	File Name
ZMD31150 Feature Sheet	ZMD31150_FS_Rev_*.PDF
ZMD31150 Functional Description	ZMD31150_FD_Rev_*.PDF
ZMD31150 High Voltage Protection Description	ZMD31150_HV_PROT_Rev_*.PDF
ZMD31150 Dice Package	ZMD31150_DicePackagePin_Rev_*.PDF
ZMD31150 Bandwidth Calculation Sheet	ZMD31150_Bandwidth_Calculation_Rev*.xls
ZMD Temperature Profile Calculation Sheet	ZMD_TempProfile_Rev_*.xls
ZMD31150 Application Kit Description	ZMD31150_APPLKIT_Rev_*.pdf
ZMD31150 Application Notes	ZMD31150_AN*.pdf

Visit ZMDI's website www.zmdi.com or contact your nearest sales office for the latest version of these documents.

9 Glossary

Term	Description
ADC	Analog-to-Digital Converter
CMC	Calibration Microcontroller
CMV	Common Mode Voltage
SCC	Sensor Connection Check
SSC+	Positive-biased Sensor Short Check
SSC-	Negative-biased Sensor Short Check

10 Document Revision History

Revision	Date	Description
0.46	June 12, 2008	First release after format update
0.47	July 20, 2008	Update after review
1.01	September 20, 2008	“6.” – fit rate added ”1.5.2” – ROM check time revised/corrected ”5.3.4.3” – SSC – no detection limit added
1.02	September 20, 2009	adjust to new ZMDI template
1.03	October 2, 2009	change to ZMDI denotation
1.04	November 2, 2009	formatting and linking issues solved

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