

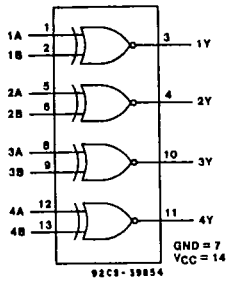
CD54/74HC7266

File Number 1780

HARRIS SEMICOND SECTOR

27E D 430227J 0018007 T HAS

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

Quad 2-Input Exclusive-NOR Gate

Type Features:

- Four independent Exclusive-NOR gates
- Buffered inputs and outputs

Applications

- Logical comparators
- Parity generators and checkers
- Adders/Subtractors

The RCA CD54/74HC7266 contains four independent EXCLUSIVE-NOR gates in one package. They provide the system designer with a means for implementation of the EXCLUSIVE-NOR function.

This device is functionally the same as the TTL226. They differ in that the HC7266 has active high and low outputs whereas the 226 has open collector outputs.

The CD54HC7266 is supplied in 14-lead ceramic dual-in-line packages (F suffix). The CD74HC7266 is supplied in 14-lead plastic dual-in-line package (E suffix), in a 14-lead dual-in-line surface-mount plastic package (M-suffix), and is also available in chip form (H suffix).

Family Features:

- Fanout (Over Temperature Range):
Standard Outputs - 10 LSTTL Loads
Bus Driver Outputs - 15 LSTTL Loads
- Wide Operating Temperature Range:
CD74HC: -40 to +85°C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- Alternate Source is Philips/Signetics
- 2 to 6 V Operation
High Noise Immunity: $N_{IL} = 30\%$, $N_{IH} = 30\%$ of V_{CC} ,
@ $V_{CC} = 5 V$
- CMOS Input Compatibility
 $I_i \leq 1 \mu A$ @ V_{OL} , V_{OH}

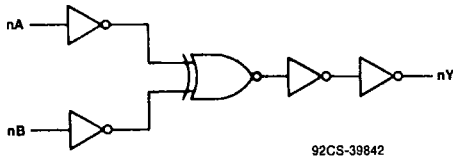


Fig. 1 - Logic diagram each gate.

TRUTH TABLE

INPUTS		OUTPUT
nA	nB	nY
L	L	H
L	H	L
H	L	L
H	H	H

H = HIGH voltage level.
L = LOW voltage level.

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MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE, (V_{cc}):

(Voltages referenced to ground) -0.5 to +7 V
 DC INPUT DIODE CURRENT, I_{IK} (FOR V_I < -0.5 V OR V_I > V_{cc} + 0.5 V) ±20mA
 DC OUTPUT DIODE CURRENT, I_{OK} (FOR V_O < -0.5 V OR V_O > V_{cc} + 0.5 V) ±20mA
 DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR -0.5 V < V_O < V_{cc} + 0.5 V) ±25mA
 DC V_{cc} OR GROUND CURRENT (I_{cc}) ±50mA

POWER DISSIPATION PER PACKAGE (P_D):

For T_A = -40 to +60°C (PACKAGE TYPE E) 500 mW
 For T_A = +60 to +85°C (PACKAGE TYPE E) Derate Linearly at 8 mW/°C to 300 mW
 For T_A = -55 to +100°C (PACKAGE TYPE F, H) 500 mW
 For T_A = +100 to +125°C (PACKAGE TYPE F, H) Derate Linearly at 8 mW/°C to 300 mW
 For T_A = -40 to +70°C (PACKAGE TYPE M) 400 mW
 For T_A = +70 to +125°C (PACKAGE TYPE M) Derate Linearly at 6 mW/°C to 70 mW

OPERATING-TEMPERATURE RANGE (T_A):

PACKAGE TYPE F, H -55 to +125°C
 PACKAGE TYPE E, M -40 to +85°C

STORAGE TEMPERATURE (T_{stg}) -65 to +150°C

LEAD TEMPERATURE (DURING SOLDERING):

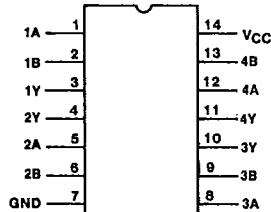
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. +265°C
 Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm)
 with solder contacting lead tips only +300°C

RECOMMENDED OPERATING CONDITIONS:

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T _A = Full Package-Temperature Range) V _{cc} .*	2	6	V
DC Input or Output Voltage V _I , V _O	0	V _{cc}	V
Operating Temperature T _A : CD74 Types CD54 Types	-40 -55	+85 +125	°C
Input Rise and Fall Times t _r , t _f at 2 V at 4.5 V at 6 V	0 0 0	1000 500 400	ns

*Unless otherwise specified, all voltages are referenced to Ground.



TOP VIEW
 TERMINAL ASSIGNMENT

92CS-39841

TERMINAL ASSIGNMENT

CD54/74HC7266

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STATIC ELECTRIC CHARACTERISTICS

CHARACTERISTIC	CD54/74HC7266										UNITS
	TEST CONDITIONS			74HC/54HC TYPES			74HC TYPE		54HC TYPE		
	V _I V	I _O mA	V _{CC} V	+25°C			-40/ +85°C		-55/ +125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
High-Level Input Voltage	V _{IH}		2	1.5	—	—	1.5	—	1.5	—	V
			4.5	3.15	—	—	3.15	—	3.15	—	
			6	4.2	—	—	4.2	—	4.2	—	
Low-Level Input Voltage	V _{IL}		2	—	—	0.5	—	0.5	—	0.5	V
			4.5	—	—	1.35	—	1.35	—	1.35	
			6	—	—	1.8	—	1.8	—	1.8	
High-Level Output Voltage	V _{OH}	V _{IL} or V _{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	V
				4.5	4.4	—	—	4.4	—	4.4	
	CMOS Loads TTL Loads	V _{IL} or V _{IH}	-4 -5.2	4.5 6	3.98 5.48	— —	— —	3.84 5.34	— —	3.7 5.2	V
				6	5.9	—	—	5.9	—	5.9	
Low-Level Output Voltage	V _{OL}	V _{IL} or V _{IH}	0.02	2	—	—	0.1	—	0.1	—	V
				4.5	—	—	0.1	—	0.1	—	
	CMOS Loads TTL Loads	V _{IL} or V _{IH}	4 5.2	4.5 6	— —	— —	0.26 0.26	— —	0.33 0.33	— —	V
				6	—	—	0.26	—	0.33	—	
Input Leakage Current	I _I	V _{CC} or Gnd		6	—	—	±0.1	—	±1	—	μA
Quiescent Device Current	I _{CC}	V _{CC} or Gnd	0	6	—	—	2	—	20	—	μA

SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, Input t_r, t_f = 6 ns)

CHARACTERISTIC	C _L pF	TYPICAL VALUES 54/74HC	UNITS	
Propagation Delay, Any Input	t _{PLH} t _{PHL}	15	9	ns
Power Dissipation Capacitance*	C _{PD}	—	33	pF

*C_{PD} is used to determine the dynamic power consumption, per gate.
P_D = V_{CC}² f_i (C_{PD} + C_L) where:
f_i = input frequency.
C_L = output load capacitance.
V_{CC} = supply voltage.

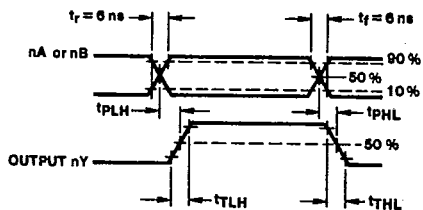
SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns)

CHARACTERISTIC	V _{CC}	25°C		-40°C to +85°C		-55°C to +125°C		UNITS	
		HC		74HC		54HC			
		Min.	Max.	Min.	Max.	Min.	Max.		
Propagation Delay	t _{PLH} , t _{PHL}	2	—	115	—	145	—	150	ns
		4.5	—	23	—	29	—	35	
		6	—	30	—	25	—	30	
Output Transition Time	t _{TLH} , t _{THL}	2	—	75	—	95	—	110	ns
		4.5	—	15	—	19	—	22	
		6	—	13	—	16	—	19	
Input Capacitance	C _I	—	—	10	—	10	—	10	pF

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Fig. 2 - Transition times and propagation delay times.

