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TYPES SN54182, SN54S182, SN74182, SN74S182
LOOK-AHEAD CARRY GENERATORS
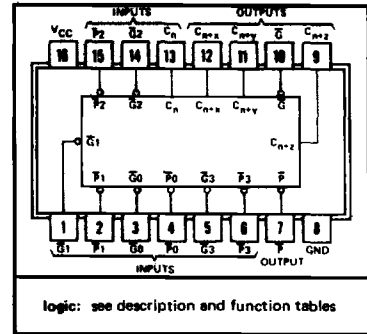
BULLETIN NO. DL-S 7611823, DECEMBER 1972–REVISED OCTOBER 1976

- **Directly Compatible for Use With:**
  SN54181/SN74181, SN54LS181/SN74LS181,
  SN54S281/SN74S281, SN54S381, SN74S381,
  SN54S481/SN74S481

SN54182, SN54S182 . . . J OR W PACKAGE
SN74182, SN74S182 . . . J OR N PACKAGE
(TOP VIEW)

logic: see description and function tables

PIN DESIGNATIONS

ALTERNATIVE	DESIGNATIONS†	PIN NOS.	FUNCTION
$\overline{G0}, \overline{G1}, \overline{G2}, \overline{G3}$	G0, G1, G2, G3	3, 1, 14, 5	CARRY GENERATE INPUTS
$\overline{P0}, \overline{P1}, \overline{P2}, \overline{P3}$	P0, P1, P2, P3	4, 2, 15, 6	CARRY PROPAGATE INPUTS
C_n	$\overline{C_n}$	13	CARRY INPUT
$C_{n+x}, C_{n+y}, C_{n+z}$	$\overline{C}_{n+x}, \overline{C}_{n+y}, \overline{C}_{n+z}$	12, 11, 9	CARRY OUTPUTS
$\overline{G}$	Y	10	CARRY GENERATE OUTPUT
$\overline{P}$	X	7	CARRY PROPAGATE OUTPUT
V_{CC}		16	SUPPLY VOLTAGE
GND		8	GROUND

† Interpretations are illustrated on page 7-273

description

The SN54182, SN54S182, SN74182, and SN74S182 are high-speed, look-ahead carry generators capable of anticipating a carry across four binary adders or group of adders. They are cascadable to perform full look-ahead across n-bit adders. Carry, generate-carry, and propagate-carry functions are provided as enumerated in the pin designation table above.

When used in conjunction with the '181, 'LS181, or 'S181 arithmetic logic unit (ALU), these generators provide high-speed carry look-ahead capability for any word length. Each '182 or 'S182 generates the look-ahead (anticipated carry) across a group of four ALU's and, in addition, other carry look-ahead circuits may be employed to anticipate carry across sections of four look-ahead packages up to n-bits. The method of cascading '182 or 'S182 circuits to perform multi-level look-ahead is illustrated under typical application data.

The carry functions (inputs, outputs, generate, and propagate) of the look-ahead generators are implemented in the compatible forms for direct connection to the ALU. Reinterpretations of carry functions as explained on the '181, 'LS181, and 'S181 data sheet are also applicable to and compatible with the look-ahead generator. Logic equations for the '182 and 'S182 are:

$$C_{n+x} = G0 + P0\ C_n$$
$$C_{n+y} = G1 + P1\ G0 + P1\ P0\ C_n$$
$$C_{n+z} = G2 + P2\ G1 + P2\ P1\ G0 + P2\ P1\ P0\ C_n \quad \text{or}$$
$$\overline{G} = \overline{G3 + P3\ G2 + P3\ P2\ G1 + P3\ P2\ P1\ G0}$$
$$\overline{P} = \overline{P3\ P2\ P1\ P0}$$

$$\overline{C}_{n+x} = \overline{Y0\ (X0 + C_n)}$$
$$\overline{C}_{n+y} = \overline{Y1\ [X1 + Y0\ (X0 + C_n)]}$$
$$\overline{C}_{n+z} = \overline{Y2\ \{ X2 + Y1\ [X1 + Y0\ (X0 + C_n)]\}}$$
$$Y = Y3\ (X3 + Y2)\ (X3 + X2 + Y1)\ (X3 + X2 + X1 + Y0)$$
$$X = X3 + X2 + X1 + X0$$

logic

FUNCTION TABLE FOR $\overline{G}$ OUTPUT

INPUTS							OUTPUT
$\overline{G3}$	$\overline{G2}$	$\overline{G1}$	$\overline{G0}$	$\overline{P3}$	$\overline{P2}$	$\overline{P1}$	$\overline{G}$
L	X	X	X	X	X	X	L
X	L	X	X	L	X	X	L
X	X	L	X	L	L	X	L
X	X	X	L	L	L	L	L
All other combinations							H

FUNCTION TABLE FOR $\overline{P}$ OUTPUT

INPUTS				OUTPUT
$\overline{P3}$	$\overline{P2}$	$\overline{P1}$	$\overline{P0}$	$\overline{P}$
L	L	L	L	L
All other combinations				H

H = high level, L = low level, X = irrelevant
Any inputs not shown in a given table are irrelevant with respect to that output.

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logic

functional block diagram

FUNCTION TABLE
FOR C_{n+x} OUTPUT

INPUTS			OUTPUT
$\overline{G0}$	$\overline{P0}$	C_n	C_{n+x}
L	X	X	H
X	L	H	H
All other combinations			L

FUNCTION TABLE
FOR C_{n+y} OUTPUT

INPUTS					OUTPUT
$\overline{G1}$	$\overline{G0}$	$\overline{P1}$	$\overline{P0}$	C_n	C_{n+y}
L	X	X	X	X	H
X	L	L	X	X	H
X	X	L	L	H	H
All other combinations					L

FUNCTION TABLE FOR C_{n+z} OUTPUT

INPUTS							OUTPUT
$\overline{G2}$	$\overline{G1}$	$\overline{G0}$	$\overline{P2}$	$\overline{P1}$	$\overline{P0}$	C_n	C_{n+z}
L	X	X	X	X	X	X	H
X	L	X	L	X	X	X	H
X	X	L	L	L	X	X	H
X	X	X	L	L	L	H	H
All other combinations							L

H = high level, L = low level, X = irrelevant
Any inputs not shown in a given table are irrelevant with respect to that output.
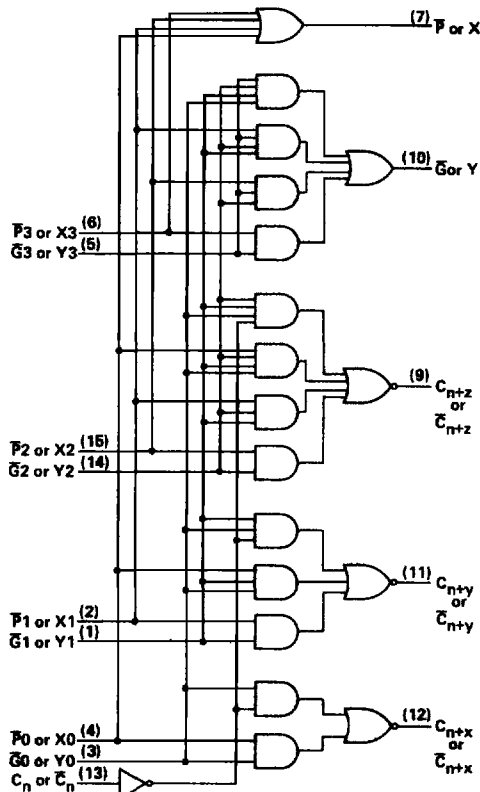
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	. . . .	7 V
Input voltage	. . . .	5.5 V
Interemitter voltage (see Note 2)	. . . .	5.5 V
Operating free-air temperature range: SN54', SN54S' Circuits	. . . .	−55°C to 125°C
SN74', SN74S' Circuits	. . . .	0°C to 70°C
Storage temperature range	. . . .	−65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter input transistor. For these circuits, this rating applies to each $\overline{G}$ input in conjunction with any other $\overline{G}$ input or in conjunction with any $\overline{P}$ input.

recommended operating conditions

	SN54182			SN74182			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−800			−800	μA
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS[†]	SN54182			SN74182			UNIT
			MIN	TYP[‡]	MAX	MIN	TYP[‡]	MAX	
V_{IH} High-level input voltage			2			2			V
V_{IL} Low-level input voltage					0.8			0.8	V
V_{IK} Input clamp voltage		V_{CC} = MIN, I_I = −12 mA			−1.5			−1.5	V
V_{OH} High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA	2.4	3.4		2.4	3.4		V
V_{OL} Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA		0.2	0.4		0.2	0.4	V
I_I Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH} High-level input current	C_n input	V_{CC} = MAX, V_I = 2.4 V			80			80	μA
	$\overline{P}3$ input				120			120	
	$\overline{P}2$ input				160			160	
	$\overline{P}0$, $\overline{P}1$, or $\overline{G}3$ input				200			200	
	$\overline{G}0$ or $\overline{G}2$ input				360			360	
	$\overline{G}1$ input				400			400	
I_{IL} Low-level input current	C_n input	V_{CC} = MAX, V_I = 0.4 V			−3.2			−3.2	mA
	$\overline{P}3$ input				−4.8			−4.8	
	$\overline{P}2$ input				−6.4			−6.4	
	$\overline{P}0$, $\overline{P}1$, or $\overline{G}3$ input				−8			−8	
	$\overline{G}0$ or $\overline{G}2$ input				−14.4			−14.4	
	$\overline{G}1$ input				−16			−16	
I_{OS} Short-circuit output current[§]		V_{CC} = MAX	−40		−100	−40		−100	mA
I_{CCH} Supply current, all outputs high		V_{CC} = 5 V, See Note 3		27			27		mA
I_{CCL} Supply current, all outputs low		V_{CC} = MAX, See Note 4		45	65		45	72	mA

[†]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
[‡]All typical values are at V_{CC} = 5 V, T_A = 25°C.
[§]Not more than one output should be shorted at a time and duration of the short-circuit test should not exceed one second.
NOTES: 3. I_{CCH} is measured with all outputs open, inputs $\overline{P}3$ and $\overline{G}3$ at 4.5 V, and all other inputs grounded.
    4. I_{CCL} is measured with all outputs open; inputs $\overline{G}0$, $\overline{G}1$, and $\overline{G}2$ at 4.5 V; and all other inputs grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH} Propagation delay time, low-to-high-level output	C_L = 15 pF, R_L = 400 Ω, See Note 5		11	17	ns
t_{PHL} Propagation delay time, high-to-low-level output			15	22	ns

NOTE 5: Load circuit and voltage waveforms are shown on page 3-10.

recommended operating conditions

	SN54S182 MIN	NOM	MAX	SN74S182 MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−1			−1	mA
Low-level output current, I_{OL}			20			20	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS[†]	SN54S182 MIN	TYP[‡]	MAX	SN74S182 MIN	TYP[‡]	MAX	UNIT
V_{IH} High-level input voltage			2			2			V
V_{IL} Low-level input voltage					0.8			0.8	V
V_{IK} Input clamp voltage		V_{CC} = MIN, I_I = −18 mA			−1.2			−1.2	V
V_{OH} High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −1 mA	2.5	3.4		2.7	3.4		V
V_{OL} Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 20 mA			0.5			0.5	V
I_I Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH} High-level input current	C_n input	V_{CC} = MAX, V_I = 2.7 V			50			50	μA
	$\overline{P}3$ input				100			100	
	$\overline{P}2$ input				150			150	
	$\overline{P}0, \overline{P}1$, or $\overline{G}3$ input				200			200	
	$\overline{G}0$ or $\overline{G}2$ input				350			350	
	$\overline{G}1$ input				400			400	
I_{IL} Low-level input current	C_n input	V_{CC} = MAX, V_I = 0.5 V			−2			−2	mA
	$\overline{P}3$ input				−4			−4	
	$\overline{P}2$ input				−6			−6	
	$\overline{P}0, \overline{P}1$, or $\overline{G}3$ input				−8			−8	
	$\overline{G}0$ or $\overline{G}2$ input				−14			−14	
	$\overline{G}1$ input				−16			−16	
I_{OS} Short-circuit output current§		V_{CC} = MAX	−40		−100	−40		−100	mA
I_{CCH} Supply current, all outputs high		V_{CC} = 5 V, See Note 3		35			35		mA
I_{CCL} Supply current, all outputs low		V_{CC} = MAX, See Note 4		69	99		69	109	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time and duration of the short-circuit test should not exceed one second.
NOTES: 3. I_{CCH} is measured with all outputs open, inputs $\overline{P}3$ and $\overline{G}3$ at 4.5 V, and all other inputs grounded.
4. I_{CCL} is measured with all outputs open; inputs $\overline{G}0$, $\overline{G}1$, and $\overline{G}2$ at 4.5 V; and all other inputs grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

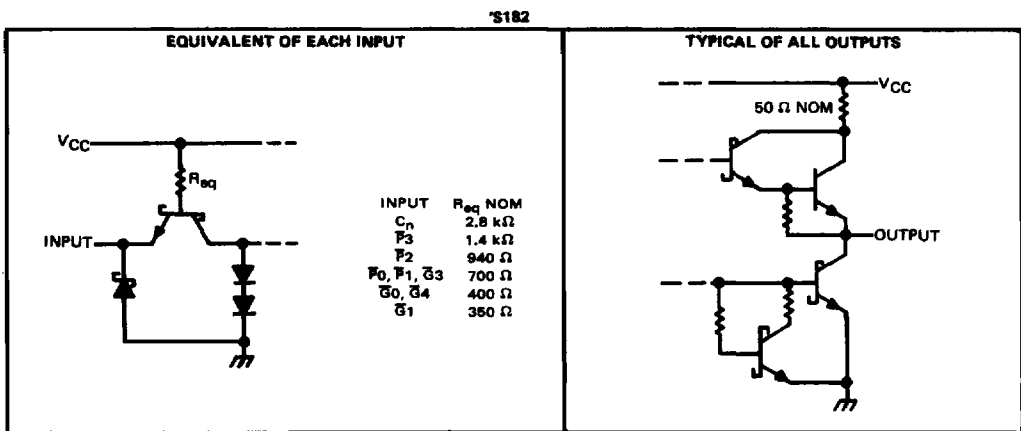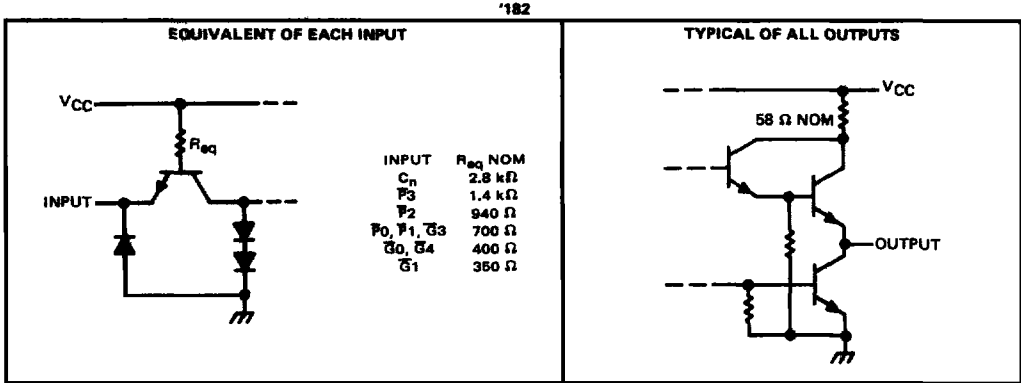| PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	$\overline{G}0, \overline{G}1, \overline{G}2, \overline{G}3$, P0, P1, P2, or P3	C_{n+x}, C_{n+y}, or C_{n+z}	R_L = 280 Ω, C_L = 15 pF, See Note 5		4.5	7	ns
t_{PHL}					4.5	7	
t_{PLH}	$\overline{G}0, \overline{G}1, \overline{G}2, \overline{G}3$, P1, P2, or P3	$\overline{G}$			5	7.5	ns
t_{PHL}					7	10.5	
t_{PLH}	$\overline{P}0, \overline{P}1, \overline{P}2$, or $\overline{P}3$	$\overline{P}$			4.5	6.5	ns
t_{PHL}					6.5	10	
t_{PLH}	C_n	C_{n+x}, C_{n+y}, or C_{n+z}			6.5	10	ns
t_{PHL}					7	10.5	

¶t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
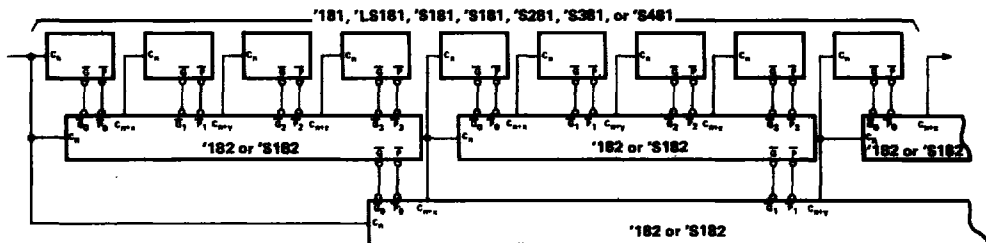NOTE 5: Load circuit and voltage waveforms are shown on page 3-10.

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schematics of inputs and outputs

'182

EQUIVALENT OF EACH INPUT	TYPICAL OF ALL OUTPUTS

INPUT	R_{eq} NOM
C_n	2.8 kΩ
$\overline{P}_3$	1.4 kΩ
$\overline{P}_2$	940 Ω
$\overline{P}_0, \overline{P}_1, \overline{G}_3$	700 Ω
$\overline{G}_0, \overline{G}_4$	400 Ω
$\overline{G}_1$	350 Ω

58 Ω NOM

'S182

EQUIVALENT OF EACH INPUT	TYPICAL OF ALL OUTPUTS

INPUT	R_{eq} NOM
C_n	2.8 kΩ
$\overline{P}_3$	1.4 kΩ
$\overline{P}_2$	940 Ω
$\overline{P}_0, \overline{P}_1, \overline{G}_3$	700 Ω
$\overline{G}_0, \overline{G}_4$	400 Ω
$\overline{G}_1$	350 Ω

50 Ω NOM

TYPICAL APPLICATION DATA

'181, 'LS181, 'S181, 'S181, 'S281, 'S381, or 'S481

'182 or 'S182

'182 or 'S182

'182 or 'S182

'182 or 'S182

64-BIT ALU, FULL-CARRY LOOK-AHEAD IN THREE LEVELS
Remaining inputs and outputs of '181, 'LS181, 'S181 'S281, 'S381, and 'S481 are not shown.

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