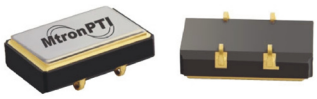
M5RJ Series

9x14 mm, 3.3 Volt, LVPECL/LVDS, Clock Oscillator



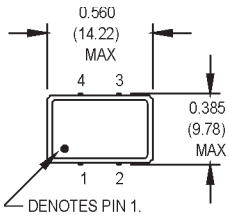
- Integrated phase jitter of less than 1 ps from 12 kHz to 20 MHz
- Ideal for 10 and 40 Gigabit Ethernet and Optical Carrier applications

Ordering Information

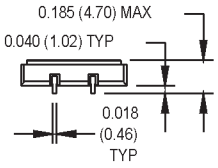
M5R 1 8 Z Q J -R 00.0000 MHz

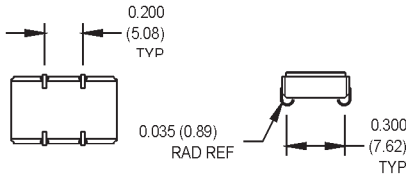
- **Product Series**
- **Temperature Range**
  - 1: 0°C to +70°C
  - 2: -40°C to +85°C
  - 6: -20°C to +70°C
  - 7: -0°C to +85°C
  - 8: 0°C to +50°C
- **Stability**
  - 3: ±100 ppm
  - 4: ±50 ppm
  - 5: ±35 ppm
  - 6: ±25 ppm
  - 8: ±20 ppm
- **Output Type**
  - E: Complementary, pins 1 & 4, enable (enabled w/pin 2 low)
  - R: Complementary, pins 1 & 4, enable (enabled w/pin 2 high)
  - S: Complementary, pins 4 & 5, enable (enabled w/pin 2 low)
  - U: Complementary, pins 4 & 5
  - Z: Complementary, pins 1 & 3
- ***Symmetry/Output Logic Type**
  - P: 45/55% PECL
  - Q: 40/60% PECL
- **Package/Lead Configurations**
  - J: J-lead
- **RoHS Compliance**
  - Blank: non-RoHS compliant part
  - -R: RoHS compliant part
- **Frequency (customer specified)**

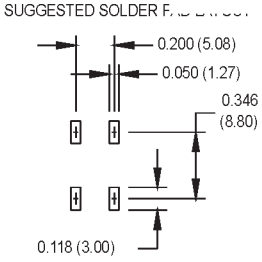
* Contact the factory regarding LVDS output availability
M2003Sxxx - Contact factory for datasheet.

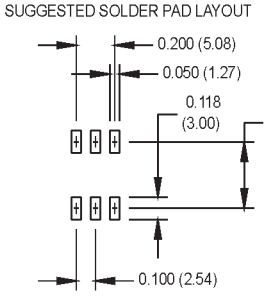


FREQUENCY RANGE	AVAILABLE OUTPUT TYPES
19.440 to 170.000 MHz	Z, E, R
170.000 to 800.000 MHz	S, U

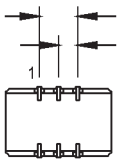


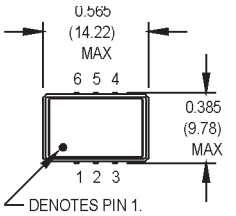


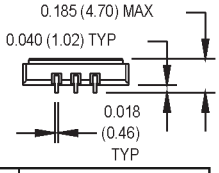




All dimensions in inches (mm).







Pin Connections (Z, E, and R Output Types)

FUNCTION	4 Pin	6 Pin
Output/Q	1	1
Enable		2
Ground/Cover	2	3
Output Q	3	4
N/C		5
+Vcc	4	6

Pin Connections (S and U Output Types)

PIN	FUNCTION
1	N/C
2	N/C or Enable
3	Ground/Cover
4	Output Q
5	Output/Q
6	+Vcc

Electrical Specifications

PARAMETER	Symbol	Min.	Typ.	Max.	Units	Condition/Notes
Frequency Range	F	19.44		245.76	MHz	See Note 1
Operating Temperature	TA	(See Ordering Information)				
Storage Temperature	Ts	-55		+125	°C	
Frequency Stability	ΔF/F	(See Ordering Information)				See Note 2
Aging						
1st Year			±2		ppm	
Thereafter (per year)			±1		ppm	
Input Voltage	Vcc	3.135	3.3	3.465	V	
Input Current	Icc			75	mA	
Output Type						LVPECL/LVDS
Load		50 Ohms to Vcc -2.0 V Or Thevenin equivalent				PECL load
Symmetry (Duty Cycle)		(See Ordering Information)				@ Vcc-1.3 VDC
Output Skew				200	ps	PECL
Differential Voltage		250	340	450	mV	LVDS
Logic "1" Level	Voh	Vcc-1.02			V	PECL
Logic "0" Level	Vol			Vcc-1.63	V	PECL
Rise/Fall Time	Tr/Tf			0.55	ns	@ 20/80% LVPECL
			.50	1.0	ns	@ 20/80% LVDS
Enable Function		PECL low: output active PECL high: output disables				"E" and "S" output types
		80% Vcc min. Or N/C: output active 20% Vcc max.: output disables				"R" output type
Start up Time			5		ms	
Phase Jitter	ϕ J					
Below 600 MHz				1	ps RMS	Integrated 12 kHz - 20 MHz
600 MHz and above				0.5	ps RMS	Integrated 12 kHz - 20 Mhz

1. Consult factory for exact frequency availability.
2. Calibration, deviation over temperature, shock, vibration, and aging.

PECL Load - see load circuit diagram #5. LVDS Load - see load circuit diagram #9.

Please see **www.mtronpti.com** for our complete offering and detailed datasheets. Contact us for your application specific requirements: MtronPTI **1-800-762-8800.**

Revision: 08-13-07

MtronPTI Lead Free Solder Profile