MTC-20278/9 ILT

Quad ISDN U-Interface ISDN Standard Products

Data Sheet
Rev. 2.0 - February 2000

Key Features

- **Quad ISDN LT 'U' interface functions in a single monolithic integrated circuit**
- **Pin compatible 2B1Q and 4B3T line code versions**
  - *** MTC-20278 ILTQ for 2B1Q**
  - *** MTC-20279 ILTT for 4B3T**
- **Full compliance with the applicable ETSI, FTZ and ITU requirements**
- **DECT Synchronization Support (2BTQ)**
- **Digital interface bus using industry-standard GCI**
- **Minimal external components**
- **3.3V operating voltage**
- **80 pin Plastic Quad Flat Pack package**

Key Applications

- **ISDN Exchange Line Cards**
- **Remote Access Multiplex Systems**
- **FTTx Systems**

Ordering Information

Part number	Package	Temp.
MTC-20278PQ-I	80PQFP	-40 to + 85°C
MTC-20278PQ-C	80PQFP	0 to + 70°C
MTC-20279PQ-I	80PQFP	-40 to + 85°C
MTC-20279PQ-C	80PQFP	0 to + 70°C

General Description

The MTC-20278/9 chip contains all the functions necessary to make 4 'U' interfaces in an ISDN Line Termination card. It comprises 4, fully integrated echo-canceling 'U' interfaces, plus the necessary support and test functions. The general block diagram is shown in Figure 1. By integrating 4 complete U Interfaces in a single high density package, the MTC-20278/9 makes it possible to integrate more lines on one card, this reducing the cost per line. Two versions of the device are available - the MTC-20278 offering the 2B1Q line code, and the MTC-20279 which has 4B3T line coding. Both devices are pin compatible, and are fully compliant with the relevant parts of ETSI, FTZ and ITU requirements for ISDN connection.

The MTC-20278/9 device offers a user transport rate of 144kbit/s full duplex (2B + D) per channel, as well as fully automatic control of activate/deactivate protocols, and full support of the maintenance channel. Digital I/O for Power-feed Control, and DECT Synchronization (MTC-20278 only) are provided for 4 identical channels.

The digital interface on the 'exchange' side uses the industry-standard GCI interface in 2 Mbit burst mode. This mode allows for 8 channels to be multiplexed onto the same interface. The MTC-20278/9 can be set to respond to either the first 4 or the last 4 timeslots in the GCI frame. This allows two devices, totalling 8 ISDN lines, to be multiplexed onto the same GCI interface.

The MTC-20278/9 takes all timing information from the GCI clocks, and so does not require a separate clock oscillator.

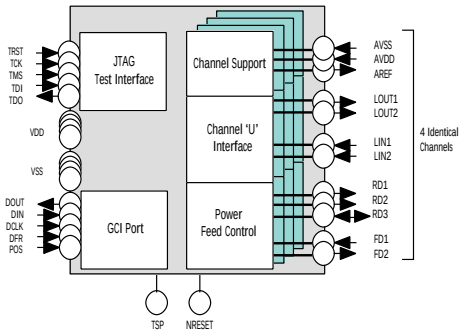

Fig.1: General Block Diagram

Relevant Standards

- ETSI TS 102 080, 1998
- ETS 300 012
- ETS 300 297
- CCITT / ITU Recommendation G.961
- ANSI T1.601, BA ISDN specifications 1992

Functional Characteristics

The U-Interface

NOTE: Some of the specifications in this section refer to the U0 Interface and not to the line ports (LOUT1, LOUT2, LIN1, LIN2). The characteristics at the line port are affected by the design of the transformer and the other external components.

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Physical Characteristics
The quaternary symbol stream on the U-interface complies to the following physical characteristics:

1) Symbol Rate
The symbol rate is 80 kbaud ± 1 ppm and applies to synchronous symbol transmission. The symbol rate is controlled by the external clock.

2) Input Jitter
The ILTQ tolerates a sinusoidal input jitter of the quaternary symbols as shown in Figure 5.

3) Output Jitter
The peak-to–peak jitter produced by the ILTQ doesn't exceed 0.02 UI when measured via a high pass filter with a cut-off frequency of 30Hz. Without this filter, the same measurement doesn't read more than 0.1 UI. To obtain this performance, the jitter on the GCI input clock should not exceed 15ns peak-to-peak

4) Transmit Signal Amplitude
The absolute peak value VImax of a single pulse VI at U0 interface terminated with a 135Ω resistance is 2.5V ± 5%. See Figure 2 and 8.

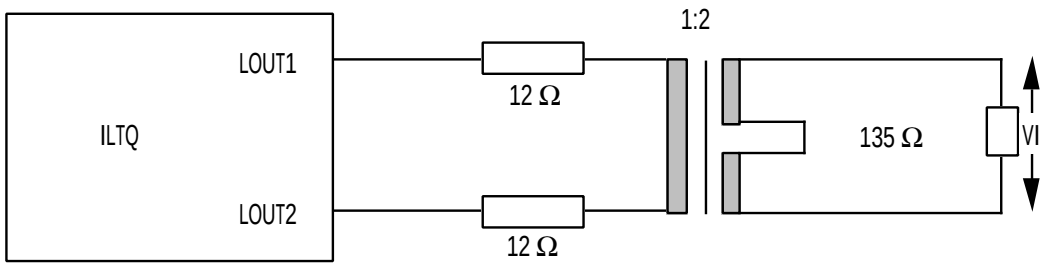

Fig.2: Test Circuit for Single Pulse VI

5) Stability

The transmit signal amplitude measured over a periode of one minute doesn't vary by more than 1% beginning 5ms after the ILTQ is switched into power-up state.

6) Transmit Spectrum

The spectrum of the quaternary transmit signal at U0 interface doesn't exceed the limits given in Figure 7.

7) Pulse Shape

A single pulse measured across a 135Ω resistance at U0 interface complies to the spectral requirements presented in Figure 7 and the pulse mask requirements given in Figure 8.

8) Maximum Voltage

The maximum peak-to-peak value VUmax of the voltage VU as shown in Figure 3 with full receive signal (short line) is 2.5V. Due to the analog echo subtraction the maximum peak-to-peak value Vinmax of the voltage Vin between LIN1 and LIN2 is 1.7V.

9) Input/Output Impedance

The line terminating impedance is 135Ω in power-up and in power-down state. The return loss at U0 measured against 135Ω (real) exceeds; 20 dB between 10kHz and 25kHz.

- slope below 10kHz: 20 dB / decade
- slope above 25kHz: -20 dB / decade

10) Load

The load is given by the line transformer and the subscriber line. The loops are standardized by the ANSI and ETSI documents.
Turns ratio of line transformer 1:2
Transformer coil inductance (from line side): 15 mH ± 10%

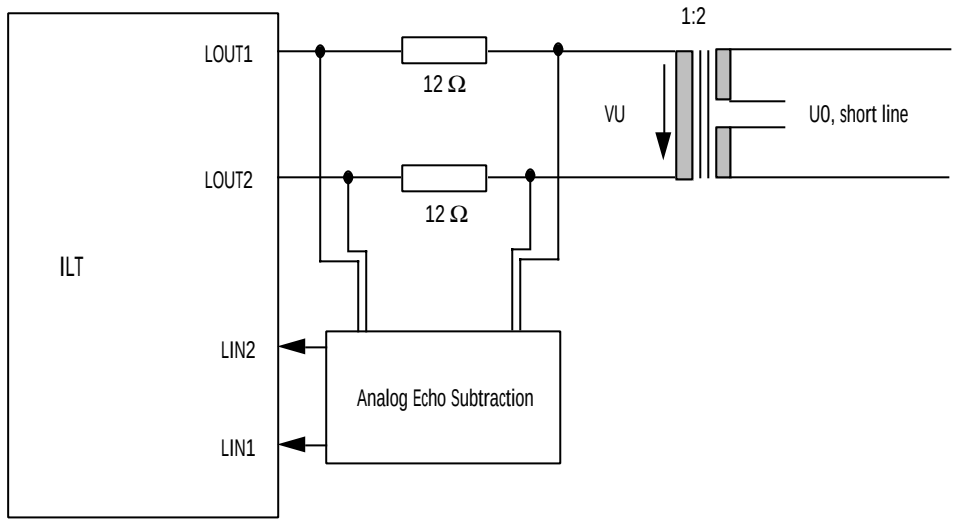

Fig.3: Test Circuit for Voltages VU and Vin at UO Interface

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Requirements for the U- Line Ports

NOTE: Some of the specifications in this section refer to the UK0 Interface and not to the line ports (LOUT1, LOUT2, LIN1, LIN2). The characteristics at the line port are affected by the design of the transformer and the other external components.

Physical Characteristics
The ternary symbol stream on the U-interface must comply to the following physical characteristics:

1) Symbol Rate
The symbol rate is 120 kbaud ± 1 ppm and applies to synchronous symbol transmission. The symbol rate is controlled by an external clock.

2) Input Jitter
The ILTT tolerates a sinusoidal input jitter of the ternary symbols as indicated in Figure 4.

3) Output Jitter
The peak-to-peak jitter produced by the ILTT doesn't exceed 0.02 UI (166ns), when measured via a high pass filter with a cut-off frequency of 30Hz. Without this filter the same measurement doesn't read more than 0.1 UI. This performance is only guaranteed when the input jitter at the GCI clock is less than 15ns peak-to-peak.

4) Transmit Signal Amplitude
The absolute peak value VImax of a single pulse VI at UK0 interface terminated with a 150Ω resistance is 2V ± 0.2V. See the following Figure. The absolute peak value of the coded ternary signal measured at UK0 interface terminated with 150Ω doesn't exceed 4V.
See Figure 4.

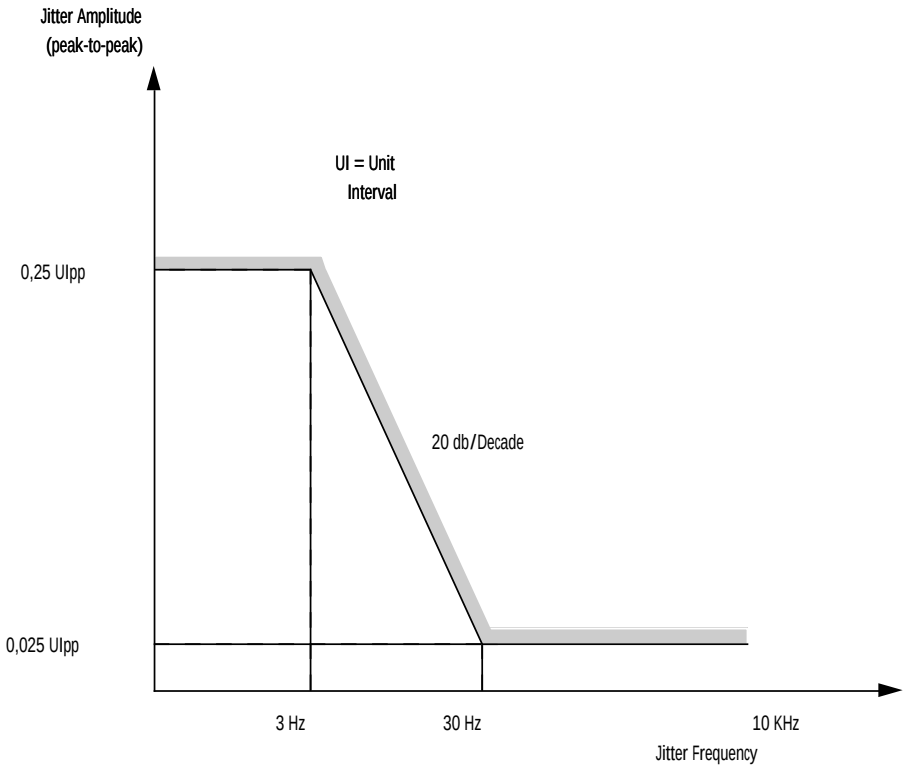


Fig.4: Range of Admissable Sinusoidal Input Jitter, MTC-20278 and MTC-20279

5) Stability

The transmit signal amplitude measured over a period of one minute doesn't vary by more than 1% beginning 5ms after the ILTT is switched into power-up state.

6) Transmit Spectrum

The spectrum of the ternary transmit signal at UK0 interface doesn't exceed the limits given in Figure 6.

7) Pulse Shape

A single pulse measured across a 150Ω resistance at the UK0 interface comply to the spectral requirements presented in Figure 7 and the pulse mask requirements given in Figure 8.

8) Maximum Voltage

The maximum peak-to-peak value VUmax of the voltage VU as shown in Figure 5 with full receive signal (short line), that must be accepted, is 4V. Due to the analog echo subtraction the maximum peak-to-peak value Vinmax of the voltage Vin between LIN1 and LIN2 is 2.7V. For ILTT, the value of n must be 1.6.

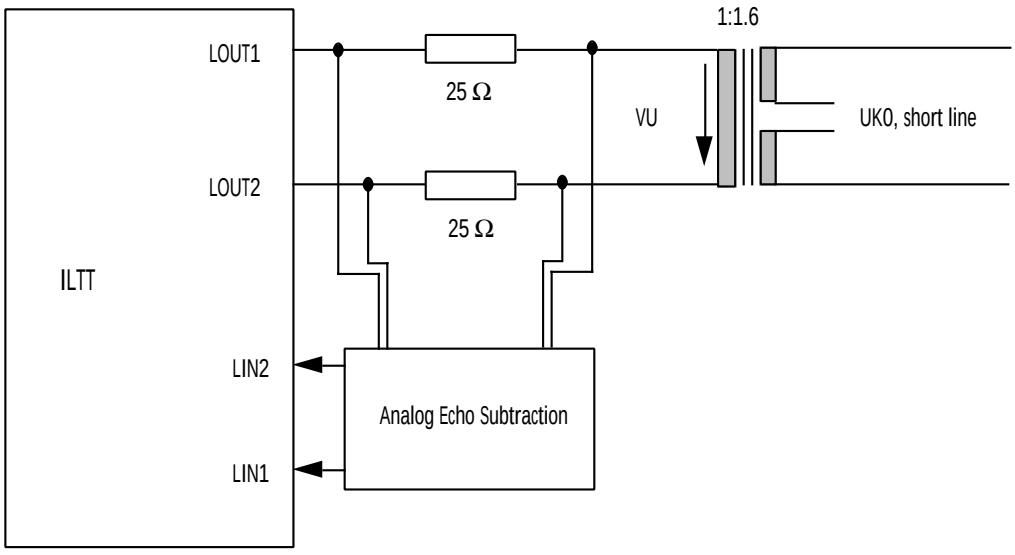


Fig.5: Test Circuit for Voltages VU and Vin at UK0 Interface

9) Input/Output Impedance

The line terminating impedance must be 150Ω in power-up and in power-down state. The return loss at UK0 measured against 150Ω real must exceed 16 dB between 12kHz and 50kHz.

- slope below 12kHz: 20 dB/decade
- slope above 50kHz: -10 dB/decade

10) Load

The load is given by the line transformer and the subscriber line.
Turns ratio of line transformer: 1.6
Transformer coil inductance (from line side): 6.8mH ± 10%.

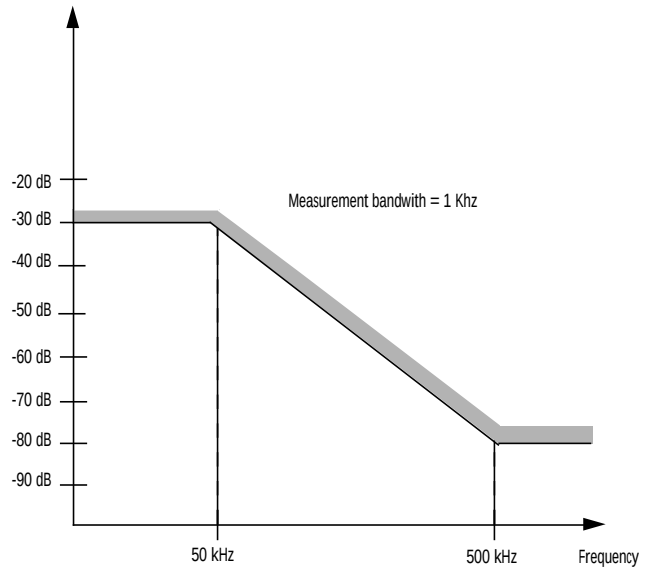


Fig.6: Spectrum of Signal at UK0 Interface, MTC-20278

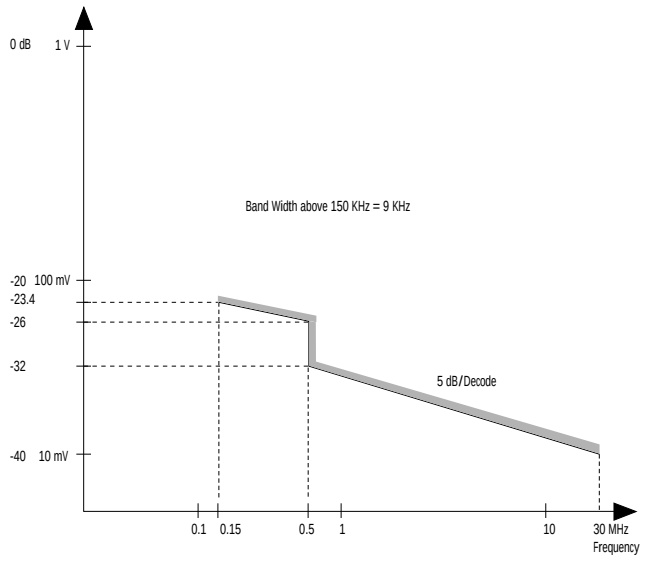


Fig.7: Single Pulse Mask

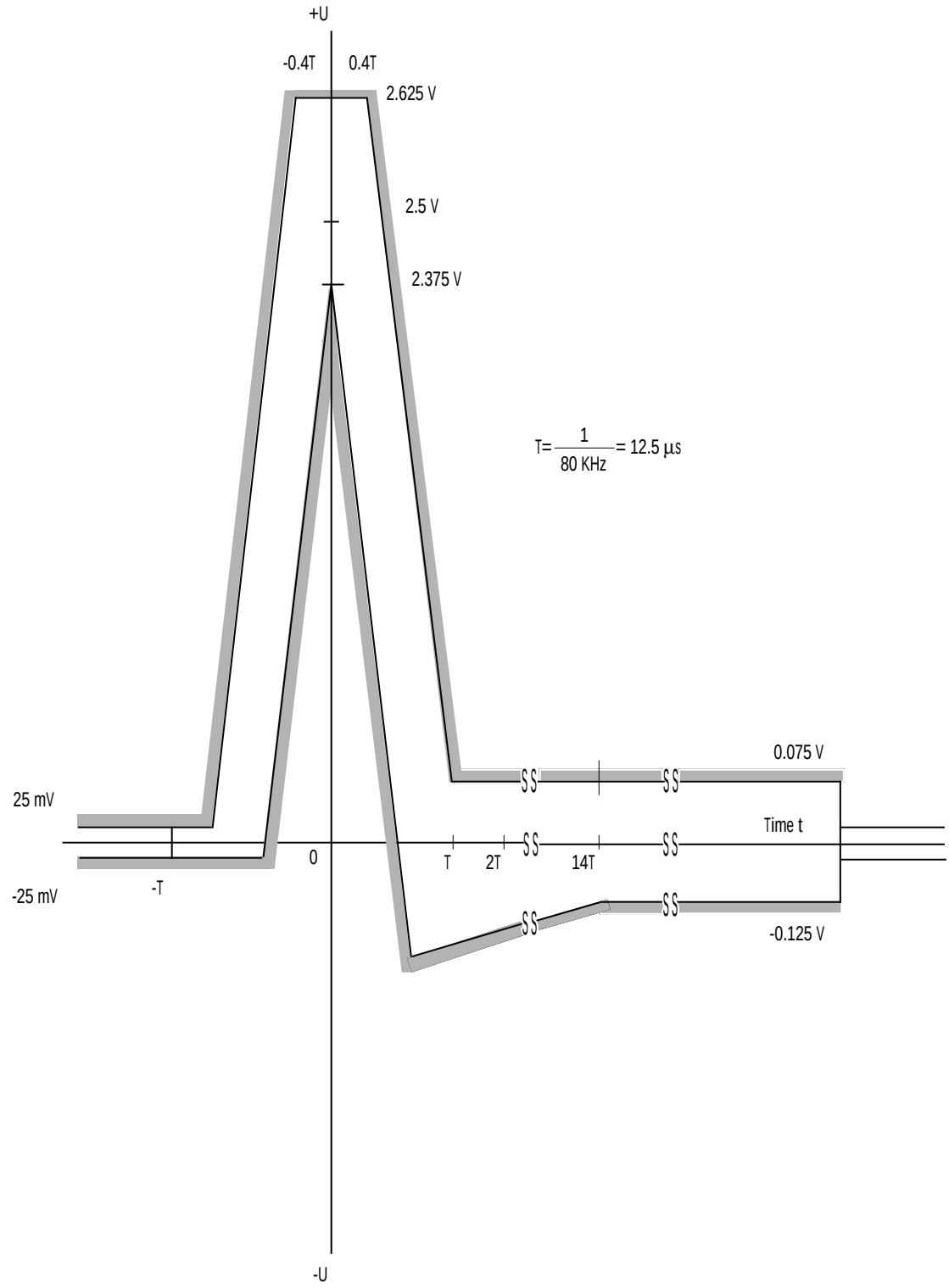


Fig.8: Single Pulse Mask, MTC-20278

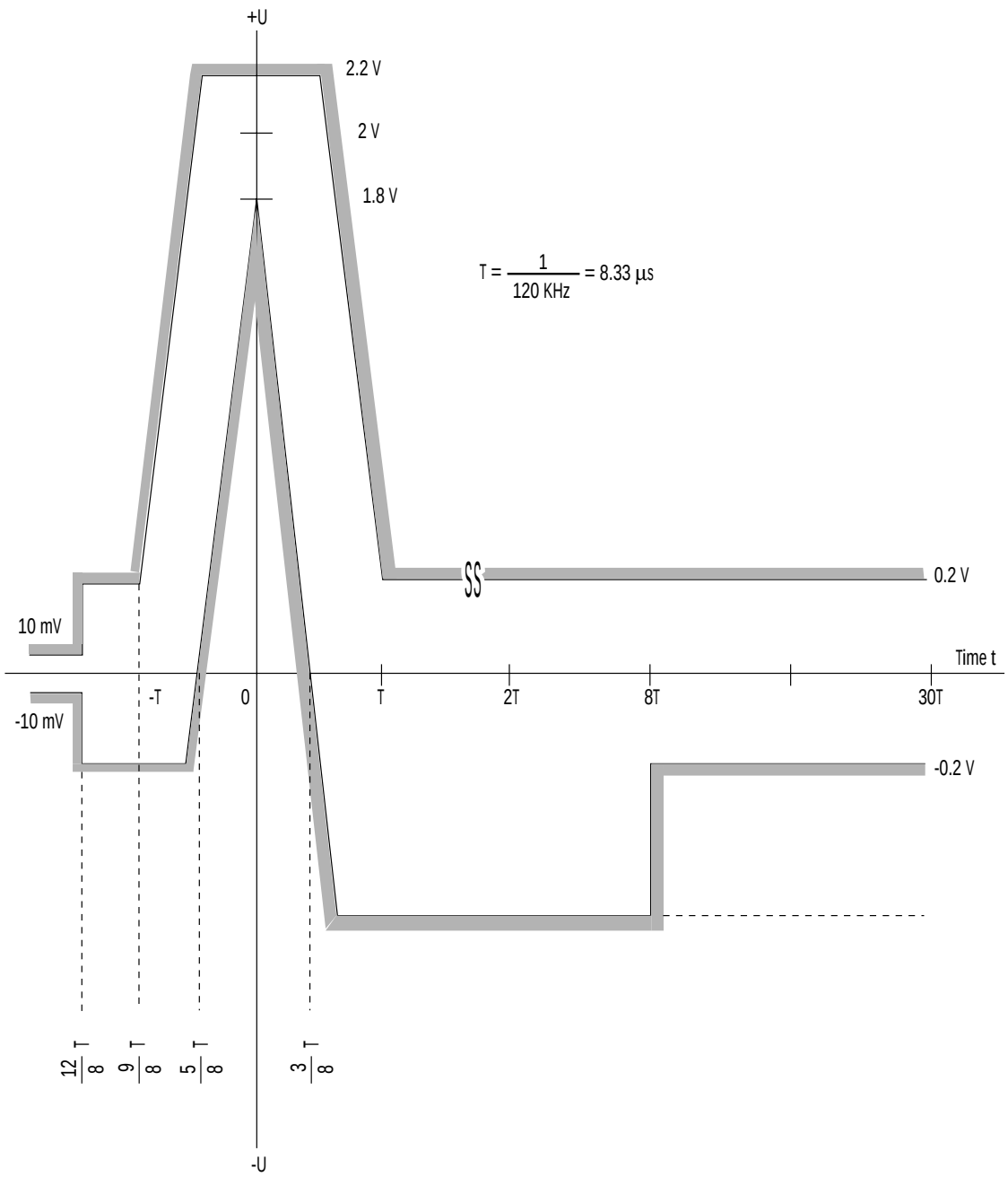


Fig.9: Single Pulse Mask, MTC-20279

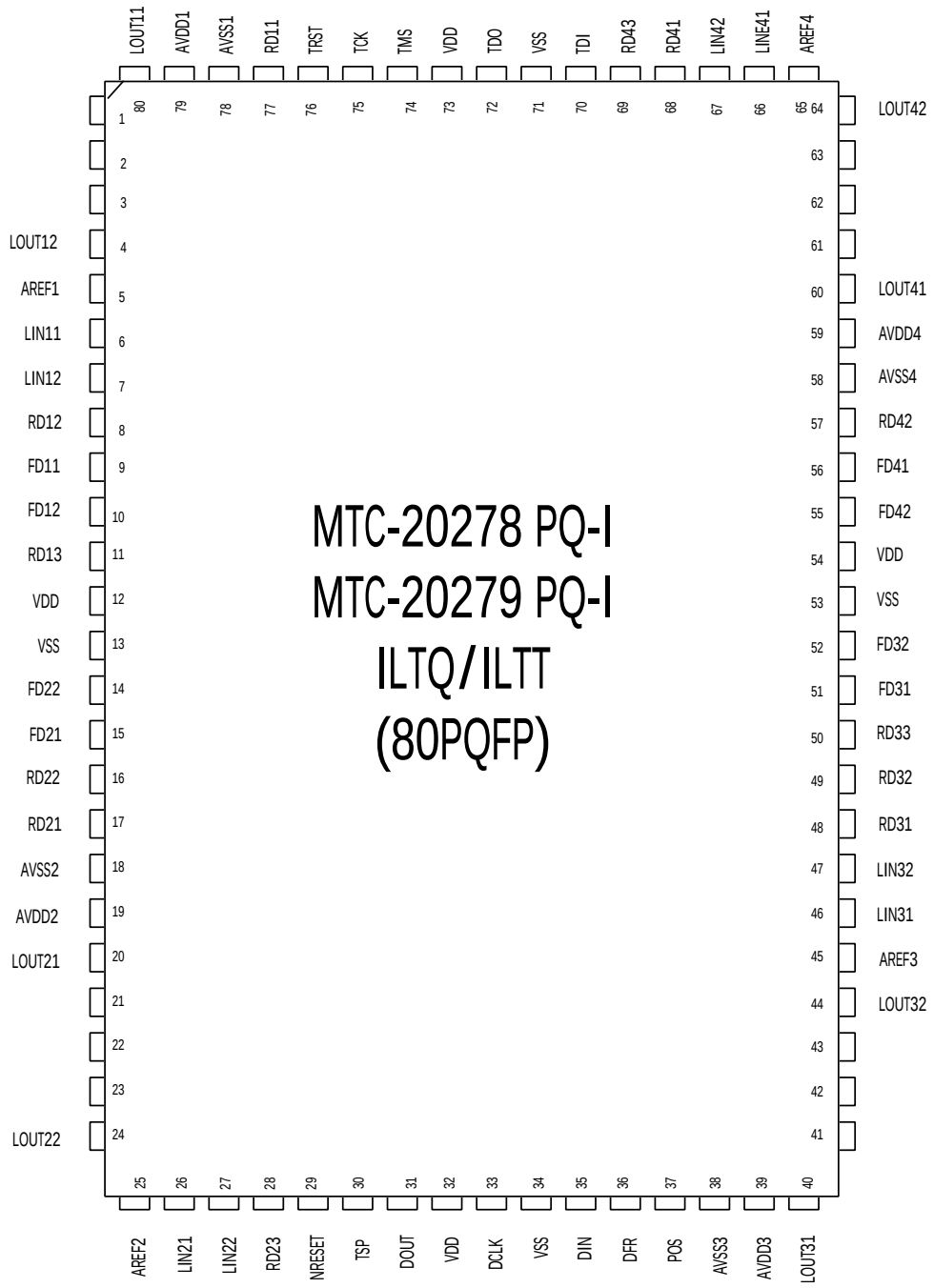


Fig.10: ILT Pinout - 80 PQFP

Pin Description

Nr.	Function	Name	Dir.	Description
80		LOUT11	O	U-Interface analog outputs. The pins LOUT11 and LOUT12 connect the U-driver outputs via termination resistors and the line coupling transformer to the U0 reference point.
4		LOUT12	O	
6		LIN11	I	U-Interface analog inputs from the analog hybrid
7		LIN12	I	
5	U1	AREF1	O	Analog ground. Used as reference voltage for A/D and D/A.
79	Interface	AVDD1	P	+3.3V power supply for analog U-Interface functions
78		AVSS1	P	0V ground for analog U-Interface functions
77		RD11 / SPICS	O	Relay drivers 1
8		RD12 / SPICK	O	
11		RD13	IO	Bidirectional I/O. Put in Input mode after HW reset, not affected by SW reset
9		FD11 / SPIDI	I	Power feed status and control 1
10		FD12 / SPIDO	O	
20		LOUT21	O	U-Interface analog outputs. The pins LOUT21 and LOUT22 connect the U-driver outputs via termination resistors and the line coupling transformer to the U0 reference point.
24		LOUT22	O	
26		LIN21	I	U-Interface analog inputs from the analog hybrid
27		LIN22	I	
25	U2	AREF2	O	Analog ground. Used as reference voltage for A/D and D/A
19	Interface	AVDD2	P	+3.3V power supply for analog U-Interface functions
18		AVSS2	P	0V ground for analog U-Interface functions
17		RD21	O	Relay drivers 2
16		RD22	O	
28		RD23	IO	Bidirectional I/O. Put in Input mode after HW reset, not affected by SWreset
15		FD21 / SEL0	I	Power feed status and control 2
14		FD22	O	
40		LOUT31	O	U-Interface analog outputs. The pins LOUT31 and LOUT32 connect the U-driver outputs via termination resistors and the line coupling transformer to the U0 reference point.
44		LOUT32	O	
46		LIN31	I	U-Interface analog inputs from the analog hybrid
47		LIN32	I	
45		AREF3	O	Analog ground. Used as reference voltage for A/D and D/A.
39	U3	AVDD3	P	+3.3V power supply for analog U-Interface functions
38	Interface	AVSS3	P	0V ground for analog U-Interface functions
48		RD31	O	Relay drivers 3
49		RD32	O	
50		RD33	IO	Bidirectional I/O. Put in Input mode after HW reset, not affected by SW reset
51		FD31 / SEL1	I	Power feed status and control 3
52		FD32	O	

60		LOUT41	O	U-Interface analog outputs. The pins LOUT41 and LOUT42 connect the U-driver outputs via termination resistors and the line coupling transformers to the U0 reference point.	
64		LOUT42	O		
66		LIN41	I	U-Interface analog inputs from the analog hybrid	
67	U4	LIN42	I		
65	Interface	AREF4	O	Analog ground. Used as reference voltage for A/D and D/A.	
59		AVDD4	P	+3.3V power supply for analog U-Interface functions	
58		AVSS4	P	0V ground for analog U-Interface functions	
68		RD41	O	Relay drivers 4	
57		RD42	O		
69		RD43	IO	Bidirectional I/O. Put in Input mode after HW reset, not affected by SW reset	
56		FD41	I	Power feed status and control 4	
55		FD42	O		
31		DOUT	O	GCI data output at 2048 Kbits/s. Open drain output.	
35	GCI	DIN	I	GCI data input at 2048 Kbit/s	
33	Interface	DCLK	I	4096kHz GCI clock	
36		DFR	I	8kHz GCI frame clock which identifies the beginning of the frame of DIN and DOUT	
					Normal use
76		TRST	I	TAP controller reset, active low	0
75	JTAG	TCK	I	TAP controller clock, maximum 10MHz	0
74	Test	TMS	I	TAP controller mode selection	0
70	Interface	TDI	I	TAP controller input	0
72		TDO	O	TAP controller output	open
29		NRESET	I	Hardware reset, active low. Schmit trigger input with treshold at 1.65V (CMOS level).	
30	General	TSP/DECT	I	1. Transmit Single Pulses. ILT transmits single pulses of alternating maximum positive and negative polarity. Pulse repetition rate is 666Hz. Applications: test purposes and search tone on the line. 2. DECT synchronization of the U-superframes (2B1Q only) The distinction between the 2 modes is made based on the duty cycle of the applied input signal: if logic '1' is present for more then 200ms, TSP is assumed ; otherwise, a DECT sync is executed.	
37		POS	I	ILT works in burst mode and consists of 4 line drivers, 1 line per burst. POS = '0' means the 4 fisrt GCI bursts are taken POS = '1' means the 4 last GCI bursts are taken	
12		VDD	P	+3.3V power supply for digital functions	
32		VDD	P		
54	Power	VDD	P		
73		VDD	P		
13		VSS	P	0V Ground for digital functions	
34		VSS	P		
53		VSS	P		
71		VSS	P		

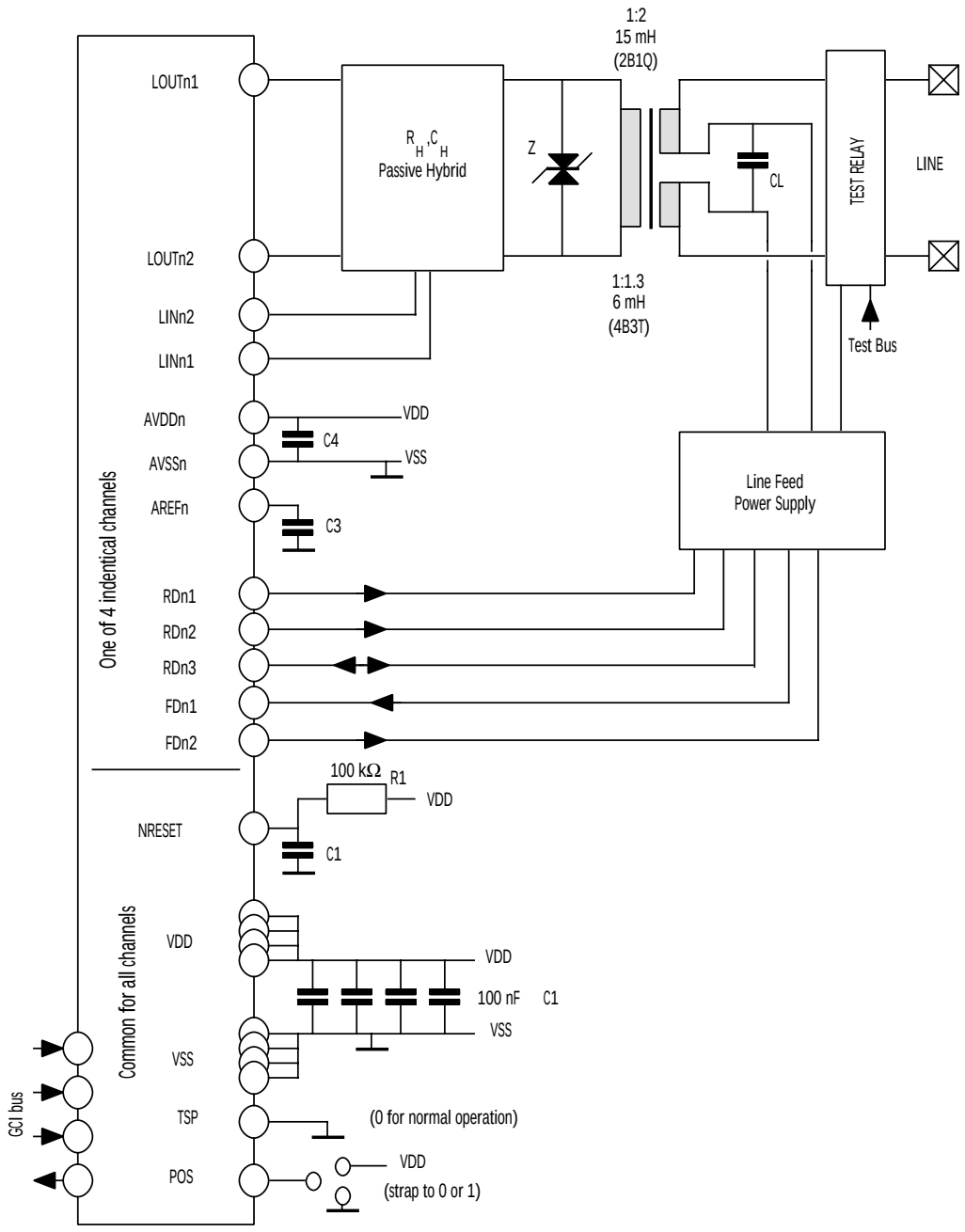


Fig.11: MTC-20278/9 ILT - Typical Component Configuration

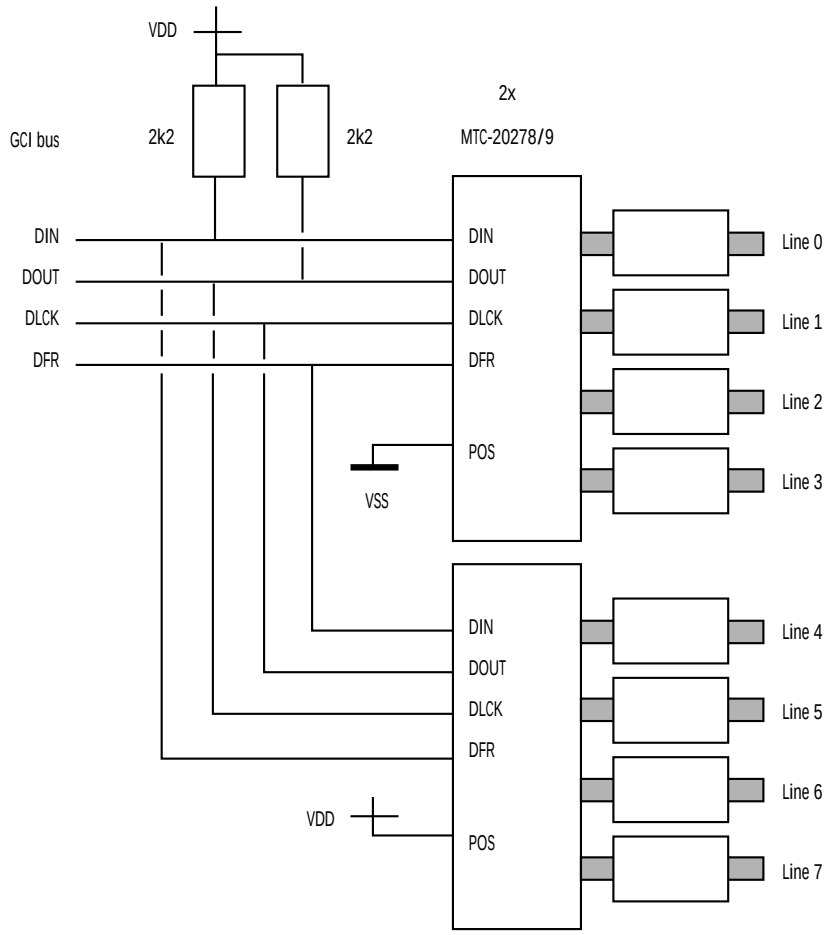


Fig.12: Connection of two, MTC-20278/9 for an 8-line access on one GCI bus

Transformer-Recommended Specifications

Table 1a (MTC-20278) **Table 1b (MTC-20279)**

	Min/Typ	Max	Min/Typ	Max
Turns Ratio	2:1			1.6:1
Prelimary Inductance (mH)	14.25	15.75	5.25	6.75
Leakage Inducatance (uH)		60		60
Interwinding Capacitance (pF max.)	90			90
PRI DCR (Ohms)	6	7	6	7
SEC DCR (Ohms)	2.8	3.3	3.5	4.2
	(Alcatel Part Code TMP 00087 0003)		(Alcatel Part Code TMP 00087 0002)	

Recommended Component Values

Table 2

Component	Function	Value	Comment
Rh	U feed bridge and hybrid resistors	see Fig. 13/14	±1%
R1	reset delay	100kΩ	±5%
C1	reset delay	100 nF	±5%
C2	Digital supply decoupling	100 nF	
C3	Analog reference decoupling	100 nF	
C4	Analog supply decoupling	100 nF	
CL	Line-feed coupling	2.2 µF	250V
Ch	Hybrid capacitance	see Fig. 13/14	2%
Z	overvoltage protection		

Common Hybrid Shematics for 4B3T (MTC-20279) and 2B1Q (MTC-20278)

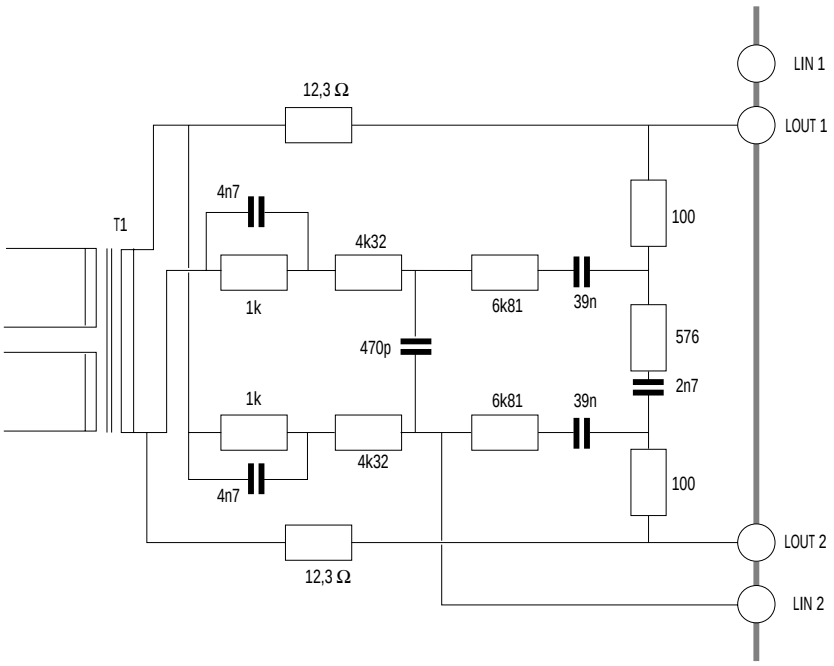


Fig.13: MTC-20278 - Recommended Hybrid component Configuration

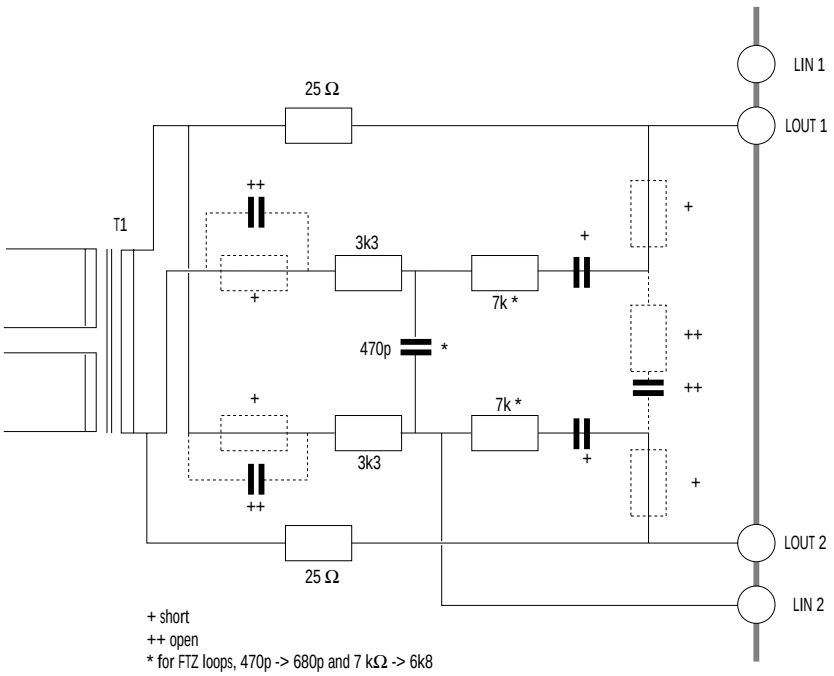


Fig.14: MTC-20279 - Recommended Hybrid component Configuration

MTC-20278

Logical Characteristics of the U Interface

The quaternary symbol stream crossing the U-interface complies with the following logical characteristics:

Frame Structure
The information flow across the subscriber line uses frames as shown in Figure 15. The length of such a frame corresponds to 120 quaternary symbols being transmitted within 1.5ms. The frame structure is detailed as follows.

B+B+D - Data
108 quaternary symbols represent 216 bits of scrambled and encoded B+B+D data. The 108 quaternary symbols are transmitted in succession. These blocks are assembled as follows:

Data of:	B1 +	B2 +	D +	B1 +	B2 +	D
Number of bits:	8	8	2	8	8	2

Synchronizing Word
9 quaternary symbols in each direction represent a non-scrambled synchronizing word. They are used to generate frame clocks. If they are out of position for 60 . . . 200 consecutive frames, the line resynchronization procedure is started. The quaternary values and the frame positions are as follows:
From LT to NT or analog loop in LT (loop 1) and from NT to LT.

SW Polarity:	+3	+3	-3	-3	-3	+3	-3	+3	+3
ISW Polarity:	-3	-3	+3	+3	+3	-3	+3	-3	-3

Quad Position	1-9	10-117	118-120
Bit Position	1-18	19-234	235-240

Frame 1	ISW	2B+D	2B+D	···	2B+D	2B+D	M1	···	M6
Frame 2	SW	2B+D	2B+D	···	2B+D	2B+D	M1	···	M6
Frame 3	SW	2B+D	2B+D	···	2B+D	2B+D	M1	···	M6
Frame 4	SW	2B+D	2B+D	···	2B+D	2B+D	M1	···	M6
Frame 5	SW	2B+D	2B+D	···	2B+D	2B+D	M1	···	M6
Frame 6	SW	2B+D	2B+D	···	2B+D	2B+D	M1	···	M6
Frame 7	SW	2B+D	2B+D	···	2B+D	2B+D	M1	···	M6
Frame 8	SW	2B+D	2B+D	···	2B+D	2B+D	M1	···	M6

Fig.15: Frame and Superframe Structure

Maintenance and Service Channel

3 quaternary symbols per frame are transmitted to convey maintenance and embedded operations channel information. This information is contained in a superframe consisting of 8 frames (duration: 12ms). The start of a superframe in the up and downstream directions is marked by a single inversion of the synchronisation word. The quaternary symbol sequences represent data that can be transmitted at a rate of 4 kbit/s. They are transmitted immediately before the sync word.

The M symbol is used for various purposes:
1) Maintenance Channel (control test loops and report frame errors)
2) Service Channel (carry transparent user data in both directions)
In detail the following convention applies (LT to NT):

ACT:	Activation bit (set to ONE during activation)
AIB:	Alarm indication bit (set = 0 to indicate interruption)
CRC:	Cyclic Redundancy Check: covers 2B+D & M4: 1 = most significant bit; 2 = next most significant bit, etc.
DEA:	turn-off bit (set = 0 to announce turn-off)

EOC:	Embedded operations channel:
	a = address bit;
	dm = data/message indicator;
	i = information (data/message).

FEBE:	Far end block error bit (ZERO for errored multiframes)
UOA:	U-only-activation bit

	M1	M2	M3	M4	M5	M6
Frame 1	EOC a1	EOC a2	EOC a3	ACT	1	1
Frame 2	EOC dm	EOC i1	EOC i2	DEA	1	FEBE
Frame 3	EOC i3	EOC i4	EOC i5	1	CRC 1	CRC 2
Frame 4	EOC i6	EOC i7	EOC i8	1	CRC 3	CRC 4
Frame 5	EOC a1	EOC a2	EOC a3	1	CRC 5	CRC 6
Frame 6	EOC dm	EOC i1	EOC i2	1	CRC 7	CRC 8
Frame 7	EOC i3	EOC i4	EOC i5	UOA	CRC 9	CRC 10
Frame 8	EOC i6	EOC i7	EOC i8	AIB	CRC 11	CRC 12

Encoding

The encoding of a binary bit stream is made such that 2 binary bits correspond to 1quaternary symbol. The first symbol of a frame will always contain the information of the first 2 bits of a B1 channel (although these bits are of course scrambled.

In the receive direction, the first symbol of the quaternary frame is always converted (after descrambling) into the first two bits of a B1 channel.
The exact convertion is done according to the following rules (ANSI specification):

Quaternary Symbol	First bit (sign)	Second bit (Magnitude)
+3	1	0
+1	1	1
-1	0	1
-3	0	0

Scrambling
The received binary data stream is divided by generating polynomials.

The scrambler contains supervision circuitry which flags if a continuous series of ones or zeros have been detected at the output for a complete 1ms frame.

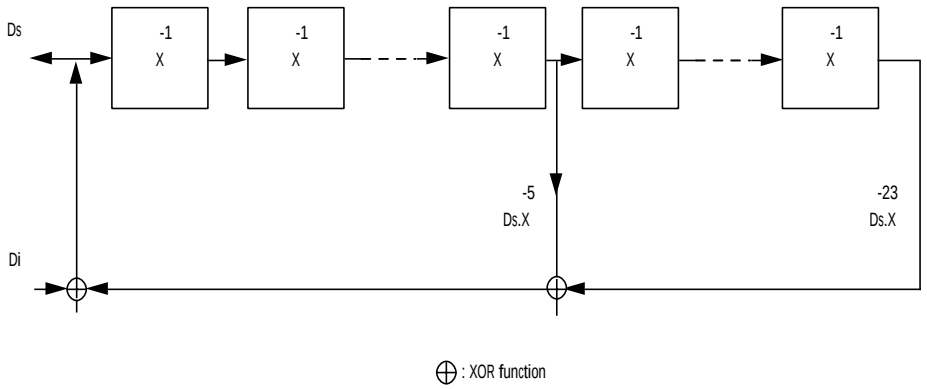


Fig.16: LT Transmit Scrambler

Descrambling
The quaternary signals received on each side of the subscriber line are converted back into a binary bit stream and multiplied by the generating polynomials in order to recover the original data.

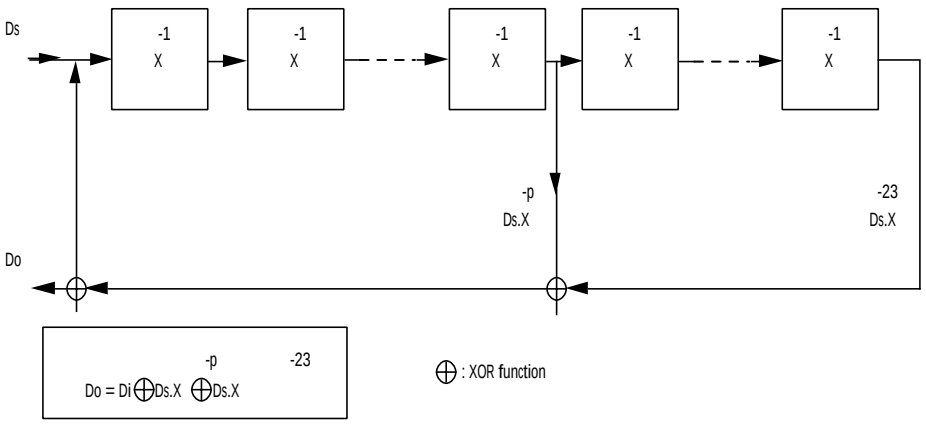


Fig.17: LT Receive Descrambler

Activation and Deactivation
In order to reduce the power consumption of circuits connected to the subscriber line, ILTQ can be switched to stand-by or powered down during the idle period. The components are powered up again during the line activation procedure. Two states are defined:

- Power-down state
  Power consumption of the majority of the functions is reduced by stopping the clocks; maximum power reduction;
- Power-up state
  All functions powered up; GCI interface is activated; exchange of C/I messages possible.

The activation procedure consists of three phases: awake (see the following sections), synchronize, and connect through.
The phases of activation are shown in the following table.

Phase	Indication LT
power-down	DC
awake	ACT
synchronize	
connect through	CT

Conditions for ACT and CT (see table 3 on page 22).

Maximum activation time (from command ACT to indication CT) without repeater for LT +NT:

- < 300ms under normal conditions (starting with stored coefficients: See note on DECT synchronisation).
- 15s after reset of the coefficients

With repeater, the activation may take twice as long.

Maximum activation time (from command ACT to indication CT) without repeater for LT:

- < 150ms under normal conditions (starting with stored coefficients)
- 10s after reset of the coefficients

The deactivation procedure consists of two phases: line deactivation and power-down (see table 3).

The deactivation can be initiated only by the command DEAC in the LT. The deactivation of the LT can be initiated only by INFO U0. The phases of deactivation are indicated in the following table.

Phase	Indication LT
power-up (connected through)	CT
Line deactivation	DEAC
power-down	DC

Conditions for DC and DEAC (see table 3 on page 22).

Deactivation time (from Command DEAC to Indication DC) is of the order of 4ms.
With repeater the deactivation may take twice as long.

Reset
The ILTQ can be reset via an external pin (NRESET = LOW) or via the command RES in the C/I channel. Normally the ILTQ is reset via the pin NRESET (hardware reset).
The ILTQ is initialized such that a "cold start" (resetting of the coefficients) is performed.
Resetting the component affects the status of the driver pins; after HW reset the drivers are switched off (low output level) but not changed after SW reset. (See also the Monitor channel).

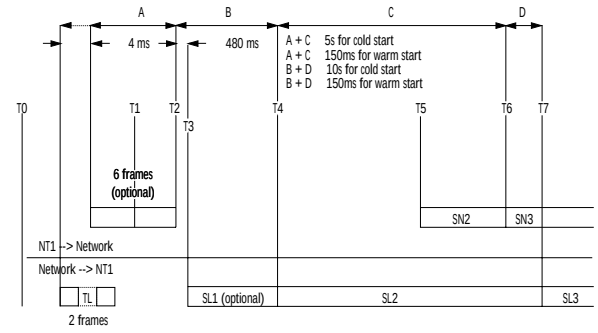
Loops
For maintenance purposes a loop can be closed by applying the correct command via the M channel or the GCI C/I channel.

Activation signals

The MTC-20278 can transmit any of the signals shown in Table 3.

Table 3: LT Activation Signals

Information Station	Description
TL	A 10 kHz tone consisting of alternating four + 3 quats followed by four - 3 quats for a time period of two frames.
SL0	No signal transmitted.
SL1	Synchronization word present, no superframe synchronization word (ISW), and 2B+D+M = 1.
SL2	Synchronization word present, superframe synchronization word (ISW) present, 2B+D = 0, and M = Normal.
SL3	Synchronization word present, superframe synchronization word (ISW) present. M channel bits active. Transmitted 2B+D data operational when M4 act bit = 1. When M4 act = 0, transmitted 2B+D data = 0.



Time: Description of event or state:
T0 RESET state.
T1 Network and NT1 are awake.
T2 NT1 discontinues transmission, indicating that the NT1 is ready to receive signal.
T3 Network responds to termination of signal and begins transmitting signal towards to NT1.
T4 Network begins transmitting SL2 towards the network, indicating that the network is ready to receive SN2.
T5 NT1 begins transmitting SN2 towards the network, indicating that NT1 has acquired FW frame and detected SL2.
T6 NT1 has acquired multiframe marker and is fully operational.
T7 Network has acquired multiframe marker and is fully operational.
NOTE 1: If the TL is repeated due to the persistence of FE 1, the repetition interval shall be > 25ms. At a repetition interval larger than 480ms, the state machine will cause a TL tone if FE 1 remains.
NOTE 2: The maximum time between TL tone is defined to be 4ms. This requirement is unnecessarily strict. To allow transceivers which cannot meet this the LT should wait for, and accept the TN tone, for a period of 10ms from the beginning of issuing the TL tone.

Fig.18a: State sequence for transceiver start-up

DECT Synchronisation

The 4 U frames and superframes are aligned with the DECT synchronisation signal with a precision of 1 symbol, in the activation procedure.

At the rising edge of the DECT signal, bit and frame counters are set to zero. DECT synchronisation needs soft or hard reset, precludes total power-down (that is replaced by partial power-down), and warm-start may require 2.4 additional seconds. The DECT signal has a periodicity of 2.4 seconds and the width of the pulse can be between 13 and 375 microseconds.

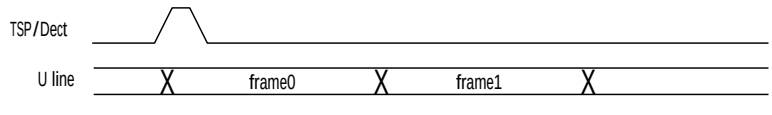


Fig.18b: Dect Synchronisation

MTC-20279

Logical Characteristics of the GCI Interface

The ternary symbol stream crossing the U-interface comply with the following logical characteristics:

Data of:	B1 +	B2 +	D +	B1 +	B2 +	D
Number of bits:	8	8	2	8	8	2

Frame Structure
The information flow across the subscriber line utilizes frames as shown in Figure 9. The length of such a frame corresponds to 120 ternary symbols being transmitted within 1ms. The frame structure is detailed as follows.

B+B+D - Data
108 ternary symbols (T1 . . . T8) represent 144 bits of scrambled and encoded B+B+D data. The 108 ternary symbols are divided into four equally structured groups in which each group of 27 ternary symbols corresponds to a block of 36 binary bits (consult also Figure 9 and Figure 10). These blocks are assembled as follows:

Synchronizing Word
11 ternary symbols in each direction (SW1, SW2) represent a non-scrambled synchronizing word. They are used to generate frame clocks. If they are out of position for 60 . . . 200 consecutive frames, the line resynchronization procedure is started. The ternary values and the frame positions are as follows:

From LT to NT or analog loop in LT (loop 1) (LT Transmit):

Frame position:	110	111	112	113	114	115	116	117	118	119	120
SW1 Polarity:	+	+	+	-	-	-	+	-	-	+	-

From NT to LT (LT Receive):

Frame position:	50	51	52	53	54	55	56	57	58	59	60
SW1 Polarity:	-	+	-	-	+	-	-	-	+	+	+

Table 4: Ternary Frame Structure

LT -› NT or analog loop in LT (loop 1)

1	2	3	4	5	6	7	8	9	10	11	12	
T1	T1	T1	T1	T1	T1	T1	T1	T1	T1	T1	T1	12
T1	T1	T1	T1	T1	T1	T1	T1	T1	T1	T1	T1	24
T1	T1	T1	T2	T2	T2	T2	T2	T2	T2	T2	T2	36
T2	T2	T2	T2	T2	T2	T2	T2	T2	T2	T2	T2	48
T2	T2	T2	T2	T2	T2	T3	T3	T3	T3	T3	T3	60
T3	T3	T3	T3	T3	T3	T3	T3	T3	T3	T3	T3	72
T3	T3	T3	T3	T3	T3	T3	T3	T3	T4	T4	T4	84
M1	T4	T4	T4	T4	T4	T4	T4	T4	T4	T4	T4	96
T4	T4	T4	T4	T4	T4	T4	T4	T4	T4	T4	T4	108
T4												120

NT -› LT

1	2	3	4	5	6	7	8	9	10	11	12	
T5	T5	T5	T5	T5	T5	T5	T5	T5	T5	T5	T5	12
T5	T5	T5	T5	T5	T5	T5	T5	T5	T5	T5	T5	24
M2	T5	T5	T5	T6	T6	T6	T6	T6	T6	T6	T6	36
T6	T6	T6	T6	T6	T6	T6	T6	T6	T6	T6	T6	48
T6												60
T6	T6	T6	T6	T6	T6	T7	T7	T7	T7	T7	T7	72
T7	T7	T7	T7	T7	T7	T7	T7	T7	T7	T7	T7	84
T7	T7	T7	T7	T7	T7	T7	T7	T7	T8	T8	T8	96
T8	T8	T8	T8	T8	T8	T8	T8	T8	T8	T8	T8	108
T8	T8	T8	T8	T8	T8	T8	T8	T8	T8	T8	T8	120

Legend:
T1 . . . T8: B + B + D - Data (ternary)
M1, M2: Maintenance and Service Data (ternary)
SW1, SW2: Synchronizing Word

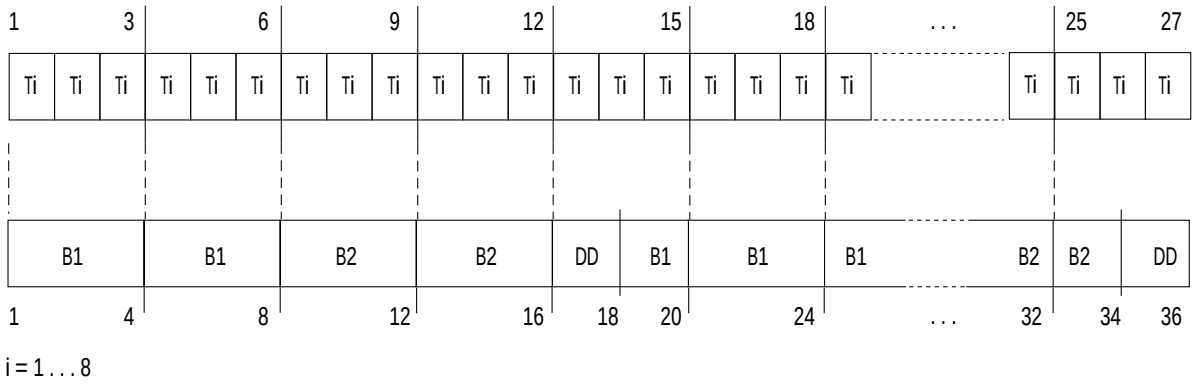


Fig.19: Binary to Ternary Unit Correspondence of B + B + D - Data

Maintenance and Service Channel

The ternary symbols (M1, M2) represent non-scrambled data that can be transmitted at a rate of 1 kBaud. The frame position for M1 is 85 and for M2 it is 25 (see Figure 9).
The M symbol is used for various purposes:

1) Maintenance Channel (control test loops and report frame errors)
2) Service Channel (carry transparent user data in both directions); this is not supported by the MTC-20279.
In detail the following convention applies:

Table 5: Service and Maintenance Data Convention

	Meaning	Encoding	Direction
	Idle	0	Both
Maintenance Channel (M + Channel)	Loop 2 in NT (1)	++++.....	from LT to NT
	Loop 4 in RPTR	+0+0+.....	from LT to RPTR
	Frame Error (2)	+ (single symbol)	from NT to LT

NOTE 1:
A loop function is performed, if on eight consecutive frames the ternary encoding is recognized.
A loop function is finished if eight consecutive ternary zeros are recognized, or on line deactivation.

NOTE 2:
One or more code violations detected by RDS (Running Digital Sum) checks or non-permissible series of 8 0_polarity symbols within one frame lead to one frame error.

Encoding
The encoding of a binary bit stream is made such that 4 binary bits correspond to 3 symbols of the ternary symbol stream (4B/3T encoding scheme). The encoding follows the rules of modified monitoring state 43 (MMS 43) which contains four alphabets. The left most bit of the binary value in column 1 of Figure 12 represents the first received bit of the binary bit stream.
Corresponding to this, the left most indicated symbol of the ternary word is transmitted first.

The alphabet used for encoding of a given binary block depends on the digital sum of previous three ternary symbols transmitted. Therefore, the alphabet to be used for encoding of the next binary block is indicated by a suffix number beside each ternary word.
After reset any alphabet can be used.
The running digital sum (RDS) is computed in the RDS monitor (RDSM) from the received ternary symbols.

When at the end of a ternary block the running digital sum equals zero or five a code violation has occured.
The RDS monitor is reset to one at the beginning of each frame. RDS errors which are reported back from the NT to the LT are also accumulated in the RDS monitor.
One or more RDS errors or one or more series of five or more zeros within one frame lead to one frame error.

Table 6: MMS 43 - Code

Binary Information	Ternary Alphabets (left symbol is transmitted first)			
	S1	S2	S3	S4
0001	0-+1	0-+2	0-+3	0-+4
0111	-0+1	-0+2	-0+3	-0+4
0100	-+01	-+02	-+03	-+04
0010	+-01	+-02	+-03	+-04
1011	+0-1	+0-2	+03	+0-4
1110	0+-1	0+-2	0+-3	0+-4
1001	+-+2	+-+3	+-+4	- - -1
0011	00+2	00+3	00+4	- - 02
1101	0+02	0+03	0+04	-0-2
1000	+002	+003	+004	0- -2
0110	-++2	-++3	- -+2	- -+3
1010	++-2	++-3	+- -2	+- -3
1111	++03	00-1	00-2	00-3
0000	+0+3	0-01	0-02	0-03
0101	0++3	-001	-002	-003
1100	+++4	-+-1	-+-2	-+-3

Note that the received 3T-word 000 is transformed into a 4B-word of 0000. This pattern occurs only during deactivation.

Scrambling
The received binary data stream is divided by generating polynomials.

The scrambler contains supervision circuitry which flags if a continuous series of ones or zeros have been detected at the output for a complete 1ms frame.

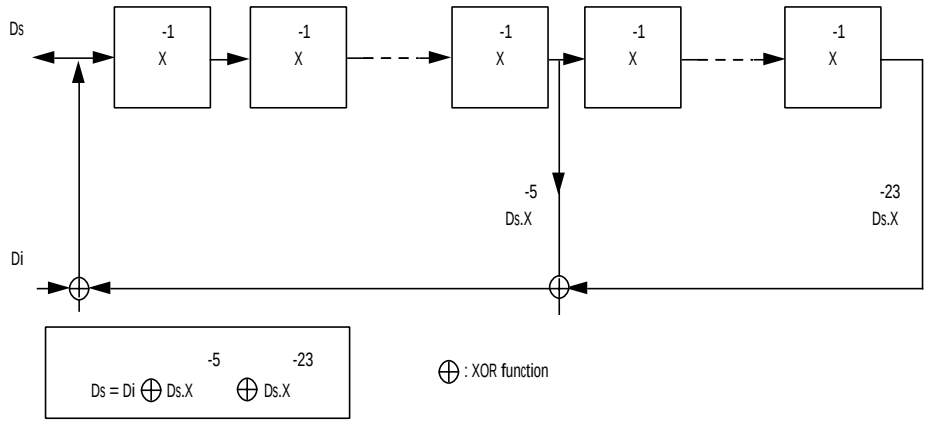


Fig.20: LT transmit scrambler

Descrambling
The ternary signals received on each side of the subscriber line are converted back into a binary bit stream and multiplied by the generating polynomials in order to recover the original data.

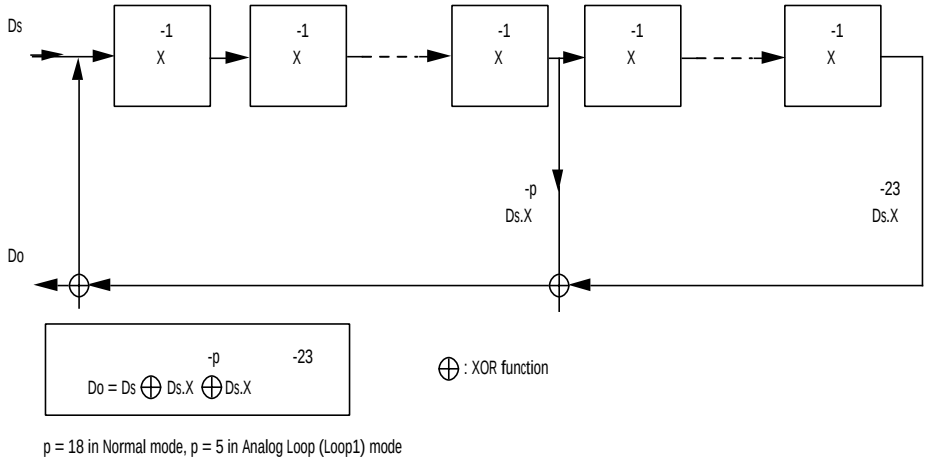


Fig.21: LT receive descrambler

Activation and Deactivation
In order to reduce the power consumption of circuits connected to the subscriber line,the ILTT is powered down during idle period. The components are powered up again during the line activation procedure. Two states are defined:

- Power-down state
  Power consumption of the majority of the functions is reduced by stopping the clocks; maximum power reduction;

- Power-up state
  All functions powered up.

The activation procedure consists of three phases: awake (see the following sections), synchronize, and connect through.

The phases of activation are indicated according to the following table.

Phase	Indication
	LT
power-down	DC
awake	ACT
synchronize	RDS
connect through	CT

Conditions for RDS, ACT and CT see 8.2.

Maximum activation time (from command ACT to indication CT) without RPTR:

- ≤ 210ms under normal conditions (starting with stored coefficients)

- 1.5s after reset of the coefficients

The deactivation procedure consists of two phases: line deactivation and power-down (see 8.2).

The deactivation can be initiated only by the command DEAC in the LT. The deactivation of the LT can be initiated only by INFO U0. The phases of deactivation are indicated in the following table.

Phase	Indication
	LT
power-up (connected through)	CT
Line deactivation	DEAC
power-down	DC

Conditions for DC and DEAC see 8.2.

Deactivation time (from Command DEAC to Indication DC) is in the order of 4ms.
With RPTR the deactivation may take twice as long.

Note:
When powered down, execution of commands via the M-Channel is not possible. To allow M-Channel commands to be used, issue the DGAC command on the CII bits.

Reset
The ILTT can be reset via an external pin (NRESET = LOW) or via the command RES in the C/I channel. Normally the ILTT is reset via the pin NRESET (hardware reset).
Both reset requests cause via the activation/deactivation control (ACDECO) and the reset logic a reset for various functional blocks. The ILTT is initialized such that after reset a “cold start” (resetting of the coefficients) is forced. Resetting the component affects the status of the Relay drivers; after HW reset the Relay drivers are switched off (low output level), but after a SW reset the status of the Relay drivers is not modified. See also 8.4.

Loop2 (Loop in NT)
For maintenance purposes a loop can be closed by applying the correct command into the M channel or into the GCI C/I channel.

Logical Characteristics of the GCI Interface

Data Format and Timing at the GCI Interface (DIN, DOUT, DCLK, DFR)

Continuous Modes

- Nominal bitrate of data (DIN and DOUT): 2048 kbit/s
- Nominal frequency of clock (DCLK): 4096kHz
- Nominal frequency of frame clock (DFR): 8kHz

The following Figure shows the timing of data and clocks at the digital interface 2048 kbit/s (continuous modes). See the AC characteristics section for details. Transitions of the data occur after even-numbered rising edges of the clock DCLK. The data is valid on the odd-numbered rising edges of the clock DCLK.
Even-numbered rising edges of the clock are defined as the second rising edge following the rising edge of the frame clock and every second rising edge thereafter.

The frame is marked by the rising edge of the frame clock DFR and the data/frames are sampled on falling edge of DCLK. Note that the position of the falling edge of DFR is not important. One frame contains 8 bursts 4 bytes. The data streams at DIN and DOUT consist of 32 bytes per frame. See Figure 13. The input data DIN and the output data DOUT are synchronous and in phase.
Depending on the level of the pin POS. The quad-LT takes the 4 first or the 4 last time-slots.

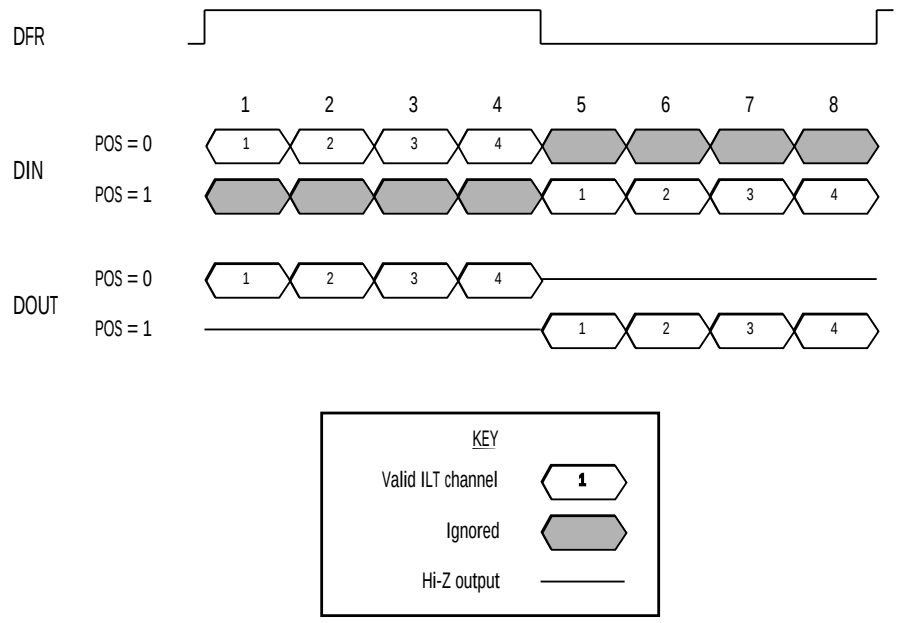


Fig.22: GCI Bus Multiplexing Timing Diagram

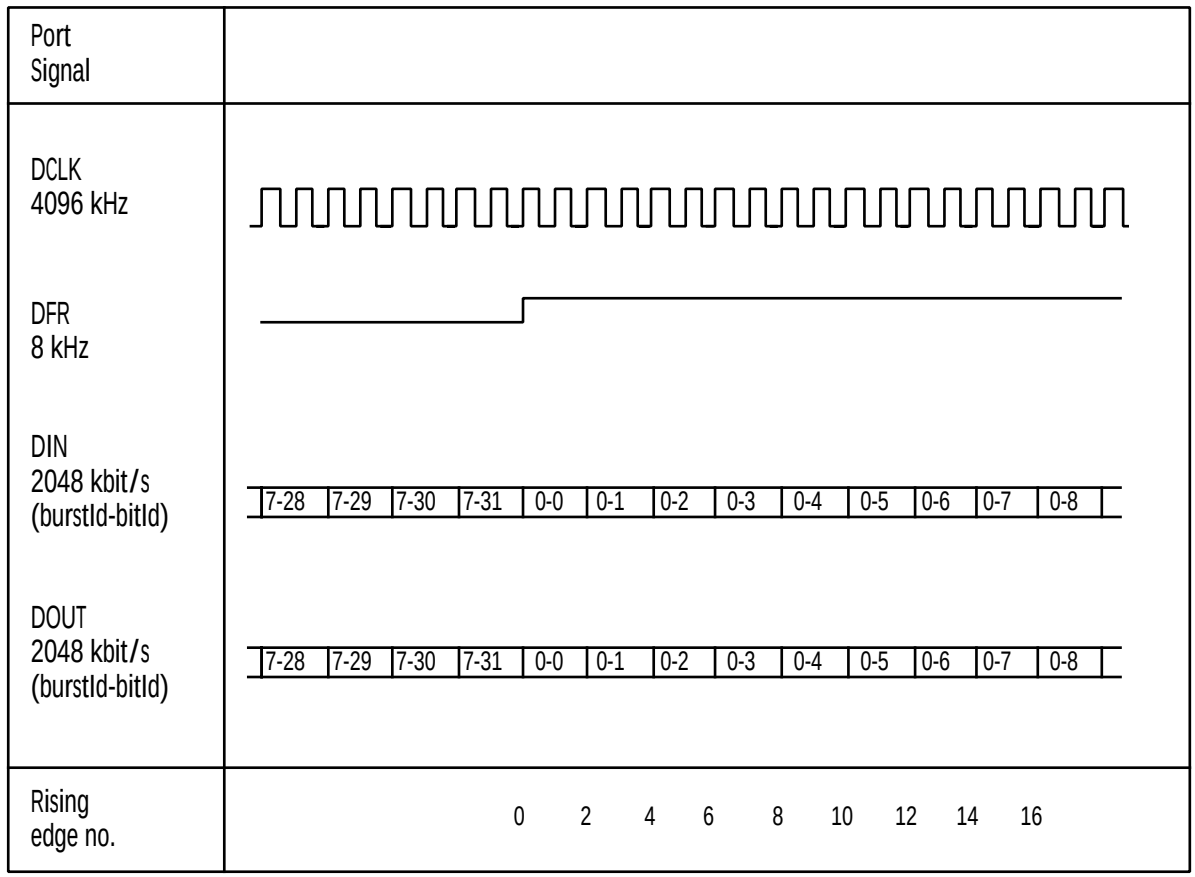


Fig.23: Timing of Data and Clocks at the 2048 kbit/s Interface

Frame Format

Within each time-slot, 4 bytes are transmitted:

1st byte B1: B channel (64 kbit/s data), transparent
2nd byte B2: B channel (64 kbit/s data), transparent
3rd byte B2*: Monitor channel
4th byte B1*: 2 bit D channel (16 kbit/s data)
4 bit C/I channel A1, A2, A3, A4
A, E bit used to control the transfer of information on the Monitor channel

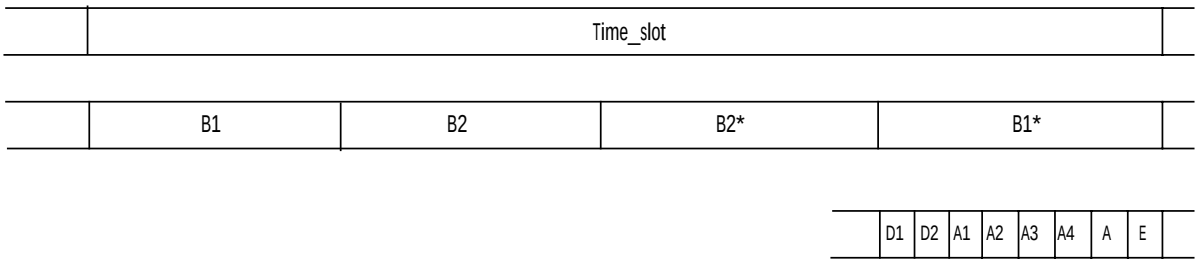


Fig.24: GCI Frame Format

Command and Indicate (C/I) Channel (A bits), MTC-20278

Command (DIN)

Deactivate	DEACR	0000	Request to deactivate U0. The transmitter outputs INFO U0. After detecting the disappearance of an incoming signal at U0 the indication DC is transmitted at module interface.
Reset	RESI	0001	Reset of ILTQ to initial state.
Reset receiver	RESR	0100	Reset of the ILTQ receiver only
Send Single Pulses	TXSSP	0101	The ILTQ transmits single pulses at 1.5ms time intervals with alternate polarity +3/-3.
Test	TEST	0110	The ILTQ will be connected through from module interface to line interface (transparent) without wake-up procedure.
U activation request	ARUO	0111	Activation request of the U0 interface only.
Activate	ACT	1000	Request to activate. ACT is indicated. The ILTQ is set in power-up state, executing the complete activation of layer 1: the wake-up procedure is executed by transmission of INFO U2W. After successful wake-up process, the synchronization procedure is started by transmission of INFO U2 (in case of LT).
Activation request 2	ACTX	1001	Activation request without 15 sec limit.
Analog Loop	AL	1010	ACT is indicated.The analog transmitter output is looped back to the receiver input (channels B+B+D), which is disconnected from the U0 interface.
Activation request 3	ACT0	1101	Activation request with ACT bit = 0.
DeactivateConfirmation	DCON	1111	No signal is transmitted at U0 and the ILTQ is powerd down. The wake-up detect circuitry remains enabled: thus a detected wake-up signal INFO U1W is able to power-up the UIC and to initiate the activation procedure, as in case of control ACT applied.

Note that RES or RES1 do not change the driver pins status while a hard reset configures RDi3 as input.
Note that at power-up, a DC command has to be given prior to any other command or DIN has to be one.

Indication (DOUT)

Deactivate	DEACA	0001	The ILTQ is deactivating. Data transmission is impossible.
Loss of synchronization	RSYN	0100	Loss of synchronization.
Error indication 2	EIST	0101	Error indication on the S/T interface.
U activation indication	UAIN	0111	U activation indication.
Activate	ACT	1000	The signal INFO U1W has been recognized by the wake-up detect circuitry. The ILTQ is powered up and the activation procedure will be executed.
Activation request info.	ARMB	1001	Activation request maintenance bits
Error indication 3	EIRTI	1011	Error indication for timeout T1 (15s) or error on the U0 interface.
ConnectionThrough	CT	1100	The transparent channels are connected through from module to line interface (transparent). The activation of Layer 1 up to the terminals is completed.
Loss of signal level on U	LSLU	1101	Loss of signal level on U.
Deactivate indication	DIN	1111	After deactivation of U0 (by the command DEAC) the disappearance of incoming signal (INFO U0) has been detected.

Summary of C/I Codes:

Evaluation of any command is done according to a double last look criterion: any command is executed only after the same command has been detected in two successive frames. Until then, the preceding command is considered valid.

In case commands are received that are not included in the list, the last recognized command is considered valid. Commands which are logically impossible in the current state are ignored (cfr ETR 80).

The indications are transmitted continuously in each frame.

Under no circumstances can an indication that is not included in the list be transmitted.

Table 8: C/I Codes Summary

Code A-bits						
1	**2**	**3**	**4**	**HEX**	**DIN**	**DOUT**
0	0	0	0	0	DEACR	
0	0	0	1	1	RESI	DEACA
0	0	1	0	2		
0	0	1	1	3		
0	1	0	0	4	RESR	RSYN
0	1	0	1	5	TXSSP	EIST
0	1	1	0	6	TEST	
0	1	1	1	7	ARUO	UAIN
1	0	0	0	8	ACT	ACT
1	0	0	1	9	ACTX	ARMB
1	0	1	0	A	AL	
1	0	1	1	B		EIT1
1	1	0	0	C		CT
1	1	0	1	D	ACT0	LSLU
1	1	1	0	E		
1	1	1	1	F	DCON	DIN

A and E Bits

The A and E bits provide a handshake procedure for the transfer of monitor channel messages.
The transmitted E bit is put low for one frame when a new information has been written in the monitor channel. The transmitter then waits for confirmation indicted by the receiver puting low the A bit for one frame.
Thus to send a monitor message from the Exchange to the ILTQ, the E bit on DIN and the A bit on DOUT are used. In the opposite direction, the E bit on DOUT and the A bit on DIN are used.

Monitor Channel

Monitor messages sent to the ILTQ are 2 bytes long and monitor messages returned by the ILTQ are also 2 bytes long.

The monitor messages are split into 3 categories:
- MON-0: EOC programming
- MON-2: Overhead bits
- MON-8: Local functions

MON-0 messages
Format:
0000 AAA1 FFFF FFFF

0000 = MON-0 command
AAA = Address
0 = NT
1..6 = Repeater
7 = Broadcast
FF...FF: EOC code (see table)

Code (hex)	Down stream	Up stream	
00	Hold	Hold	Hold
50	CCLB		Complete loop
51	CLB1		Close Loop B1
52	CLB2		Close Loop B2
53	RCCRC		Request corrupt CRC
54	NCCRC		Notify corrupt CRC
AA		NAC	Not able to comply
FF	Return		Return to normal
XX		ACKN	Acknowledge*

* ACKN: Acknowledge. The NT will acknowledge a valid MON command by echoing it in the upstream direction.

MON-2 messages

Format:

0010 $D_{11..8}$ $D_{7..4}$ $D_{3..0}$

Only the Up stream EOC messages are supported. Down stream EOC commands are controlled by the ILTQ.

	Up stream	
D11	ACT	Activation bit
D10	1	
D9	1	
D8	PS1	Power supply 1bit
D7	1	
D6	FEBE	Far-end block error occured
D5	PS2	Power supply 2 bit
D4	NTM	
D3	CSO	Nt-activation with cold start only
D2	1	
D1	SAI	S activity indicator
D0	1	

After hard reset:
- RDx1: output
- RDx2: output
- RDx3: input
- FDx1: input
- FDx2: output

MON-command 817x will set the value of the driving pins

The MON-command 816x will change the direction of the RDx3 pin:
8160: input direction
8168: output direction

Note: so, for applications requiring 3 driver pins and 2 sens pins, the MON-command and Hard-reset can affect them.

The status of the drivers is not affected by a soft-reset, only MON-command and HARD-reset can affect them.

The MON-commands are executed in “soft-reset” mode.

MON-8 messages
Format: 1000 000A $D_{7..4}$ $D_{3..0}$

A	$D_{7..0}$	Down stream	Up stream	
0	1111 0000	SCCRC		Corrupt CRC
0	1111 1111	RTN		Return to Normal
0	1111 1011	RBECN		Read Near-end block error counter
0	1111 1010	RBECF		Read Far-end block error counter
0	aaaa aaaa		ABEC*	Answer block error counter
1	0111 dcba	SETDD		Set state of driver pins a: RDi1 b: Di2 c: FDi2 d: not used (RDi3 is INPUT)
1	0110 dcba	SETDO		Set status of driver pins a: RDi1 b: RDi2 c: FDi2 d: RDi3 (pin is OUTPUT)
1	0000 0000	RSP		Read status pins
1	xxxx xxxba		ASP	Answer status pins a: read the pin FDi1 b: read the pin RDi3 (used as sens pin)
1	1000 0000	RPDUI		Read propagation delay U-interface
e	aaaa aaaa		APDUI	Answer propagation delay on U-interface
0	1111 1001	ZFEBE		Set FEBE-Bit to zero
0	0000 0000	RCID		Read chip identification
0	0000 1000		ACID	Answer chip identification

e is 3 bits in length.
Total delay (inns) is given by the approximate formula:

D = N * 12,500 + S * M * 65ns

Where:

N is the value represented by bits 10..8 of PDu
S is +1 when bit 7 of APDU is 0, or -1 if it is 1
M is the value represented by bits 6..0 of PDu

PDu is the 11-bit propagation-delay (U interface) word.

A more precise description can be found in application note ”DECT delay calibration for ILTQ”.

Format: 1000 100A $D_{7..4}$ $D_{3..0}$

A	$D_{7..0}$	Down stream	Up stream	
0	cccc cccc	RCF		Read coefficients at address cccc cccc
0	0000 0000		DCF	Data coefficients, 1 byte, put to zero

MTC-20278 State Machine

activationRequest
CI = ACT
CI = ACTX
CI = ACT0
CI = UAR
CI = AL

CI	CMD.	IND.
0	DEAC	
1	RES	DEAC
2		
3		
4	RES1	RSY
5	SSP	EI2
6	TEST	
7	UAR	UAI
8	ACT	ACT
9	ACTX	ARM
A	AL	
B		EI3
C		CT
D	ACT0	LSL
E		
F	DC	DI

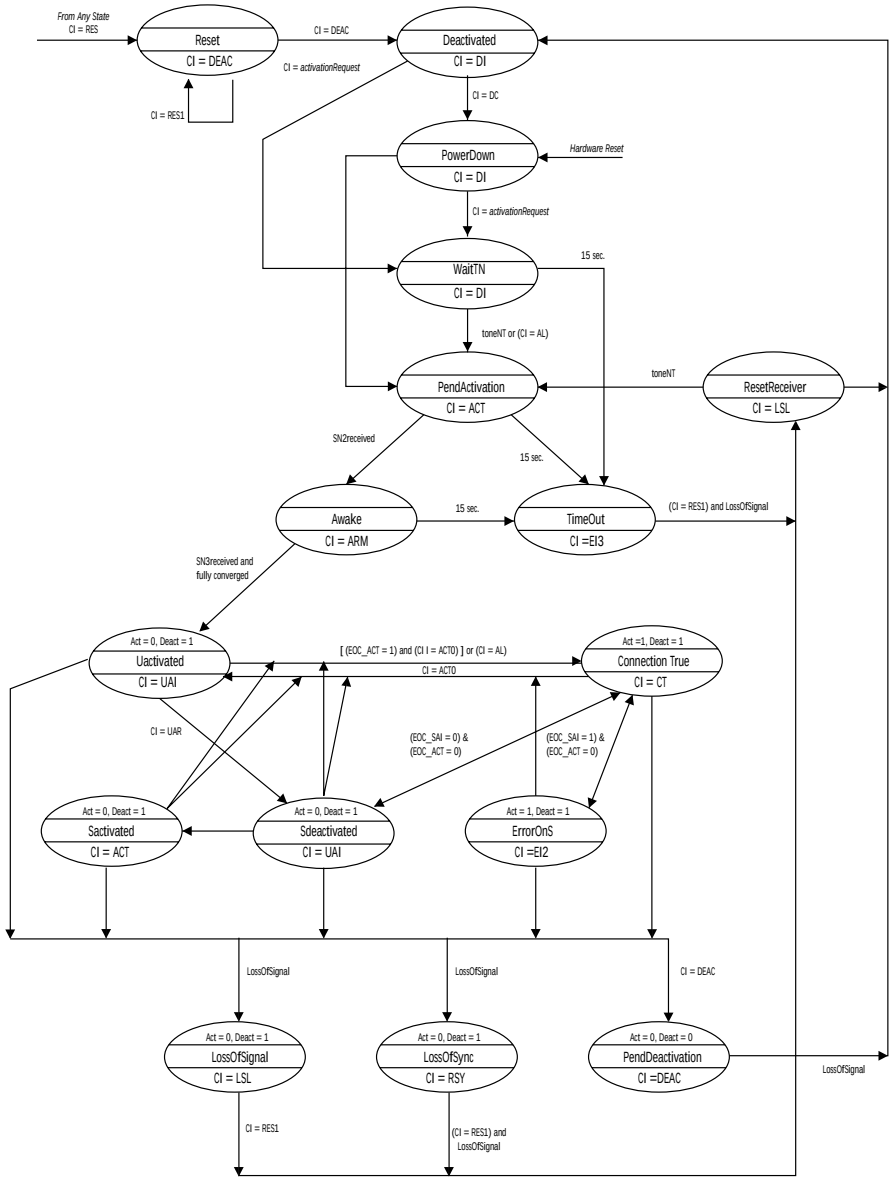
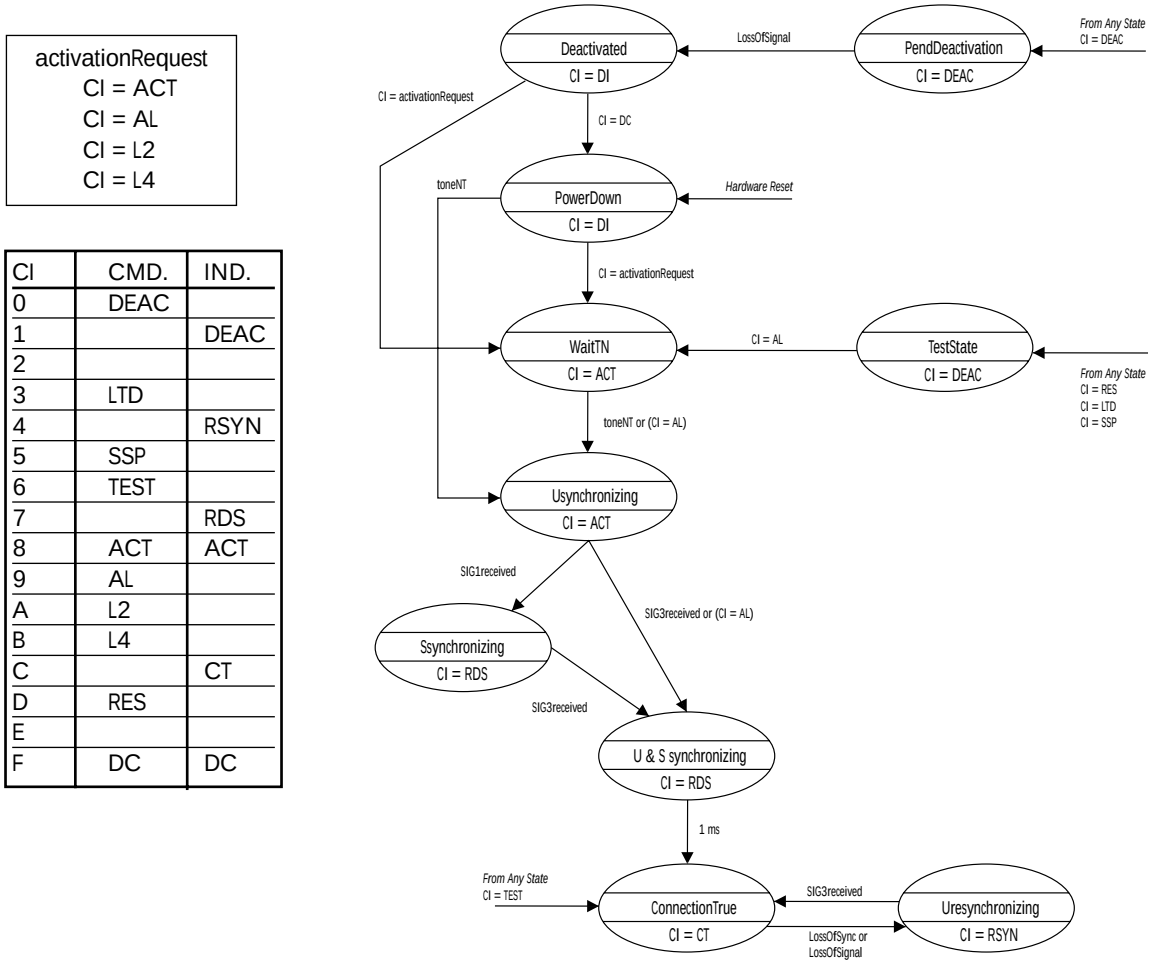


Fig.25: MTC-20278 State Machine



CI	CMD.	IND.
0	DEAC	
1		DEAC
2		
3	LTD	
4		RSYN
5	SSP	
6	TEST	
7		RDS
8	ACT	ACT
9	AL	
A	L2	
B	L4	
C		CT
D	RES	
E		
F	DC	DC

Fig.26: MTC-20279 State Machine

Command and Indicate (C/I) Channel (A bits), MTC-20279

Command (DIN)

Activate	ACT 1000	ACT is indicated. The ILTT is set in power-up state, executing the complete activation of layer 1: the wake-up procedure is executed by transmission of INFO U2W. After successful wake-up process, the synchronization procedure is started by transmission of INFO U2 (in case of LT). When the receiver has been synchronized RDS is indicated. When INFO U3 is recognized, INFO U4H is transmitted. Then the transparent channels are connected through from module to line interface (transparent).
Analog Loop U4H	AL 1001	ACT is indicated. The analog transmitter output is looped back to the receiver input (channels B+B+D), which is disconnected from UK0 interface. The ILTT is set in power-up state, executing the activation of layer 1: A pseudo wake-up procedure is executed. After successful wake-up procedure the transmitter generates INFO U2. When synchronization is completed successfully, RDS is indicated. INFO is transmitted. The UIC is connected through from module interface to line interface transparent).
Loop 2	L2 1010	ACT is indicated.Command to close loop 2 in the NT.As ACT, with the difference that continuous positive polarity is transmitted in the M symbol at UK0. NOTE: An L2 command can be applied in the deactivated state as well as in the activated state.
Loop 4	L4 1011	ACT is indicated.Command to close loop 4 in the RPTR. As ACT with the difference that continuous +/0 code is transmitted in the M symbol at UK0.
Deactivate	DEAC 0000	Request to deactivate UK0. The transmitter outputs INFO U0. After detecting the disappearance of an incoming signal at UK0 the indication DC is transmitted at module interface. A wake-up signal will be disregarded.
Deactivate Confirmation	DC 1111	No signal is transmitted at UK0 and the ILTT is powered down. The wake-up detect circuitry remains enabled: thus a detected wake-up signal INFO U1W is able to power-up the UIC and to initiate the activation procedure, as in case of control ACT applied. NOTE: This command can be used to deactivate UK0 in case that after the command DEAC the disappearance of an incoming signal is not detected and there is no indica tion DC.
Reset	RES 1101	Reset of ILTT to initial state.
Send SinglePulses	SSP 0101	The ILTT transmits single pulses at 1ms time intervals with alternate polarity.
Test	TEST 0110	The ILTT will be connected through from module interface to line interface (transparent) without wake-up procedure.
Line Termination Disable	LTD 0011	The ILTT stops transmitting signals on the corresponding channel, ignoring awake signals. The channel stays in this state until a command RES, DEAC or DC is issued. It then goes in power-down. Note that if RES or DEAC are used, they have to be followed by DC.

Indication (DOUT)

Activate	ACT 1000	(1) The signal INFO U1W has been recognized by the wake-up detect circuitry.The ILTT is powered up and the activation procedure will be executed. (2) The control ACT is acknowledged by ACT. The controls L2, L4, AL are also ackn. by ACT (not included in FTZ 1 R 210).
Running Digital Sum	RDS 0111	During activation procedure, the receiver has synchronized (on INFO U1/U3/U5). Evaluation of transmission quality is enabled.
Connection Through loop	CT 1100	The transparent channels are connected through from module to line interface (transparent). The activation of Layer 1 up to the terminals is completed. In case of a 4 the activation up to the loop is completed. In case of loop 2 the activation up to the NT is completed.
Deactivate	DEAC 0001	The ILTT is deactivating. Data transmission is impossible.A wake-up signal at UK0 will be disregarded.The ILTT transmits either INFO U0 or single pulses (when the command SSP or TSP is applied).
Deactivate Confirmation	DC 1111	After deactivation of UK0 (by the command DEAC) the disappear ance of in incoming signal (INFO U0) has been detected.
Resynchronization	RSYN 0100	The receiver has lost framing and is attempting to resynchronize. The ILTT remains connected through from module to line interface (transparent).

List of codes:
Evaluation of any command is done according to a double last look criterion: any command is followed only after the same command has been detected in two successive frames. Until then the preceding command is considered valid.

In case commands are received that are not included in the list the last recognized command is considered valid. Commands which are logically impossible to receive in the correct state are ignored (cfr ETR 80).

The indications are transmitted continuously in each frame.

Under no circumstances an indication that is not included in the list is transmitted.

Code A-bits						
1	2	3	4	HEX	DIN	DOUT
0	0	0	0	0	DEAC	
0	0	0	1	1		DEAC
0	0	1	0	2		
0	0	1	1	3	LTD	
0	1	0	0	4		RSYN
0	1	0	1	5	SSP	
0	1	1	0	6	TEST	
0	1	1	1	7		RDS
1	0	0	0	8	ACT	ACT
1	0	0	1	9	AL	ARMB
1	0	1	0	A	L2	
1	0	1	1	B	L4	
1	1	0	0	C		CT
1	1	0	1	D	RES	
1	1	1	0	E		
1	1	1	1	F	DC	DC

DEAC = Deactivate
LTD = Line Termination Deactivate
RSYN = Resynchronization
SSP = Send Single Pulses
TEST = Test
ACT = Activate
AL = Analog Loop
L2 = Loop 2
L4 = Loop 4 Deactivate
CT = Connection Through
DC = Deactivate Confirmation

Master clock

The master clock of 15.36 MHz is derived by PLL from the 4096 MHz GCI clock. It is only available to the internal circuits.

Boundry Scan

The JTAG State Machine

Production test of the device IO pins is performed using the JTAG state machine implemented in the on-chip ARM. The test controller state transitions are shown in the following Figure 27.

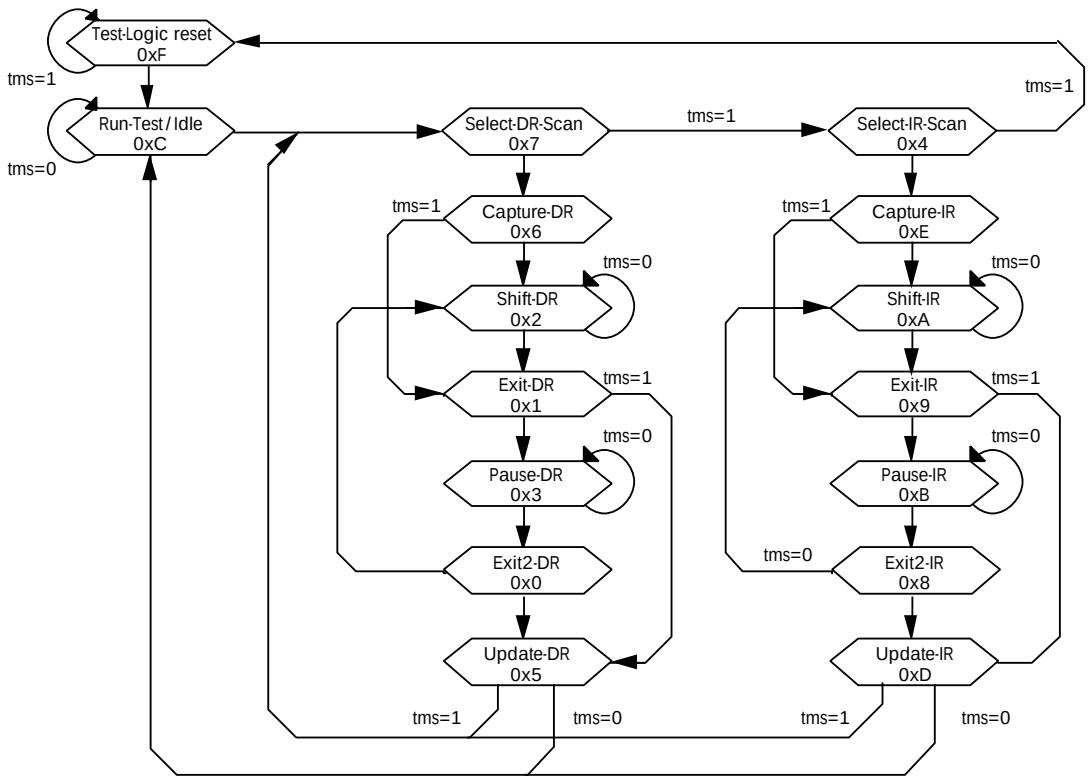


Fig.27: JTAG State Machine

Reset

The boundary scan interface includes a state-machine controller (TAP controller) according to the IEEE standard. In order to force the TAP controller into the correct state after power-up of the device, a reset pulse must be applied to the TRST signal. If the boundary scan interface is to be used, TRST must be driven LOW, and then HIGH again. If the boundary scan is not to be used, the TRST input pin should be tied permanently low. A clock on TCK is not necessary to reset the device.

Instruction Register

The instruction register is 4 bits in length.
There is no parity bit. The fixed value loaded into the instruction register during the CAPTURE-IR controller state is 0001.

Public Instructions

The following public instructions are supported

Instruction	Binary code
EXTEST	0000
SCAN_N	0010
SAMPLE/PRELOAD	0011
INTEST	1100
BYPASS	1111

Codes not listed in the table should be considered reserved and must not be used during boundary scan testing.
In the descriptions that follow, TDI and TMS are sampled on the rising edge of TCK and all output transitions on TDO occur as a result of the falling edge of TCK

EXTEST (0000)
The scan chain is placed in test mode by the EXTEST instruction. The EXTEST instruction connects the scan chain between TDI and TDO.
In the CAPTURE-DR state, inputs from the system logic and outputs from the output scan cells to the system are captured by the scan cells. In the SHIFT-DR state, the previously captured test data is shifted out of the scan chain via the TDO pin, while new test data is shifted in via the TDI input. This data is applied immediately to the system logic and system pins.

SAMPLE/PRELOAD (0011)
The scan chain is placed in test mode by the SAMPLE/PRELOAD instruction. This instruction connects the scan chain between TDI and TDO.
In the CAPTURE-DR state, inputs from the system logic and outputs from the output scan cells to the system are captured by the scan cells. In the SHIFT-DR state, the previously captured test data is shifted out of the scan chain via the TDO pin. The capture of the pins levels can be done in normal operation.

INTEST (1100)
The scan chain is placed in test mode by the INTEST instruction. This instruction connects the scan chain between TDI and TDO.
In the CAPTURE-DR state, the value of the data applied from the core logic to the output scan cells is captured. At the same time, the value of the data applied from the system logic to the input scan cell is also captured by the scan cells.
In the SHIFT-DR state, the previously captured test data is shifted out of the scan chain via the TDO pin, while new test data is shifted in via the TDI input.

BYPASS (1110)
The BYPASS instruction connects a 1 bit shift register (the BYPASS register) between the TDI pin and the TDO pin. When the BYPASS instruction is loaded into the instruction register, all the scan cells are placed in their normal mode of operation. The instruction has no effect on the system pins.
In the CAPTURE-DR state, a logic 0 is captured by the bypass register. In the SHIFT-DR state, test data is shifted into the bypass register via the TDI pin and out via the TDO pin after a delay of one TCK cycle. Note that the first bit out will be a zero. The bypass register is not affected in the update-DR state.

SCAN_N (0010)
This instruction connects the Scan Path Select Register between TDI and TDO. During the CAPTURE-DR state, the fixed value 1000 is loaded into the register. During the SHIFT-DR state, the ID number of the desired scan path is shifted into the scan path select register. In the UPDATE-DR state, the scan register of the selected scan chain is connected between TDI and TDO, and remains connected until a subsequent SCAN_N instruction is issued. On reset, scan chain 3 is selected by default. The scan path select register is 4 bits long.

Test Data Registers

There are a number of data registers which may be connected between TDI and TDO. They are: Bypass register, Instruction register, Scan chain select register, Scan chain 3 (all others scan chains are reserved). Only the bypass register, instruction register, scan chain select register and scan chain 3 are discussed.

Bypass Register
Purpose: Bypasses the device during scan test by providing a path between TDI and TDO.
Length: 1 bit
Operating mode: when the BYPASS instruction is the current instruction in the instruction register, serial data is transferred from TDI to TDO in shift-DR state with a delay of one TCK clock cycle. There is no parallel output from the bypass register. A logic 0 is loaded from the parallel input of the bypass register in the CAPTURE-DR state.

Instruction Register
Purpose:Changes the current TAP instruction.
Length: 4 bits
Operating mode: when in SHIFT-IR state, the instruction register is selected as the serial path between TDI and TDO. During the CAPTURE-IR state, the values 0001 binary is loaded into this register. This is shifted out during shift-IR (LSB first), while a new instruction is shifted in (LSB first). During the UPDATE-IR state, the value in the instruction register becomes the current instruction. On reset, IDCODE (reserved) becomes the current instruction.

Scan Chain Select Register
Purpose: changes the currently active scan chain.
Length: 4 bits
Operating mode: The external boundary scan is selected by default at reset. It is not allowed to select other registers for boundary scan testing. The external boundary scan corresponds to the scan chain number 3.

External Boundary Scan Register
Purpose: boundary scan testing
Length: 25 bits
Operation: following digital component pins are scanned and tested in boundary scan mode
The relation betweeen the scanned pins and the scan register sequence is described in the following table (all digital pins are included in the boundary scan except for TDI, TDO,TMS, TCK, FD21, FD31)

Pin	Direction	INTEST		EXTEST	
		TDI	TDO	TDI	TDO
RD11	out		x	x	
RD43	inout	x	x	x	x
RD41	out		x	x	
RD42	out		x	x	
FD41	in	x			x
FD42	inout	x	x	x	x
FD32	inout	x	x	x	x
RD33	inout	x	x	x	x
RD32	out		x	x	
RD31	out		x	x	
POS	in	x			x
DFR	in	x			x
DIN	in	x			x

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Pin	Direction	INTEST		EXTEST	
		TDI	TDO	TDI	TDO
DCLK	in	x			x
DOUT	out		x	x	
TSP	in	x			x
NRESET	in	x			x
RD23	inout	x	x	x	x
RD21	out		x	x	
RD22	out		x	x	
FD22	out		x	x	
RD13	inout	x	x	x	x
FD12	inout	x	x	x	x
FD11	in	x			x
RD12	out		x	x	

Data entered at TDI will shift from position RD11 to RD12. Total delay between TDI and TDO is 26 clocks of TCK.
The positions marked 'x' in the table should be interpreted as follows:

INTEST: data shifted in through TDI will be presented to the internal chip inputs
data from the internal chip outputs will be shifted to TDO
EXTEST: data shifted in through TDI will be presented to the external chip pins
data from the external chip pins will be shifted to TDO

Electrical Characteristics and Ratings

Symbol	Parameter	Conditions	Min	Max	Unit
VIH	High Level Input Voltage		80% of VDD		V
VIL	Low Level Input Voltage			20% of VDD	V
VIH NRESET	Rising NRESET		1.7	1.9	V
VIL NRESET	Falling NRESET		0.9	1.1	V
VOH	High Level Output Voltage		85% of VDD		V
VOL	Low Level Output Voltage			0.4	V
CIN	Input Capacitance, all inputs			1	pF
COUT	Load Capacitance, all outputs			100	pF

The NRESET input is a Schmitt Trigger input.

Absolute Maximum Ratings, Operating Ranges and Storage Conditions

Absolute Maximum Ratings

Stresses above those listed in this clause can cause permanent device failure. Exposure to absolute maximum ratings for extended periods can effect device reliability.

Symbol	Description	Min	Max	Unit
DVDD, AVDD	power supply voltage	VSS - 0.3	3.63	V
VIN	input voltage on any pin	VSS - 0.3	VDD + 0.3 AND < 3.63	V

Operating Ranges

Operating ranges define the limits for functional operation and schematic characteristics of the device as described above, and for the reliability specifications as listed. Functionality outside these limits is not implied.

Total cumulative dwell time outside the normal power supplyVoltage range or the ambient temperature under bias must be less than 0.1% of the useful life as defined in the reliability section.

Symbol	Description	Min	Max	Unit
DVDD, AVDD	power supply	3.135	3.465	V
PTOT	total power consumption		250 (1)	mW/line
PPD	power down power consumption		16 (2)	mW/line
Tamb	ambient temperature - I version	-40	85	°C
Tamb	ambient temperature - C version	0	70	°C
SNAVDD	analog supply noise		30	mVPP
SNDVDD	digital supply noise		100	mVPP

(1) U nominally loaded (U: 135Ω line equivalent) for random signal.

(2) Transition from power-up to power-down automatically follows when transmission on U is terminated. Transition to power-up state occurs when a wakeup signal is received from U or when activity is detected on the data input of the GCI interface.

AC Characteristics

GCI Pins
Timing for: DCLK, DFR, DIN, DOUT

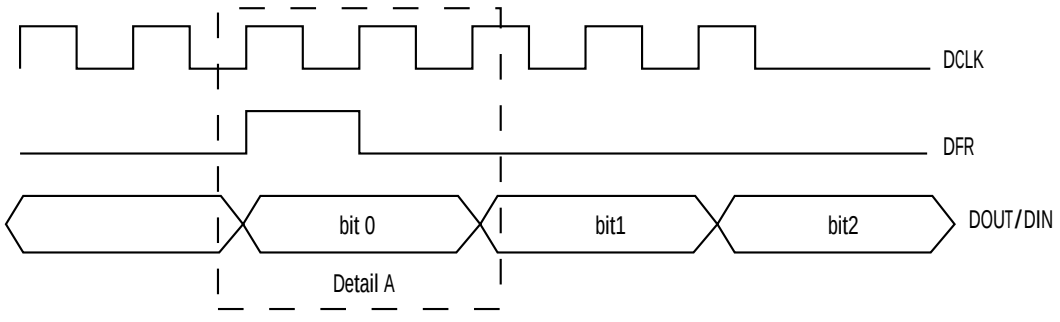


Fig.28: Timing for: DCLK, DFR, DIN, DOUT

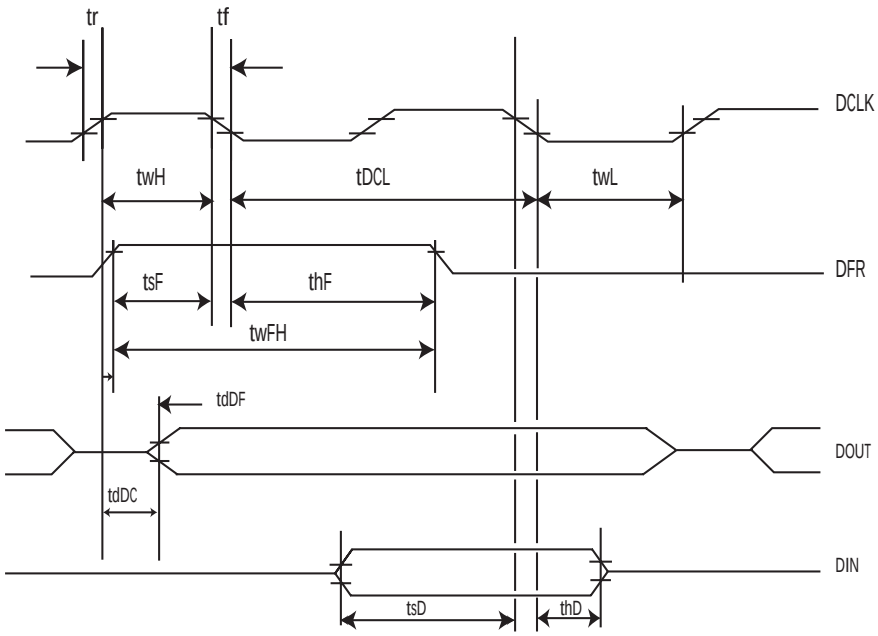


Fig.29: Timing for: DCLK, DFR, DIN, DOUT

Timing ReferenceVoltages

Voltage	High	Low
Output	2.4V	0.4V
Input	2.0V	0.8V

Parameter	Signal	Mnem.	Units	Min	Max
Clock Period	DCLK	tDCL	ns	239	249
Pulse width (2048 kbps)	DCLK	twL, twH	ns	90	-
Frame	DFR	tsF	ns	70	tDCL-50
Frame Rise/Fall	DFR	tr, tf	ns		60
Frame Width H	DFR	twFH	ns	130	-
Frame Width L	DFR	twFL	ns	tDCL	-
Frame Hold	DFR	thF	ns	50	-
Data delay, Clock	DOUT	tdDC	ns	-	100 (1)
Data delay, Frame	DOUT	tdDF	ns	-	150 (1)
Data setup	DIN	tsD	ns	twH + 20	-
Data Hold	DIN	thD	ns	50	-

Note 1: Cload = 150pF.

Timing for JTAG, PINS: TCK, TMS, TDI, TDO (TRST asynchronous).

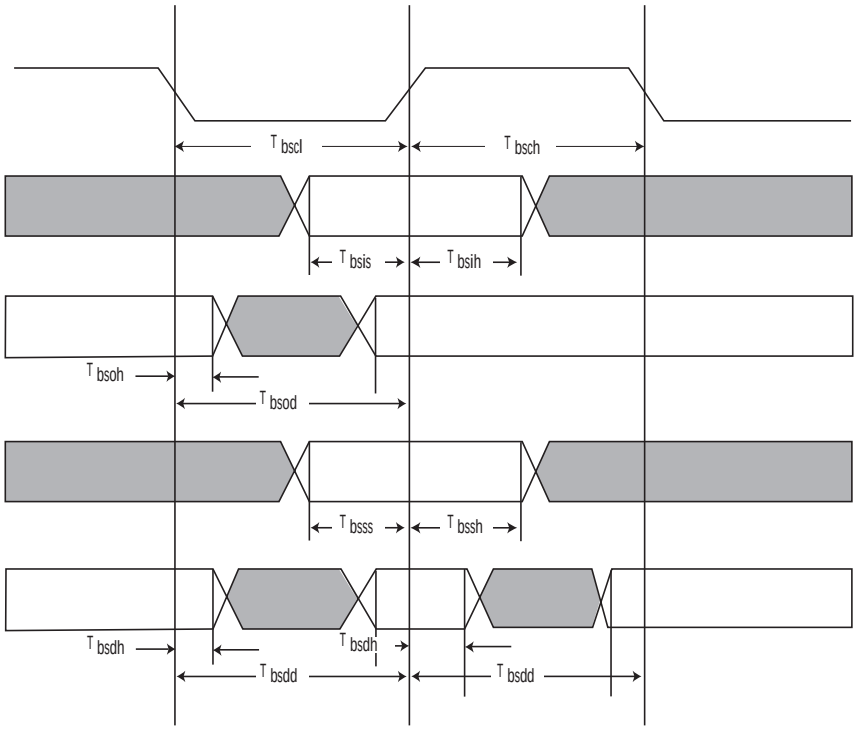


Fig.30: Timing for JTAG, PINS: TCK, TMS, TDI, TDO (TRST asynchronous)

Symbol	Parameter (Time inns)	Min	Typ	Max	Notes
Tbscl	TCK low period	15.1			
Tbsch	TCK high period	15.1			
Tbsis	TDI, TMS setup to [TCr]	3.6			
Tbsih	TDI, TMS hold from [TCr]	7.6			
Tbsoh	TDO hold time	2.4			
Tbsod	TCr to TDOValid			16.4	
Tbsss	I/O signal setup to [TCr]	3.6			
Tbssh	I/O signal hold from [TCr]	7.6			
Tbsdh	data output hold time	2.4			
Tbsdd	TCf to data outputValid			17.1	
Tbsr	Reset period	25			

Operating Environment

The components are intended for application in equipment for indoor operation without forced cooling air flow, only convection.

Storage Conditions

Temperature should be in the range -55 to 110°C.
In case of IC deliveries in dry bag, the conditions of time and humidity during storage are specified in Alcatel specification16650.
In case of IC deliveries not in dry bag, the conditions for a maximum storage period of 2 years are as follows:

Ambient Temperature (°C)	Relative Humidity (%)
20	80
30	70
40	60
50	50

Quality

Product Accaptance Tests

All products are tested 100%, at ambient temperature with full temperature range guardband, by means of production test programs that guarantee optimal coverage of the product specification.

Lot-by-lot Acceptance Test

Lot conformance to specification of products delivered in Volume production is guaranteed by means of following tests:

Test	Conditions	AQL Level	Inspection Level
Electrical, functional and parametric	To product specification at Tamb = 25°C with full temperature range performance guardband.	0.04	II
ExternalVisual	Physical damage to body or leads. Dimensions affecting PCB manufacturability such as bent leads, coplanarity, ...	0.04	II
ExternalVisual	Correctness of marking	0.65	II

Delivery lot certification

Each delivery lot is accompanied by a Certificate of Conformance.

Quality system

A quality system with certification against ISO9001 is maintained.

Reliability Specification

In order to guarantee the specified reliability, a product qualification for each product is performed. This qualification is described in the Alcatel Microelectronics specification document 15503.
In order to minimize reliability testing, structural similarity is applied. Methods and criteria are defined in the documents 15501 (assembly) and 15502 (wafer fabrication).
Monitoring of assembly and wafer fabrication is performed according to the specifications 15910 and 15205. These monitoring tests include the solderability tests.

The Intrinsic Failure Rate

When operating the component under benign conditions, the intrinsic failure rate will not exceed:

- 5000 ppm during the early failure period defined below

- the long term failure rate as specified below after the early failure period

Failures due to external overstresses such as ESD,Voltage and current overstress (e.g. due to EMI), excessive mechanical and thermal shocks, ... are not included in these Figures (see next paragraph).

Tjunction (°C)	Early failure period (Hrs)	Long term failure rate (FIT)
55	8760	100
65	4000	200
75	2000	400
85	1000	800
90	800	1000

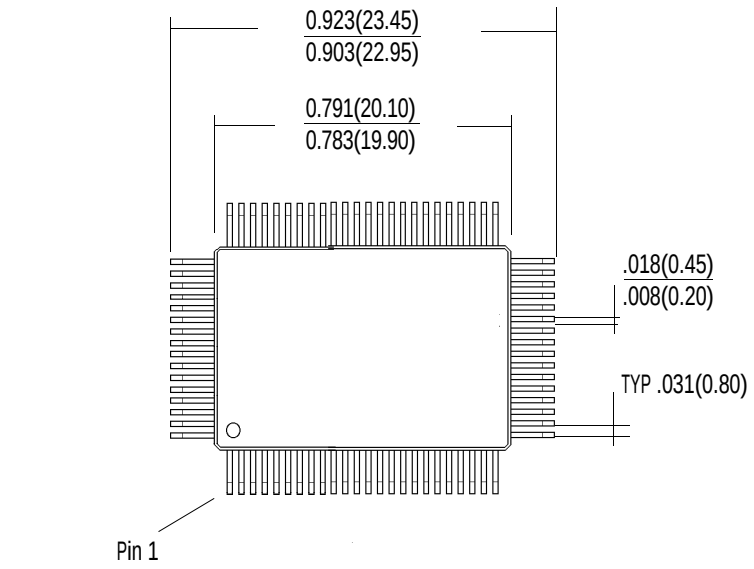
External Stress Immunity

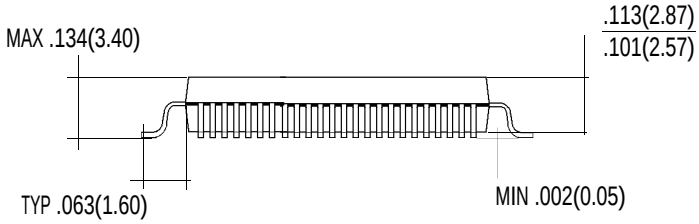
Electrostatic discharges:
The device withstands 1000Volts Standardized Human Body Modle ESD pulses when tested according to MIL883C method 3015.5 (pin combination 2).

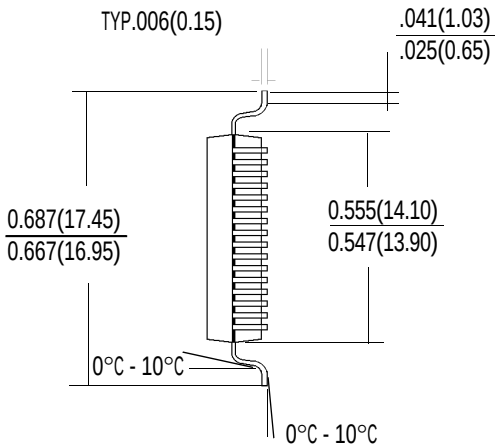
Latch-up:
Static latch-up protection level is 100 mA at 25°C when tested according to JEDEC no. 17.

The Useful Life

The useful life, when used under moderate conditions, is at least 25 years. The term useful life is specified as the point in the lifetime where the intrinsic failure rate exceeds the long term failure rate specified above.







All dimensions are in inches and parenthetically in millimeters.
Inches dimensions are approximated.

Fig.31: 80 PQFP Package Drawing

MTC-20278/9 ILTQ/ILTT

Notes

MTC-20278/9 ILTQ/ILTT

Notes

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