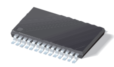


DUAL-OUTPUT LOW-DROPOUT VOLTAGE REGULATORS

FEATURES

- **Dual Output Voltages for Split-Supply Applications**
- **Output Current Range of 0mA to 1.0A per Regulator**
- **3.3V/2.5V, 3.3V/1.8V, and 3.3V/Adjustable Output**
- **Fast-Transient Response**
- **2% Tolerance Over Load and Temperature**
- **Dropout Voltage Typically 350mV at 1A**
- **Ultra-low 85μA Typical Quiescent Current**
- **1μA Quiescent Current During Shutdown**
- **Dual Open-Drain Power-On Reset with 200ms Delay for Each Regulator**
- **28-Pin PowerPAD™ TSSOP Package**
- **Thermal Shutdown Protection for Each Regulator**

DESCRIPTION

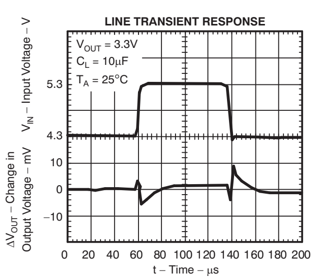
The TPS767D3xx family of dual voltage regulators offers fast transient response, low dropout voltages and dual outputs in a compact package and incorporating stability with 10μF low ESR output capacitors.

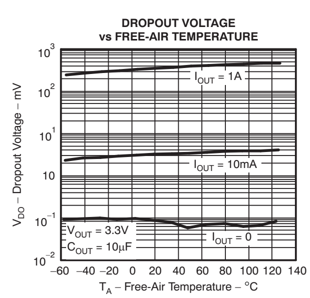
The TPS767D3xx family of dual voltage regulators is designed primarily for DSP applications. These devices can be used in any mixed-output voltage application, with each regulator supporting up to 1A. Dual active-low reset signals allow resetting of core-logic and I/O separately.

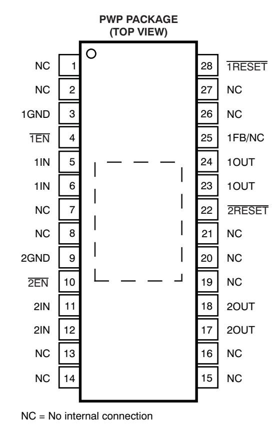
Because the PMOS device behaves as a low-value resistor, the dropout voltage is very low (350mV typically at an output current of 1A for the TPS767D325) and is directly proportional to the output current. Additionally, since the PMOS pass element is a voltage-driven device, the quiescent current is very low and independent of output loading (typically 85μA over the full range of output current, 0mA to 1A). These two key specifications yield a significant improvement in operating life for battery-powered systems. This LDO family also features a sleep mode; applying a TTL high signal to $\overline{EN}$ (enable) shuts down the regulator, reducing the quiescent current to 1μA at T_J = +25°C.

The $\overline{RESET}$ output of the TPS767D3xx initiates a reset in microcomputer and microprocessor systems in the event of an undervoltage condition. An internal comparator in the TPS767D3xx monitors the output voltage of the regulator to detect an undervoltage condition on the regulated output voltage.

The TPS767D3xx is offered in 1.8V, 2.5V, and 3.3V fixed-voltage versions and in an adjustable version (programmable over the range of 1.5V to 5.5V). Output voltage tolerance is specified as a maximum of 2% over line, load, and temperature ranges. The TPS767D3xx family is available in a 28-pin PWP TSSOP package. They operate over a junction temperature range of –40°C to +125°C.







This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

AVAILABLE OPTIONS(1)

DEVICE	REGULATOR 1 V_{OUT} (V)	REGULATOR 2 V_{OUT} (V)
TPS767D301	Adjustable (1.5V – 5.5V)	3.3V
TPS767D318	1.8V	3.3V
TPS767D325	2.5V	3.3V

(1) For the most current specifications and package information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating temperature range (unless otherwise noted).

	TPS767D3xx	UNIT
Input voltage range, V_{1IN}, V_{2IN} (2)	–0.3 to +13.5	V
Enable voltage range, $V_{\overline{1EN}}$, $V_{\overline{2EN}}$	–0.3 to V_{IN} + 0.3	V
Output voltage range, V_{1OUT}, V_{2OUT}	–0.3 to +7.0	V
$\overline{\text{RESET}}$ voltage range, $V_{\overline{1RESET}}$, $V_{\overline{2RESET}}$	–0.3 to +16.5	V
Peak output current	Internally limited	
ESD rating, HBM	2	kV
Continuous total power dissipation	See Dissipation Ratings table	
Operating junction temperature range, T_J	–40 to +125	°C
Storage temperature range, T_{stg}	–65 to +150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network terminal ground.

POWER DISSIPATION RATINGS

PACKAGE	AIR FLOW (CFM)	$T_A \le$ +25°C POWER RATING	DERATING FACTOR ABOVE t_a = +25°C	T_A = +70°C POWER RATING	T_A = +85°C POWER RATING
PWP(1)	0	3.58 W	35.8 mW/°C	1.97 W	1.43 W
	250	5.07 W	50.7 mW/°C	2.79 W	2.03 W

(1) This parameter is measured with the recommended copper heat sink pattern on a 4-layer PCB, 1oz. copper on 4-in × 4-in ground layer. For more information, refer to TI technical brief literature number SLMA002.

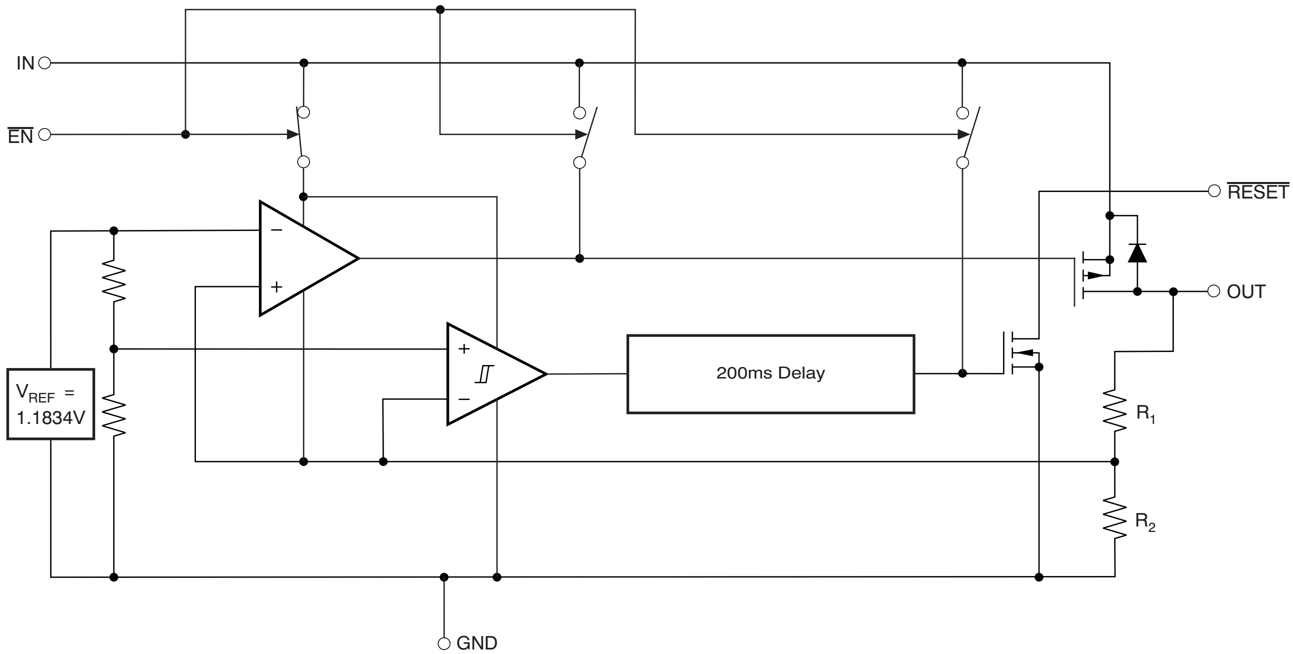
ELECTRICAL CHARACTERISTICS

Over operating temperature range (T_J = –40°C to +125°C), $V_{IN} = V_{OUT(nom)}$ + 1V, I_{OUT} = 1mA, $V_{\overline{EN}}$ = 0V, and C_{OUT} = 10µF, unless otherwise noted. Adjustable channels are set to V_{OUT} = 3.3V. Typical values are at T_J = 25°C.

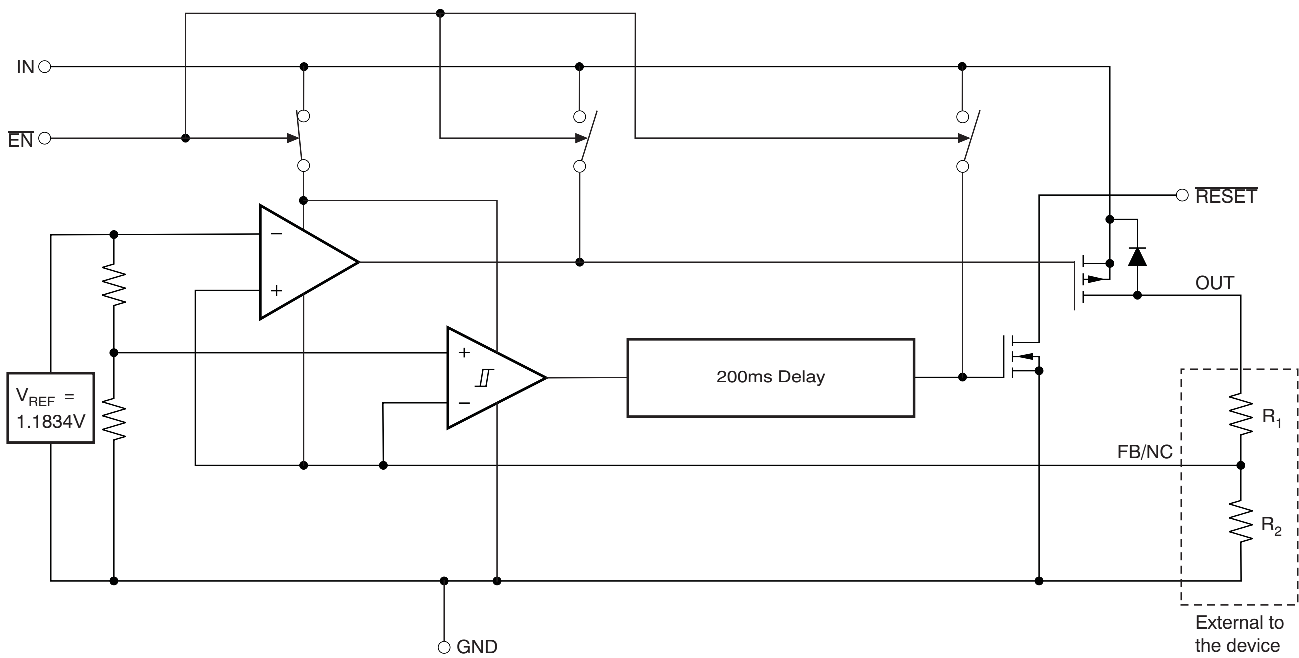
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range, V_{1IN}, V_{2IN} (1)		2.7		10	V
V_{OUT}	Adjustable V_{OUT} range, V_{1OUT}, V_{2OUT}		1.5		5.5	V
	Accuracy, adjustable V_{OUT} channels (1)	V_{OUT} + 1V ≤ V_{IN} ≤ 5.5V; 10 µA ≤ I_{OUT} ≤ 1A	–2.0		+2.0	%
	Accuracy, fixed V_{OUT} channels (1)	V_{OUT} + 1V ≤ V_{IN} ≤ 10V; 10 µA ≤ I_{OUT} ≤ 1A	–2.0		+2.0	%
$\Delta V_{OUT}\%/\Delta V_{IN}$	Line regulation (1)	V_{OUT} + 1.0V ≤ V_{IN} ≤ 10V		0.01		%/V
$\Delta V_{OUT}\%/\Delta I_{OUT}$	Load regulation	10 µA ≤ I_{OUT} ≤ 1A		3		mV
V_{DO}	Dropout voltage (2) ($V_{IN} = V_{OUT}$ (nom) – 0.1V)	V_{OUT} = 3.3V, I_{OUT} = 1A		350	575	mV
I_{CL}	Output current limit, per LDO	V_{OUT} = 0V, T_J = +25°C		1.7	2	A
I_{GND}	Ground pin current, per LDO	10µA ≤ I_{OUT} ≤ 1A		85	125	µA
I_{SHDN}	Standby current, per LDO	2.7V ≤ V_{IN} ≤ 10V, $V_{\overline{EN}} = V_{IN}$		1	10	µA
I_{FB}	FB current input (Adjustable)	V_{FB} = 1.5V		2		nA
PSRR	Power-supply ripple rejection	f = 1kHz, C_{OUT} = 10µF		60		dB
V_N	Output noise voltage	BW = 200Hz to 100kHz, V_{OUT} = 1.8V, I_C = 1A, C_{OUT} = 10µF		55		μV_{RMS}
$V_{EN(HI)}$	High-level enable input voltage	T_J = +25°C	2.0			V
$V_{EN(LO)}$	Low-level enable input voltage	T_J = +25°C			0.8	V
$I_{\overline{EN}}$	Input current	$V_{\overline{EN}}$ = 0V, T_J = +25°C	–1	0	1	µA
		$V_{\overline{EN}} = V_{IN}$, T_J = +25°C	–1		1	
Reset	Minimum input voltage for valid $\overline{\text{RESET}}$	$I_{OUT(\overline{RESET})}$ = 300µA		1.1		V
	Trip threshold voltage	V_{OUT} decreasing, T_J = +25°C	92		98	$\%V_{OUT}$
	Hysteresis voltage	Measured at V_{OUT}		0.5		$\%V_{OUT}$
	Output low voltage	V_I = 2.7V, T_J = +25°C, $I_{OUT(\overline{RESET})}$= 1mA		0.15	0.4	V
	Leakage current	$V_{(\overline{RESET})}$ = 7V, T_J = +25°C			1	µA
	$\overline{\text{RESET}}$ time-out delay	T_J = +25°C	100	200	400	ms
T_{SD}	Thermal shutdown temperature			150		°C
T_J	Operating junction temperature		–40		+125	°C

(1) Minimum $V_{IN} = V_{OUT} + V_{DO}$ or 2.7V, whichever is greater.
(2) Dropout voltage (V_{DO}) is not measured for channels with $V_{OUT(nom)}$ < 2.8V since minimum V_{IN} = 2.7V.

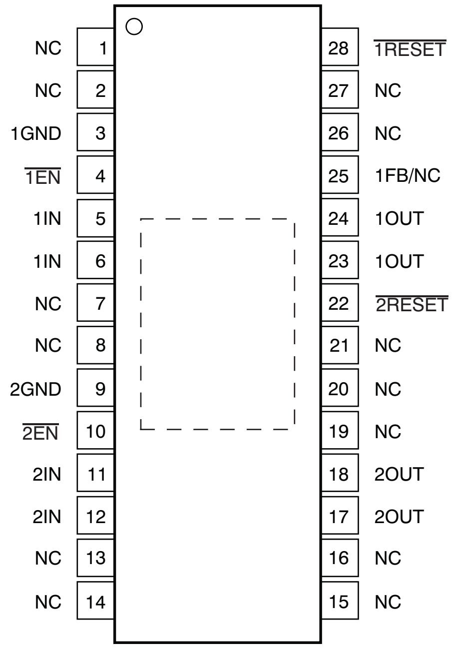
FUNCTIONAL BLOCK DIAGRAM—Fixed Voltage Version (one regulator channel)



FUNCTIONAL BLOCK DIAGRAM—Adjustable Version (one regulator channel)



PWP PACKAGE
(TOP VIEW)



NC = No internal connection

TERMINAL FUNCTIONS

TERMINAL		DESCRIPTION
NAME	**NO.**	
1GND	3	Regulator #1 ground
$\overline{\text{1EN}}$	4	Regulator #1 enable
1IN	5, 6	Regulator #1 input supply voltage
2GND	9	Regulator #2 ground
$\overline{\text{2EN}}$	10	Regulator #2 enable
2IN	11, 12	Regulator #2 input supply voltage
2OUT	17, 18	Regulator #2 output voltage
$\overline{\text{2RESET}}$	22	Regulator #2 reset signal
1OUT	23, 24	Regulator #1 output voltage
1FB/NC	25	Regulator #1 output voltage feedback for adjustable output; no connection for fixed output
$\overline{\text{1RESET}}$	28	Regulator #1 reset signal
NC	1, 2, 7, 8, 13–16, 19, 20, 21, 26, 27	No internal connection

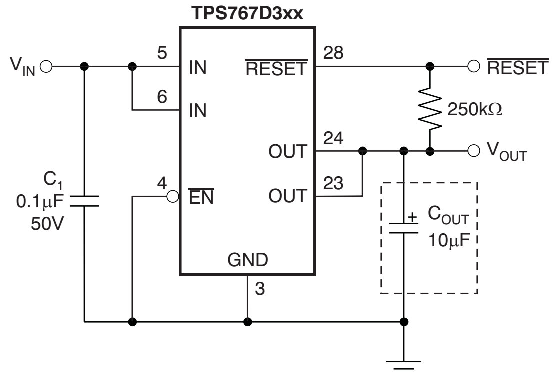
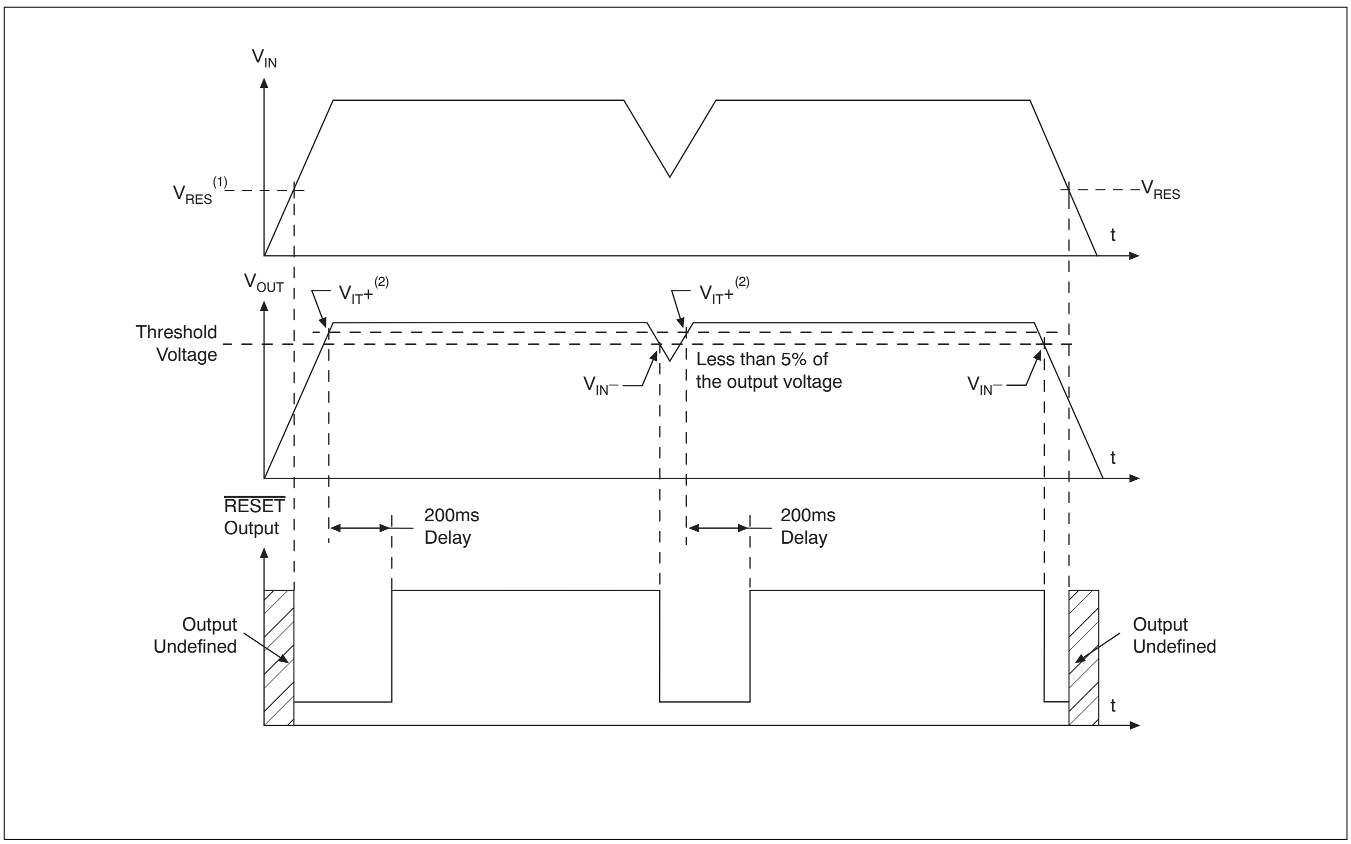


Figure 1. Typical Application Circuit (Fixed Versions) for Single Channel

TIMING DIAGRAM



(1) V_{RES} is the minimum input voltage for a valid $\overline{\text{RESET}}$.

(2) V_{IT} —Trip voltage is typically 5% lower than the output voltage (95% V_{OUT}).

TYPICAL CHARACTERISTICS

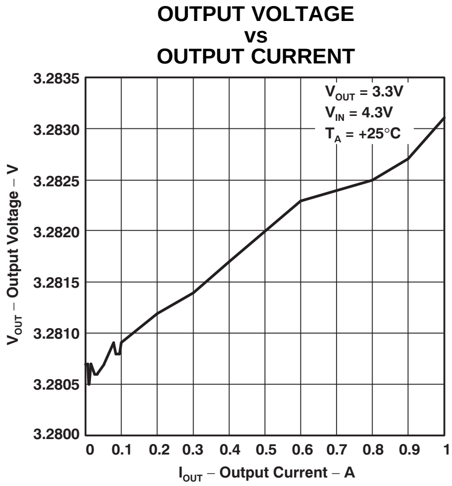


Figure 2.

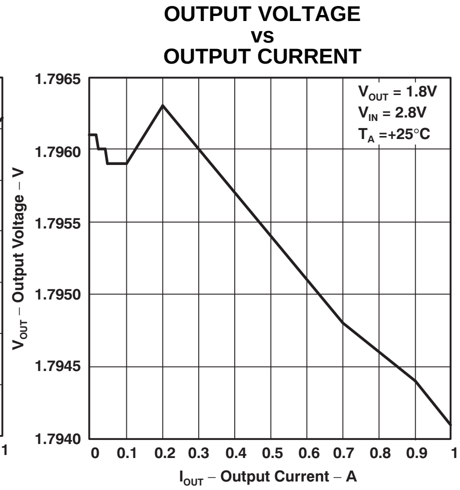


Figure 3.

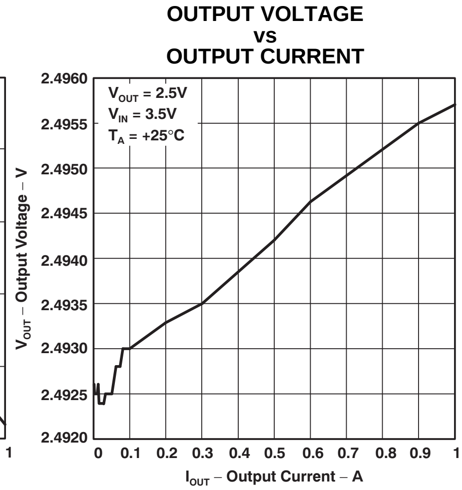


Figure 4.

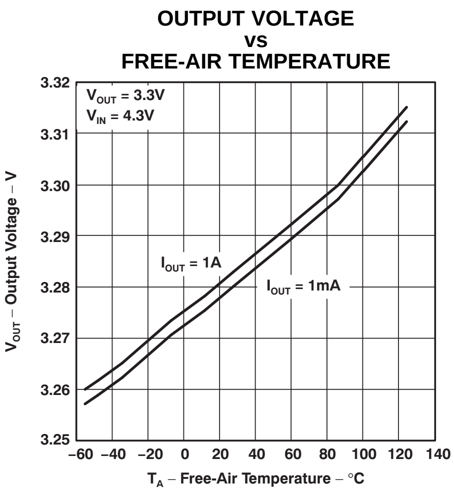


Figure 5.

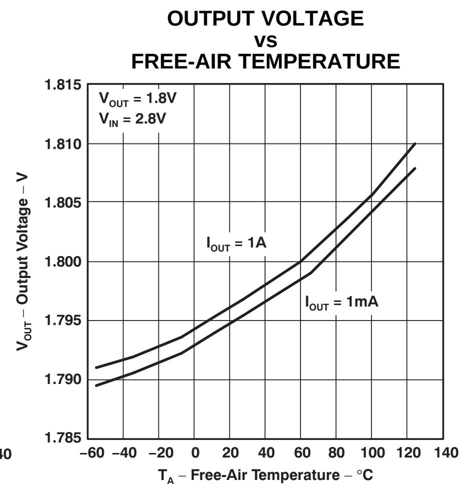


Figure 6.

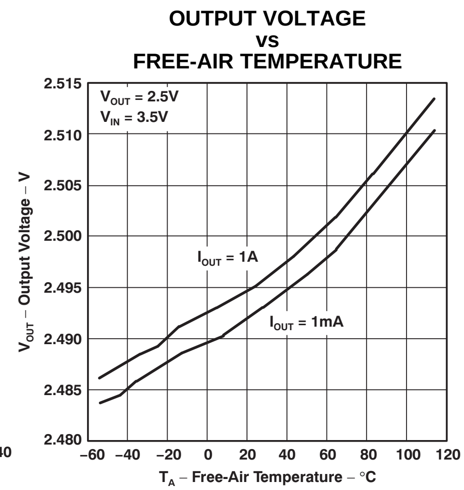


Figure 7.

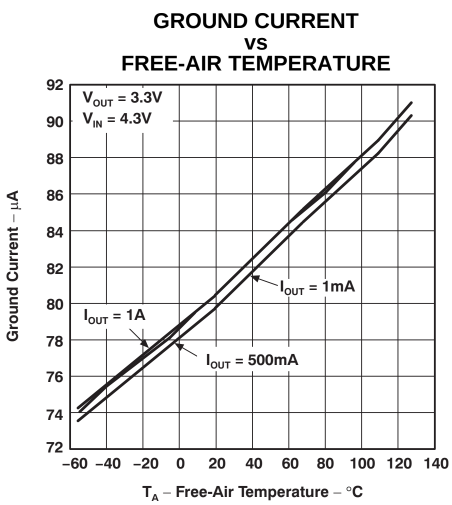


Figure 8.

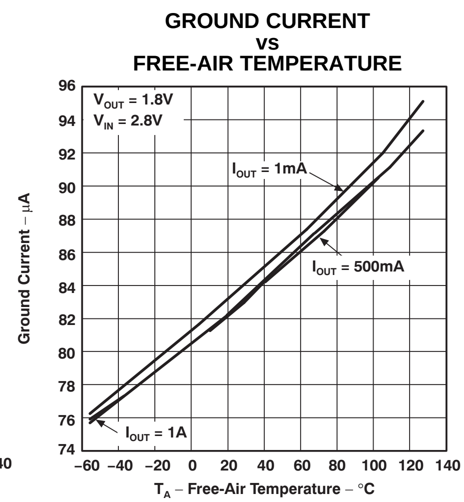


Figure 9.

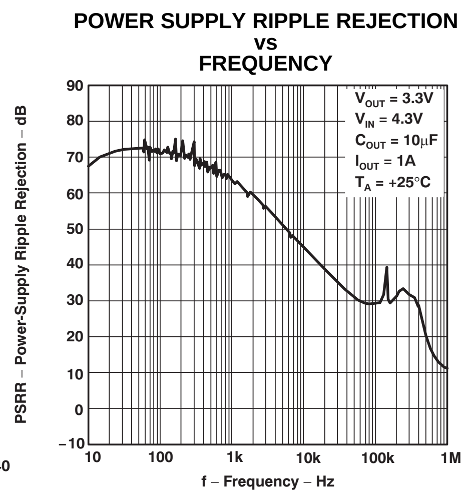


Figure 10.

TYPICAL CHARACTERISTICS (continued)

OUTPUT SPECTRAL NOISE DENSITY vs FREQUENCY

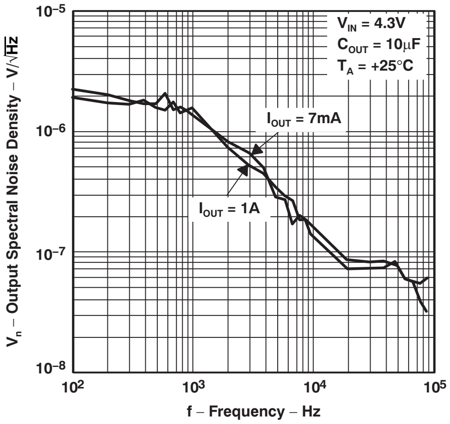


Figure 11.

OUTPUT IMPEDANCE vs FREQUENCY

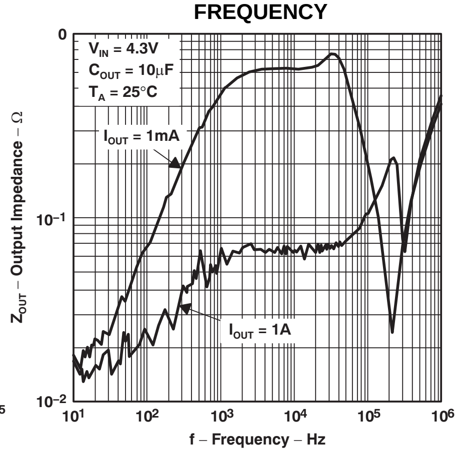


Figure 12.

DROPOUT VOLTAGE vs FREE-AIR TEMPERATURE

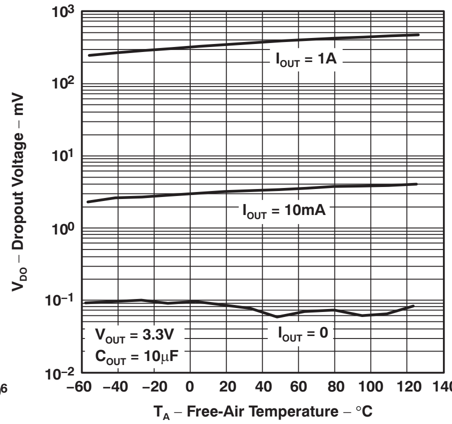


Figure 13.

LINE TRANSIENT RESPONSE

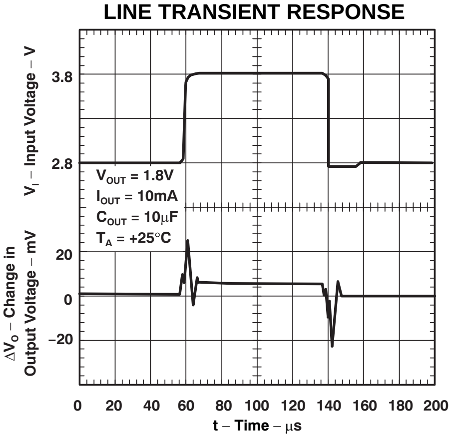


Figure 14.

LOAD TRANSIENT RESPONSE

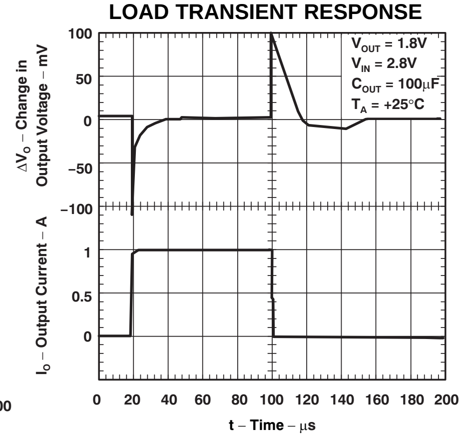


Figure 15.

LINE TRANSIENT RESPONSE

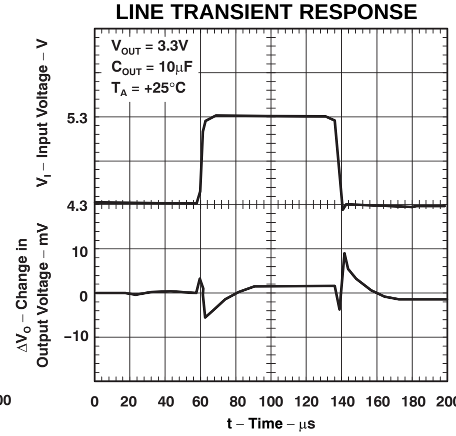


Figure 16.

LOAD TRANSIENT RESPONSE

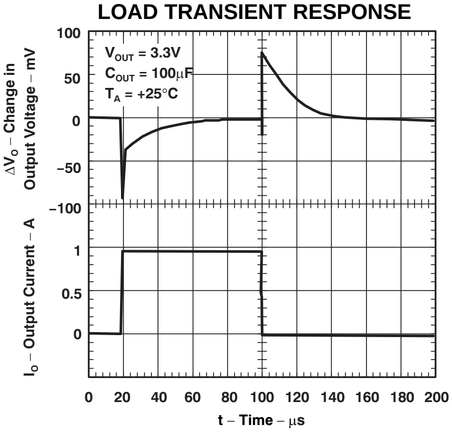


Figure 17.

OUTPUT VOLTAGE vs TIME (AT START-UP)

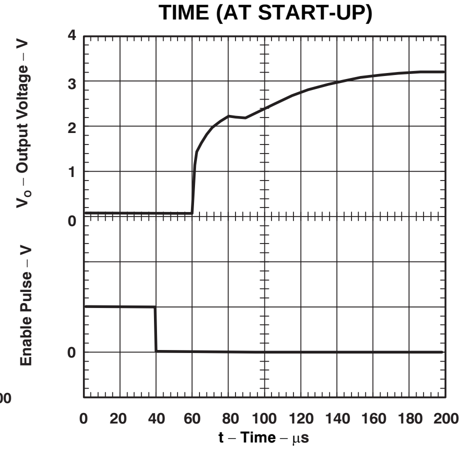


Figure 18.

DROPOUT VOLTAGE vs INPUT VOLTAGE

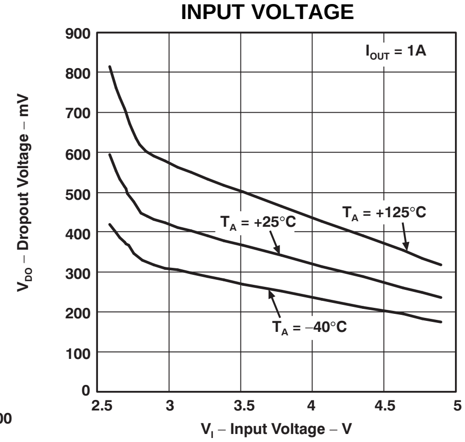


Figure 19.

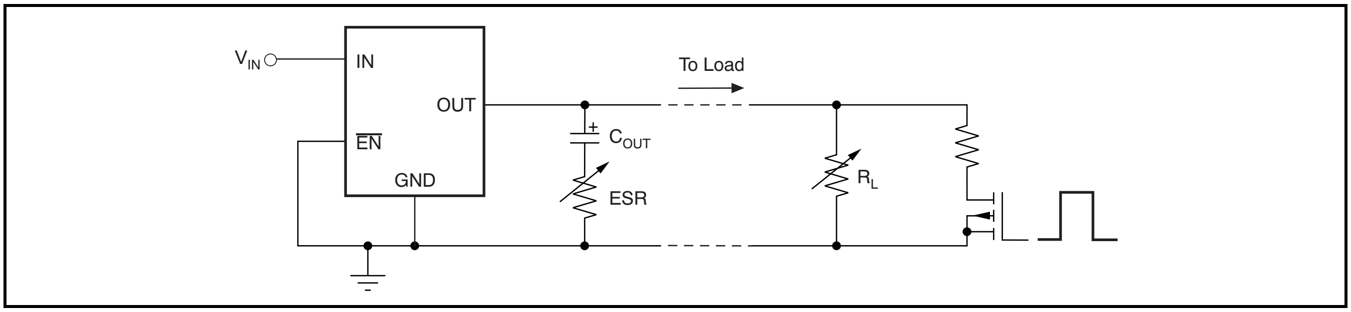


Figure 20. Test Circuit for Typical Regions of Stability (Figure 21 through Figure 24) (Fixed Output Options)

Equivalent series resistance (ESR) refers to the total series resistance, including the ESR of the capacitor, any resistance added externally, and PWB trace resistance to C_{OUT}.

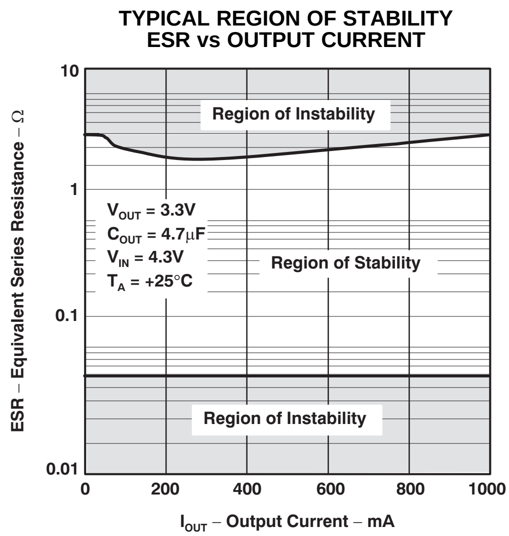


Figure 21.

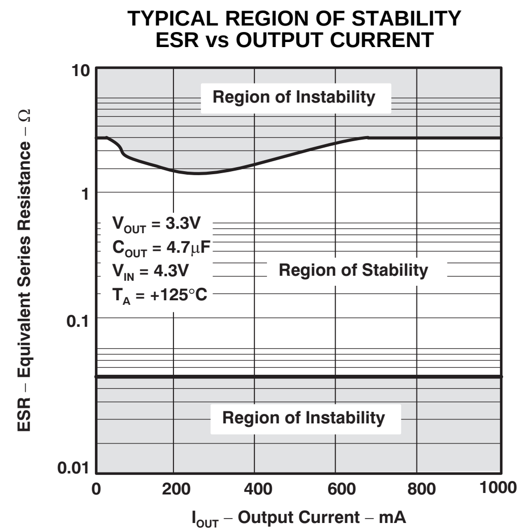


Figure 22.

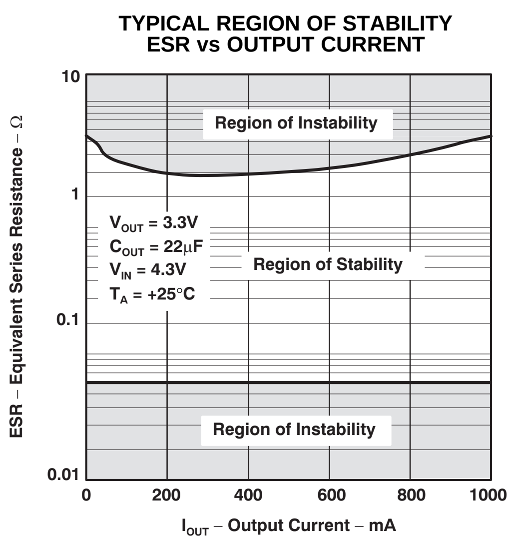


Figure 23.

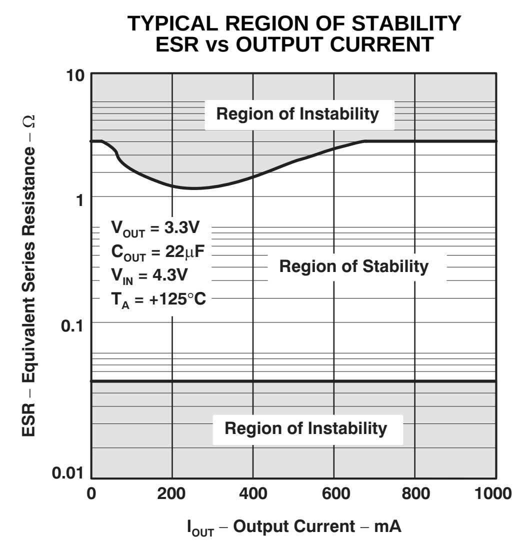


Figure 24.

APPLICATION INFORMATION

The features of the TPS767D3xx family (low-dropout voltage, ultra low quiescent current, power-saving shutdown mode, and a supply-voltage supervisor) and the power-dissipation properties of the TSSOP PowerPAD package have enabled the integration of the dual LDO regulator with high output current for use in DSP and other multiple voltage applications. Figure 25 shows a typical dual-voltage DSP application.

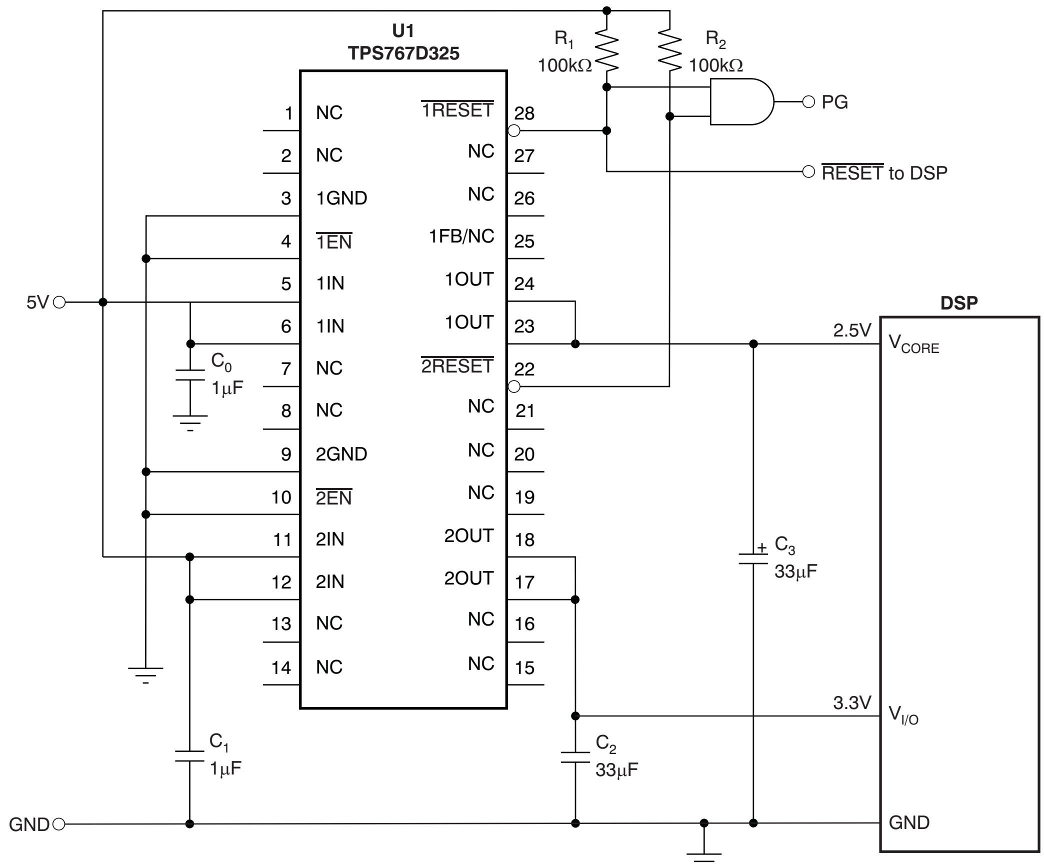


Figure 25. Dual-Voltage DSP Application

DSP power requirements include very high transient currents that must be considered in the initial design. This design uses higher-valued output capacitors to handle the large transient currents.

DEVICE OPERATION

The TPS767D3xx features very low quiescent current, which remain virtually constant even with varying loads. Conventional LDO regulators use a pnp pass element, the base current of which is directly proportional to the load current through the regulator ($I_B = I_C/\beta$). Close examination of the data sheets reveals that these devices are typically specified under near no-load conditions; actual operating currents are much higher as evidenced by typical quiescent current versus load current curves. The TPS767D3xx uses a PMOS transistor to pass current; because the gate of the PMOS is voltage driven, operating current is low and invariable over the full load range. The TPS767D3xx specifications reflect actual performance under load condition.

Another pitfall associated with the pnp pass element is its tendency to saturate when the device goes into dropout. The resulting drop in β forces an increase in I_B to maintain the load. During power-up, this translates to large start-up currents. Systems with limited supply current may fail to start up. In battery-powered systems, it means rapid battery discharge when the voltage decays below the minimum required for regulation. The TPS767D3xx quiescent current remains low even when the regulator drops out, eliminating both problems.

The TPS767D3xx family also features a shutdown mode that places the output in the high-impedance state (essentially equal to the feedback-divider resistance) and reduces quiescent current to under 2μA. If the shutdown feature is not used, $\overline{EN}$ should be tied to ground. Response to an enable transition is quick; regulated output voltage is typically re-established in 120μs.

MINIMUM LOAD REQUIREMENTS

The TPS767D3xx family is stable even at zero load; no minimum load is required for operation.

FB-PIN CONNECTION (ADJUSTABLE VERSION ONLY)

The FB pin is an input pin to sense the output voltage and close the loop for the adjustable option. The output voltage is sensed through a resistor divider network as is shown in Figure 26 to close the loop. Normally, this connection should be as short as possible; however, the connection can be made near a critical circuit to improve performance at that point. Internally, FB connects to a high-impedance, wide-bandwidth amplifier and noise pickup feeds through to the regulator output. Routing the FB connection to minimize/avoid noise pickup is essential. In fixed output options, this pin is not connected.

EXTERNAL CAPACITOR REQUIREMENTS

An input capacitor is not required; however, a ceramic bypass capacitor (0.047pF to 0.1μF) improves load transient response and noise rejection when the TPS767D3xx is located more than a few inches from the power supply. A higher-capacitance electrolytic capacitor may be necessary if large (hundreds of milliamps) load transients with fast rise times are anticipated.

Like all low dropout regulators, the TPS767D3xx requires an output capacitor connected between OUT and GND to stabilize the internal control loop. The minimum recommended capacitance value is 10μF and the ESR (equivalent series resistance) must be between 60mΩ and 1.5Ω. Capacitor values of 10μF or larger are acceptable, provided the ESR is less than 1.5Ω. Solid tantalum electrolytic, aluminum electrolytic, and multilayer ceramic capacitors are all suitable, provided they meet the requirements described previously.

When necessary to achieve low height requirements along with high output current and/or high ceramic load capacitance, several higher ESR capacitors can be used in parallel to meet the previous guidelines.

PROGRAMMING THE TPS767D301 ADJUSTABLE LDO REGULATOR

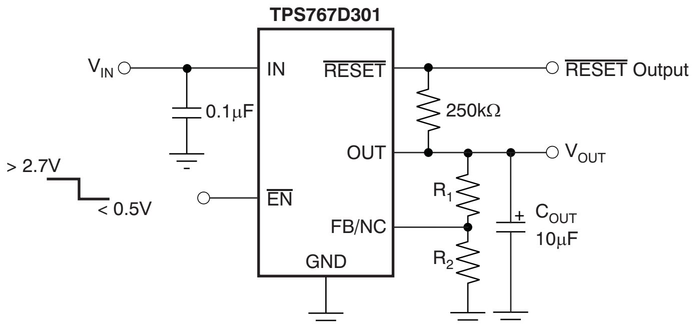
The output voltage of the TPS767D301 adjustable regulator is programmed using an external resistor divider as shown in Figure 26. The output voltage is calculated using:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_1}{R_2}\right) \tag{1}$$

Resistors R_1 and R_2 should be chosen for approximately 40μA divider current. Lower-value resistors can be used but offer no inherent advantage and waste more power. Higher values should be avoided as leakage currents at FB increase the output voltage error.

The recommended design procedure is to choose R_2 = 30.1 kΩ to set the divider current at 40µA and then calculate R_1 using:

$$R_1 = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) \times R_2 \qquad (2)$$



OUTPUT VOLTAGE PROGRAMMING GUIDE

OUTPUT VOLTAGE	R_1	R_2	UNIT
2.5V	33.2	30.1	kΩ
3.3V	53.6	30.1	kΩ
3.6V	61.9	30.1	kΩ
4.75V	90.8	30.1	kΩ

Figure 26. TPS767D301 Adjustable LDO Regulator Programming

RESET INDICATOR

The TPS767D3xx features a $\overline{\text{RESET}}$ output that can be used to monitor the status of the regulator. The internal comparator monitors the output voltage: when the output drops to 95% (typical) of its regulated value, the $\overline{\text{RESET}}$ output transistor turns on, taking the signal low. The open-drain output requires a pullup resistor. If not used, it can be left floating. $\overline{\text{RESET}}$ can be used to drive power-on reset circuitry or as a low-battery indicator.

REGULATOR PROTECTION

The TPS767D3xx PMOS-pass transistor has a built-in back-gate diode that safely conducts reverse currents when the input voltage drops below the output voltage (for example, during power-down). Current is conducted from the output to the input and is not internally limited. When extended reverse voltage is anticipated, external limiting may be appropriate.

The TPS767D3xx also features internal current limiting and thermal protection. During normal operation, the TPS767D3xx limits output current to approximately 1.7A. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds +150°C (typ), thermal-protection circuitry shuts it down. Once the device has cooled below +130°C (typ), regulator operation resumes.

POWER DISSIPATION AND JUNCTION TEMPERATURE

Specified regulator operation is assured to a junction temperature of +125°C; the maximum junction temperature should be restricted to +125°C under normal operating conditions. This restriction limits the power dissipation the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation, $P_D$max, and the actual dissipation, P_D, which must be less than or equal to $P_D$max.

The maximum-power-dissipation limit is determined using the following equation:

$$P_D\,max = \frac{T_J\,max - T_A}{R_{\Theta JA}} \tag{3}$$

Where:

- $T_J$max is the maximum allowable junction temperature.
- $R_{\theta JA}$ is the thermal resistance junction-to-ambient for the package, that is, 28°C/W for the 28-terminal PWP with no airflow.
- T_A is the ambient temperature.

The regulator dissipation is calculated using:

$$P_D = \left(V_{IN} - V_{OUT}\right) \times I_{OUT} \tag{4}$$

Power dissipation resulting from quiescent current is negligible. Excessive power dissipation will trigger the thermal protection circuit.

Revision History

Changes from Revision F (February 2008) to Revision G	Page
• Changed Corrected symbol for FB current in *Electrical Characteristics*	3

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