1.0 INTRODUCTION

The WD33C296A/WD33C197A/WD33C193A are high-performance PCI SCSI bus controller devices optimized for workstations, servers, disk array controllers, and high-end desktop personal computers. These devices are architecturally similar and software compatible.

To make for easier reading the term WD33C296A is referred to for all three devices. Differences between devices are noted where applicable

1.1 GENERAL DESCRIPTION

The WD33C296A is an 8/16-bit wide parallel SCSI bus protocol control device with emphasis on Host adaptor and disk array controller applications. The SCSI bus side is compatible with the WD33C96A ESBC device, with its programmability through task file registers and Writable Control Store (WCS).

The Host side is a Peripheral Component Interconnect (PCI) local bus based system, which is capable of becoming a bus master as well as being a slave to the host CPU.

In addition, a Reduced Instruction Set Controller (RISC) processor is built in to the WD33C296A to support more advanced applications. Such applications include scatter/gather handling and autonomous management of multiple threaded I/O tasks.

1.1.1 PCI Local Bus Interface

The Local Bus Interface (Host bus side) interfaces to a PCI bus. The PCI is capable of becoming a Bus Master and performs burst transfers.

During target transactions (task file register read or write, data FIFO read or write), the PCI interface can handle 8, 16 or 32 bit wide access. Each task file register is 8 bits wide, but up to four registers (32 bit) can be read or written at a time. Depending on the register and type of access, various wait states are inserted by delaying the generation of TRDY. In order to facilitate higher efficiency bus cycles, byte merging is supported.

The WD33C296A has three channels of PCI bus master DMA.

- Advanced Mode I/O to PCI (data transfer)
- Microcode Download from PCI
- Advanced Mode I/O to Local RAM (SCSI control block transfer)

The WD33C296A can deal with 32-bit wide memory and 32, 16 or 8-bit wide I/O port. To enhance the performance for the most demanding applications, cache memory line read/write command is supported during burst transfers, which can be as long as 128-bytes (32 double-word).

The channels 4 and 5 DMA are added to the WD33C196A, which work very much like channels 2 (externale memory/resource access for RISC) and 3 (microcode download) DMA respectively, except the implied source/destination port is the external memory port instead of the PCI bus.

The operation register is shared with channel 2 or 3 DMA, so coding style and microcode architecture do not have to change very much to take advantage of the external local memory.

1.1.2 SCSI Bus Interface

The SCSI bus interface can perform 16-bit fast SCSI timing for 10 million transfer cycles per second, or 20 MB/s.

The internal protocol/transfer sequencer permits cutting down the protocol overhead to a minimum. The sequencer is run off of the user-programmable 128-bit by 30-bit Writable Control Store. Combined with the Host of task file registers, it provides the highest degree of flexibility for high-performance SCSI applications.

There is a set of custom designed SCSI I/O transceivers at the SCSI bus pins, allowing the WD33C296A to connect to the parallel cable bus directly. It also has a 60 mA active negation driver with programmable slew rate control for smooth, noise-free operation while it is driving. The receiver has 500 mV hysteresis to reject most spurious transitions for stable operations. While there is no substitute for well designed cable and termina-

tions, the WD33C296A should function reliably even in a difficult environment. SCSI I/O transceiver also allows hot-plug operation where a device may be plugged in or removed from the active bus without disturbing the on-going transactions.

1.1.3 Internal RISC Processor

The WD33C296A has an internal RISC processor which can be used in "Advanced Mode." When programmed properly, the WD33C296A operates at the level of a "SCSI Bus Coprocessor" to the Host CPU. Possible applications include emulating other SCSI protocol devices such as WD33C93 scatter/gather management or multi-threaded I/O process handler, which significantly reduces the Host CPU overhead and makes device driver development much simpler.

The WD33C296A has 2K words of code RAM where user's custom code may be loaded. The custom code may be loaded using the device's bus master DMA function or loaded by the Host CPU as a PIO slave.

1.1.4 External Memory Port

The WD33C296A family has External Memory Port to support cold boot ROM.

The WD33C296A External Memory Port also supports the following additional functions:

- Cold boot ROM/Flash RAM
- RISC processor local storage
- SCSI control block (SCB) local storage

Neither memory is required for normal operation of the WD33C296A device. They can be left out for the minimum implementations. They should be used to enhance performance/system capacity with the implementation cost as a trade-off.

1.1.5 Testability

The WD33C296A is capable of performing the following test features:

- Partial scan test to ensure a high fault coverage to reduce defective device shipment.
  - Independent scan paths for SCSI and PCI.
  - External scan control in test mode.
- Built-in-Self-Test utilizing internal RISC processor to test its own functionality after the device is mounted on the board.
  - Diagnostic routine may be loaded externally.
- All pins can be tristated to support board test.
  - Exercised using a test mode.
- IEEE 1149.1 JTAG boundary scan is supported.
  - Five pins are added compatible with PCI Test Access Port pins arrangement, so the device can be scanned from the motherboard.

Note the WD33C296A test port is designed for boundary scan only, internal scan through TAP is not supported.

1.1.6 Compatibility

Except for the following conditions, the WD33C296A SCSI core section is functionally compatible with the WD33C95/96A ESBC device.

- A partial differential mode support.
- Task file register addresses are byte-packed, not word-aligned.
- LRC is not supported.
- Odd-byte reconnect is not supported.
- Host side DMA architecture is significantly altered; instead of generic DMA handshake, a PCI type is used.

WCS level compatibility is maintained.

While its architecture is significantly different, using a special microcode in Advanced mode, the WD33C296A is capable of emulating WD33C93-type controller. It can maintain register and interrupt level compatibility; its performance may yet be faster than the original WD33C93.

1.2 FEATURES

High Performance

- Extremely low overhead (<20 µs) SCSI bus protocol.
- High-speed SCSI bus data transfers, up to 20 MB/s (16-bit, synchronous).
- PCI Bus master DMA, up to 132 MB/s burst rate (33 MHz clock, 32-bit, bus master burst cycle).
- Independent, pipelined, 32-bit transfer counters to support seamless scatter/gather transfers.
- FIFO depth of 160-bytes total (32 in SCSI core, 128 in PCI).
- Expanded support for advanced memory commands:
  - Memory Read Line/Multiple
  - Memory Write and Invalidate (WD33C296A only)
  - Byte Merging Support
- Enhanced External Memory Port to be used for SCB and scatter/gather list buffering, up to 64K by 16 bit words, to support more concurrent SCSI tasks without increased PCI bus overhead. It can also be used to store the microcode overlay modules.
- Built-in program memory for internal RISC processor.

Flexibility

- User-programmable WCS permits fine tuning of protocol sequence and exception handling.
- The bus master DMA seamlessly supports variable length scatter and gather operation.
- Internal RISC processor with custom code download capability can simplify device interaction, reduce interrupts to the Host CPU.
- Byte merging support
- Re-writable device and vendor ID registers for product customization

System Integrity

- IEEE 1149.1 JTAG boundary scan.
- High-performance SCSI I/O circuitry to ensure the best signal quality.
  - 60 mA active negation drivers to allow usage of high current terminators.
  - 500 mV (typical) hysteresis receiver for rejecting unwanted signal transitions.
  - Driver rise and fall may be programmed in four steps.
  - Capable of proposed SCSI-3 hot plugging.
- PCI specification 2.1 compliant drivers on Local bus side.

Ease of Integration

- Boot ROM/Flash RAM (WD33C296A) on the External Memory Port up to 64 by 8-bit bytes.
- Programmable address decode logic built-in.
- Built-in program memory for internal RISC processor.
- Both Host and SCSI buses are properly buffered to connect directly to the respective bus.

Miscellaneous

- Five general purpose I/O pins for board utilities such as:
  - Terminator and Vterm On/Off
  - Serial E^2PROM support
  - LED driver
  - Jumper replacement

1.3 WD33C296A FAMILY OF DEVICES

There are three devices that share the general characteristics of the WD33C296A family.

- WD33C296A
  This is the full specification device that incorporates all the functions described in this document.

- WD33C197A
  This is a lower cost version of the device that has all the basic functionalities of the WD33C296A, less External RAM support for the internal RISC, the flash RAM support, and general purpose I/O port.

- WD33C193A
  This is the 8-bit SCSI only version of the WD33C197A. It supports 8-bit bus only.

Table 1-1 lists the differences among the three devices

ITEM	33C296A	33C197A	33C193A
SCSI Bus Width	8/16	8/16	8
FIFO Depth	128 + 32	128 + 32	128 + 32
Boot ROM Support	Yes	Yes	Yes
Flash RAM Support	Yes	No	No
Local Mem Support	Yes	No	No
Boot ROM Size	up to 64KB	up to 64KB	up to 64KB
Flash RAM Size	up to 64KB	N/A	N/A
SRAM Size	up to 64KW	N/A	N/A
General Purpose I/O	5	5	5
JTAG Support	Yes	Yes	Yes
PCI Device ID	3296 Hex	3197 Hex	3193 Hex
Pkg Pin Count	160	160	160

TABLE 1-1. DEVICE FAMILY DIFFERENCES

1.4 STANDARD COMPLIANCE

The WD33C296A device complies to proposed American National Standard for Information systems SCSI-3 Parallel Interface (SPI) X3T9.2/91-010.

The WD33C296A device complies to revision 2.1 of the PCI Local Bus specification.