SEEQ
Technology Incorporated

80C24
AutoDUPLEX™
CMOS Ethernet Interface Adapter

PRELIMINARY DATA SHEET *December 10, 1996*

Functional Features

- ***Low Power CMOS Technology Ethernet Serial Interface Adapter with Integrated Manchester Code Converter (MCC™), AUI and 10Base-T Transceiver with Output Wave Shaping and on chip filters.***
- ***Meets IEEE 802.3 10Base-5, 10Base-2, 10Base-T Standards***
- ***Direct Interface to SEEQ, INTEL, AMD & NATIONAL LAN Controllers***
- ***Automatic or Manual Selection of AUI/10Base-T Interface***
- ***Provides AutoDUPLEX™ Detect Function for SEEQ LAN Controllers and Doubles Bandwidth to 20 MBits/sec for Switched Networks***
- ***Status Indicators: Link, Transmit & Receive, Port Selection-AUI/TP, TP Cable Polarity***
- ***Diagnostic Loopback Support***
- ***Power On Reset with Power Down Mode to Conserve System Power***
- ***Separate Analog/Digital Power and Ground Pins to Minimize Noise***

Interface Features

- ***Meets IEEE 10Base-T Standards and IEEE 802.3 standards for AUI.***
- ***On Chip Transmit Wave Shaping and Low Pass Filter Circuits - No External Filters Required***
- ***Selectable Termination Impedance to Support UTP and STP Cables, (100 ohms, 150 ohms)***
- ***Long Cable Mode Support > 100 Meters***
- ***Automatic Polarity Correction***
- ***Link Integrity Test Disable, Selectable Coded Link Pulse for AutoDUPLEX Mode***
- ***Low differential and common mode noise on TP transmit outputs.***
- ***Differential Transmit Drivers to support 50 Meters of AUI Cable Lengths.***
- ***Direct AUI interface to the Manchester Code Converter.***

MCC and AutoDUPLEX are trademarks of SEEQ Technology, Inc.

Note: Check for latest Data Sheet revision before starting any designs.

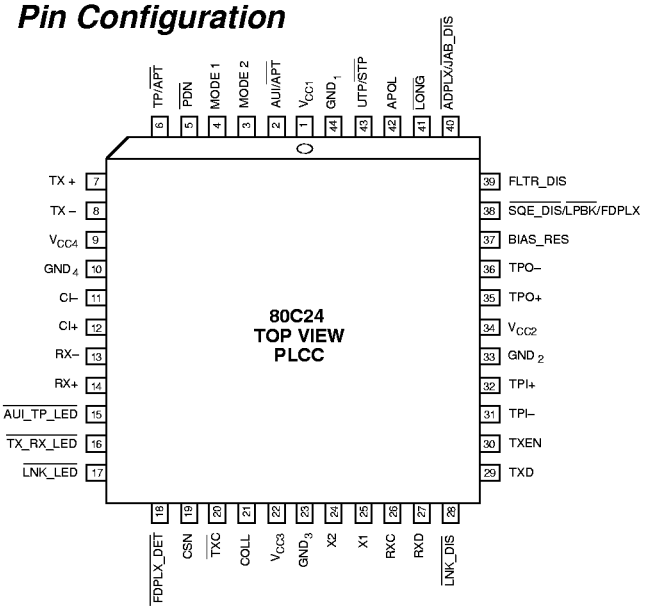
Call SEEQ Technology (510) 226-7400 x3051.

SEEQ Data Sheets are now on the Web, access SEEQ Home Page www.seeq.com.

General Description

The SEEQ 80C24 is a CMOS single chip Ethernet serial interface adapter with a completely integrated Manchester Code Converter (MCC), AUI & 10Base-T transceiver with wave shaping & filters eliminating the need for external filters. The 80C24 is designed to interface directly with SEEQ's family of Ethernet data link controllers- 8003, 80C03, 8005, 80C04, Intel, AMD & National's controllers. The chip provides automatic polarity correction, automatic port selection, support for cables longer than 100m, UTP/STP cable selection, power down mode, separate analog & digital ground pins & a link disable feature. It also provides a selectable coded link pulse to implement AutoDUPLEX function together with SEEQ's 80C03, 80C04 & NCORE controllers allowing seamless full duplex operation in switched network implementations doubling network bandwidth to 20 Mbps in 10Base-T. The 80C24 is typically suitable for adapter boards, motherboards and stand-alone TP transceiver designs & switching hubs.

Pin Configuration



Note: Refer to Appendix B for the Thin Quad Flat Package (TQFP).

80C24 Pin Description

Pin	Name	I/O	Description
1	V_{CC1}	—	Power supply pin. +5V ±5%.
2	AUI/$\overline{\text{APT}}$	Input Pulldown[1]	AUI Port/autoport select input. AUI/$\overline{\text{APT}}$ TP/$\overline{\text{APT}}$ 0 0 Automatic port selection enabled when $\overline{\text{LNK\_DIS}}$=1 0 1 TP port selected 1 0 AUI port selected 1 1 Invalid
3,4	MODE2, MODE1	Inputs Pulldown	Controller interface mode select input. These pins select one of four possible controller interfaces. Controller MODE2 MODE1 SEEQ 0 0 NSC 0 1 INTEL 1 0 AMD 1 1
5	$\overline{\text{PDN}}$	Input Pulldown	Powerdown input. When $\overline{\text{PDN}}$ = 0, all functions are disabled and power consumption is reduced to a minimum.
6	TP/$\overline{\text{APT}}$	Input Pullup[2]	TP Port/autoport select input. See AUI/$\overline{\text{APT}}$.
7	TX+	Output	AUI transmit output, positive.
8	TX–	Output	AUI transmit output, negative.
9	V_{CC4}	—	Power supply pin. +5V ±5%.
10	GND_4	—	Ground pin.
11	CI–	Input	AUI collision input, negative.
12	CI+	Input	AUI collision input, positive.
13	RX–	Input	AUI receive input, negative.
14	RX+	Input	AUI receive input, positive.
15	$\overline{\text{AUI\_TP\_LED}}$	Output	Port select indication output. This pin is an open drain output and is capable of driving an LED from V_{CC}. This pin also indicates reverse polarity on the twisted pair inputs by blinking on and off when the polarity is reversed. $\overline{\text{AUI\_TP\_LED}}$ = High Z AUI port selected. = 0 TP port selected.
16	$\overline{\text{TX\_RX\_LED}}$	Output	Transmit and receive activity output. This output goes low and stays low for a minimum of 0.2 sec, when there is packet transmission or reception on the TP or AUI port. This pin is an open drain output and is capable of driving an LED from V_{CC}.

[1] Pulldown indicates that the pin is pulled down internally so that the default state is low.
[2] Pullup indicates that the pin is internally pulled up so that the default state is high.

Pin Description cont'd

Pin	Name	I/O	Description
17	$\overline{\text{LNK\_LED}}$	Output	Link pulse detect output. When $\overline{\text{LNK\_LED}}$ = 0, link pulse is detected on twisted pair receive input. This pin is an open drain output and is capable of driving an LED from V_{CC}.
18	$\overline{\text{FDPLX\_DET}}$	Output	Full duplex detect output. When $\overline{\text{FDPLX\_DET}}$ = 0, the device has been placed in the full duplex mode by either selection or by the AutoDUPLEX feature.
19	CSN	Output	Carrier sense output. This controller interface output indicates valid data and collisions on the receive TP or AUI inputs.
20	$\overline{\text{TXC}}$	Output	Transmit clock output. This controller interface output provides a 10MHZ clock to the controller. Transmit data from the controller on TXD is clocked in on edges of $\overline{\text{TXC}}$.
21	COLL	Output	Collision output. This controller interface output is asserted when collision between transmit and receive data is occuring, and during SQE test.
22	V_{CC3}	—	Power supply pin. +5V ±5%.
23	GND_3	—	Ground pin.
24	X2	Output	Crystal oscillator output. The master clock for the device is generated by either placing a crystal between X1 and X2, or by applying an external clock to X1.
25	X1	Input	Crystal oscillator input. The master clock for the device is generated by either placing a crystal between X1 and X2, or by applying an external clock to X1.
26	RXC	Output	Receive clock output. This controller interface output provides a 10MHZ clock to the controller. Receive data on RXD is clocked out on edges of RXC.
27	RXD	Output	Receive data output. This controller interface output contains receive data decoded from the receive TP/AUI inputs and is clocked out on edges of RXC.
28	$\overline{\text{LNK\_DIS}}$	Input Pullup	Link disable input. When $\overline{\text{LNK\_DIS}}$ = 0, link pulse functions are disabled; that is, no link pulses are transmitted on TP outputs, link pulse detection on receive TP inputs ignored.
29	TXD	Input	Transmit data input. This controller interface input contains data to be transmitted on either TP or AUI transmit outputs and is clocked in on edges of $\overline{\text{TXC}}$.
30	TXEN	Input	Transmit enable input. This controller interface input has to be asserted when data on TXD is valid.
31	TPI –	Input	Twisted pair receive input, negative.
32	TPI+	Input	Twisted pair receive input, positive.
33	GND_2	—	Ground pin.
34	V_{CC2}	—	Power supply pin. +5V ±5%.

Pin Description cont'd

Pin	Name	I/O	Description
35	TPO+	Output	Twisted pair transmit output, positive.
36	TPO–	Output	Twisted pair transmit output, negative.
37	BIAS_RES	Output	Bias resistor set. A resistor tied between this pin and A_{GND} sets the twisted pair transmit peak output current level on TPO±.
38	$\overline{SQE\_DIS}$/ $\overline{LPBK}$/ FDPLX	Input Pullup	SQE disable/loopback/full duplex enable input. This pin has three distinct functions. The pin is configured as one of the first two functions, $\overline{SQE\_DIS}$ and $\overline{LPBK}$, depending on whether TP or AUI port is selected. IF TP PORT IS SELECTED AND $\overline{LNK\_DIS}$ = 1 $\overline{SQE\_DIS}$ = 1 SQE test enabled = 0 SQE test disabled IF AUI PORT IS SELECTED AND $\overline{LNK\_DIS}$ = 0 $\overline{LPBK}$ = 1 Loopback disabled = 0 Loopback enabled This pin can be configured as the third function, FDPLX, by setting AUI/$\overline{APT}$ = 0, TP/$\overline{APT}$ = 0. $\overline{LNK\_DIS}$ = 0, FDPLX = 1. This pin combination forces the device into the full duplex mode. It is important to note that the link pulses will be present even though the $\overline{LNK\_DIS}$ pin is held low. This happens only in this particular mode.
39	FLTR_DIS	Input Pulldown	Filter disable input. When FLTR_DIS=1, the internal transmit and receive filters are disabled.
40	$\overline{ADPLX}$/ $\overline{JAB\_DIS}$	Input Pullup	Autoduplex enable/jabber disable input. This pin changes function depending on whether TP or AUI port is selected. IF TP PORT IS SELECTED AND $\overline{LNK\_DIS}$ = 1 $\overline{ADPLX}$ = 1 Half duplex selected = 0 Autoduplex on IF AUI PORT IS SELECTED AND $\overline{LNK\_DIS}$ = 0 JAB_DIS = 1 Jabber enabled = 0 Jabber disabled
41	$\overline{LONG}$	Input Pullup	Long cable mode input. When $\overline{LONG}$ = 0, the receive input thresholds are reduced to accomodate cable lengths in excess of 100 meters.
42	APOL	Input Pulldown	Autopolarity input. When APOL = 1, this pin enables the autopolarity function and automatically corrects for reversed polarity on the twisted pair receive inputs, TPI±.
43	UTP/$\overline{STP}$	Input Pullup	Cable type select input. This pin adjusts the twisted pair transmit output current level to accomodate either 100 ohm (UTP) or 150 ohm (STP) cable. UTP/$\overline{STP}$ = 1 100 ohm cable (UTP) = 0 150 ohm cable (STP)
44	GND_1	—	Ground pin.

BLOCK DESCRIPTION

Functional Description

The 80C24 is an Ethernet adapter with a completely integrated Manchester Code Converter, 10Base-T transceiver with on chip filters. The device contains both 10Base-T and AUI interfaces compliant with IEEE 802.3 specifications. The chip is divided into four major blocks, namely (i) The controller interface (ii) The Encoder / Decoder (iii) The twisted pair interface and (iv) The AUI. The input signals are received on the TP or AUI receivers depending on which is selected. Both the twisted pair and AUI receivers contain a threshold comparator to validate the signal and a zero crossing comparator for checking the transitions. Then the data is sent to the PLL in the decoder to separate the data from the clock. On the other side, digital transmit data is clocked into the device via the controller interface. The data is then sent to the Manchester encoder to be encoded. Encoded data is then transmitted on the twisted pair or AUI based on the selected port.

The Controller Interface

The 80C24 is designed to interface directly to SEEQ's 80C03, 80C04 & NCORE controllers, INTEL's 82586/596/592/593 LAN controllers, NSC and AMD's controllers with the use of MODE1 & MODE2 pins . The controller interface consists of the Transmit/Receive data (TXD/RXD), transmit/receive Clocks ($\overline{TXC}$/RXC), the Transmit Enable (TXEN) input, the collision output (COLL), the Full Duplex acknowledgment ($\overline{FDPLX\_DET}$) and the Carrier Sense Output (CSN) pins. On the transmit side, data on TXD is clocked into the device on the edges of $\overline{TXC}$ clock output only when the data valid signal (TXEN) is asserted. On the receive side, data on RXD is clocked out on edges of RXC. In the SEEQ, NSC and AMD modes, RXC follows $\overline{TXC}$ for 2.2 µs in the TP mode or 1.8 µs in the AUI mode and then switches to the recovered clock. In the Intel mode, RXC is held low for 2.2 µs in the TP mode or 1.8 µs in the AUI mode while the PLL is acquiring lock and then switches to the recovered lock. The $\overline{FDPLX\_DET}$ pin signifies to the controller that full duplex channels have been established.

The following mode table illustrates the selection of the appropriate inputs to match the controller.

MODE 2	MODE 1	Controller
0	0	SEEQ
0	1	NSC
1	0	INTEL
1	1	AMD

The Encoder/Decoder

Manchester encoding is a process of combining the clock & the data stream together so that they can be transmitted on the twisted pair interface or AUI at the transceiver side. Once encoded, the first half contains the complement of the data and the second half contains the true data, so that a transition is always guaranteed at the middle of a bit cell. Data encoding and transmission begins with TXEN going active, and the subsequent data is clocked on the edges of $\overline{TXC}$ and then gets encoded. The end of a transmit packet occurs at a bit cell center if the last bit is a "ONE" or at a bit boundary if the last bit is a "ZERO".

The decoding is a process of recovering the encoded data stream coming from the receiver side and decoding it back into the clock and data outputs using the phase locked loop technique. The PLL is designed to lock into the preamble of the incoming signal at less than 20 bit times with a maximum jitter of ±13.5 ns at the TPI or AUI inputs and can also sample the incoming data with this amount of jitter. The ENDEC asserts the CSN signal to indicate to the controller that the data and clock received are valid and available. There is an inhibit period after the end of a frame after a node has finished transmitting for 4.4 µs during which CSN is deasserted irregardless of the state of the receiver and collision status.

Twisted Pair Interface

(a) The transmitter function

The transmitter transfers Manchester encoded data from the ENDEC to the twisted pair cable. The circuit consists of a set of functional blocks to provide pre-coded waveshaped, pre-equalized and smoothed waveforms so that the outputs are made to appear as though it had passed through a 5-7th order external elliptic passive filter, thereby eliminating the need for an external filter. The waveform generator consists of a ROM, DAC, PLL, filter and a output driver to preshape the output waveform transmitted onto the twisted pair cable to meet the pulse template requirements outlined in IEEE STD 802.3 and illustrated in figure 12. The DAC first converts the data pulse into a stair stepped representation of the desired output waveform, which goes through a second order low-pass filter. The DAC values are determined from the ROM addresses, which are chosen to have different values for long and short data bits so as to shape the pulse to meet the 10Base-T waveform template. The line driver takes the smoothed current waveform and converts it into an high current output that can drive the TP directly without any external filters. The current output is also guaranteed to have a very low common mode and differential noise. The interface to the twisted pair cable requires a transformer

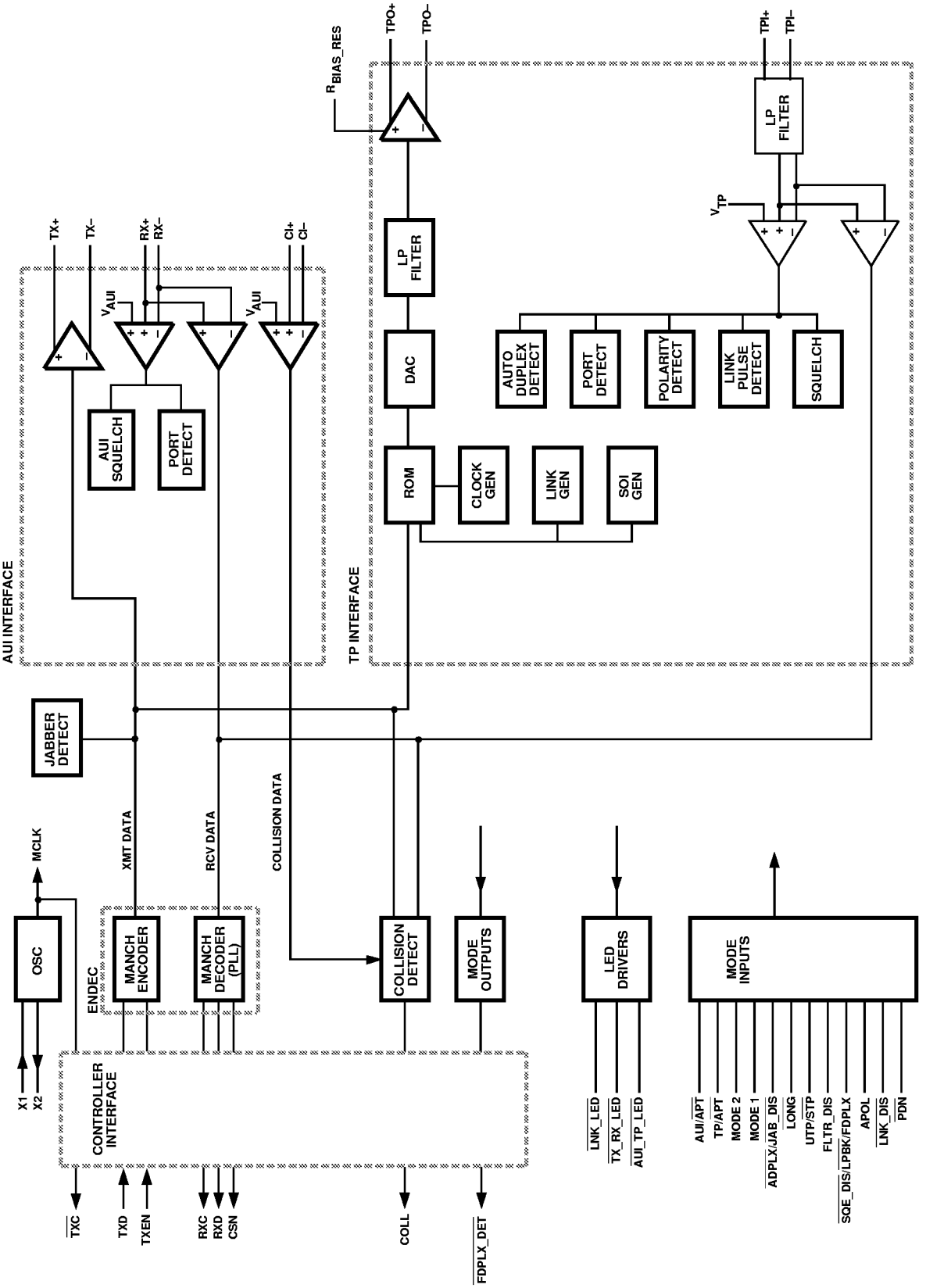


Figure 1. 80C24 Block Diagram

with a ratio of 2:1 on transmit and a 1:1 on receive, with two 200 ohm resistors connected as shown in figure 2. The output driver is a current source. The output current level is set by the values of the resistor tied between the BIAS_RES (Pin 37) & GND. The current level is determined by the following equation.

$$I_{OUT} = (R_{BIAS\_RES}/10K)* 50\ mA$$

Though a 10K resistor will meet the template requirements specified with a no load condition, a capacitive or inductive loading can influence the level, because the transmitter has a current source output. So, in a actual application, it might be necessary to adjust the value to compensate the loading involved. For example, the bias resistance value for a loading of 10 pf will be 8K approximately.

(b) The receiver function

The receiver receives the Manchester-encoded data from the twisted pair lines(TPI±) and passes it on to the ENDEC side, where it gets decoded back into the receive clock RXC and the receive data RXD. The inputs first goes through a receive filter, which is a continuous time 3rd order low pass filter with a typical 3 dB cutoff frequency of 20-25 Mhz. The filter's output then passes through two different types of comparators, namely threshold and zero crossing. The threshold comparator compares the TPI± inputs with fixed positive and negative thresholds called the squelch levels. The zero crossing comparator senses the transition point on the TPI± inputs without introducing excess jitter and the outputs goes to the PLL in the decoder. The receiver is transformer coupled and needs to be terminated with a 100Ω resistor or two 50Ω resistor and a capacitor as described in figure 2.

(c) Full Duplex Functions

The Full Duplex scheme allows the simultaneous transmission on the TPO± and simultaneous reception on the TPI± without interruption, effectively doubling the bandwidth to 20 MBPS in switched network implementations on 10Base-T. The 80C24 can be made to operate either in the AutoDUPLEX or in the Forced FullDuplex scheme.

The 80C24 is switched on to the AutoDUPLEX mode when an active LOW signal is detected on the $\overline{ADPLX}$/$\overline{JAB\_DIS}$ (pin 40) in the TP mode. In this configuration, Full duplex mode is automatically established by the successful detection of double pulses embedded within the regular link pulses. The 80C24 sends the double pulses in 16 pulse intervals constantly on the TPO± pins and continually monitors the TPI± pins for similar type of double pulses within a time window of 210 ±6ms. Once the double pulses are detected, the $\overline{FDPLX\_DET}$ (Pin 18) will go low to acknowledge to the controller that the network will allow simultaneous transmission and reception on the TP port. The maximum distance between two consecutive pulses in a double pulse is 5.4 µs.

The Forced Full-Duplex mode can be established by the following pin combinations.

1. AUI/$\overline{APT}$ (pin 2) = 0, TP/$\overline{APT}$ (pin 6) = 0;	*Sets 80C24 in Autoport.*
2. $\overline{LNK\_DIS}$ (pin 28) = 0.	*Disables Link.*
3. $\overline{SQE\_DIS}$/$\overline{LPBK}$/FDPLX = 1	*Forces the 80C24 into FullDuplex.*

In this combination, forced full duplex is effectively established and Collision, SQE & the LoopBack functions are disabled.

(d) Squelch functions

The squelch function is used to discriminate noise from link test pulses and valid data to prevent the noise from activating the receiver. It is accomplished by a squelch comparator which compares the TPI± signals with a fixed positive and negative squelch value. The output from the comparator goes to a receive squelch circuit which determines whether the input data is valid or not. If the data is invalid, the transceiver enters into an squelched state. The input voltage should exceed ±300mV p-p for five bit times max. (with alternating polarity) for unsquelching to occur. In the Unsquelch state, the value of the threshold in the comparator is reduced to take care of hysteresis effects. While in the unsquelch state, the receive squelch circuit looks for the SOI (Start of Idle) signal at the end of the packet. When the SOI signal is detected, the receive squelch is turned on again.

(e) The Link integrity functions

The 80C24 monitors the TPI± pins continuously for valid data and link pulse activity. If neither data or link test pulse is detected for a minimum time, the transceiver enters into a Link Test Fail State and disables the transmitter, receiver, collision presence and the SQE functions. For the transceiver to exit this state, it should receive three consecutive link pulses or valid data at the TPI± inputs to resume normal packet transmission and reception. On the other hand, the transmitter generates link pulses periodically when it's not transmitting data to indicate to the network that the link is intact. Please refer to figure 14 for the diagram illustrating the Transmit Link Pulse Voltage Template as specified in the IEEE 802.3. The Link function could be disabled by providing an active low input to pin 28 ($\overline{LNK\_DIS}$). In this mode, link pulses are neither transmitted nor received. A link pulse detect output capable of driving a LED is also provided for link indication.

(f) The Start of Idle (SOI) pulse

The transmit SOI pulse is a positive pulse inserted at the end of every transmission to signal the end and the start of idle period to corresponding receivers. The output pulse is also shaped by the transmit waveshaper to meet the pulse requirements specified in IEEE 802.3. Please refer to figure 13 for the Transmit Start Of Idle Pulse voltage template diagram. The receiver detects the SOI pulse by sensing the missing data transitions with the zero crossing comparator. Once the SOI pulse is detected, another SOI pulse is generated and sent to the Controller interface outputs.

(g) Automatic Polarity Correction

The 80C24 provides autopolarity detection and correction functions for the twisted pair receiver peak detectors to determine whether normal or inverted data is received over the TPI± pins. Automatic polarity is enabled by making APOL (Pin 42) HIGH. The polarity reversal can be indicated by connecting a LED to the AUI_TP_LED pin, which would blink when a reversal is observed. A polarity reversed condition is sensed when four opposite link pulses are detected without the expected polarity or if 3-4 frames are received with a reversed start-of-idle.

(h) Jabber functions

The jabber function detects abnormally long streams of Manchester-encoded data on the TXD input with the help of a Jabber detect circuit. The jabber circuit uses a Jabber timer, which monitors the TXEN pin. It starts counting at the beginning of each transmission. If the timer expires before TXEN goes inactive, the 80C24 enters a jabber state disabling the transmit/loopback functions and enabling the collision functions. If TXEN goes inactive before the timer expires, the timer is reset and becomes ready for the next transmission. The jabber function can be disabled in the AUI mode by applying an active low signal to the ADPLX/JAB_DIS (pin 40). The jabber function can also be disabled in TP mode for certain pin combinations described in Appendix A.

(i) Loopback functions

Loopback in the TP mode is internally enabled when Manchester encoded data is transmitted on TPO± and no data is received on the TPI± in order to simulate Coax Ethernet behavior. When internal loopback is enabled, the transmitted data is loopbacked into the RXD and sent to the controller. The loopback function is disabled during Link Fail State, Jabber State and during Full-Duplex Operation.

In the AUI mode, internal loopback function can be forcefully enabled by applying an active low to SQE_DIS/LPBK/FDPLX (pin 38) and the transmit data can be loopbacked for diagnostic purposes.

(j) Long mode

The 80C24 can be made to support longer cable lengths (> 100 meters) by applying an active LOW signal to the LONG (pin 41) pin. When this pin is LOW, the threshold levels of the internal threshold comparators are lowered to accommodate the longer cable length. In normal mode, it supports a cable with 11.5dB of attenuation and in the LONG mode an additional 4dB of attenuation is supported.

(k) Cable mode

The UTP/STP pin can be used to configure the 80C24 to be used with a selectable termination impedance of 100 ohms or 150 ohms for use with either UTP or STP cable types respectively. The STP mode is selected by tying this pin LOW. When tied LOW, the output current is reduced so as to keep the amplitude of the transmit signal unchanged from the template when the STP cable is attached.

(l) Signal Quality Error Test

The Signal Quality Error test is used to indicate a successful transmission (i,e A transmission without interruptions such as Collision, jabber or Link failure) to the DTE.When the SQE is enabled, a COLL signal is presented to the controller when the transmitter goes idle after a successful transmission of a frame on the twisted pair network. The Signal Quality Error test can be disabled by applying an active low to SQE_DIS/LPBK/FDPLX (pin 38) since it becomes necessary to disable SQE tests for applications such as repeaters. When this pin is tied low, only the SQE functions are disabled and the normal collision detection functionality is left unchanged during regular transceiver operations. The maximum duration of the SQE test is 850 ns and the maximum SQE test wait delay is 700ns.

AUI Interface

The differential transmit output pair TX+/TX- sends the encoded data on to an external transceiver and is capable of driving 50 meters of 78ohm shielded AUI cable directly with a jitter of 0.5 ns max. The receive input differential pair RX+/RX- goes through the AUI squelch comparator and the zero crossing comparator. The AUI squelch comparator compares the input signals with fixed minimum and maximum values of -175mv and -325mv respectively, and passes it on to the squelch circuit to determine data validity. The zero crossing comparator senses the transition point of the input pair without introducing excess jitter and passes the data to the phase locked loop of the decoder. The CI+/CI- are the collision input pair signals which would expect a 5 Mhz or a 10 Mhz square wave from an external transceiver.

Collisions

Collisions are generated when two stations try to contend for the network at the same time, which would result in simultaneous activity detected on the TPO± and TPI±. When this happens, COLL will be asserted to indicate to the controller the simultaneous transmission of two or more stations on the network. CSN is also asserted during collision. For further details, about timing, refer to figures 7 and 8.

Oscillator

The internal clock generator is controlled either by an external parallel resonant crystal connected across the X1 & X2 or by connecting an clock to the input pin X1. This external 20 Mhz clock is used by the clock circuitry and the PLL to generate a 10 Mhz ± 0.01% transmit clock. The manchester encoding process uses both the 10Mhz and 20Mhz clocks.

Crystal Specification:

1. *Parallel resonant mode*
2. *Frequency ..... 20 MHz ±0.01% @ 0 – 70°C*
3. *Equivalent Series Resistance ..... 25 Ω max.*
4. *Load Capacitance ..... 20 pf max.*
5. *Case Capacitance ..... 7 pf max.*

Automatic Port Selection

The automatic port selection feature of the 80C24 can be enabled by applying active low inputs to the AUI/$\overline{APT}$ (pin 2) & TP/$\overline{APT}$ (pin 6) respectively. In this mode, 80C24 automatically selects either the TP or AUI port by detecting the presence or absence of activity on the TPI± and RX± respectively. In the Autoport mode, the device powers up with the TP port active. If no activity is detected for a period of 800 ms on the TP port, the device automatically switches to AUI mode. The device will stay in AUI mode as long as no activity is detected on the TP port. Note that activity is defined as the presence of either link pulses or packets.

Powerdown

The 80C24 can be made to go into a low power mode by applying an active low signal to $\overline{PDN}$ (pin 5). In this mode, all the functions in the device are disabled and the power consumption is reduced to a bare minimum of 0.5 mA or less.

Power Supply Decoupling

There are four sets of V_{CC}/GND on the 80C24: (V_{CC1}/GND_1, VCC_2/GND_2, VCC_3/GND_3, and VCC_4/GND_4.

All V_{CC}'s should be connected together as close as possible to the device with a large V_{CC} plane. If the V_{CC}'s vary in potential by even a small amount, noise and latchup can result.

All GND's should also be connected together as close as possible to the device with a large ground plane. If the GND's vary in potential by even a small amount, noise and latchup can result.

A 0.01-0.1 µF decoupling capacitor should be connected between each V_{CC}/GND set as close as possible to the device pins, preferably within 0.5". The value of the decoupling capacitor should be selected based on whether the noise on V_{CC}-GND is high or low frequency. A conservative approach would be to use two decoupling capacitors on each V_{CC}/GND set, one 0.1µF for low frequency and one 0.001 µF for high frequency noise on the power supply.

The V_{CC} connection to the transmit transformer center tap shown in Figure 2 has to be well decoupled in order to minimize common mode noise injection from V_{CC} onto the TP wires. It is recommended that a 0.01 µF decoupling capacitor be placed between the center tap V_{CC} to the 80C24 GND plane. This decoupling capacitor should be physically placed within 0.5" of the transformer center tap.

The PCB layout and power supply decoupling discussed above should provide sufficient decoupling to acheive the following when measured at the device: (1) the resultant AC noise voltage measured across each V_{CC}/GND set should be less than 100 mV_{PP}, (2) all V_{CC}'s should be within 50 m V_{PP} of each other, and (3) all GND's should be within 50m V_{PP} of each other.

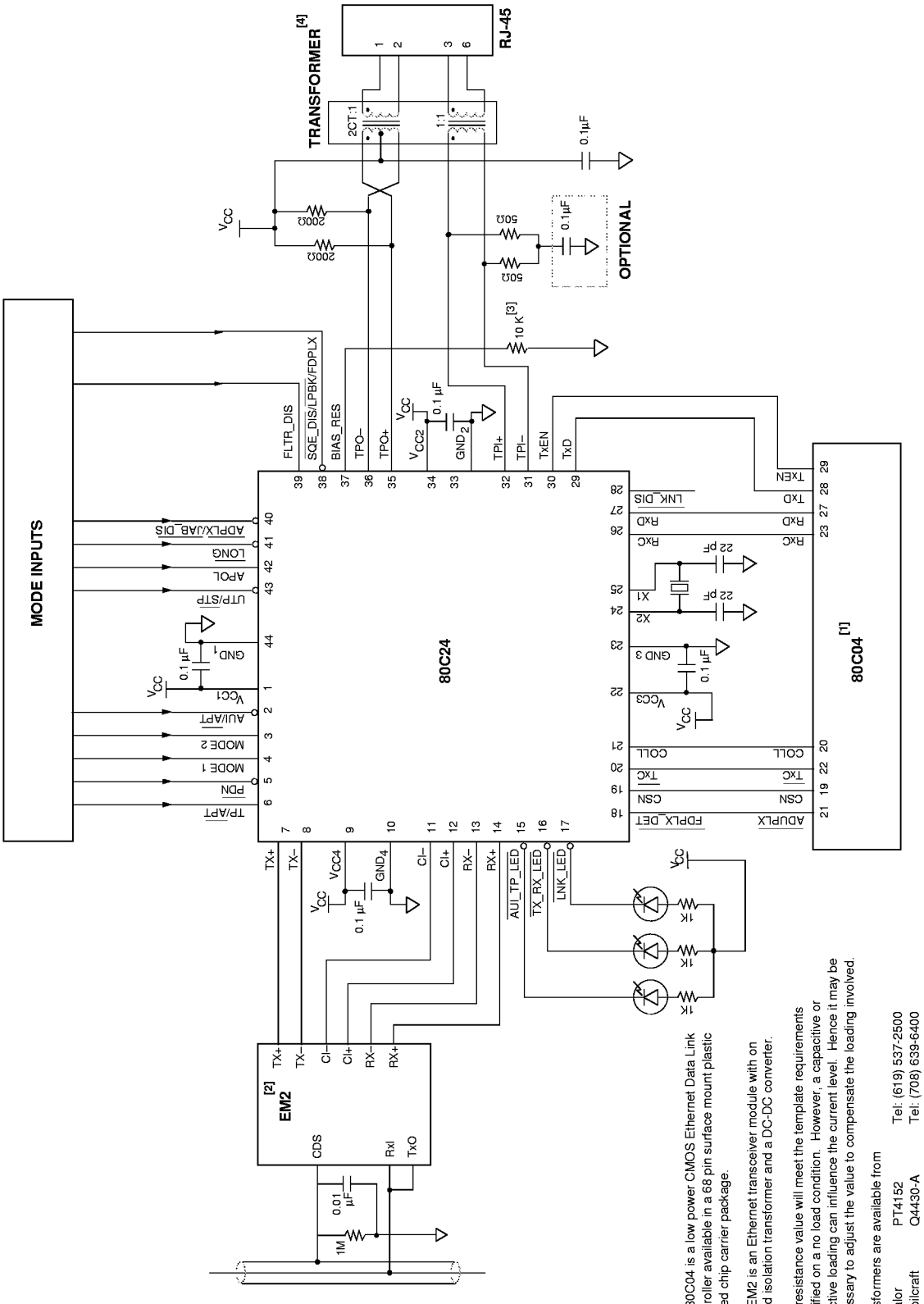


Figure 2. 80C24 in a Typical Application

Notes:

1. The 80C04 is a low power CMOS Ethernet Data Link Controller available in a 68 pin surface mount plastic leaded chip carrier package.
2. The EM2 is an Ethernet transceiver module with on board isolation transformer and a DC-DC converter.
3. This resistance value will meet the template requirements specified on a no load condition. However, a capacitive or inductive loading can influence the current level. Hence it may be necessary to adjust the value to compensate the loading involved.
4. Transformers are available from

a. Valor	PT4152	Tel: (619) 537-2500
b. Coilcraft	Q4430-A	Tel: (708) 639-6400
c. PCA	EPE6047S	Tel: (818) 892-0761
d. Belfuse	A553-SEEQ-01	Tel: (201) 432-4463
e. FEE Fil_mag	23Z128	Tel: (619) 569-6577

Absolute Maximum Ratings

V_{CC} Supply Voltage ..... –0.3V to 7V
All Inputs and Outputs ..... –0.3 to V_{CC} + 0.3 V
Latchup Current ..... ±25 mA
Package Power Dissipation ..... 1 Watt @ 25°C
Storage Temperature ..... –65 to +150°C
Operating Temperature ..... –65 to +125°C
Lead Temperature (Soldering, 10 sec) ..... 250°C

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

Power Supply Characteristics

Test conditions are as follows:

1. T = 0–70°C
2. V_{CC} = 5V ±5%
3. 20 MHZ ±.01%
4. BIAS_RES = 10K, with no load.

Sym.	Parameter	Limit Min	Limit Typ	Limit Max	Unit	Conditions
I_{CC}	V_{CC} Power Supply Current		110	150	mA	Transmitting, TP selected
			85	110	mA	Transmitting, AUI selected
				0.5	mA	Powerdown

DC Digital I/O Characteristics

Test conditions are as follows:

1. T = 0–70°C
2. V_{CC} = 5V ±5%
3. 20 MHZ ±.01%
4. BIAS_RES = 10K, with no load.

Sym.	Parameter	Limit Min	Limit Typ	Limit Max	Unit	Conditions
V_{IL}	Input Low Voltage			0.8	Volt	All except X1
				1.5	Volt	X1
V_{IH}	Input High Voltage	2			Volt	All except X1
		3.5			Volt	X1
I_{IH}	Input High Current			1	µA	V_{IN}= V_{CC} X1
		20	60	120	µA	V_{IN}= V_{CC} AUI/$\overline{APT}$, MODE1-2, $\overline{PDN}$, FLTR_DIS, APOL
I_{IL}	Input Low Current			–1	µA	V_{IN}= GND X1
		–20	–60	–120	µA	V_{IN}= GND $\overline{LNK\_DIS}$, $\overline{SQE\_DIS}$/$\overline{LPBK}$/FDPLX $\overline{ADPLX}$/$\overline{JAB\_DIS}$, $\overline{LONG}$, UTP/$\overline{STP}$, TP/$\overline{APT}$

DC Digital I/O Characteristics cont'd

Sym.	Parameter	Limit			Unit	Conditions
		Min	Typ	Max		
V_{OL}	Output Low Voltage			0.4	Volt	I_{OL}= 2.1 mA All except $\overline{\text{AUI\_TP\_LED}}$, $\overline{\text{TX\_RX\_LED}}$, $\overline{\text{LNK\_LED}}$
				1.2	Volt	I_{OL}= –20mA $\overline{\text{AUI\_TP\_LED}}$, $\overline{\text{TX\_RX\_LED}}$, $\overline{\text{LNK\_LED}}$
V_{OH}	Output High Voltage			4	Volt	I_{OH}= –400µA All except $\overline{\text{AUI\_TP\_LED}}$, $\overline{\text{TX\_RX\_LED}}$, $\overline{\text{LNK\_LED}}$
I_{OZ}	Output Leakage Current			–1	µA	V_{OH}= V_{CC} $\overline{\text{AUI\_TP\_LED}}$, $\overline{\text{TX\_RX\_LED}}$, $\overline{\text{LNK\_LED}}$
C_{IN}	Input Capacitance		5		pF	
C_{OUT}	Output Capacitance		5		pF	

Twisted Pair Interface Characteristics

Unless otherwise specified, all test conditions are as follows:

1. T = 0–70°C
2. V_{CC} = 5V ±5%
3. 20MHZ ±.01%
4. BIAS_RES = 10K, with no load.
5. TPO± loading as shown in Figure 2 or equivalent.
6. 10Mhz sine wave on TPI±

Sym.	Parameter	Limit			Unit	Conditions
		Min	Typ	Max		
TOV	TPO± Differential Output Voltage	2.2	2.5	2.8	Vpk	
TOVT	TPO± Differential Output Voltage Template	See Figure 12				
TSOI	TPO± SOI Output Voltage Template	See Figure 13				
TLPT	TPO± Link Pulse Output Voltage Template	See Figure 14				
TOIV	TPO± Differential Output Idle Voltage			±50	mV	Measured on Secondary Side of XFMR in Fig. 2
TOIA	TPO± Output Current	44	50	56	mA pk	UTP cable mode
		29	33	37	mA pk	STP cable mode
TOIR	TPO± Output Current Adjustment Range	0.70		1.40		V_{CC} = 5V Adjustable with BIAS_RES
TCMA	TPO± Common Mode AC Output Voltage		10	50	mV pk	Relative to Value at BIAS_RES = 10K
THD	TPO± Harmonic Distortion			–27	dB	
TOR	TPO± Output Resistance		10K		ohms	
TOC	TPO± Output Capacitance		15		pF	
RST	TPI± Squelch Threshold	310		540	mVpk	$\overline{\text{LONG}}$ = 1
		190		330	mVpk	$\overline{\text{LONG}}$ = 0
RUT	TPI± Unsquelch Threshold	190		330	mVpk	$\overline{\text{LONG}}$ = 1
		115		200	mVpk	$\overline{\text{LONG}}$ = 0
RZT	TPI± Zero Cross Switching Threshold			20	mVpk	
ROCV	TPI± Input Open Circuit Voltage	(V_{CC}/3)–0.25	V_{CC}/3	(V_{CC}/3)+0.25	Volt	

Twisted Pair Interface Characteristics cont'd

Sym.	Parameter	Limit			Unit	Conditions
		Min	Typ	Max		
RCMR	TPI± Input Common Mode Voltage Range	V_{CC}/3–1.0		V_{CC}/3+1.0	Volt	
RDR	TPI+/– Input Differential Voltage Range			V_{CC}	Volt	
RCRR	TPI+/– Input Common Mode Rejection Ratio			–20	dB	0–10Mhz
RIR	TPI+/– Input Resistance	5K			ohm	
RIC	TPI+/– Input Capacitance		10		pF	

AUI Characteristics

Unless otherwise specified, all test conditions are as follows:

1. T = 0–70°C
2. V_{CC} = 5V ±5%
3. 20MHZ ±.01%
4. BIAS_RES = 10K with no load.
5. 78 ohm, 27µH load on TX±
6. 10Mhz sine wave on RX±, CI±

Sym.	Parameter	Limit			Unit	Conditions
		Min	Typ	Max		
AOV	TX±, Differential Output Voltage	550		1200	mVpk	
AORF	TX±, Output Rise And Fall Time			5	nS	tR, tF measured at 10-90% points
AOIV	TX±, Differential Output Idle Voltage			±40	mV	
AOVU	TX±, Differential Output Voltage Undershoot During Idle			–100	mV	
AOCD	TX±, Common Mode DC Output Voltage	V_{CC}/3.5	V_{CC}/3.0	V_{CC}/2.1	Volt	
AOCA	TX±, Common Mode AC Output Voltage			40	mV pk	
AOR	TX±, Output Resistance			75	ohms	
AOC	TX±, Output Capacitance		15		pF	
AIST	RX±, CI± Squelch Threshold	-175		-325	mV	
AIUT	RX±, CI± Unsquelch Threshold	-100		-225	mV	
AIZT	RX±, CI± Zero Cross Switching Threshold			20	mVpk	
AIOC	RX±, CI± Input Open Circuit Voltage	(V_{CC}/3)–.25	V_{CC}/3	(V_{CC}/3)+.25	Volt	
AICR	RX±, CI± Input Common Mode Voltage Range	(V_{CC}/3)–1.0		(V_{CC}/3)+1.0	Volt	
AIVR	RX±, CI± Input Differential Voltage Range	0		V_{CC}	Volt	
AIR	RX±, CI± Input Resistance	5K	10K		ohm	
AIC	RX±, CI± Input Capacitance		10		pF	

AC Test Timing Conditions

Unless otherwise specified, all test conditions for timing characteristics are as follows:

1. T = 0 – 70°C
2. V_{CC} = 5v ±5%
3. 20MHZ ±.01%
4. BIAS_RES = 10K, with no load.
5. Input Conditions
   - All Inputs: t_R, t_F< = 10ns from 20-80% points
6. Output Loading
   - TPO±: 50 ohms to V_{CC} on each output, 10pF
   - TX±: 78 ohms differentially, 10pF
   - Open Drain Digital Outputs: 1K pullup, 50pF
   - All Other Digital Outputs: 50pF
7. Measurement Points
   - TPO±, TPI±, TX±, RX±, CI±: Zero crossing during data and ±.3V point at start/end of signal
   - X1: V_{CC}/2
   - All other inputs and outputs: 1.5 Volts

20 MHZ Input Clock Timing Characteristics

Sym.	Parameter	Limit			Unit	Conditions
		Min	Typ	Max		
t_1	X1 Cycle Time	49.995	50.005	50.005	nS	
t_2	X1 High Time	15			nS	
t_3	X1 Low Time	15			nS	

Refer to Figure 3 for timing diagram.

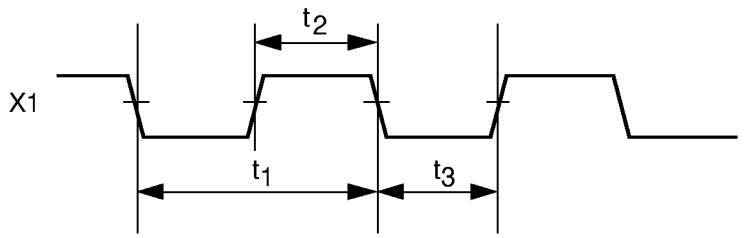
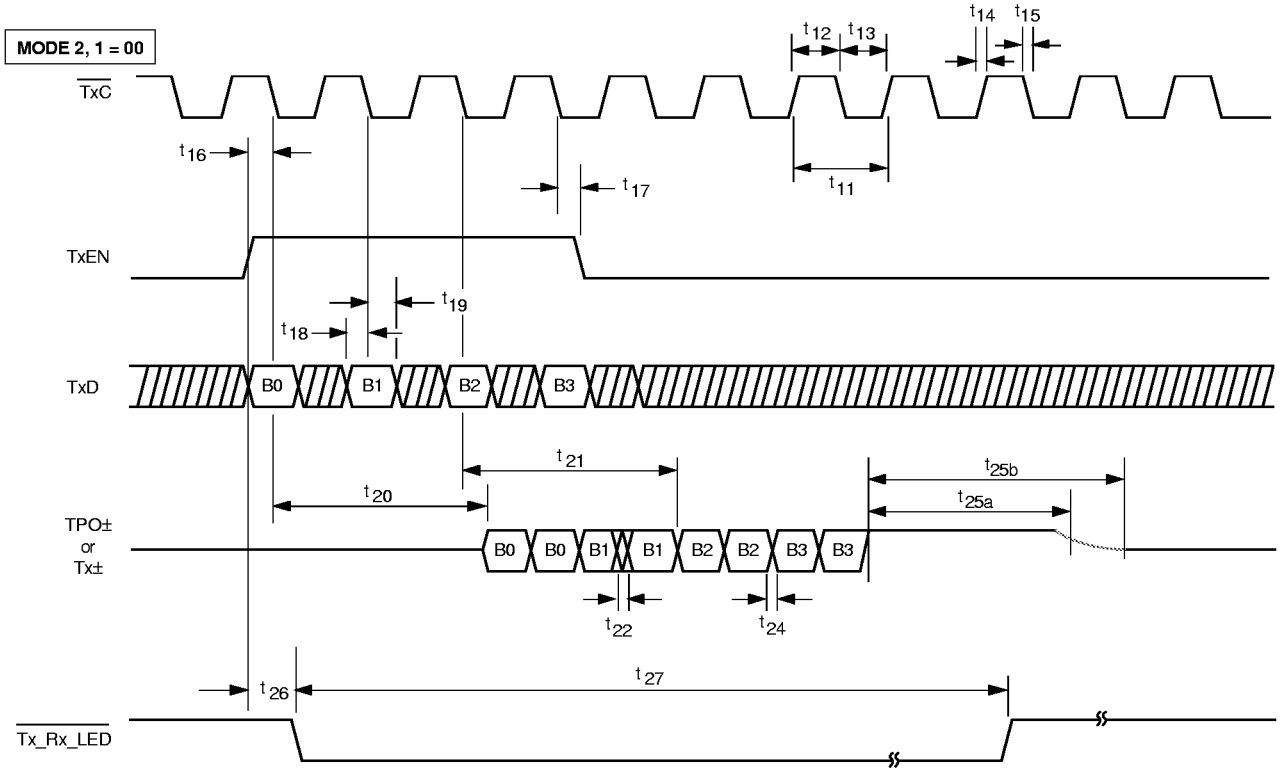


Figure 3. 20 MHZ Input Clock Timing

Transmit Timing Characteristics

Sym.	Parameter	Limit Min	Limit Typ	Limit Max	Unit	Conditions
t_{11}	$\overline{TXC}$ Cycle Time	99.99	100	100.01	nS	
t_{12}	$\overline{TXC}$ High Time	40		60	nS	
t_{13}	$\overline{TXC}$ Low Time	40		60	nS	
t_{14}	$\overline{TXC}$ Rise Time			5	nS	
t_{15}	$\overline{TXC}$ Fall Time			5	nS	
t_{16}	TXEN Setup Time	30			nS	
t_{17}	TXEN Hold Time	0			nS	
t_{18}	TXD Setup Time	30			nS	
t_{19}	TXD Hold Time	0			nS	
t_{20}	Transmit Bit Loss			2	Bits	TP and AUI
t_{21}	Transmit Propagation Delay			2	Bits	TP and AUI
t_{22}	Transmit Output Jitter			8	nS	TP
				0.5		
t_{24}	Transmit Output Rise and Fall Time	See Figure 12			nS	TP
				5	nS	AUI
t_{25A}	Transmit SOI Pulse Width to 0.3V Point	250			nS	TP Measure TPO± from last zero cross to 0.3V point.
		200			nS	AUI Measure TX± from last zero cross to 0.3V point.
t_{25B}	Transmit SOI Pulse Width to 40 mV Point			4500	nS	TP Measure TPO± from last zero cross to 40mV point.
				7000	nS	AUI Measure TX± from last zero cross to 40 mV point.
t_{26}	$\overline{TXEN}$ assert to $\overline{TX\_RX\_LED}$ assert			150	nS	
t_{27}	$\overline{TX\_RX\_LED}$ assert time	195		225	mS	Due To TX Activity

Refer to Figure 4 for timing diagram.



MODE 2, 1 = 01 SAME AS MODE [2, 1] = 00 EXCEPT $\overline{\text{TxC}}$ IS INVERTED (RISING EDGE TRIGGERED).

MODE 2, 1 = 10 SAME AS MODE [2, 1] = 00 EXCEPT TxEN IS INVERTED (ACTIVE LOW).

MODE 2, 1 = 11 SAME AS MODE [2, 1] = 00 EXCEPT $\overline{\text{TxC}}$ IS INVERTED (RISING EDGE TRIGGERED).

Figure 4. Transmit Timing

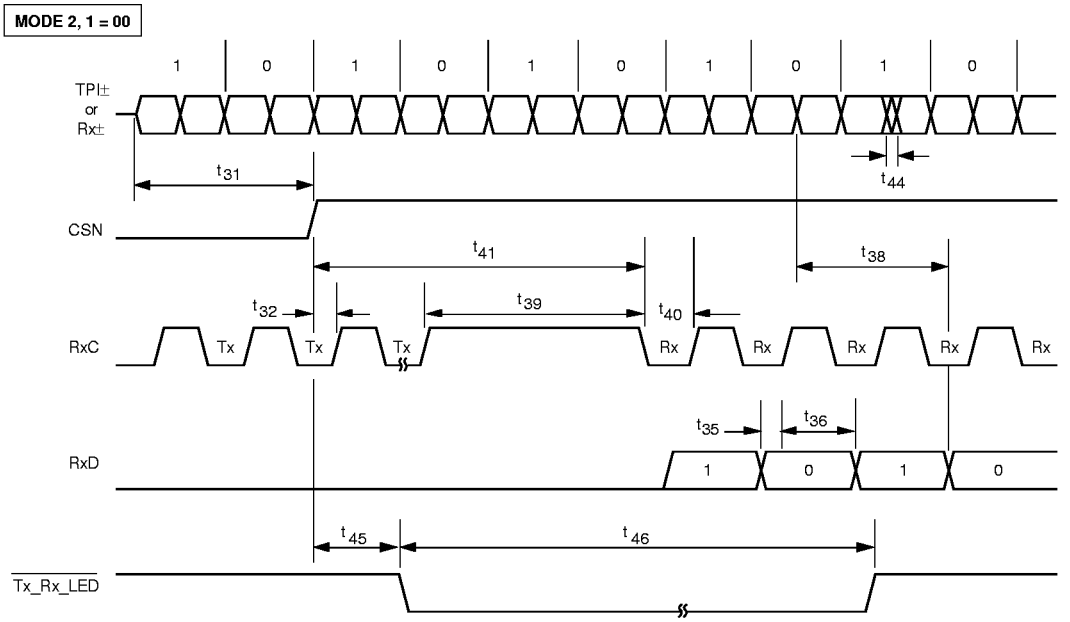
Receive Timing Characteristics

Sym.	Parameter	Limit			Unit	Conditions
		Min	Typ	Max		
t_{31}	CSN Assert Delay Time			600	nS	TP
				240	nS	AUI
t_{32}	CSN Assert Setup Time	30			nS	
t_{33}	CSN Deassert Hold Time	20			nS	Mode [2,1] = 00, 01, 11
		10		35	nS	Mode [2,1] = 10
t_{35}	RXC to RXD Setup Time	40			nS	
t_{36}	RXC to RXD Hold Time	30			nS	
t_{38}	RXD Propagation Delay			200	nS	
t_{39}	RXC High Time	40		200	nS	Mode [2,1] = 00, 01, 11
		40		60	nS	Mode [2,1] = 10
t_{40}	RXC Low Time	40		60	nS	Mode [2,1] = 00, 01, 11
		40		2200	nS	Mode [2,1] = 10 Start of Packet
		40		250	nS	Mode [2,1] = 10 End of Packet
t_{41}	CSN Assert To RXC Switchover From TX Clock To RX Clock			2200	nS	TP
				1800	nS	AUI
t_{42}	CSN Deassert To RXC Switchover From Rx Clock To Tx Clock			200	nS	
t_{43}	SOI Pulse Width Required For Idle Detection	125		200	nS	TP Measure TPI± from last zero cross to .3v point.
		125		160	nS	AUI Measure RX± from last zero cross to .45v point.
t_{44}	Receive Input Jitter			±13.5	nS	Data
				±8.5	nS	Preamble
t_{45}	CSN Assert To $\overline{\text{TX\_RX\_LED}}$ Assert			100	nS	
t_{46}	$\overline{\text{TX\_RX\_LED}}$ Assert time	195		225	mS	Due To RX Activity
t_{49}	RXC, RXD, CSN Output Rise And Fall Times			10	nS	

Refer to Figures 5 and 6 for timing diagram.

NOTES:

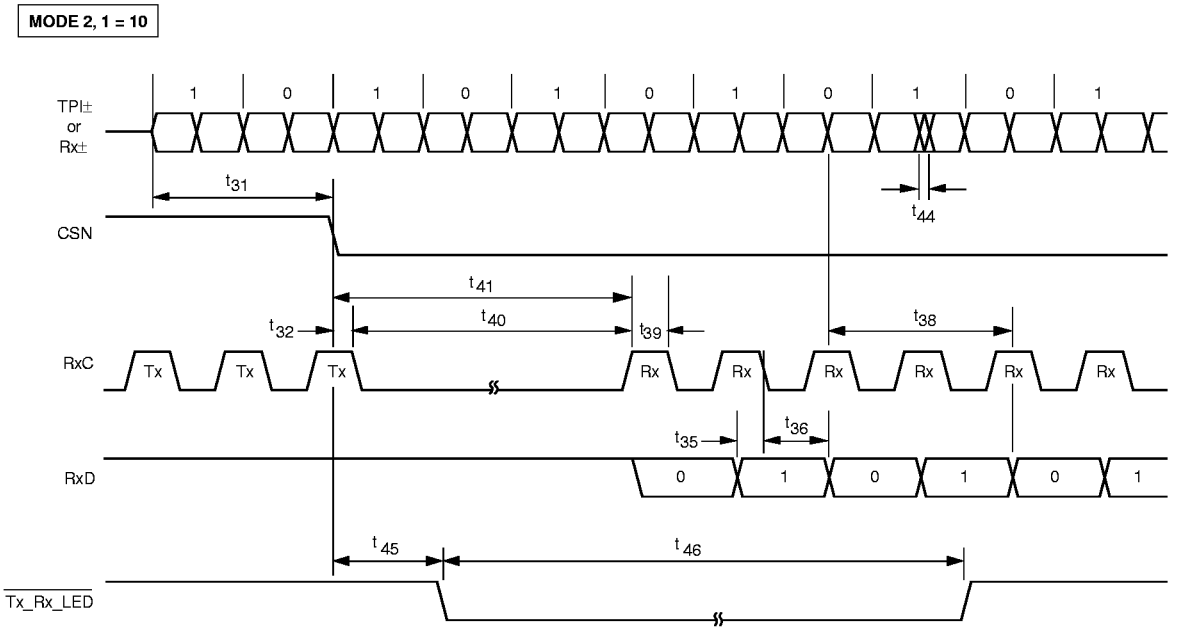
1. CI+ and CI– asserts and deasserts COLL, asynchronously, and asserts and deasserts CSN synchronously with RxC.
2. If CI+ and CI– arrives within 4.5 µs from the time CSN was deasserted; CSN will not be reasserted (on transmission node only).
3. When CI+ and CI– terminates, CSN will not be deasserted if Rx+ and Rx– are still active.
4. When the node finishes transmitting and CSN is deasserted, it cannot be asserted again for 4.5 µs.



MODE 2, 1 = 01 SAME AS MODE [2, 1] = 00

MODE 2, 1 = 11 SAME AS MODE [2, 1] = 00 AND RxC IS SHUTOFF DURING IDLE.

Figure 5a. Receive Timing — Start of Packet for SEEQ, NSC and AMD's Controllers



NOTE:
SAME AS MODE [2, 1] = 00 EXCEPT CSN IS INVERTED (ACTIVE LOW), RxC IS INVERTED (FALLING EDGE TRIGGERED), RxC IS SHUTOFF DURING t_{41} ACQUISITION TIME, RxD IS HIGH DURING t_{41} ACQUISITION TIME AND DURING IDLE TIME.

Figure 5b. Receive Timing — Start of Packet for Intel's Controllers

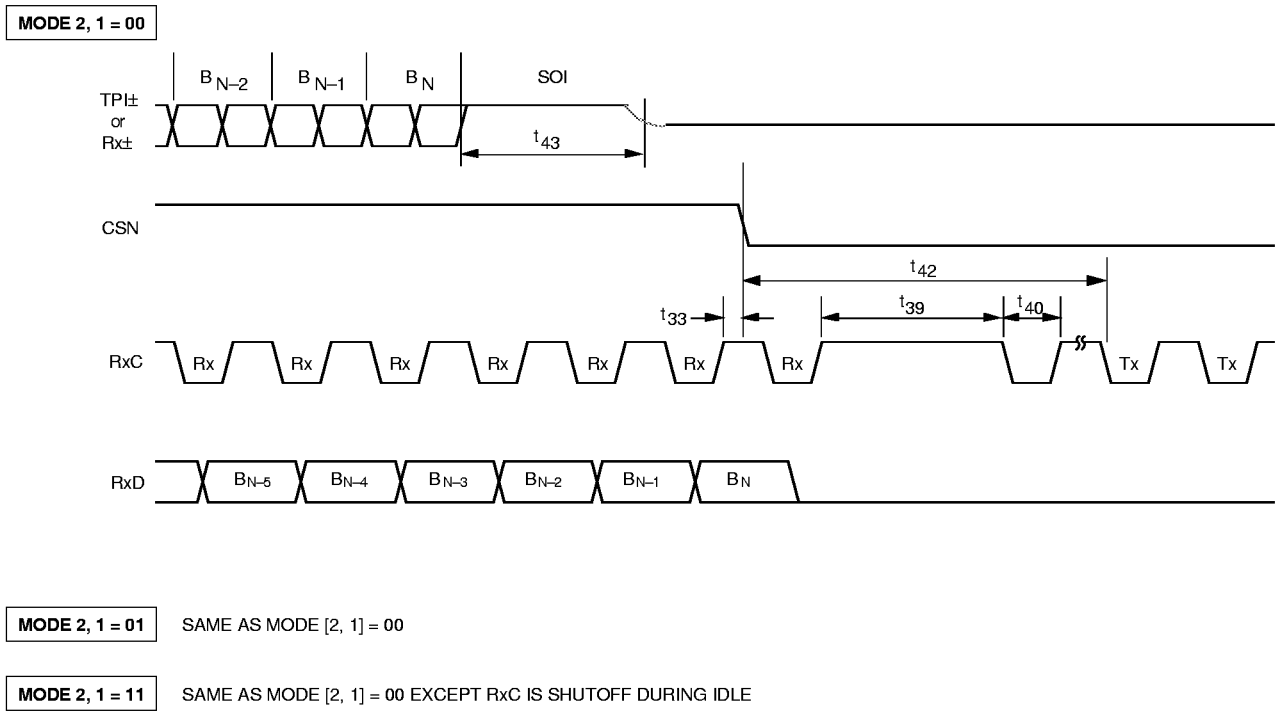
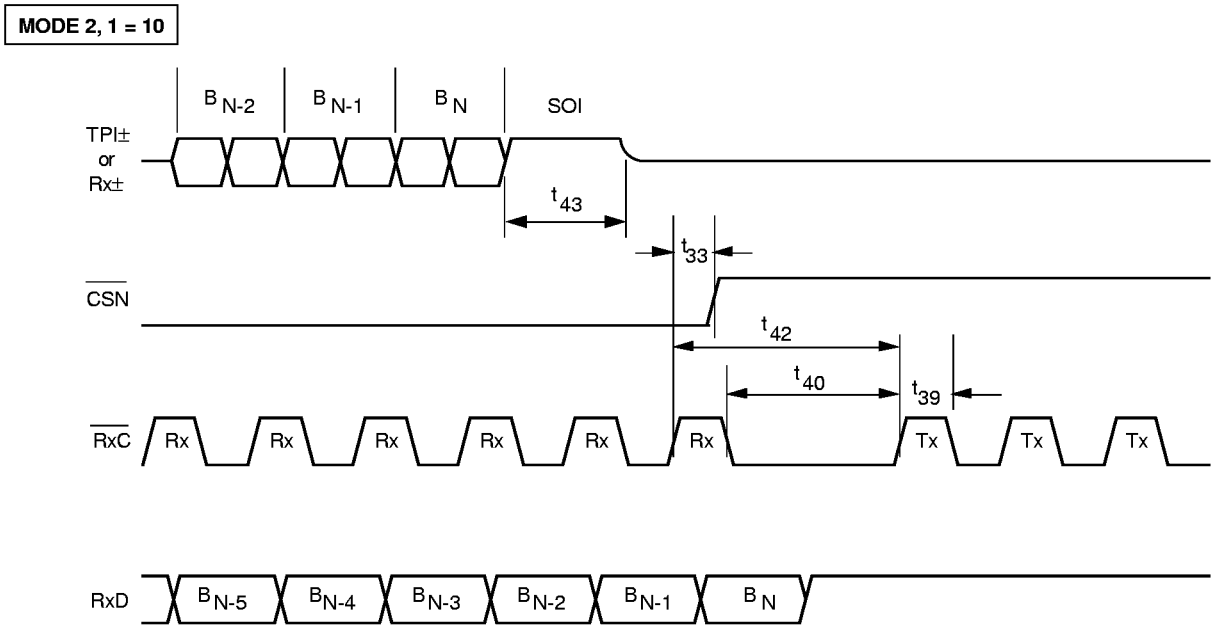


Figure 6a. Receive Timing — End of Packet for SEEQ, NSC and AMD's Controllers.



NOTE:

SAME AS MODE [2, 1] = 00 EXCEPT TxEN IS INVERTED (ACTIVE LOW), RxC IS INVERTED RxC IS SHUTOFF DURI
t_{41} ACQUISITION TIME, RxD IS HIGH DURING t_{41} ACQUISITION TIME, REFER TO FIGURE 6a.

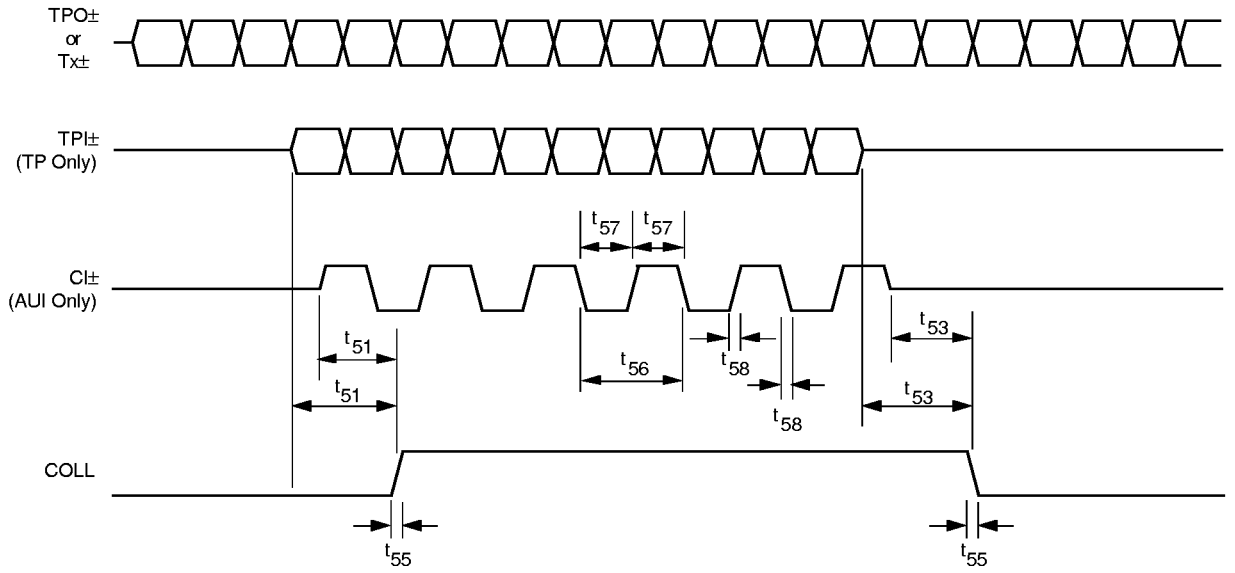
Figure 6b. Receive Timing — End of Packet for Intel's Controllers.

Collision Timing Characteristics

Sym.	Parameter	Limit			Unit	Conditions
		Min	Typ	Max		
t_{51}	COLL Assert Delay Time - Rcv After Xmt			600	nS	TP TPI± to COLL
				300	nS	AUI CI± to COLL
t_{52}	COLL Assert Delay Time - Xmt After Rcv			600	nS	TP TPO± to COLL
				300	nS	AUI CI± to COLL
t_{53}	COLL Deassert Delay Time - Rcv After Xmt			500	nS	TP TPI± to COLL
				500	nS	AUI CI± to COLL
t_{54}	COLL Deassert Delay Time - Xmt After Rcv			500	nS	TP TPO± to COLL
				500	nS	AUI CI± to COLL
t_{55}	COLL Rise And Fall Time			10	nS	
t_{56}	CI± Cycle Time	80		117	nS	
t_{57}	CI± Low Or High Time	35		70	nS	
t_{58}	CI± Rise And Fall Time			10	nS	

Refer to Figures 7 and 8 for timing diagram.

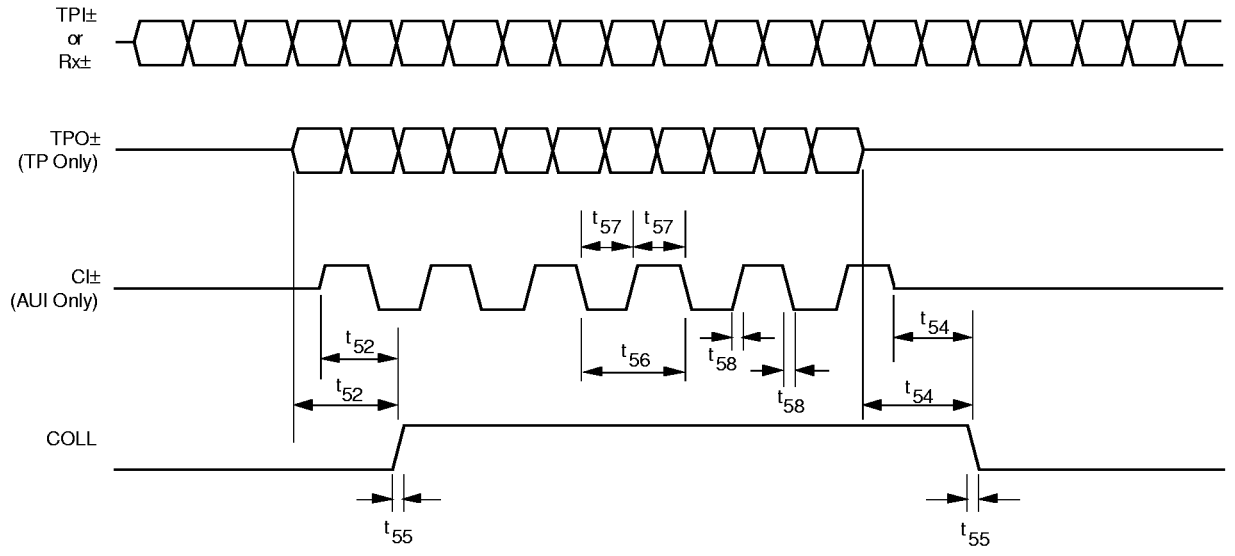
MODE 2, 1 = 00, 01, 11



MODE 2, 1 = 10 SAME AS MODE [2, 1] = 00 EXCEPT COLL IS INVERTED (ACTIVE LOW)

Figure 7. Collision Timing — Receive After Transmit

MODE 2, 1 = 00, 01, 11



MODE 2, 1 = 10 SAME AS MODE 2, 1 = 00 EXCEPT COLL IS INVERTED (ACTIVE LOW)

Figure 8. Collision Timing — Transmit After Receive

Link Pulse Timing Characteristics

Sym.	Parameter	Limit			Unit	Conditions
		Min	Typ	Max		
t_{61}	Transmit Link Pulse Width	75		125	nS	
t_{62}	Transmit Link Pulse Period	11		15	mS	
t_{63}	Transmit Link Pulse To Double Link Pulse Spacing	5.0	5.2	5.4	µS	Full Duplex Mode Signalling
t_{64}	Transmit Double Link Pulse Interval Spacing	16		16	Link Pulses	Full Duplex Mode Signalling
t_{65}	Receive Link Pulse Width Required For Detection	35		200	nS	
t_{66}	Receive Link Pulse Minimum Period Required For Detection	2	4	7	mS	Link_Test_Min
t_{67}	Receive Link Pulse Maximum Period Required For Detection	50		150	mS	Link_Loss and Link_Test_Max
t_{68}	Receive Link Pulse To Double Link Pulse Spacing Required For Full Duplex Mode Detection	4.8		5.6	µS	Full Duplex Mode Detection
t_{69}	Receive Double Link Pulse Minimum Period Required For Full Duplex Mode Detection	204	210	216	mS	Full Duplex Mode Detection
t_{70}	Receive Double Link Pulse Maximum Period Required for Full Duplex Detection	750		850	mS	Full Duplex Detection Mode
t_{71}	Receive Link Pulse Assert	2	3	10	Link Pulses	
t_{72}	Receive Full Duplex Assert			7	µS	Full Duplex Mode Detection

Refer to Figure 9 for timing diagram.

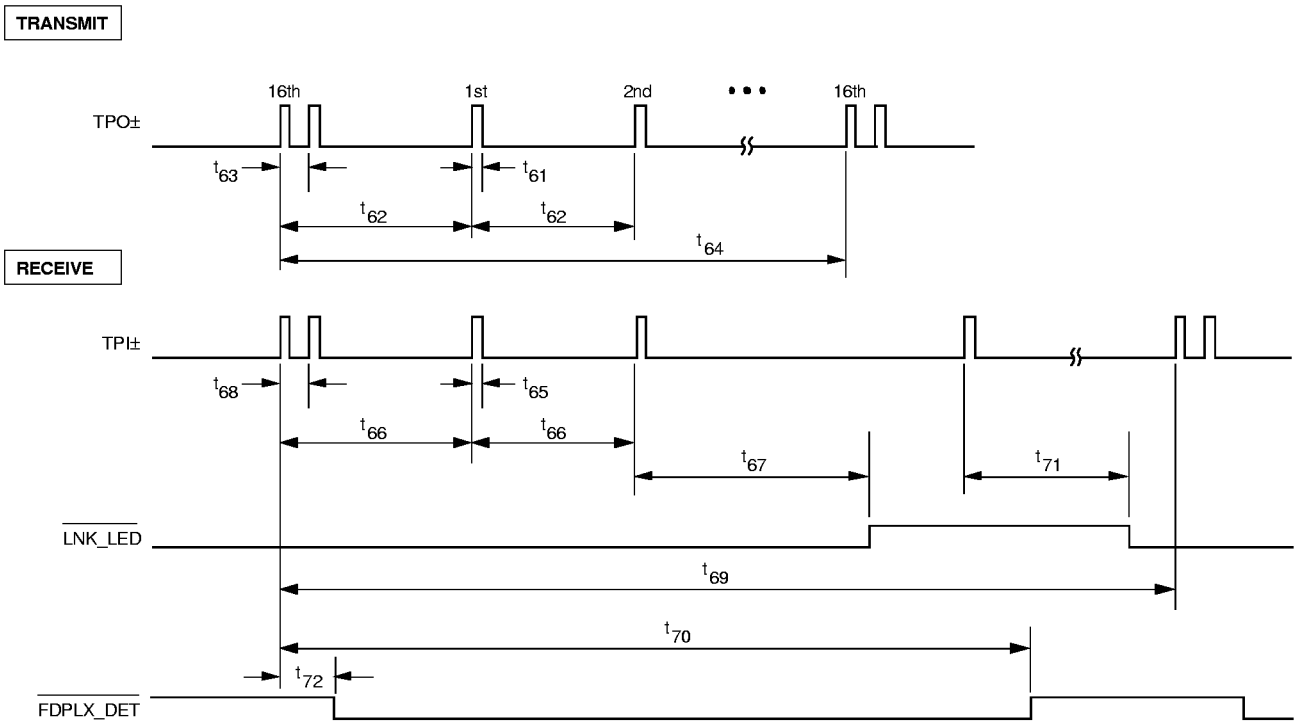


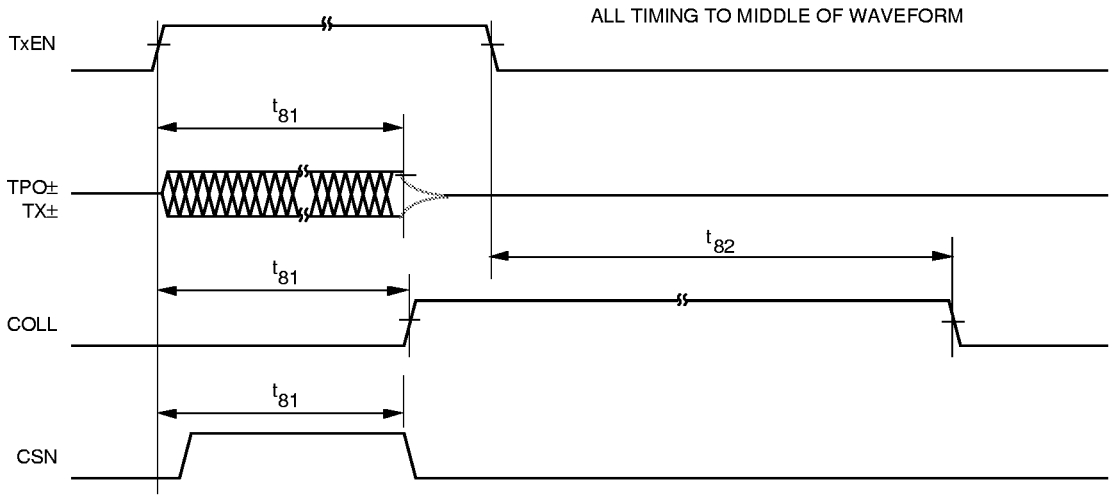
Figure 9. Link Pulse Timing

Jabber Timing Characteristics

Sym.	Parameter	Limit			Unit	Conditions
		Min	Typ	Max		
t_{81}	Jabber Activation Time	40		60	mS	TP and AUI
t_{82}	Jabber Deactivation Time	400		430	mS	TP and AUI

Refer to Figure 10 for timing diagram

MODE 2,1 = 00



MODE 2,1 = 01 SAME AS MODE 2, 1 = 00

MODE 2,1 = 10 SAME AS MODE 2, 1 = 00 EXCEPT COLL IS INVERTED (ACTIVE LOW), CSN IS INVERTED, AND TxEN IS INVERTED.

MODE 2,1 = 11 SAME AS MODE 2, 1 = 00

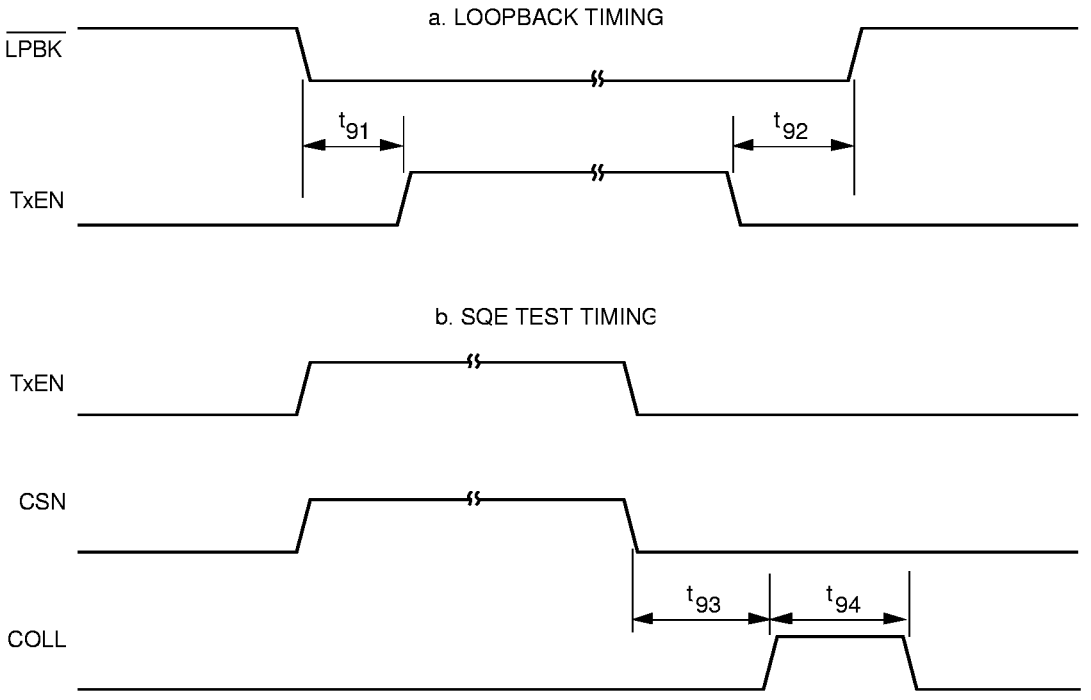
Figure 10. Jabber Timing

Loopback/SQE Timing Characteristics

Sym.	Parameter	Limit			Unit	Conditions
		Min	Typ	Max		
t_{91}	$\overline{\text{LPBK}}$ Setup Time	5			µS	AUI Only
t_{92}	$\overline{\text{LPBK}}$ Hold Time	5			µS	AUI Only
t_{93}	SQE Pulse Delay	600		700	nS	
t_{94}	SQE Pulse Width	750		850	nS	

Refer to Figure 11 for timing diagram.

MODE 2,1 = 00



MODE 2,1 = 01 SAME AS MODE [2, 1] = 00 EXCEPT $\overline{\text{LPBK}}$ INVERTED (ACTIVE HIGH)

MODE 2,1 = 10 SAME AS MODE [2, 1] = 00 EXCEPT TxEN INVERTED, CSN INVERTED

MODE 2,1 = 11 SAME AS MODE [2, 1] = 00 EXCEPT $\overline{\text{LPBK}}$ INVERTED (ACTIVE HIGH)

Figure 11. Loopback/SQE Test Timing

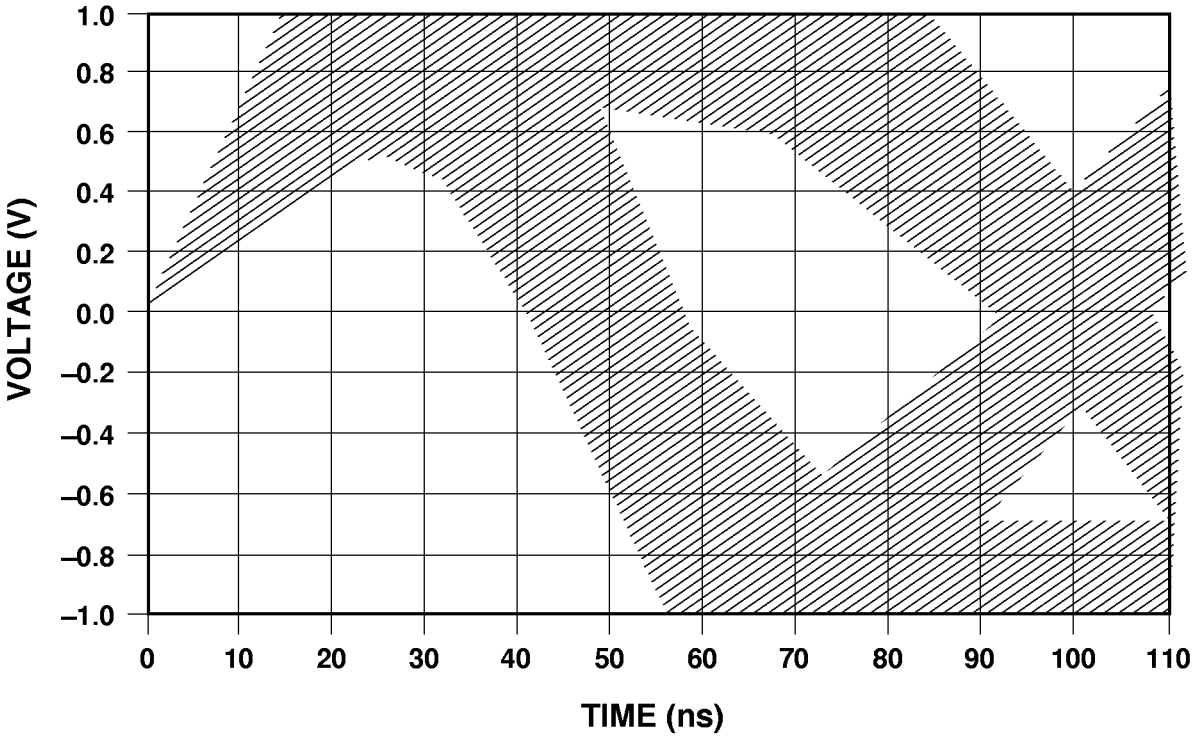
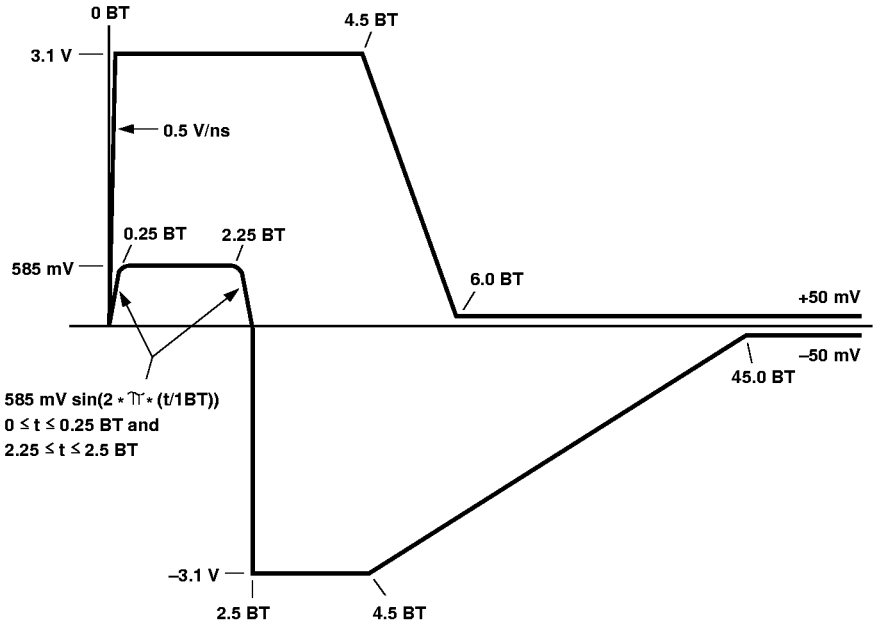
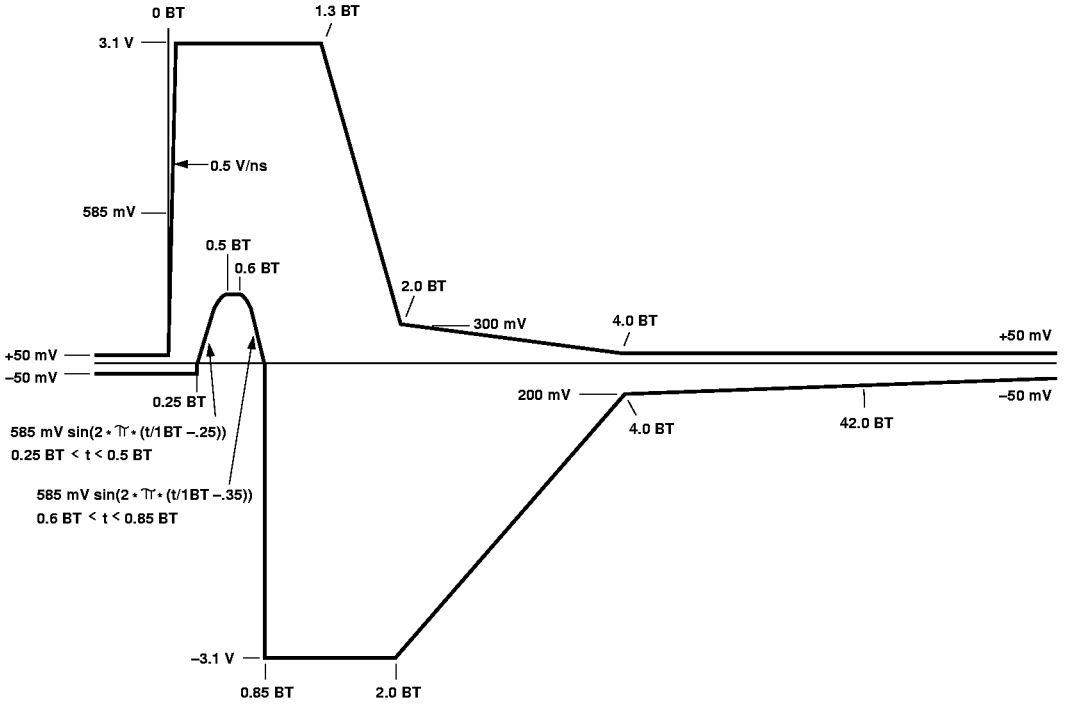


Figure 12. Twisted Pair Output Voltage Template with Line Model.



With and Without Line Model

Figure 13. Transmit Start of Idle Pulse Voltage Template

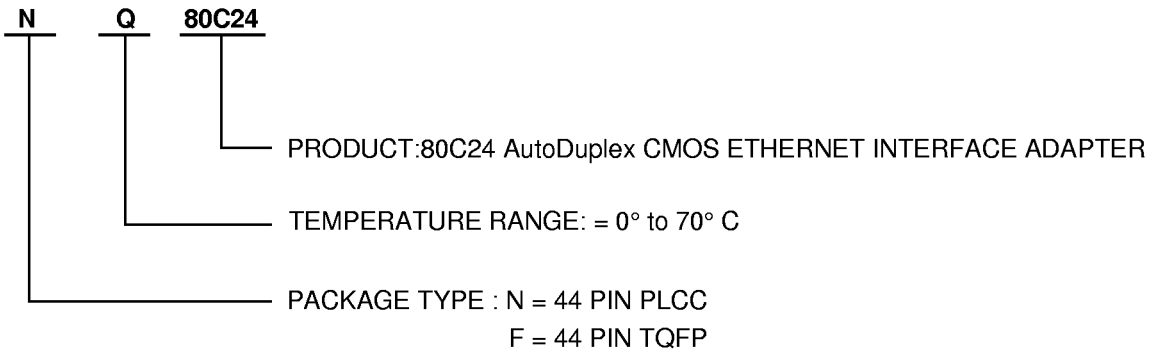


With and Without Line Model

Figure 14. Transmit Link Pulse Voltage Template

Ordering Information

PART NUMBER



Revision History

4/15/96

- All references to separate 'digital' and 'analog' power and grounds deleted.
- There are four sets of V_{CC}/GND on the 80C24: V_{CC1}/GND_1, V_{CC2}/GND_2,V_{CC3}/GND_3, and V_{CC4}/GND_4.
- Page 9, Power Supply Decoupling suggestions added to page.
- Page 12, DC Digital I/O Characteristics: V_{OL} (max) changed from 0.8 to 1.2 V.
- Page 15, AUI Characteristics: AOCD (max) changed from Vcc/2.5 to Vcc/2.1.
- Page 31, Table replaced with addendum dated April 1995.

9/9/96

- Pages 33, 34, PLCC and TQFP dimension diagrams have been added to this data sheet.

12/10/96

- Pages 17, Transmit Timing Characteristics, TXEN Hold Time (min.) has been changed from 40 to 0.

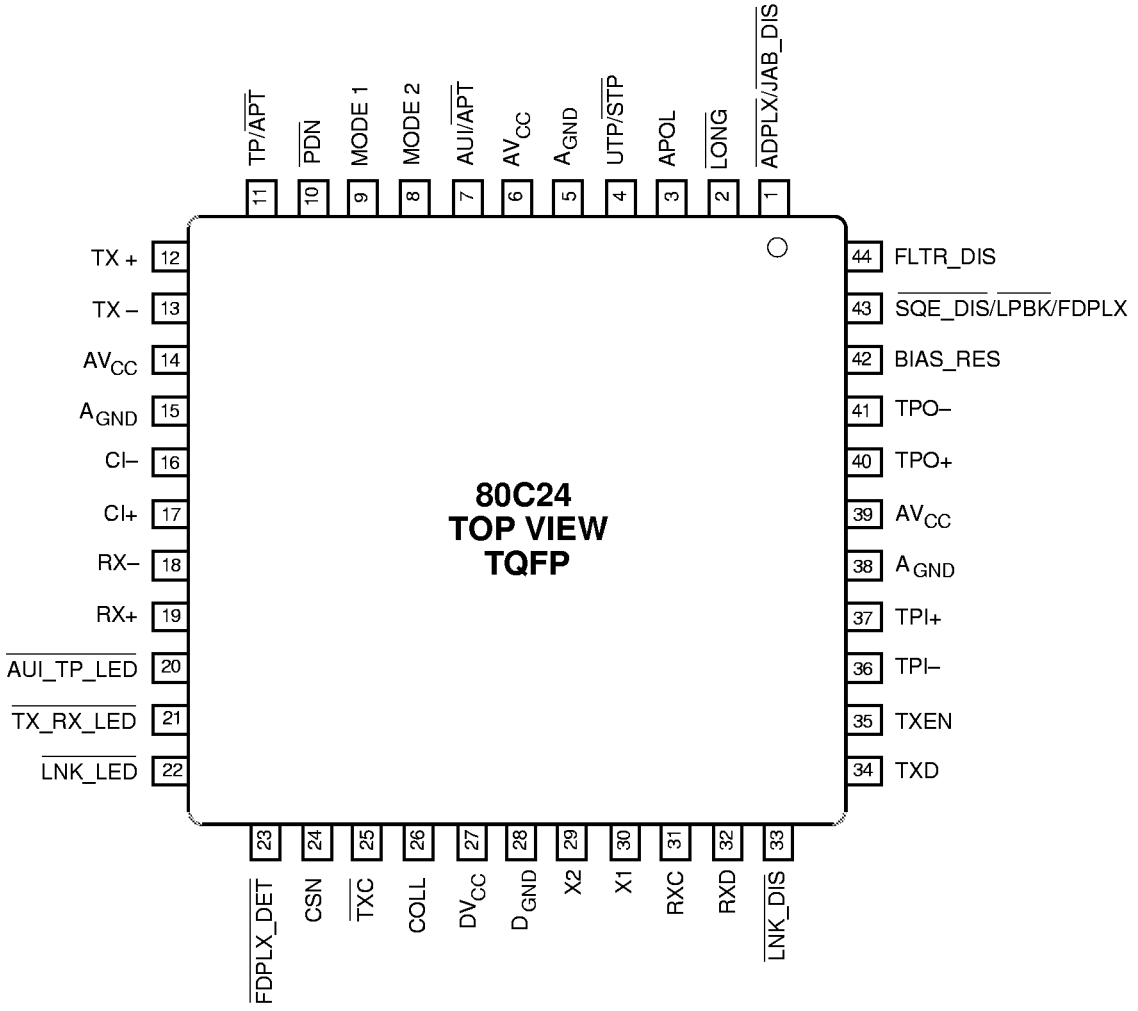
Mode Port Select Table

This Mode/Port Select Table lists out all the possible pin combinations and describes the corresponding features that are enabled in those combinations.

			INPUTS					FEATURES						
PORT GROUP		**SYMBOL**	**AUI/$\overline{APT}$ (2)**	**$\overline{ADPLX}$/$\overline{JAB\_DIS}$ (40)**	**$\overline{LNK\_DIS}$ (28)**	**$\overline{SQE\_DIS}$/$\overline{LPBK}$/FDPLX (38)**	**TP/$\overline{APT}$ (6)**	**PORT**	**JABBER**	**LINK TEST**	**SQET**	**AUTO FDX**	**FDX**	**LOOPBACK**
AUTOPORT		Apt 1	L	H	H	H	L	TP	✔	✔	✔			
								AUI	✔	✔				
To Enable Autoport Pins 2, 6 -- L & Pin 28 -- H		Apt 2	L	H	H	L	L	TP	✔	✔				
								AUI	✔	✔				
Pins 40 & 38 Can Be Varied to Have Features as Desired.		Apt 3	L	L	H	H	L	TP FDX	✔	✔		✔		
								NFDX	✔	✔	✔	✔		
								AUI	✔	✔				
		Apt 4	L	L	H	L	L	TP FDX	✔	✔		✔		
								NFDX	✔	✔		✔		
								AUI	✔	✔				
Auto Port Forced Full Duplex Mode[1]		Apt 5	L	H	L	H	L		✔	✔			✔	
		Apt 6	L	L	L	H	L			✔			✔	
TP ONLY		TP 1	L	H	H	H	H		✔	✔	✔			
		TP 2	L	H	H	L	H		✔	✔				
TP Only Mode Pin 2 -- L & Pin 6 -- H		TP 3	L	L	H	H	H	FDX	✔	✔		✔		
								NFDX	✔	✔	✔	✔		
Pins 40, 28 & 38 Can Be Varied to Have Features as Desired.		TP 4	L	L	H	L	H	FDX	✔	✔		✔		
								NFDX	✔	✔		✔		
		TP 5	L	H	L	H	H		✔		✔			
		TP 6	L	H	L	L	H		✔					
		TP 7	L	L	L	H	H				✔			
		TP 8	L	L	L	L	H							
Forced Full Duplex		TP 9	L	H	L	L	L		✔				✔	
		TP 10	L	L	L	L	L						✔	
AUI ONLY		AUI 1	H	H	H	H[3]	X		✔					
AUI Only Mode Pin 2 -- H Pins 40 Can Be Varied.		AUI 2	H	L	H	H[3]	X							
		AUI 3	H	H	L	H[3]	X		✔				✔	
Pin 38 -- H[3]		AUI 4	H	L	L	H[3]	X						✔	
LOOPBACK	Intel & SEEQ Mode	LPBK 1	H	H	X	L	X		✔		✔			✔[2]
Loopback Mode Pin 2 -- H, Pin 38 -- L Pin 40 Can Be Varied.		LPBK 2	H	L	X	L	X				✔			✔[2]
	AMD & National	LPBK 3	H	H	X	H	X		✔		✔			✔[2]
		LPBK 4	H	L	X	H	X				✔			✔[2]

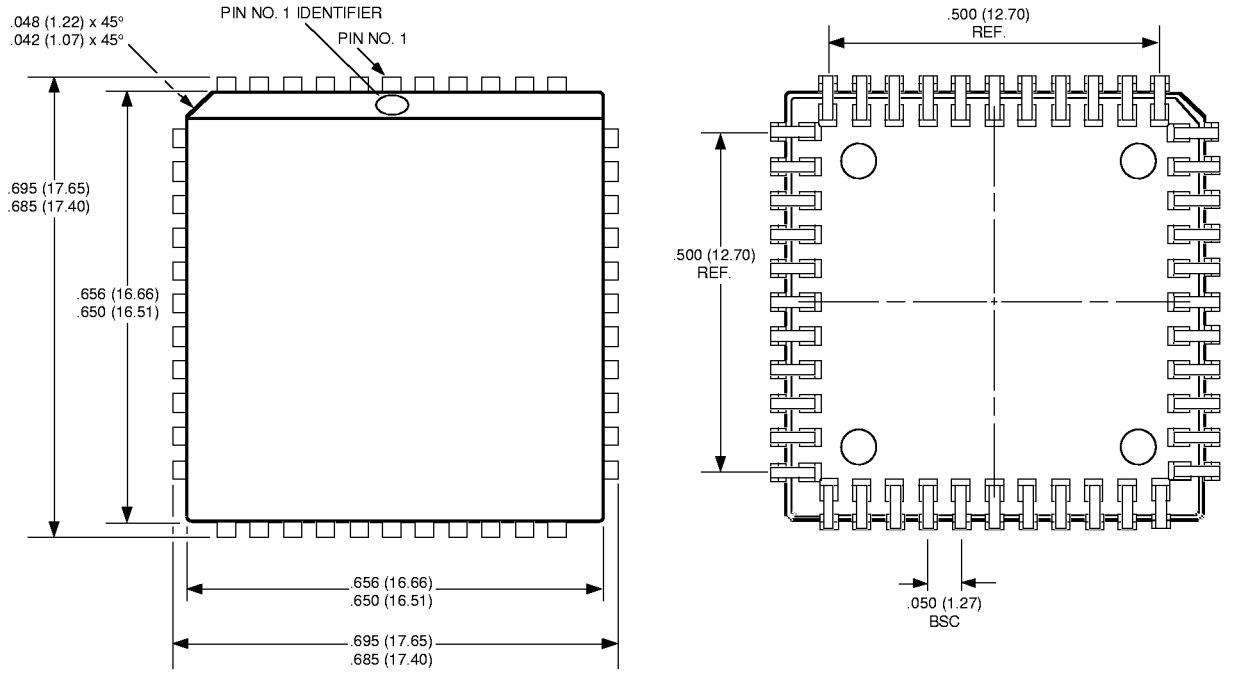
Notes:
[1]. Note that the link presence is indicated even though the LNK_DIS is Low.
[2]. Internal.
[3]. Values shown for pin (38) are for Intel & SEEQ mode. Reverse the polarity for the AMD & National Mode.

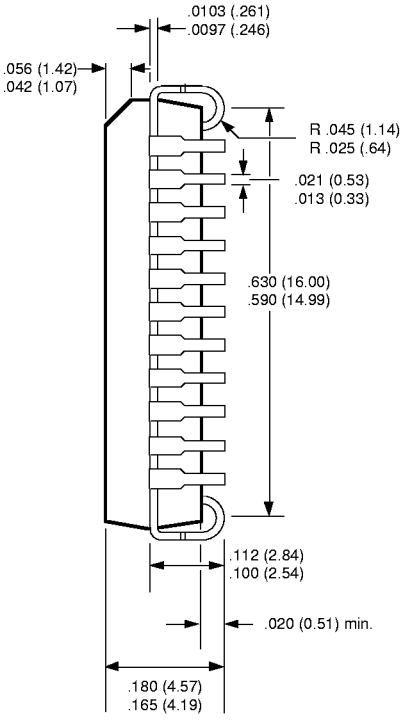
Pin Configuration



Surface Mount Packages

44 Pin Plastic Leaded Chip Carrier Type N

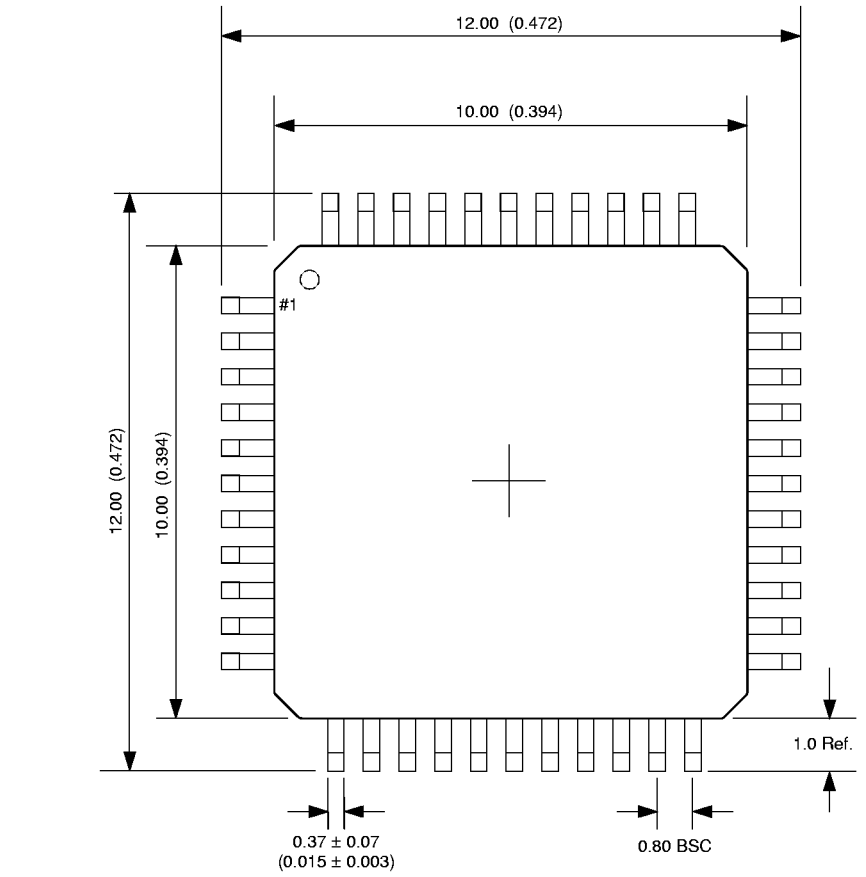


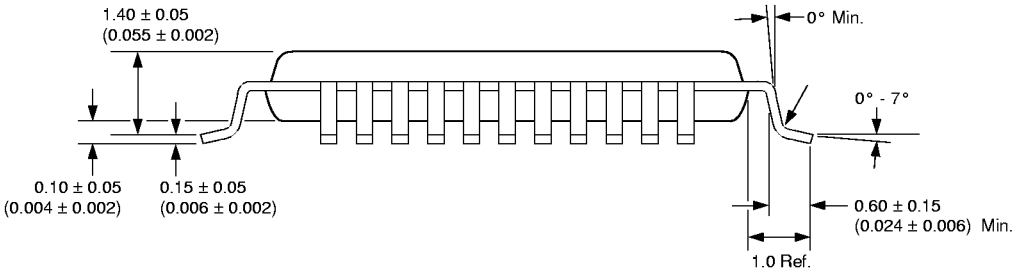


Notes

1. **All dimensions are in inches and (millimeters).**
2. **Dimensions do not include mold flash. Maximum allowable flash is .008 (.20).**
3. **Formed leads shall be planar with respect to one another within 0.004inches.**

44-Pin TQFP





Notes
1. **All dimensions are in inches and (millimeters).**
2. **Dimensions do not include mold flash. Maximum allowable flash is .01 (.254).**