CA1391, CA1394

TV Horizontal Processors

CA1391E – Positive Horizontal Sawtooth Input
CA1394E – Negative Horizontal Sawtooth Input

Features:

- **Internal shunt regulator**
- **Linear balanced phase detector**
- **Preset hold control capability**
- **±300-Hz pull-in (typ.)**
- **Low thermal frequency drift**
- **Small static phase error**
- **Variable output duty cycle**
- **Adjustable dc loop gain**

The RCA-CA1391E and CA1394E are monolithic integrated circuits designed for use in the low-level horizontal section of monochrome or color television receivers. Functions include a phase detector, an oscillator, a regulator, and a pre-driver.

The CA1391E and CA1394E are electrically equivalent and pin compatible with industry types 1391 and 1394 in similar packages.

These types are supplied in an 8-lead dual-in-line plastic (Mini-DIP) package, and operate over an ambient temperature range of 0 to +85°C.

MAXIMUM RATINGS, *Absolute-Maximum Values at* $T_A = 25^oC$

DC SUPPLY CURRENT	40 mA
DC OUTPUT VOLTAGE	40 V
DC OUTPUT CURRENT	30 mA
SYNC INPUT VOLTAGE	5 V_{p-p}
SAWTOOTH INPUT VOLTAGE	5 V_{p-p}
DEVICE DISSIPATION:	
Up to $T_A = 25^oC$	625 mW
Above $T_A = 25^oC$ derate linearly	5 mW/°C
AMBIENT TEMPERATURE RANGE:	
Operating	0 to +85°C
Storage	−65 to +150°C
LEAD TEMPERATURE (During Soldering):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 seconds max.	+260°C
THERMAL RESISTANCE	200°C/W

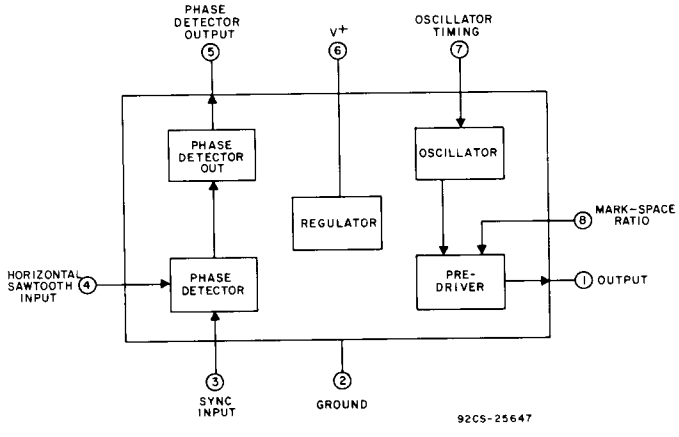

Fig.1 – Functional block diagram of the CA1391E, CA1394E.

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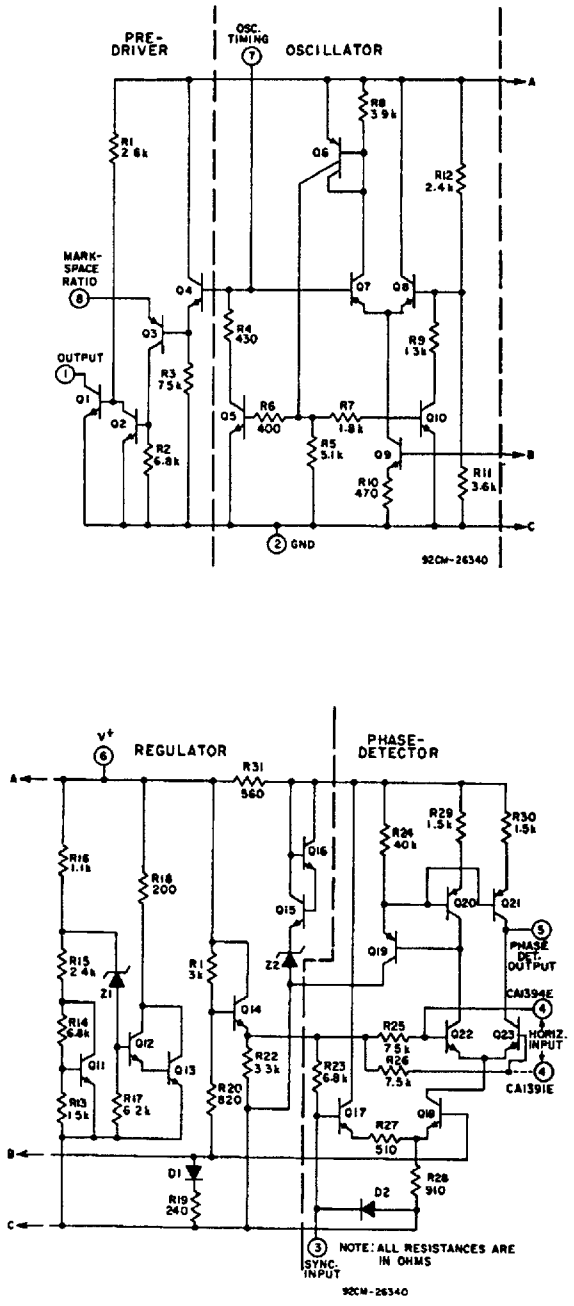

Fig.2 – Schematic diagram of CA1391E, CA1394E.

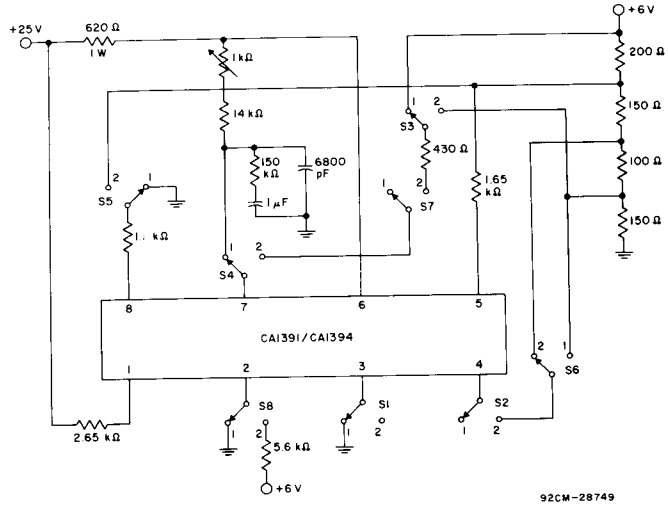

Fig.3 – DC test circuit.

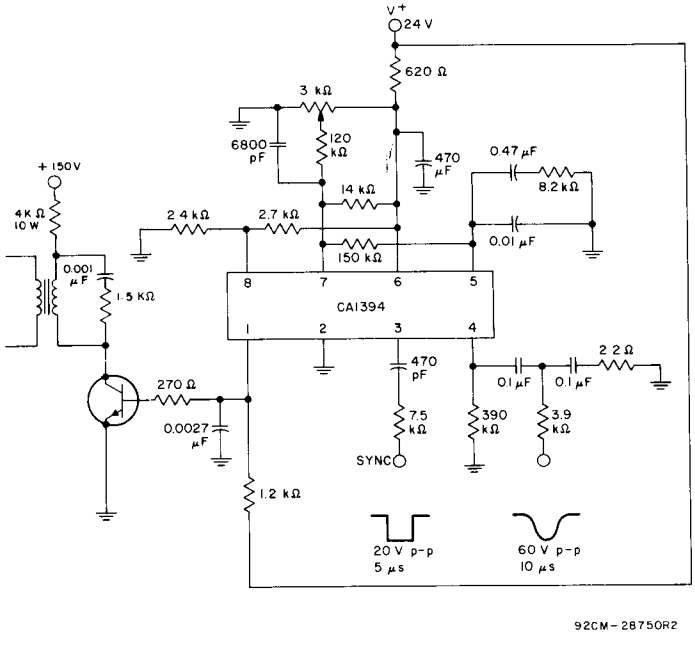

Fig.4 – Typical circuit application.

ELECTRICAL CHARACTERISTICS at T_A = 25°C (See Fig.3)

CHARACTERISTIC	TEST CONDITIONS	LIMITS			UNITS
		Min.	Typ.	Max.	
Supply Voltage	S1, S5, S6 = 2 S2, S3, S4, S7, S8 = 1 Measure term. 6 to Gnd	8	–	9	V
Free-Running Frequency	S1, S5, S6 = 2 S2, S3, S4, S7, S8 = 1 Counter to term. 1	14734	–	16734	Hz
Output Leakage	S2, S3, S6, S8 = 1 S1, S4, S5, S7 = 2 Measure term. 1 to 25 V	–	10	–	mV
Output Saturation	S2, S3, S5, S6, S8 = 1 S1, S4, S7 = 2 Measure term. 1 to Gnd	–	60	–	mV
Phase Detector Bias	S2, S5, S6, S8 = 1 S1, S3, S4, S7 = 2 Measure term. 3 to Gnd	–	1.9	–	V
Phase Detector Leak	S5, S8 = 1 S1, S2, S3, S4, S6, S7 = 2 Measure term. 5 to +4 V	−2	–	+2	mV
Phase Detector Low	S1, S5, S8 = 1 S2, S3, S4, S6, S7 = 2 Measure term. 5 to +4 V	−0.55*	–	–	V
Phase Detector High	S1, S5, S6, S8 = 1 S2, S3, S4, S7 = 2 Measure term. 5 to +4 V	+0.55*	–	–	V
Phase Detector Balance	$V_{DET2} + V_{DET3}$	−100	–	+100	mV
Sync Diode	S1, S2, S3, S4, S6, S7 = 1 S5, S8 = 2	0.3	–	1.2	V
Static Phase Error	See Fig.4	–	0.5	–	μs
Oscillator Pull-in Range		–	±300	–	Hz
Oscillator Hold-in Range		–	±900	–	Hz

* Polarity reversed in the CA1391.

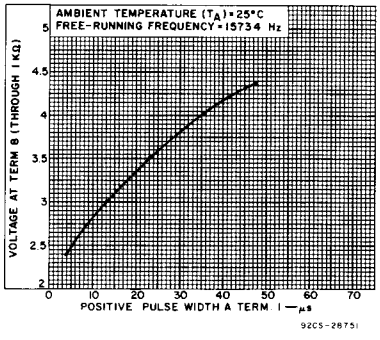

Fig.5 – Duty cycle at the pre-drive output (term.1) as it is affected by the input at term. 8.

CA1391, CA1394

CIRCUIT OPERATION

(See schematic diagram, Fig.2)

The CA1391 and CA1394 contain the oscillator, phase detector, and predriver sections necessary for the television horizontal oscillator and AFC loop.

The oscillator is an RC type with terminal 7 used to control the timing. If it is assumed that Q7 is initially off, then an external capacitor connected from terminal 7 to ground charges through an external resistance connected between terminals 6 and 7. As soon as the voltage at terminal 7 exceeds the potential set at the base of Q8 by resistors R11 and R12, Q7 turns on, and Q6 supplies base current to Q5 and Q10. Transistor Q5 discharges the capacitor through R4 until the base bias of Q7 falls below that of Q8, at which time, Q7 turns off, and the cycle repeats.

The sawtooth generated at the base of Q4 appears across R3 and turn off Q3 whenever the sawtooth voltage rises to a value that exceeds the bias set at terminal 8. By adjusting the potential at terminal 8, the duty cycle at the pre-drive output (terminal 1) may be changed.

The phase detector is isolated from the remainder of the circuit by R31, Z2, Q15 and Q16. The phase detector consists of the comparator Q22 and Q23, and the gated current source Q18. Negative-going sync pulses at terminal 3 turn off Q17, and the current division between Q22 and Q23 is then determined by the phase relationship of the sync and the sawtooth waveform at terminal 4, which is derived from the horizontal flyback pulse. If there is no phase difference between the sync and sawtooth, equal currents flow in the collectors of Q22 and Q23 during each half of the sync pulse period. The current in Q22 is turned around by current mirror Q20 and Q21 so that there is no net output current at terminal 5 for balanced conditons. When a phase offset occurs, current flows either in or out of terminal 5. In circuit applications, this terminal is connected to terminal 7 through an external low-pass filter, thereby controlling the oscillator.

Shunt regulation for the circuit is obtained by using a V_{BE} and zener multiplier. Resistors R13 and R14 multiply the V_{BE} of Q11, and the ratio of R15 and R16 multiplies the voltage of the zener diode Z1.