National Semiconductor

TBA920/TBA920S Line Oscillator Combination

General Description

The TBA920 is a monolithic integrated circuit intended for TV receivers with transistor-thyristor- or valve equipped output stages.

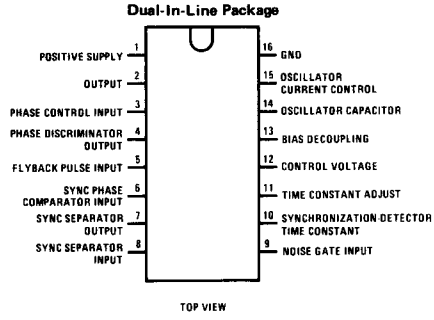
It combines the following functions:

- Noise gated sync separator
- Phase comparison between sync pulse and oscillator
- Line oscillator
- Loop gain and time constant switching (also for video recorder applications)
- Phase comparison between line-flyback pulse and oscillator
- Output stage for driving a variety of line output stages

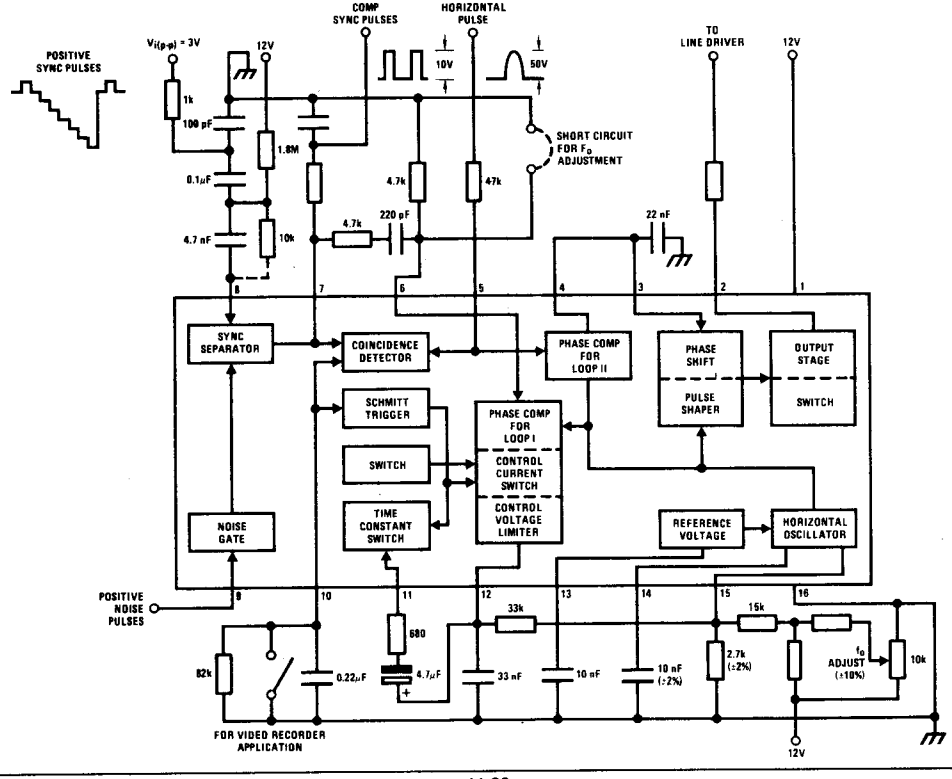
Connection Diagram

Dual-In-Line Package, Order Number TBA920 or TBA920S
See NS Package N16A

Quad-In-Line Package, Order Number TBA920Q
See NS Package N16C



Typical Application



Absolute Maximum Ratings

V1-16	13.2V	Operating Temperature Range	−20°C to +60°C
I_2 (Mean)	20 mA	Storage Temperature Range	−65°C to +150°C
I_2 (Peak)	200 mA	Lead Temperature (Soldering, 10 seconds)	300°C
I_5, I_7, I_9	10 mA	Power Dissipation (T_A = 60°C)	600 mW

Electrical Characteristics at V1-16 = 12V, T_A = 25°C as measured in application circuit

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
	Current Consumption					
I_1		I_2 = 0		36		mA
	Video Signal					
V1	Input Voltage Range		1		7	Vp-p
I_Q	Input Current During Sync Pulse			100		µA
	Noise Gating (Pin 9)					
V9-16	Input Voltage (Peak Value)		0.7			V
I_9	Input Current (Peak Value)		0.03		10	mA
	Flyback Pulse (Pin 5)					
V5-16	Input Voltage (Peak Value)			±1		V
I_5	Input Current (Peak Value)		0.05	1		mA
R5-16	Input Resistance			400		Ω
t_5	Pulse Duration at 15,625 Hz		10			µs
	Composite Sync Pulses (Positive: Pin 7)					
V7-16	Output Voltage			10		Vp-p
	Output Resistance					
R7-16	At Leading Edge of Pulse (Emitter Follower)			50		Ω
R7-16	At Trailing Edge			2.2		kΩ
R7-16 (ext)	Additional External Load Resistance		2			kΩ
	Driver Pulse (Pin 2)					
V2-16	Output Voltage			10		Vp-p
I_2	Average Output Current				20	mA
I_2	Peak Output Current				200	mA
t_2	Output Pulse Duration When Synchronized		12		32	µs
$t_{o\ tot}$	Permissible Delay Between Leading Edge of Output Pulse and Flyback Pulse at t_5 = 12µs		0		15	µs
V1-16	Supply Voltage at Which Output Pulses are Obtained		4			V
	Oscillator					
f_o	Frequency; Free Running	R15-16 = 3.3 kΩ, (Note 1)		15,625		Hz
$\frac{\Delta f_o}{f_o}$	Spread of Frequency at Nominal Values of Peripheral Components				±5	%
$\left\|\frac{\Delta f_o}{f_o}\right\|$	Frequency Change When Decreasing the Supply Down to Minimun 4V				10	%
$\frac{\delta f_o}{f_o} / \frac{\delta V_P}{V_{Pnom}}$	Influence of Supply Voltage on Frequency at Vp = 12V				5	%
$\delta f_o/\delta I_{15}$	Frequency Control Sensitivity			16.5		Hz/µA
	Control Loop I (Between Sync Pulse and Oscillator)					
V12-16	Control Voltage Range		0.8		5.5	V
	Control Current (Peak Values)					
I_{12M}		V10-16 > 4.5V, V6-16 > 1.5V		±2		mA
I_{12M}		V10-16 < 2V, V6-16 > 1.5V		±6		mA

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Electrical Characteristics (Continued)

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
	Loop Gain of APC System					
$\frac{\Delta f}{\Delta t}$	Time Coincidence Between Sync Pulse and Flyback Pulse or V10-16 > 4.5V			1		kHz/μs
$\frac{\Delta f}{\Delta t}$	No Time Coincidence or V10-16 < 2V			3		kHz/μs
Δf	Catching and Holding Range	(Note 2)		±1		kHz
t	Pull-in Time	$\Delta f/f_o$ = ±3% (Δf = 470 Hz)		20		ms
t	Switch-over From Large Control Sensitivity to Small Control Sensitivity After Catching			20		ms
	Control Loop II (Between Flyback Pulse and Oscillator)					
$t_{d\ tot}$	Permissible Delay Between Leading Edge of Output Pulse (Pin 2) and Leading Edge of Flyback Pulse		0		15	μs
$\frac{\Delta t}{\Delta t_d}$	Static Control Error	(Note 3)			0.5	%
	Overall Phase Relation					
t	Phase Relation Between Leading Edge of Sync Pulse and Middle of Flyback Pulse	(Note 4)		4.9		μs
$\lvert\Delta t\rvert$	Tolerance of Phase Relation	(Note 5)			1	μs
$\frac{\Delta f}{f_o}$	Spread of Frequency at Nominal Values of Peripheral Components					
	TBA920				±5	%
	TBA920S				±2	%
V3-16	Voltage	t_2 = 12μs		6		V
V3-16		t_1 = 32μs		8		V
I_3	Input Current				2	μA
	Time Constant Switch Voltage on Pin 10					
V10-16		For Internal R11 = 150Ω	4.5			V
V10-16		For Internal R11 = 2 kΩ			2	V

Note 1: The oscillator frequency can be changed for other TV standards by an appropriate value of C14-16.

Note 2: Adjustable with R12-15.

Note 3: The control error is the remaining error in reference to the nominal phase position between leading edge of the sync pulse and the middle of the flyback pulse caused by a variation in delay of the line output stage.

Note 4: This phase relation assumes a luminance delay line with a delay of 500 ns between the input of the sync separator and the drive to the picture tube. If the sync separator is inserted after the luminance delay line or if there is no delay line at all (black-and-white sets), then the phase relation is achieved by C5-16 = 560 pF.

Note 5: The adjustment of the overall phase relation and consequently the leading edge of the output pulse at pin 2 occurs automatically by the control loop II or by applying a dc voltage to pin 3.