

# Universal Hexadecimal Counter

The MC10136 is a high speed synchronous counter that can count up, count down, preset, or stop count at frequencies exceeding 100 MHz. The flexibility of this device allows the designer to use one basic counter for most applications, and the synchronous count feature makes the MC10136 suitable for either computers or instrumentation.

Three control lines (S1, S2, and Carry In) determine the operation mode of the counter. Lines S1 and S2 determine one of four operations; preset (program), increment (count up), decrement (count down), or hold (stop count). Note that in the preset mode a clock pulse is necessary to load the counter, and the information present on the data inputs (D0, D1, D2, and D3) will be entered into the counter. Carry Out goes low on the terminal count, or when the counter is being preset.

This device is not designed for use with gated clocks. Control is via S1 and S2.

## MC10136



**L SUFFIX**  
CERAMIC PACKAGE  
CASE 620-10



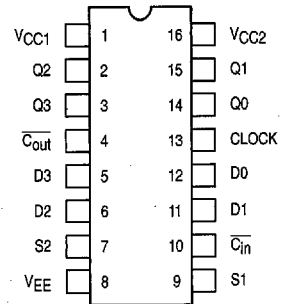
**P SUFFIX**  
PLASTIC PACKAGE  
CASE 648-08



**FN SUFFIX**  
PLCC  
CASE 775-02

$P_D = 625 \text{ mW typ/pkg (No Load)}$   
 $f_{\text{count}} = 150 \text{ MHz typ}$   
 $t_{pd} = 3.3 \text{ ns typ (C-Q)}$   
 $7.0 \text{ ns typ (C-Cout)}$   
 $5.0 \text{ ns typ (Cin-Cout)}$

### DIP PIN ASSIGNMENT



Pin assignment is for Dual-In-Line Package.  
For PLCC pin assignment, see the Pin Conversion Tables on page 6-11.

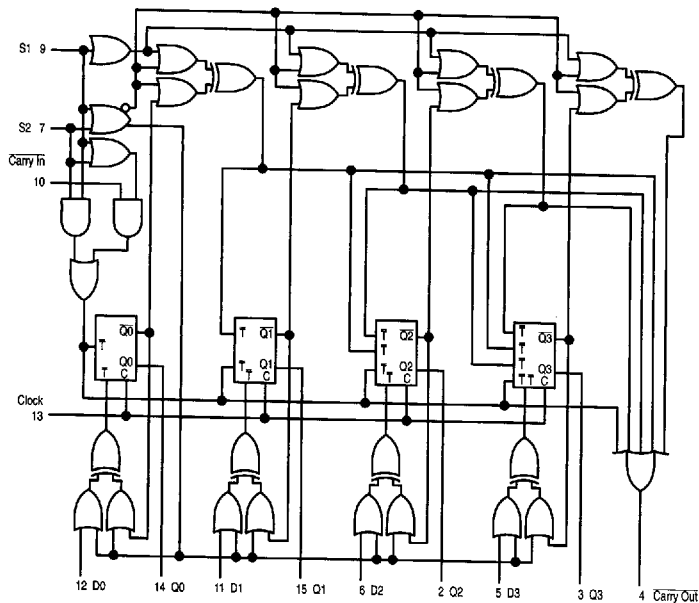
### FUNCTION TABLE

Cin	S1	S2	Operating Mode
X	L	L	Preset (Program)
L	L	H	Increment (Count Up)
H	L	H	Hold Count
L	H	L	Decrement (Count Down)
H	H	L	Hold Count
X	H	H	Hold (Stop Count)

3



LOGIC DIAGRAM



VCC1 = PIN 1  
 VCC2 = PIN 16  
 VEE = PIN 8

NOTE: Flip-flops will toggle when all T inputs are low.

3

SEQUENTIAL TRUTH TABLE\*

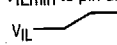
INPUTS								OUTPUTS				
S1	S2	D0	D1	D2	D3	Carry in	Clock **	Q0	Q1	Q2	Q3	Carry Out
L	L	L	L	H	H	X	H	L	L	H	H	L
L	H	X	X	X	X	X	H	L	L	H	H	H
L	H	X	X	X	X	X	L	L	H	H	H	H
L	H	X	X	X	X	X	H	L	H	H	H	L
L	H	X	X	X	X	X	H	H	H	H	H	H
L	H	X	X	X	X	X	H	H	H	H	H	H
L	L	H	H	L	L	X	H	H	H	L	L	L
H	L	X	X	X	X	L	H	L	H	L	L	H
H	L	X	X	X	X	L	H	H	L	L	L	H
H	L	X	X	X	X	L	H	L	L	L	L	L
H	L	X	X	X	X	L	H	L	L	L	L	L

\* Truth table shows logic states assuming inputs vary in sequence shown from top to bottom.  
 \*\* A clock H is defined as a clock input transition from a low to a high logic level.

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	Test Limits						Unit		
			-30°C		+25°C			+85°C			
			Min	Max	Min	Typ	Max	Min		Max	
Power Supply Drain Current	$I_E$	8		138		100	125		138	mAdc	
Input Current	$I_{inH}$	5,6,11,12		350			220		220	$\mu$ Adc	
		7		425			265		265		
		9,10		390			245		245		
		13		460			290		290		
	$I_{inL}$	All	0.5		0.5			0.3		$\mu$ Adc	
Output Voltage	Logic 1	$V_{OH}$	14 (2)	-1.060	-0.890	-0.960		-0.810	-0.890	-0.700	Vdc
Output Voltage	Logic 0	$V_{OL}$	14 (2)	-1.890	-1.675	-1.850		-1.650	-1.825	-1.615	Vdc
Threshold Voltage	Logic 1	$V_{OHA}$	14 (2)	-1.080		-0.980			-0.910		Vdc
Threshold Voltage	Logic 0	$V_{OLA}$	14 (2)		-1.655			-1.630		-1.595	Vdc
Switching Times (50Ω Load)											ns
Propagation Delay	Clock Input	$t_{13+14+}$	14	0.8	4.8	1.0	3.3	4.5	1.4	5.0	
		$t_{13+14-}$	14	0.8	4.8	1.0	3.3	4.5	1.4	5.0	
		$t_{13+4+}$	4	2.0	10.9	2.5	7.0	10.5	2.4	11.5	
		$t_{13+4-}$	4	2.0	10.9	2.5	7.0	10.5	2.4	11.5	
		Carry In to Carry Out	$t_{10-4-}$	4 (3)	1.6	7.4	1.6	5.0	6.9	1.9	
		$t_{10+4+}$	4	1.6	7.4	1.6	5.0	6.9	1.9	7.5	
Setup Time	Data Inputs	$t_{12+13+}$	14	3.5		3.5			3.5		
		$t_{12-13+}$	14	3.5		3.5			3.5		
	Select Inputs	$t_{9+13+}$	14	6.0		6.0			6.0		
		$t_{7+13+}$	14	6.0		6.0			6.0		
Carry In Input	$t_{10-13+}$	14	2.5		2.5			3.0			
	$t_{10+13+}$	14	1.5		1.5			1.5			
Hold Time	Data Inputs	$t_{13+12+}$	14	0		0			0		
		$t_{13+12-}$	14	0		0			0		
	Select Inputs	$t_{13+9+}$	14	-1.0		-1.0			-1.0		
		$t_{13+7+}$	14	-1.0		-1.0			-1.0		
	Carry In Input	$t_{13+10-}$	14	0		0			0		
		$t_{13+10+}$	14	0		0			0		
Counting Frequency	$f_{countup}$	14	125		125	150		125		MHz	
	$f_{countdown}$	14	125		125	150		125			
Rise Time (20 to 80%)		$t_{4+}$	4	0.9	3.3	1.1	2.0	3.3	1.1	3.5	ns
		$t_{14+}$	14	0.9	3.3	1.1	2.0	3.3	1.1	3.5	
Fall Time (20 to 80%)		$t_{4-}$	4	0.9	3.3	1.1	2.0	3.3	1.1	3.5	ns
		$t_{14-}$	14	0.9	3.3	1.1	2.0	3.3	1.1	3.5	

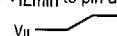
3

1. Individually test each input; apply  $V_{ILmin}$  to pin under test.
2. Measure output after clock pulse   $V_{IH}$  appears at clock input (Pin 13).
3. Before test set all Q outputs to a logic high.
4. To preserve reliable performance, the MC10136 (plastic packaged device only) is to be operated in ambient temperatures above 70°C only when 500lpm blown air or equivalent heat sinking is provided.

**ELECTRICAL CHARACTERISTICS** (continued)

			TEST VOLTAGE VALUES (Volts)						
			V <sub>IHmax</sub>	V <sub>ILmin</sub>	V <sub>IHAmin</sub>	V <sub>ILAmax</sub>	V <sub>EE</sub>		
@ Test Temperature -30°C +25°C +85°C			-0.890	-1.890	-1.205	-1.500	-5.2		
			-0.810	-1.850	-1.105	-1.475	-5.2		
			-0.700	-1.825	-1.035	-1.440	-5.2		
Characteristic	Symbol	Pin Under Test	TEST VOLTAGE APPLIED TO PINS LISTED BELOW					(V <sub>CC</sub> ) Gnd	
			V <sub>IHmax</sub>	V <sub>ILmin</sub>	V <sub>IHAmin</sub>	V <sub>ILAmax</sub>	V <sub>EE</sub>		
Power Supply Drain Current	I <sub>E</sub>	8					8	1, 16	
Input Current	I <sub>inH</sub>	5,6,11,12	5,6,11,12				8	1, 16	
		7	7			8	1, 16		
		9,10	9,10			8	1, 16		
		13	13			8	1, 16		
	I <sub>inL</sub>	All		Note 1.			8	1, 16	
Output Voltage	Logic 1	V <sub>OH</sub>	14 (2.)	12	7, 9		8	1, 16	
Output Voltage	Logic 0	V <sub>OL</sub>	14 (2.)		7, 9		8	1, 16	
Threshold Voltage	Logic 1	V <sub>OHA</sub>	14 (2.)		7, 9	12	8	1, 16	
Threshold Voltage	Logic 0	V <sub>OLA</sub>	14 (2.)		7, 9	12	8	1, 16	
Switching Times (50Ω Load)			+1.11V	+0.31V	Pulse In	Pulse Out	-3.2 V	+2.0 V	
Propagation Delay	Clock Input	t <sub>13+14+</sub>	14	12		13	14	8	1, 16
		t <sub>13+14-</sub>	14			13	14	8	1, 16
		t <sub>13+4+</sub>	4	7		13	4	8	1, 16
		t <sub>13+4-</sub>	4	7		13	4	8	1, 16
Carry In to Carry Out		t <sub>10-4-</sub>	4 (3.)	7	13	10	4	8	1, 16
		t <sub>10+4+</sub>	4	7	13	10	4	8	1, 16
Setup Time	Data Inputs	t <sub>12+13+</sub>	14		7, 9	12, 13	14	8	1, 16
		t <sub>12-13+</sub>	14		7, 9	12, 13	14	8	1, 16
	Select Inputs	t <sub>9+13+</sub>	14			9, 13	14	8	1, 16
		t <sub>7+13+</sub>	14			7, 13	14	8	1, 16
Carry In Inputs		t <sub>10-13+</sub>	14	7	9	10, 13	14	8	1, 16
		t <sub>10+13+</sub>	14	7	9	10, 13	14	8	1, 16
Hold Time	Data Inputs	t <sub>13+12+</sub>	14		7, 9	12, 13	14	8	1, 16
		t <sub>13+12-</sub>	14		7, 9	12, 13	14	8	1, 16
	Select Inputs	t <sub>13+9+</sub>	14			9, 13	14	8	1, 16
		t <sub>13+7+</sub>	14			7, 13	14	8	1, 16
Carry In Inputs		t <sub>13+10-</sub>	14	7	9	10, 13	14	8	1, 16
		t <sub>13+10+</sub>	14	7		10, 13	14	8	1, 16
Counting Frequency		f <sub>countup</sub>	14	7		13	14	8	1, 16
		f <sub>countdown</sub>	14	9		13	14	8	1, 16
Rise Time (20 to 80%)		t <sub>4+</sub>	4	7		13	4	8	1, 16
		t <sub>14+</sub>	14	7		13	14	8	1, 16
Fall Time (20 to 80%)		t <sub>4-</sub>	4	7		13	4	8	1, 16
		t <sub>14-</sub>	14	7		13	14	8	1, 16

3

1. Individually test each input; apply V<sub>ILmin</sub> to pin under test.
2. Measure output after clock pulse  V<sub>IH</sub> appears at clock input (Pin 13).
3. Before test set all Q outputs to a logic high.
4. To preserve reliable performance, the MC10136 (plastic packaged device only) is to be operated in ambient temperatures above 70°C only when 500fpm blown air or equivalent heat sinking is provided.

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C

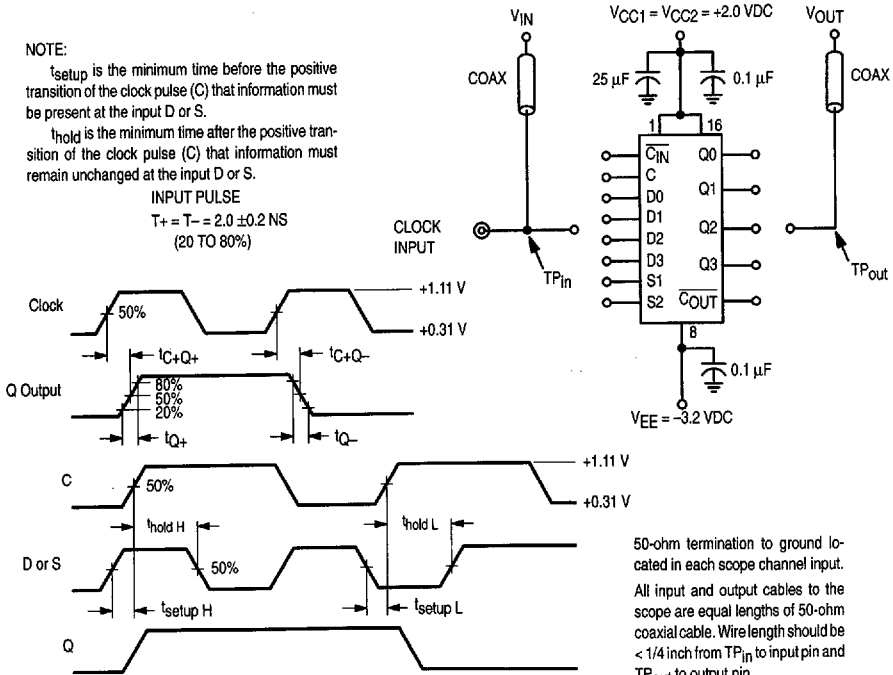
NOTE:

$t_{setup}$  is the minimum time before the positive transition of the clock pulse (C) that information must be present at the input D or S.

$t_{hold}$  is the minimum time after the positive transition of the clock pulse (C) that information must remain unchanged at the input D or S.

INPUT PULSE

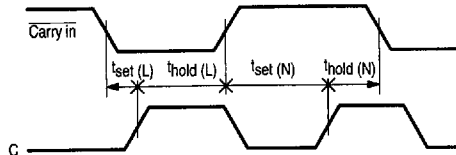
$T_+ = T_- = 2.0 \pm 0.2$  NS  
(20 TO 80%)



3

50-ohm termination to ground located in each scope channel input. All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP<sub>in</sub> to input pin and TP<sub>out</sub> to output pin. Unused outputs are connected to a 50-ohm resistor to ground.

CARRY IN SET UP AND HOLD TIMES



**APPLICATIONS INFORMATION**

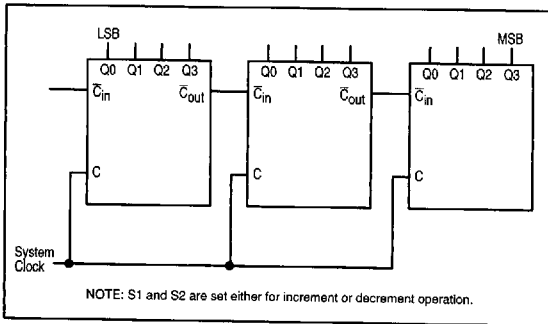
To provide more than four bits of counting capability several MC10136 counters may be cascaded. The Carry In input overrides the clock when the counter is either in the increment mode or the decrement mode of operation. This input allows several devices to be cascaded in a fully synchronous multistage counter as illustrated in Figure 1. The carry is advanced between stages as shown with no external gating. The Carry In of the first device may be left open. The system clock is common to all devices.

The various operational modes of the counter make it useful for a wide variety of applications. If used with MECL III devices, prescalars with input toggle frequencies in excess of 300 MHz are possible. Figure 2 shows such a prescaler using the MC10136 and MC1670. Use of the MC10231 in place of the MC1670 permits 200 MHz operation.

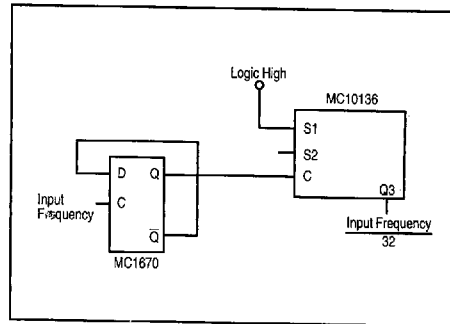
The MC10136 may also be used as a programmable counter. The configuration of Figure 3 requires no additional gates, although maximum frequency is limited to about 50 MHz. The divider modulus is equal to the program input plus one ( $M = N + 1$ ), therefore, the counter will divide by a modulus varying from 1 to 16.

A second programmable configuration is also illustrated in Figure 4. A pulse swallowing technique is used to speed the counter operation up to 110 MHz typically. The divider modulus for this figure is equal to the program input ( $M = N$ ). The minimum modulus is 2 because of the pulse swallowing technique, and the modulus may vary from 2 to 15. This programmable configuration requires an additional gate, such as  $1/2$ MC10109 and a flip-flop such as  $1/2$ MC10131.

**FIGURE 1 — 12 BIT SYNCHRONOUS COUNTER**

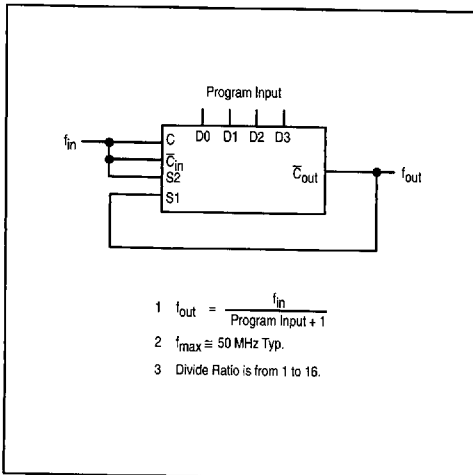


**FIGURE 2 — 300 MHz PRESCALER**



**3**

**FIGURE 3 — 50 MHz PROGRAMMABLE COUNTER**



**FIGURE 4 — 100 MHz PROGRAMMABLE COUNTER**

