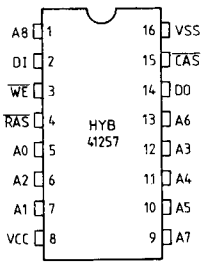
HYB 41257-12/-15/-20
262,144-Bit Dynamic Random Access Memory (RAM)

- 262,144 × 1-bit organization
- Industry standard 16 pins
- Single +5 V supply, ±10% tolerance
- Low power dissipation:
  - 385 mW active (max.)
  - 28 mW standby (max.)
- 120 ns access time
  220 ns cycle time (HYB 41257-12)
  150 ns access time
  260 ns cycle time (HYB 41257-15)
  200 ns access time
  330 ns cycle time (HYB 41257-20)
- All inputs and outputs TTL compatible
- Common I/O capability using "early write" operation
- Valid data during $\overline{CAS}$ precharge until start of next nibble cycle provides higher system data rate
- Fast nibble mode on read and write cycles via addresses A8 row and A8 column
  30 ns access time
  65 ns cycle time (HYB 41257-12)
  40 ns access time
  80 ns cycle time (HYB 41257-15)
  50 ns access time
  110 ns cycle time (HYB 41257-20)
- Read, write, read-modify-write, RAS-only-refresh, hidden refresh
- On-chip substrate bias generator
- Three-state data output
- 256 refresh cycles with 4 ms refresh period
- Redundancy incorporated for increasing yield
  - activation via laser links
  - roll-call-mode as pretest with DI at 10V provides: redundancy signature individual address decoder scrambling

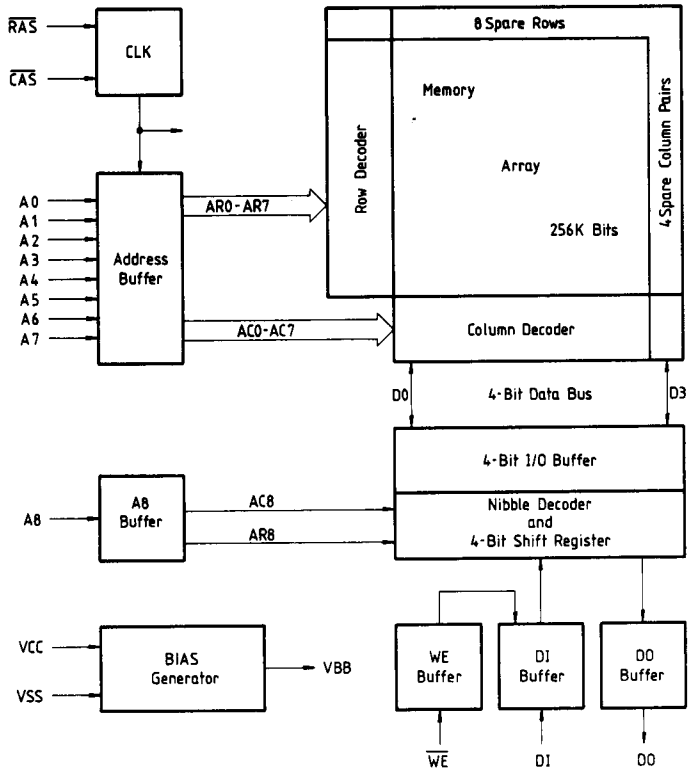
Pin configuration



Pin names	
A0 – A8	Address Inputs
$\overline{CAS}$	Column Address Strobe
DI	Data In
DO	Data Out
$\overline{RAS}$	Row Address Strobe
$\overline{WE}$	Write Enable
VCC	Power Supply (+5 V)
VSS	Ground (0 V)

The HYB 41257 is a 262,144 word by 1-bit dynamic Random Access Memory. This 5V-only component is fabricated with Siemens new high performance N-channel silicon gate technology. The use of tantalum polycide provides high speed. A Siemens proprietary chip cover protects the chip against α radiation.
Nine multiplexed address inputs permit the HYB 41257 to be packaged in an industry standard 16-pin dual-in-line package. System-oriented features include single power supply with ±10% tolerance, on-chip address and data registers which eliminate the need for interface registers, and fully TTL compatible inputs and output, including clocks.
In addition to the usual read, write and read-modify-write cycles, the HYB 41257 is capable of early and late write cycles, $\overline{RAS}$-only refresh, and hidden refresh. Common I/O capability is given by using "early write" operation.
Nibble Mode is a new feature of the HYB 41257 allowing the user to perform a serial access of 4 bits at a high data rate by using an on-chip nibble shift register which is controlled by one set of addresses on pin 1 (A8 Row and A8 Column) and the $\overline{CAS}$ clock only.
The HYB 41257 has the capability of using laser links to perform redundancy. With the roll-call mode, which is a new test feature, the user can separate repaired devices easily, and additionally gets information on the individual row and column addresses which have been repaired and how they are substituted by redundant lines.

Block Diagram



Functional Description

Device Initialization

Since the HYB 41257 is a dynamic RAM with a single 5V supply, no power sequencing is required. For power-up, an initial pause of 200 microseconds is necessary for the internal bias generator to establish the proper substrate bias voltage. To initialize the nodes of the dynamic circuitry, a minimum of 8 active cycles of the Row Address Strobe ($\overline{RAS}$) has to be performed. This is also necessary after an extended inactive state of greater than 4 milliseconds.

Adressing (A0–A8)

For selecting one of the 262,144 memory cells, a total of 18 address bits are required. First 9 Row Address bits are set up on pins A0 through A8 and latched into the row address latches by the Row Address Strobe ($\overline{RAS}$). Then the 9 column address bits are set up on pins A0 through A8 and latched into the column address latches by the Column Address Strobe ($\overline{CAS}$). All input addresses must be stable on the falling edges of $\overline{RAS}$ and $\overline{CAS}$. It should be noted that $\overline{RAS}$ is similar to a Chip Enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select activating the column decoder and the input and output buffers.

Write enable ($\overline{WE}$)

The read or write mode is selected with the $\overline{WE}$ input. A logic high (VIH) on $\overline{WE}$ dictates read mode; logic low (VIL) dictates write mode. The data input is disabled when read mode is selected. When $\overline{WE}$ goes low prior to $\overline{CAS}$, data output (DO) will remain in the high-impedance state for the entire cycle permitting common I/O operation.

Data Input (DI)

Data is written during a write or read-modify-write cycle. The falling edge of $\overline{CAS}$ or $\overline{WE}$ strobes data into the on-chip data latch. In an early write cycle $\overline{WE}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal.

Data output (DO)

The output buffer is three-state TTL compatible with a fan-out of two standard TTL loads. Data Out has the same polarity as Data In. The output is in a high impedance state until $\overline{CAS}$ is brought low. In a read cycle or read-write cycle, the output is valid after tRAC from transition of $\overline{RAS}$ when tRCD (min) is satisfied, or after tCAC from transition of $\overline{CAS}$ when the transition occurs after tRCD (max.).
In an early write cycle, the output is always in the impedance state. In a delayed write or read-modify-write cycle, the output will follow the sequence for the read cycle. With $\overline{CAS}$ going high and $\overline{RAS}$ being high, the output returns to the high impedance state within tOFF.
For nibble-mode read cycles, the data output shows a novel function that gives advantages for system application. With $\overline{RAS}$ low the data output remains valid after and during $\overline{CAS}$ high. That gives time for a proper strobing of the data despite of system time tolerances, and increases the system data rate because the minimum $\overline{CAS}$ low time, tCAS and tNAS, can be realized more easily. With $\overline{CAS}$ going low for the next nibble cycle the data output returns to the high-impedance state within tNOFF. In a read, late write, or read-modify-write mode for a normal cycle or the last nibble cycle, the data output condition depends on whether $\overline{CAS}$ or $\overline{RAS}$ is brought high first. With $\overline{CAS}$ going high and $\overline{RAS}$ at low, the data output is valid until $\overline{RAS}$ goes high and returns to the high-impedance state within tOFF referenced to $\overline{RAS}$. With $\overline{CAS}$ being low at $\overline{RAS}$ high, the data output is valid until $\overline{CAS}$ goes high and returns to the high-impedance state within tOFF referenced to $\overline{CAS}$.

Hidden refresh

$\overline{RAS}$-only refresh cycle may take place while maintaining valid output data. This feature is referred to as Hidden Refresh. Hidden Refresh is performed by holding $\overline{CAS}$ at VIL of a previous memory read cycle.

Refresh cycle

A refresh operation must be performed at least every four milliseconds to retain data. Since the output buffer is in the high impedance state unless $\overline{CAS}$ is applied, the $\overline{RAS}$-only refresh sequence avoids any output signal during refresh. Strobing each of the 256 row addresses (A0 through A7) with $\overline{RAS}$ causes all bits in each row to be refreshed. $\overline{CAS}$ can remain high (inactive) for this refresh sequence to conserve power.

Nibble-mode cycle

Nibble-mode operation allows a very fast serial data streaming up to 4 bits by applying only one set of addresses for the first bit to be accessed as normal (tCAC). By holding $\overline{RAS}$ low, only $\overline{CAS}$ has to be cycled up and then down for reading or writing the next 3 bits at a high data rate with tNAC tCAC. After 4 bits have been accessed, the following bit will be the same as the first bit accessed.
Address on pin 1 (row address A8 and column address A8) is used to select 1 of the 4 nibble bits for initial access. Toggling $\overline{CAS}$ causes row A8 and column A8 to be incremented by the internal shift register with A8 row being the least significant address, and allows access to the next nibble bit. In nibble mode, any combination of read, write, and read-modify-write operation is possible (e.g. first bit: read; second bit: write; third bit: read-modify-write, etc.).

Absolute Maximum Ratings *)

Operating Temperature Range	0 to + 70 °C
Storage Temperature Range	−65 to +150 °C
Voltages on Any Pin Relative to VSS	−1 to +7 V
Voltage on DI Relative to VSS	−1 to +11 V
Power Dissipation	1 W
Data Out Current (Short Circuit)	50 mA

D.C. Characteristics

TA = 0 to 70 °C, VSS = 0V, VCC = +5 V ±10%

Symbol	Parameter	Limit Values		Unit	Test condition
		Min.	Max.		
VIH	Input high voltage (all inputs)	2.4	VCC+1	V	1) 2)
VIL	Input low voltage (all inputs)	−1.0	0.8		
VOH	Output high voltage	2.4	–		–
VOL	Output low voltage		0.4		
ICC1	Average VCC supply current −12 tRC = 220 ns −15 tRC = 260 ns −20 tRC = 330 ns	–	 85 70 60	mA	 3)
ICC2	Standy VCC supply current		5		4)
ICC3	Average VCC supply current during $\overline{RAS}$-only refresh cycles −12 tRC = 220 ns −15 tRC = 260 ns −20 tRC = 330 ns		 65 55 45		 3)
ICC6	Average VCC supply current during nibble mode −12 tNC = 65 ns −15 tNC = 80 ns −20 tNC = 110 ns		 10 8 7		
II(L)	Input leakage current (any input)	–	10	µA	–
IO(L)	Output leakage current ($\overline{CAS}$ at logic 1, 0 ≤ Vout ≤ 5.5)				
VCC	VCC supply voltage	4.5	5.5	V	1)
VSS	VSS supply voltage	0	0		

Notes see page 6-45

Capacitance

Symbol	Parameter	Limit values		Unit	Test condition
		Min.	Max.		
CI1	Input capacitance (A0–A8)		6	pF	5)
CI2	Input capacitance ($\overline{RAS}$, DI)		7		
CI3	Input capacitance ($\overline{CAS}$, $\overline{WE}$)		8		
CO	Output capacitance (DO, $\overline{CAS}$ = VIH to disable output)				

6

*) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

1) All voltages referenced to VSS.

2) Overshooting and undershooting on input levels of 6.5 V or −2 V for a period of 30 ns max. will not influence function and reliability of the device.

3) ICC depends on frequency of operation. Maximum current is measured at the fastest cycle rate.

4) $\overline{RAS}$ and $\overline{CAS}$ are both at VIH.

5) Effective capacitance calculated from the equation $C = \frac{I \cdot \Delta t}{\Delta V}$ with $\Delta V = 3$ V or measured with Boonton meter.

A.C. Test Conditions

Input pulse levels		0 to 3.0 V
Input rise an fall times	5 ns between	0.8 and 2.4 V
Input timing reference levels		0.8 to 2.4 V
Output timing reference levels		0.4 to 2.4 V
Output load		equivalent to 2 standard TTL loads and 100 pF

A.C. Characteristics

TA = 0 to +70 °C; VCC = +5 V ±10% (unless otherwise specified; see notes 6, 7, 8)

Symbol	Parameter	Limit values						Unit
		HYB 41257-						
		-12		-15		-20		
		Min.	Max.	Min.	Max.	Min.	Max.	
tRC	Random read or write cycle time 9)	220	–	260	–	330	–	ns
tRWC	Read-modify-write cycle time 9)	265		310		390		
tRAC	Access time from $\overline{RAS}$ 10) 11)	–	120	–	150	–	200	
tCAC	Access time from $\overline{CAS}$ 10) 11) 12)		60		75		100	
tRAS	$\overline{RAS}$ pulse width	120	10^4	150	10^4	200	10^4	
tCAS	$\overline{CAS}$ pulse width	60	–	75	–	100	–	
tREF	Refresh period	–	4	–	4	–	4	ms
tRP	$\overline{RAS}$ precharge time	90	–	100	–	120	–	ns
tCRP	CAS to RAS precharge time	10		10		10		
tRCD	$\overline{RAS}$ to $\overline{CAS}$ delay time 13)	30	60	30	75	35	100	
tRSH	$\overline{RAS}$ hold time	60	–	75	–	100	–	ns
tCSH	$\overline{CAS}$ hold time	120		150		200		
tASR	Row address setup time	0		0		0		
tRAH	Row address hold time	20		20		25		
tASC	Column address setup time	0		0		0		
tCAH	Column address hold time	30		30		35		
tAR	Column address hold time referenced to $\overline{RAS}$ 14)	90		105		135		
tT	Transition time (rise and fall) 6)	3	50	3	50	3	50	
tRCS	Read command setup time	0	–	0	–	0		
tRCH	Read command hold time referenced to $\overline{CAS}$ 15)							
tRRH	Read command hold time referenced to $\overline{RAS}$ 15)	25		25		30		

Notes see page 6-48

Symbol	Parameter	Limit values						Unit
		HYB 41257-						
		-12		-15		-20		
		Min.	Max.	Min.	Max.	Min.	Max.	
tOFF	Output buffer turn-off delay 16)	0	30	0	40	0	50	ns
tWCS	Write command setup time 17)		–		–		–	
tWCH	Write command hold time	40		45		55		
tWCR	Write command hold time referenced to $\overline{RAS}$ 14)	100		120		155		
tWP	Write command pulse width	40		45		55		
tRWL	Write command to $\overline{RAS}$ lead time							
tCWL	Write command to $\overline{CAS}$ lead time							
tDS	Data in setup time 18)	0		0		0		
tDH	Data in hold time 18)	40		45		55		
tDHR	Data in hold time referenced to $\overline{RAS}$ 14)	100		120		155		
tCWD	$\overline{CAS}$ to $\overline{WE}$ delay 17)	60		75		100		
tRWD	$\overline{RAS}$ to $\overline{WE}$ delay 17)	120		150		200		
tRRW	RMW cycle $\overline{RAS}$ pulse width	165		200		260		
tCRW	RMW cycle $\overline{CAS}$ pulse width	105		125		160		
tNC	Nibble-mode cycle time 9)	65		80		110	–	
tNAC	Nibble-mode access time from $\overline{CAS}$ 10)	–	30	–	40	–	50	
tNAS	Nibble-mode setup time	30		40		50		
tNP	Nibble-mode precharge time	25		30				
tNRSH	Nibble-mode $\overline{RAS}$ hold time	30		40				
tNCWD	Nibble-mode $\overline{CAS}$ to $\overline{WE}$ delay		–		–		–	
tNCRW	Nibble-mode RMW $\overline{CAS}$ pulse width	65		85		105		
tNCWL	Nibble-mode $\overline{WE}$ to $\overline{CAS}$ lead time	30		40		50		
tNWRH	Nibble-mode write $\overline{RAS}$ hold time	45		55		75		
tNOFF	Nibble-mode output buffer turn-off delay 19)	0		0		0		
tNWP	Nibble-mode $\overline{WE}$ pulse width	30		40		50		
tNWCH	Nibble-mode $\overline{WE}$ command hold time							

Notes see page 6-48

Notes:

6) VIH and VIL are reference levels to measure timing of input signals. Also, transition times are measured between VIH and VIL.

7) An initial pause of 200 µs is required after powerup following by a minimum of eight initialization cycles prior to normal operation.

8) The time parameters specified here are valid for a transition time of tT = 5 ns for the input signals.

9) The specifications for tRC (min), tRWC (min), and nibble cycle time (tNC) are only used to indicate cycle time at which proper operation over full temperature range (0 °C ≤ TA ≤ 70 °C) is assured.

10) Measured with a load equivalent to two TTL loads and 100 pF.

11) Assumes that tRCD ≤ tRCD(max). If tRCD is greater than the maximum recommended value shown in this table, tRAC will increase by the amount that tRCD exceeds the value shown.

12) Assumes that tRCD ≥ tRCD (max).

13) Operation within the tRCD (max) limit ensures that tRAC (max) can be met. tRCD (max) is specified as a reference point only; if tRCD is greater than the specified tRCD (max) limit, then access time is controlled exclusively by tCAC.

14) tRCD + tCAH ≥ tAR min, tRCD + tDH ≥ tDHR min, tRCD + tWCH ≥ tWCR min.

15) Either tRRH or tRCH must be satisfied for a read cycle.

16) tOFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels. tOFF is referenced either to the $\overline{CAS}$ leading edge with $\overline{RAS}$ being high or to the $\overline{RAS}$ leading edge with $\overline{CAS}$ being high.

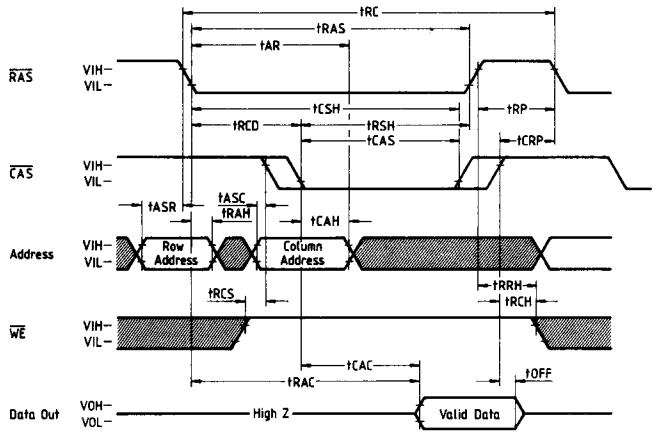
17) tWCS, tCWD and tRWC are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: If tWCS ≥ tWCS(min), the cycle is an early write cycle and the Data Out will remain open circuit (high impedance) throughout the entire cycle; if tCWD ≥ tCWD (min) and tRWD ≥ tRWD (min) the cycle is a read-write cycle and the Data Out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the Data Out (at access time) is indeterminate.

18) tDS and tDH are referenced to the leading edge of $\overline{CAS}$ in early write cycles, and to the leading edge of $\overline{WE}$ in delayed write or read-modify-write cycles.

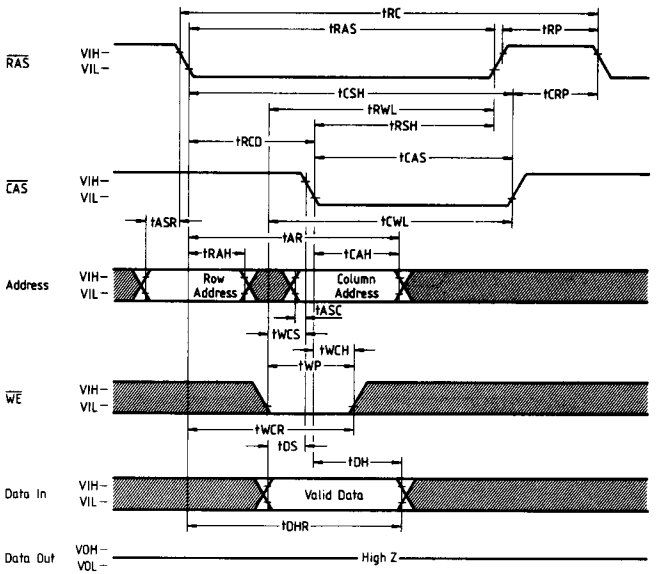
19) tNOFF (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels. tNOFF is referenced to the $\overline{CAS}$ falling edge of the next nibble cycle with $\overline{RAS}$ being low.

Waveforms

Read cycle

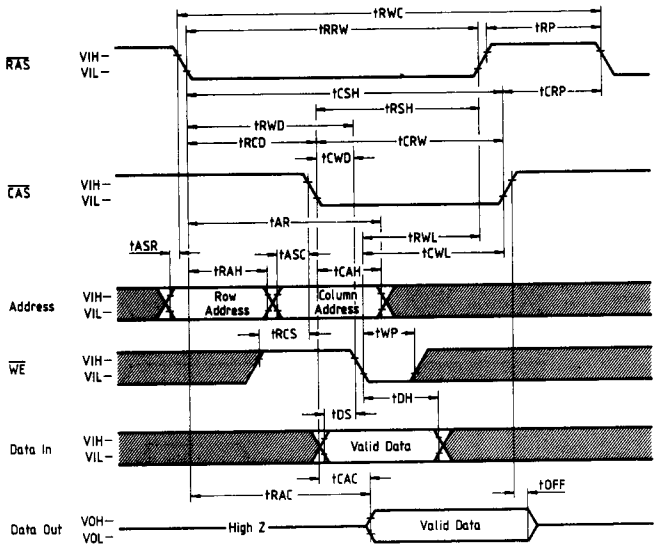


Write cycle (early write)

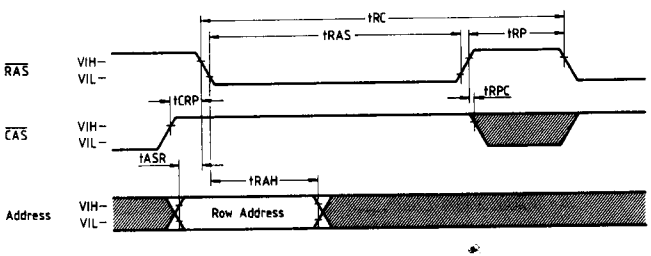


6

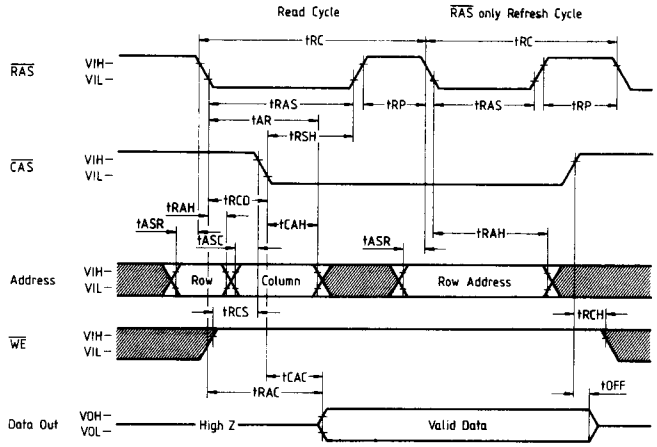
Read-modify-write or write cycle



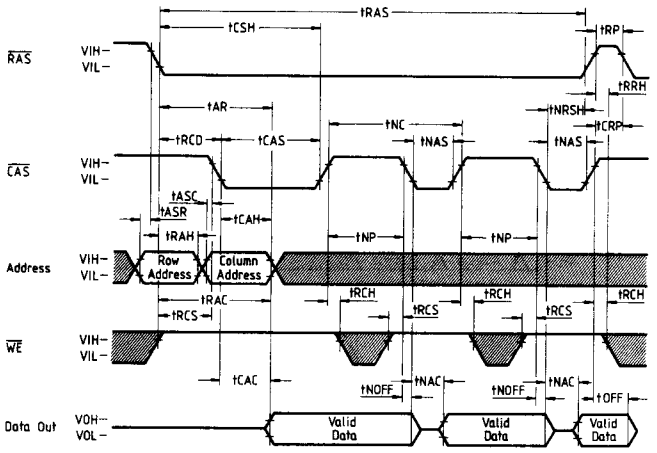
RAS-only refresh cycle
(DI and WE = don't care)



Hidden refresh cycle

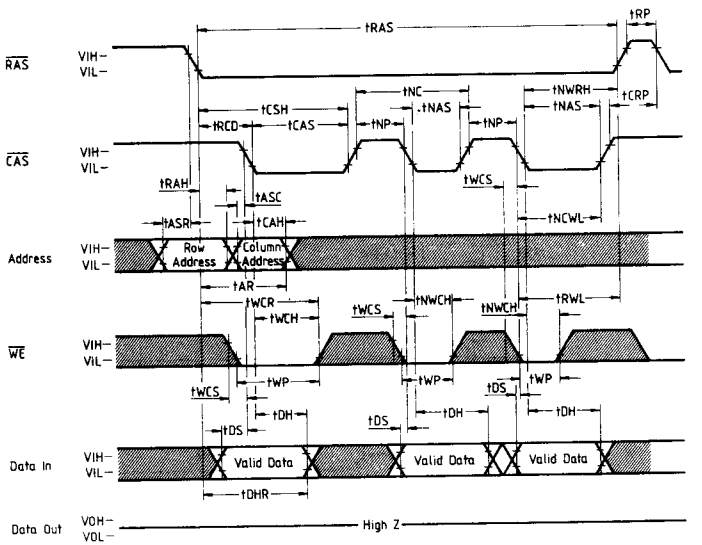


Nibble-mode read cycle

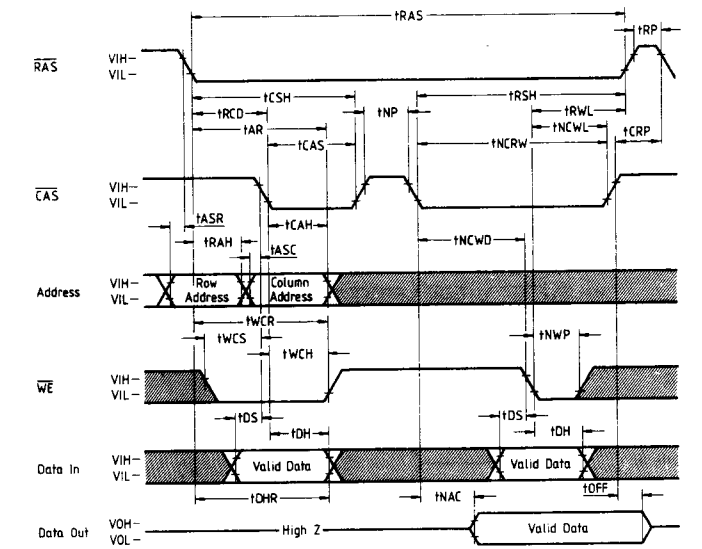


6

Nibble-mode write cycle (early write)



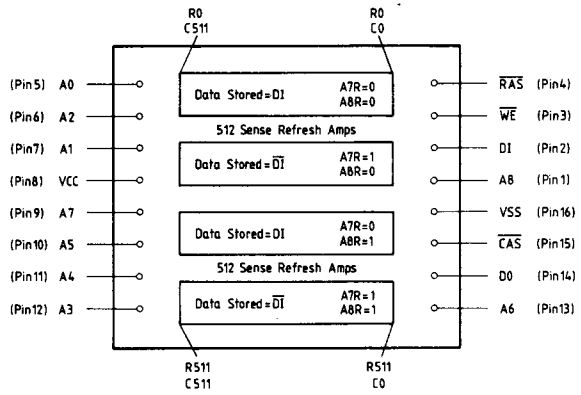
Nibble-mode read-modify-write



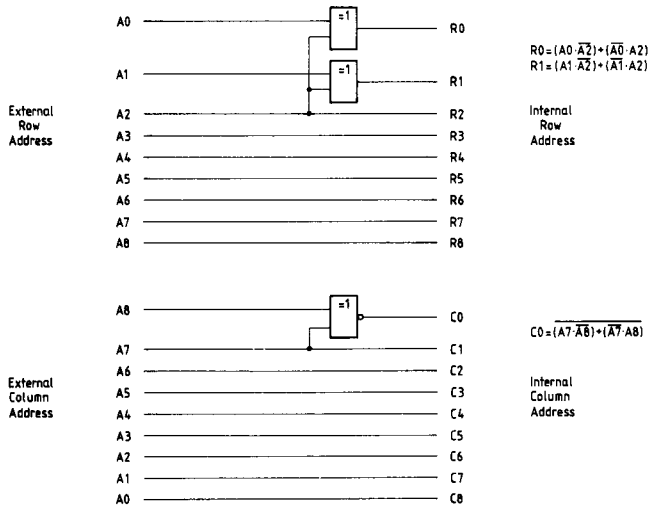
Address Decoder Scrambling (without redundancy)

The evaluation and incoming testing of RAMs normally requires a description of the internal address scrambling of the device in order to check for 'worst case' pattern.

Internal address scrambling



Address decoder scrambling



Note: The logic symbols are used solely to indicate the logic function.

6

Redundancy

Redundancy concept

The HYB 41257 takes advantage of the redundancy concept for increasing yield. This is done by providing the chip with a total of 8 spare rows and 4 spare column pairs. Two spare rows can be selected independently in each of four 64K cell arrays, and two spare column pairs can be selected independently in each of two 128K cell blocks. The spare lines can be selected by spare decoders which have to be programmed by laser technique during wafer probe.

Laser technology

For activation of redundant circuitry a laser pulse is used to open polycide links within the spare row and spare column decoders. The laser technique is used because it is mature and has proven reliable in a number of semiconductor applications including the implementation of redundant memory circuitry. Due to the fact, that the laser beam is very fine and can easily and accurately be positioned, and that it incorporates the energy for a controlled blow up of the polycide links, the laser technique is well suited for highly complex memory circuitry. All that results in a more efficient use of chip real estate.

Redundancy testability (roll-call mode)

With the redundancy concept two categories of devices, repaired and non-repaired ones, will be available. These two categories have to be separated easily and reliably by both, the manufacturer and the user (signature). When testing repaired device, the reconfigurated address scrambling which results from activating spare rows and columns has to be taken into account for efficient device testing (individual bit map recognition).
The HYB 41257 has the capability of performing these two novel functions. It is done with a simple electrical test at the beginning of the final test or incoming inspection of each device (roll-call mode). The roll-call mode for performing both signature and individual bit map recognition can be activated with DI at VIHR (10V $\pm$10%).

Signature

With DI at VIHR and performing at least one $\overline{\text{RAS}}$-only cycle with a cycle time of tRCR on any address combination, in the case of non-repaired devices the Data Output is in the high-impedance state as in normal early write cycles. For repaired devices the Data Output will go to VOLR or VOHR after the access time tRACR.

Individual bit map recognition

If the test for signature has shown a repaired device, additional tests can be performed to recognize which addresses have been repaired and how they are replaced by spare lines. Row and column redundancy can be recognized independently.

Row redundancy

Row redundancy can be recognized with DI at VIHR and $\overline{\text{CAS}}$ at high, and $\overline{\text{RAS}}$-only cycles on all 512 row address combinations. The data output is low (VOLR) for non-repaired addresses, and is high (VOHR) for repaired addresses only. Within each 64K cell array, spare row 1 is always used if only one row is to be replaced. If two rows are to be replaced in an 64K cell array, spare row 2 is used to replace the defective row with the higher address.

Column redundancy

Column redundancy can be recognized with DI at VIHR, and early write cycles with tRCDR $\leq$ tRCD (min) on all 512 column address combinations.

A8 row must be used to distinguish between the two 128K cell blocks. The data output is low (VOLR) for non-repaired addresses, and high (VOHR) for repaired addresses. Within each 128K cell block, spare column pair 1 is always used if only one column is to be replaced. Otherwise, spare column pair 2 is used to replace the defective column with the higher address.

Recommended operating conditions

Roll-call mode

DC operating conditions and characteristics (Full operating voltage and temperature range unless otherwise specified).

Symbol	Parameter	Limit values			Unit
		Min.	Typ.	Max.	
VCC VSS	Supply voltage HYB 41257-12, -15, -20 1) 1)	4.75 0	5.0 0	5.25 0	V
VIH	Logic 1 voltage: All inputs (except DI)	2.4	–	VCC+1	V
VIHR	Logic 1 voltage: DI 1) 2)	9.0	10	11	V
VIL	Logic 0 voltage: All inputs 1)	−1.0	–	0.8	V
VOHR	Output logic 1 voltage Iout = −5mA 1)	2.0	–	–	V
VOLR	Output logic 0 voltage Iout = −4.2 mA 1)	–	–	0.4	V

A.C. operating conditions and characteristics

(Full operating voltage and temperature range unless otherwise specified.)

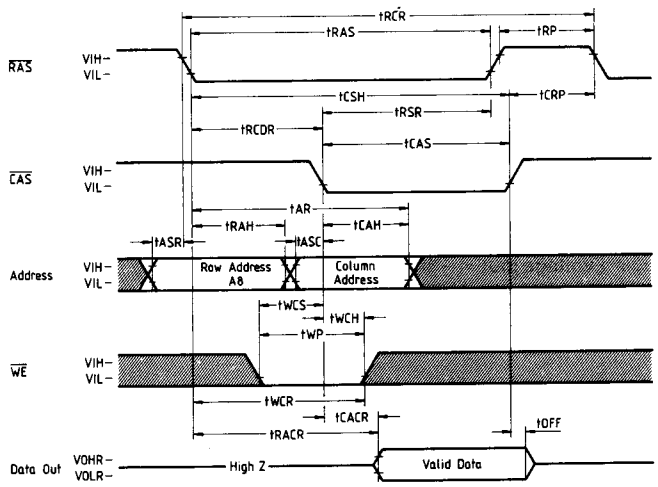
Symbol	Parameter	Limit values						Unit
		HYB 41257-						
		−12		−15		−20		
		Min.	Max.	Min.	Max	Min.	Max.	
tRCR	Roll-call cycle time	330	–	390	–	490	–	ns
tRCDR	Roll-call $\overline{RAS}$ to $\overline{CAS}$ delay	–	30	–	30	–	35	ns
tRACR	Roll-call $\overline{RAS}$ access time	–	180	–	225	–	300	ns
tCARC	Roll-call $\overline{CAS}$ access time		90		115		150	ns

1) All voltages referenced to VSS.

2) VIHR at DI must only be used for the roll-call mode test and not for normal memory tests or applications. To avoid device damage, VIHR is to be applied after the initialization conditions (initial pause of 200 ms and 8 cycles) have been satisfied, and must never exceed 11V.

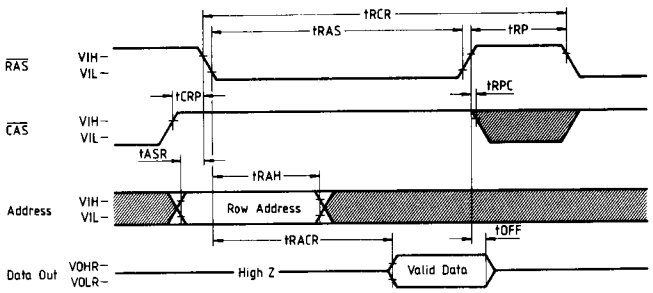
Column Redundancy

Early CAS – early write cycle
(DI at VIHR, *t*RCD = tRCD (min), row addresses A0 to A7 = don't care)

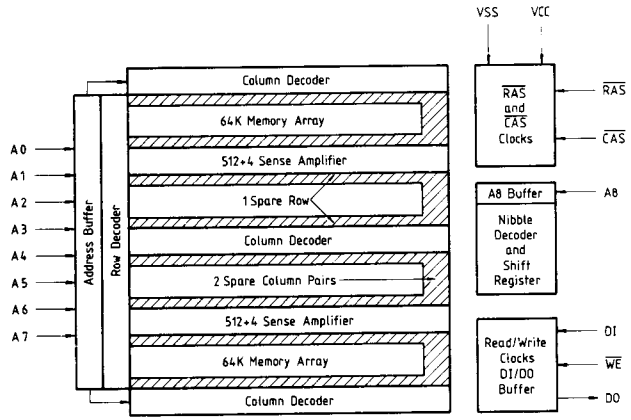


Row Redundancy and Signature

RAS-only cycle
(DI at VIHR, WE = don't care)



Siemens 256K DRAM Chip Topology



Ordering Information

Type	Description
HYB41257-P12	DRAM, access time 120 ns (P-DIP 16)
HYB41257-P15	DRAM, access time 150 ns (P-DIP 16)
HYB41257-P20	DRAM, access time 200 ns (P-DIP 16)

6