



Am486™ SXLV

High-Performance, Low-Voltage, 32-Bit Microprocessor

DISTINCTIVE CHARACTERISTICS

- **Operating voltage range 3.0 V to 3.6 V—
The best microprocessor for portable PC applications**
 - 33-MHz operating frequency
 - Over 50% longer battery life than conventional 486 notebooks
 - Wide range of chipsets and support available through the AMD® FusionPCSM Program
 - Fully static design
- **High Integration On-Chip**
 - 8-Kbyte code and data cache
 - Paged, virtual memory management
- **High-performance Design**
 - Frequent instructions execute in one clock
 - 106-Million bytes/second burst bus at 33 MHz
 - 0.7-micron CMOS process technology
 - Dynamic bus sizing for 8-, 16-, and 32-bit buses
- **Complete 32-bit Architecture**
 - Address and data buses
 - All Registers
 - 8-, 16-, and 32-bit data types
- **Multiprocessor Support**
 - Multiprocessor instructions
 - Cache consistency protocol
 - Support for second-level cache
- **System Management Mode (SMM) for system and power management**
 - System Management Interrupt (SMI) for power management independent of processor operating mode and operating system.
 - SMI is a non-maskable interrupt that has higher priority than NMI
 - Automatic save and restore of microprocessor state
 - Wide range of chipsets supporting SMM available to allow product differentiation
- **Lower heat dissipation and increased reliability**
- **IEEE 1149.1 Boundary Scan Compatibility**
- **Standard 196-Pin PQFP Package**
- **AMD advanced 0.7-micron, three-layer CMOS technology**

GENERAL DESCRIPTION

The Am486SXLV microprocessor is a low-voltage, true static implementation of the 486SX. The operating voltage range is from 3.0 V–3.6 V. The low-voltage operation of the Am486SXLV microprocessor enables longer battery life in notebook computers. The price/performance of the full 32-bit processor provides the best value for designing high-volume, mainstream 486 notebooks. At 33 MHz, this device has 56% lower operating power than the Am486SX microprocessor. Lowering the typical system operating voltage from 5.0 V to 3.3 V doubles the battery life.

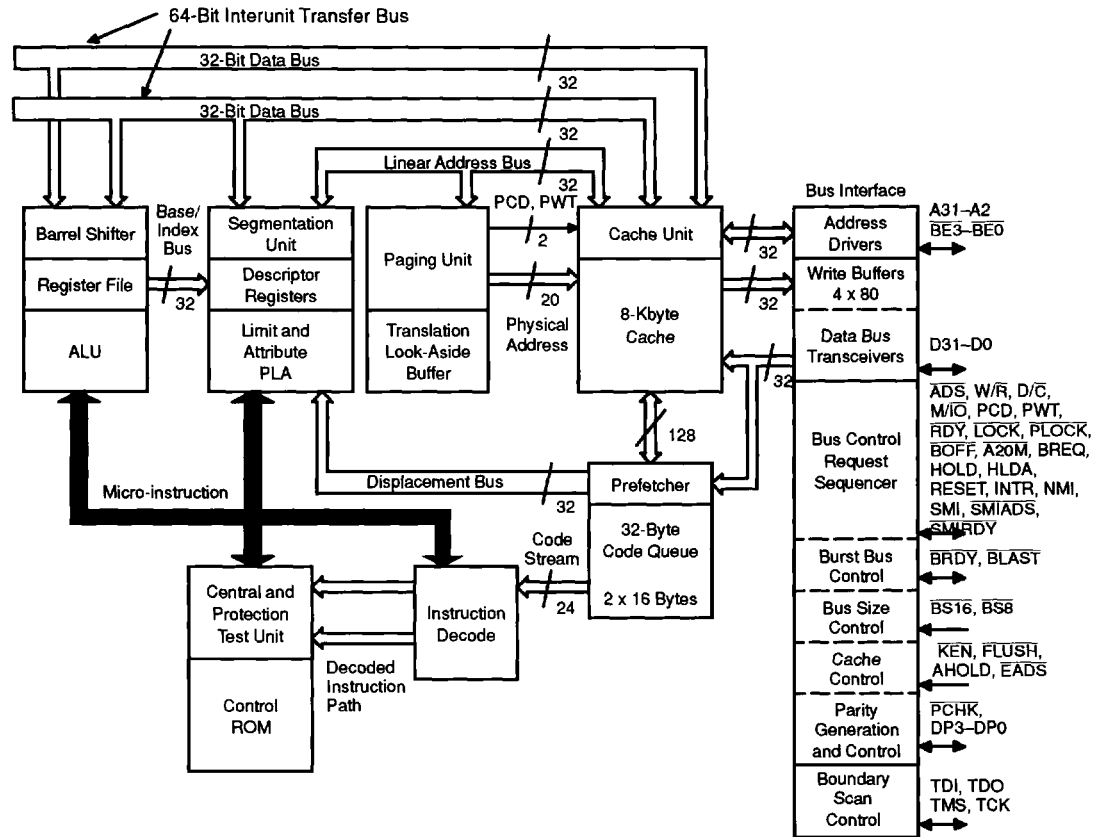
The Am486SXLV microprocessor features a static design that allows the clock to go to 0 MHz (DC) and

retain full register contents. The full static mode is achieved by operating the Am486SXLV microprocessor with a 2X clock input. The input frequency can be varied dynamically from maximum to full stop, or vice versa. The frequency change does not affect contents of the register and data integrity is maintained.

SMM is provided as a mechanism to interrupt the microprocessor operation and resume the interrupted operation transparent to the operating system or application running on the system. The Am486SXLV microprocessor supports Microsoft's Advanced Power Management specification for new "power managed" applications.

BLOCK DIAGRAM

Am486SXLV Microprocessor Pipeline 32-Bit Microarchitecture



17815A-001

PQFP Pin Designations (Functional Grouping)

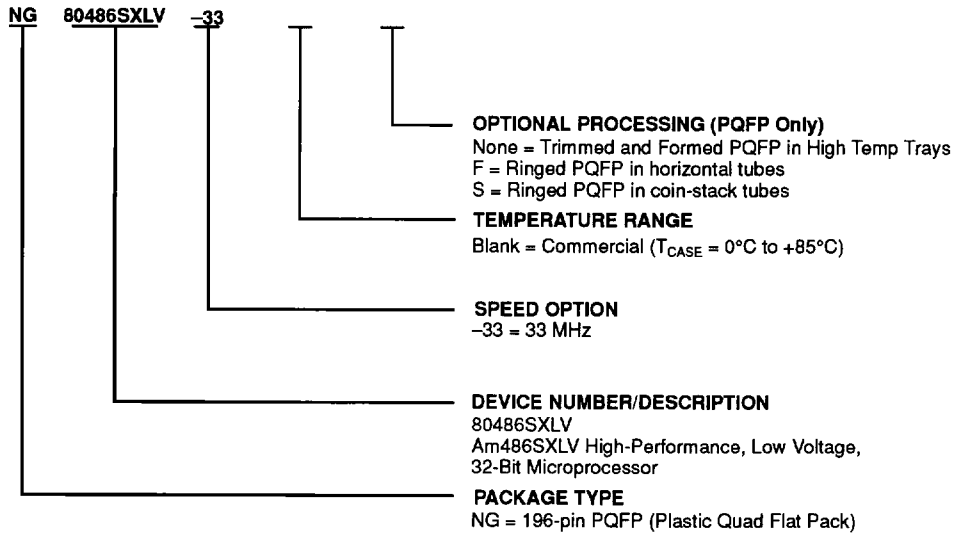
Address		Data		Control		Test		NC	V _{CC}	V _{SS}
Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin No.	Pin No.	Pin No.
A2	146	D0	17	A20M	104	TCK	128	15	6	1
A3	150	D1	18	ADS	145	TDI	185	34	19	11
A4	152	D2	20	AHOLD	129	TDO	80	52	24	21
A5	154	D3	23	BE0	117	TMS	187	56	28	22
A6	158	D4	25	BE1	116			60	36	33
A7	159	D5	26	BE2	115			64	49	40
A8	161	D6	27	BE3	113			68	54	50
A9	163	D7	29	BLAST	144			72	62	58
A10	165	D8	31	BOFF	137			73	70	66
A11	172	D9	32	BRDY	138			75	84	86
A12	174	D10	35	BREQ	118			76	93	95
A13	176	D11	37	BS8	135			77	98	96
A14	178	D12	38	BS16	136			78	107	99
A15	180	D13	39	CLK2	123			79	112	109
A16	181	D14	41	D/C	110			81	119	114
A17	183	D15	42	DP0	16			83	125	121
A18	189	D16	44	DP1	30			85	131	126
A19	191	D17	45	DP2	43			87	147	141
A20	193	D18	46	DP3	57			88	164	148
A21	2	D19	47	EADS	105			89	170	167
A22	3	D20	48	FLUSH	102			90	175	168
A23	4	D21	51	HLDA	122			91	179	177
A24	5	D22	53	HOLD	130			92	184	182
A25	7	D23	55	INTR	101			94	196	194
A26	8	D24	59	KEN	132			97		
A27	9	D25	61	LOCK	142			124		
A28	10	D26	63	M/IO	111			127		
A29	12	D27	65	NMI	100			149		
A30	13	D28	67	PCD	106			151		
A31	14	D29	69	PCHK	139			153		
		D30	71	PWT	108			155		
		D31	74	PLOCK	143			157		
				RDY	133			160		
				RESET	103			162		
				W/R	120			166		
				UP	156			169		
								171		
								173		
								186		
								188		
								190		
								192		
								195		

Superset Pins

SMM	
Pin Name	Pin No.
SMI	82
SMIADS	140
SMIRDY	134

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.



Valid Combinations		
NG	80486SXLV-33	F, S

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

PIN DESCRIPTIONS

A31–A4/A3–A2

Address Lines (Inputs/Outputs)/(Outputs)

A31–A2, together with the byte enables $\overline{BE3}$ – $\overline{BE0}$, define the physical area of memory or input/output space accessed. Address lines A31–A4 are used to drive addresses into the microprocessor to perform cache line invalidations. Input signals must meet setup and hold times t_{22} and t_{23} . A31–A2 are not driven during bus or address hold.

$\overline{A20M}$

Address Bit 20 Mask (Active Low; Input)

When asserted, the Am486SXLV microprocessor masks physical address bit 20 (A20) before performing a lookup to the internal cache or driving a memory cycle on the bus. $\overline{A20M}$ emulates the address wraparound at 1 Mbyte, which occurs on the 8086. $\overline{A20M}$ is active Low and should be asserted only when the processor is in Real Mode. This pin is asynchronous but should meet setup and hold times t_{20} and t_{21} for recognition in any specific clock. For proper operation, $\overline{A20M}$ should be sampled High at the falling edge of RESET.

\overline{ADS}

Address Status (Active Low; Output)

\overline{ADS} indicates that a valid bus cycle definition and address are available on the cycle definition lines and address bus. \overline{ADS} is driven active in the same clock as the addresses are driven. \overline{ADS} is active Low and is not driven during bus hold.

AHOLD

Address Hold (Input)

This request allows another bus master access to the Am486SXLV microprocessor's address bus for a cache invalidation cycle. The Am486SXLV microprocessor stops driving its address bus in the clock following AHOLD going active. Only the address bus is floated during address hold; the remainder of the bus remains active. AHOLD is active High and is provided with a small internal pull-down resistor. For proper operation, AHOLD must meet setup and hold times t_{18} and t_{19} .

$\overline{BE3}$ – $\overline{BE0}$

Byte Enables (Active Low; Outputs)

These pins indicate active bytes during read and write cycles. During the first cycle of a cache fill, the external system should assume that all byte enables are active. $\overline{BE3}$ applies to D31–D24, $\overline{BE2}$ applies to D23–D16, $\overline{BE1}$ applies to D15–D8, and $\overline{BE0}$ applies to D7–D0. $\overline{BE3}$ – $\overline{BE0}$ are active Low and are not driven during bus hold.

$\overline{BS8}$ / $\overline{BS16}$

Bus Size 8 (Active Low; Input)/ Bus Size 16 (Active Low; Input)

These input pins cause the Am486SXLV microprocessor to run multiple bus cycles to complete a request from devices that cannot provide or accept 32 bits of data in a single cycle. The bus sizing pins are sampled every clock. The state of these pins in the clock before \overline{RDY} is used by the Am486SXLV microprocessor to determine the bus size. These signals are active Low and are provided with internal pull-up resistors. These inputs must satisfy setup and hold times t_{14} and t_{15} for proper operation.

\overline{BLAST}

Burst Last (Active Low; Output)

\overline{BLAST} indicates that the next time \overline{BRDY} is returned, then the burst bus cycle is complete. \overline{BLAST} is active for both burst and non-burst bus cycles. \overline{BLAST} is active Low and is not driven during bus hold.

\overline{BOFF}

Backoff (Active Low; Input)

\overline{BOFF} forces the Am486SXLV microprocessor to float its bus in the next clock. The microprocessor floats all pins normally floated during bus hold, but HLDA is not asserted in response to \overline{BOFF} . \overline{BOFF} has higher priority than \overline{RDY} or \overline{BRDY} ; if both are returned in the same clock, \overline{BOFF} takes effect. The microprocessor remains in bus hold until \overline{BOFF} is negated. If a bus cycle was in progress when \overline{BOFF} was asserted, the cycle is restarted. \overline{BOFF} is active Low and must meet setup and hold times t_{18} and t_{19} for proper operation.

\overline{BRDY}

Burst Ready Input (Active Low; Input)

This input pin performs the same cycle during a burst cycle that \overline{RDY} performs during a non-burst cycle. \overline{BRDY} indicates that the external system has presented valid data in response to a read or that the external system has accepted data in response to write. \overline{BRDY} is ignored when the bus is idle and at the end of the first clock in a bus cycle.

\overline{BRDY} is sampled in the second and subsequent clocks of a burst cycle. The data presented on the data bus is strobed into the microprocessor when \overline{BRDY} is sampled active. If \overline{RDY} is returned simultaneously with \overline{BRDY} , \overline{BRDY} is ignored and the burst cycle is prematurely aborted.

\overline{BRDY} is active Low and is provided with a small pull-up resistor. \overline{BRDY} must satisfy the setup and hold times t_{16} and t_{17} .

BREQ**Internal Cycle Pending (Output)**

BREQ indicates that the Am486SXLV microprocessor has internally generated a bus request. BREQ is generated whether or not the Am486SXLV microprocessor is driving the bus. BREQ is active High and is never floated, except during three-state test mode (see $\overline{\text{FLUSH}}$).

CLK2**Clock (Input)**

CLK2 provides the fundamental timing for the Am486SXLV microprocessor. It is divided by 2 internally to generate the internal processor clock used for instruction execution. The internal clock is comprised of two phases, phase one and phase two. Each CLK2 period is a phase of the internal clock (see Figure 1). The phase of the internal processor clock can be synchronized to a known phase by ensuring the RESET signal falling edge meets its applicable setup and hold times t_{20} and t_{21} (see Figure 2). All setup, hold, float delay, and valid delay timings are references to phase one of the clock (see Figure 4). All I/O signals get sampled on the rising edge of the internal clock signal (i.e., the rising edge of phase one). Thus, it is important to synchronize the external circuitry with phase one of CLK2.

D31–D0**Data Lines (Inputs/Outputs)**

Lines D7–D0 define the least significant byte of the bus while lines D31–D24 define the most significant byte of the data bus. These signals must meet setup and hold times t_{22} and t_{23} for proper operation on reads. These pins are driven during the second and subsequent clocks of write cycles.

D/ $\overline{\text{C}}$ **Data/Control (Output)**

This bus cycle definition pin distinguishes data cycles, either memory or I/O, from control cycles. These control cycles are: interrupt acknowledge, halt, and instruction fetching.

DP3–DP0**Data Parity (Inputs/Outputs)**

Data parity is generated on all write data cycles with the same timing as the data driven by the Am486SXLV microprocessor. Even parity information must be driven back into the microprocessor on the data parity pins with the same timing as read information to ensure that the correct parity check status is indicated by the Am486SXLV microprocessor. The signals read on these pins do not affect program execution.

Input signals must meet setup and hold times t_{22} and t_{23} . DP3–DP0 should be connected to V_{CC} through a pull-up resistor in systems not using parity. DP3–DP0 are active High and are driven during the second and subsequent clocks of write cycles.

 $\overline{\text{EADS}}$ **Valid External Address (Active Low; Input)**

This pin indicates a valid external address has been driven onto the Am486SXLV microprocessor address pins. This address is used to perform an internal cache invalidation cycle. $\overline{\text{EADS}}$ is active Low and is provided with an internal pull-up resistor. $\overline{\text{EADS}}$ must satisfy setup and hold times t_{12} and t_{13} for proper operation.

 $\overline{\text{FLUSH}}$ **Cache Flush (Active Low; Input)**

$\overline{\text{FLUSH}}$ forces the Am486SXLV microprocessor to flush its entire internal cache. $\overline{\text{FLUSH}}$ is active Low and need only be asserted for one clock. $\overline{\text{FLUSH}}$ is asynchronous but setup and hold times t_{20} and t_{21} must be met for recognition in any specific clock. $\overline{\text{FLUSH}}$ being sampled Low in the clock before the falling edge of RESET causes the Am486SXLV microprocessor to enter the three-state test mode.

HLDA**Hold Acknowledge (Output)**

HLDA goes active in response to a hold request presented on the HOLD pin. HLDA indicates that the Am486SXLV microprocessor has given the bus to another local bus master. HLDA is driven active in the same clock that the Am486SXLV microprocessor floats its bus. HLDA is driven inactive when leaving bus hold. HLDA is active High and remains driven during bus hold. HLDA is never floated except during three-state test mode (see $\overline{\text{FLUSH}}$).

HOLD**Bus Hold Request (Input)**

This input pin allows another bus master complete control of the Am486SXLV microprocessor bus. In response to HOLD going active, the Am486SXLV microprocessor floats most of its output and input/output pins. HLDA is asserted after completing the current bus cycle, burst cycle, or sequence of locked cycles. The Am486SXLV microprocessor remains in this state until HOLD is deasserted. HOLD is active High and is not provided with an internal pull-down resistor. HOLD must satisfy setup and hold times t_{18} and t_{19} for proper operation.

INTR**Maskable Interrupt (Input)**

INTR indicates an external interrupt has been generated. If the internal interrupt flag is set in EFLAGS, active interrupt processing is initiated. The Am486SXLV microprocessor generates two locked interrupt acknowledge bus cycles in response to the INTR pin going active. INTR must remain active until the interrupt acknowledges have been performed to assure that the interrupt is recognized. INTR is active High and is not provided with an internal pull-down resistor. INTR is asynchronous, but must meet setup and hold times t_{20} and t_{21} for recognition in any specific clock.

\overline{KEN} **Cache Enable (Active Low; Input)**

\overline{KEN} is used to determine whether the current cycle is cacheable. When the Am486SXLV microprocessor generates a cacheable cycle and \overline{KEN} is active, the cycle becomes a cache line fill cycle. Returning \overline{KEN} active one clock before \overline{RDY} during the last read in the cache line fill causes the line to be placed in the on-chip cache. \overline{KEN} is active Low and is provided with a small internal pull-up resistor. \overline{KEN} must satisfy setup and hold times t_{14} and t_{15} for proper operation.

 \overline{LOCK} **Bus Lock (Active Low; Output)**

\overline{LOCK} indicates the current bus cycle is locked. The Am486SXLV microprocessor does not allow a bus hold when \overline{LOCK} is asserted (but address holds are allowed). \overline{LOCK} goes active in the first clock of the first locked bus cycle and goes inactive after the last clock of the last locked bus cycle. The last locked cycle ends when \overline{RDY} is returned. \overline{LOCK} is active Low and is not driven during bus hold. Locked read cycles are not transformed into cache fill cycles if \overline{KEN} is returned active.

 M/\overline{IO} **Memory/Input_Output (Output)**

This bus cycle definition pin distinguishes memory cycles from input/output cycles.

 \overline{NMI} **Non-maskable Interrupt (Input)**

This request signal indicates that an external non-maskable interrupt has been generated. \overline{NMI} is rising edge sensitive. \overline{NMI} must be held Low for at least four CLK2 periods before this rising edge. \overline{NMI} is not provided with an internal pull-down resistor. \overline{NMI} is asynchronous, but must meet setup and hold times t_{20} and t_{21} for recognition in any specific clock.

 $\overline{PCD}/\overline{PWT}$ **Page Cache Disable/Page Write-Through (Outputs)**

These reflect the state of the page attribute bits, \overline{PWT} and \overline{PCD} , in the page table entry or page directory entry. If paging is disabled or for unpaged cycles, \overline{PWT} and \overline{PCD} reflect the state of the \overline{PWT} and \overline{PCD} bits in Control Register 3. \overline{PWT} and \overline{PCD} have the same timing as the cycle definition pins (M/\overline{IO} , D/\overline{C} , and W/\overline{R}). \overline{PWT} and \overline{PCD} are active High and are not driven during bus hold. \overline{PCD} is masked by the Cache Disable Bit (CD) in Control Register 0.

 \overline{PCHK} **Parity Status (Active Low; Output)**

Parity status is driven on the \overline{PCHK} pin the clock after \overline{RDY} for read operations. The parity status is for data sampled at the end of the previous clock. A parity error is indicated by \overline{PCHK} being Low. Parity status is only checked for enabled bytes as indicated by the byte

enable and bus size signals. \overline{PCHK} is valid only in the clock immediately after read data is returned to the microprocessor. At all other times \overline{PCHK} is inactive High. \overline{PCHK} is never floated except during three-state test mode (see FLUSH).

 \overline{PLOCK} **Pseudo-lock (Active Low; Output)**

\overline{PLOCK} indicates that the current bus transaction requires more than one bus cycle to complete. Examples of such operations are segment table descriptor reads (64 bits) and cache line fills (128 bits). The Am486SXLV microprocessor drives \overline{PLOCK} active until the addresses for the last bus cycle of the transaction have been driven, regardless of whether \overline{RDY} or \overline{BRDY} have been returned.

\overline{PLOCK} is a function of the $\overline{BS8}$, $\overline{BS16}$, and \overline{KEN} inputs. \overline{PLOCK} should be sampled only if the clock \overline{RDY} is returned. \overline{PLOCK} is active Low and is not driven during bus hold.

 \overline{RESET} **Reset (Input)**

This pin forces the Am486SXLV microprocessor to begin execution at a known state. The microprocessor cannot begin execution of instructions until at least 1 ms after V_{CC} and CLK2 have reached their proper DC and AC specifications. The \overline{RESET} pin should remain active during this time to ensure proper microprocessor operation. \overline{RESET} is active High. \overline{RESET} is asynchronous but must meet setup and hold times t_{20} and t_{21} for recognition in any specific clock.

 \overline{RDY} **Non-burst Ready (Active Low; Input)**

This input pin indicates that the current bus cycle is complete. \overline{RDY} indicates that the external system has presented valid data on the data pins in response to a read, or that the external system has accepted data from the Am486SXLV microprocessor in response to a write. \overline{RDY} is ignored when the bus is idle and at the end of the bus cycle's first clock.

\overline{RDY} is active during address hold. Data can be returned to the processor while \overline{AHOLD} is active.

\overline{RDY} is active Low and is not provided with an internal pull-up resistor. \overline{RDY} must satisfy setup and hold times t_{16} and t_{17} for proper chip operation.

 \overline{SMI} **System Management Interrupt (Active Low; Async Input)**

This pin is the highest level, non-maskable interrupt to the Am486SXLV CPU that is driven by the system logic of the Am486SXLV CPU. The system logic must assert \overline{SMI} synchronously to CLK2. When this signal is activated by the system logic, the Am486SXLV microprocessor suspends normal execution and enters SMM. When the CPU rec-

ognizes the interrupt (with an active $\overline{\text{SMIADS}}$ pulse), the CPU drives $\overline{\text{SMI}}$ active Low. The CPU continues to drive $\overline{\text{SMI}}$ Low until it exits SMM via a RESET or RES4 instruction (when the system asserts RESET, it must also release $\overline{\text{SMI}}$ to prevent buffer contention). When exiting SMM, the CPU drives $\overline{\text{SMI}}$ high for two clocks and then releases $\overline{\text{SMI}}$ to a weak internal pull-up resistor. The $\overline{\text{SMI}}$ pull-up is active during RESET and whenever the CPU is not driving $\overline{\text{SMI}}$ active Low. The CPU disables the pull-up when it drives $\overline{\text{SMI}}$ active to minimize CPU power consumption. $\overline{\text{SMI}}$ is not three-stated during HLDA bus cycles. *Note: $\overline{\text{SMI}}$ should not be used to qualify SMM accesses.*

$\overline{\text{SMIADS}}$

SMI Address Status

(Active Low; Three-State; Output)

The Am486 CPU activates this pin to initiate a valid bus cycle to the separate SMM memory space. The function of $\overline{\text{SMIADS}}$ is analogous to $\overline{\text{ADS}}$. This signal validates the address and control lines for SMM memory, just as $\overline{\text{ADS}}$ validates address and control for non-SMM memory cycles. The system must terminate $\overline{\text{SMIADS}}$ initiated bus cycles with $\overline{\text{SMIRDY}}$. The Am486 CPU ignores both $\overline{\text{RDY}}$ and $\overline{\text{BRDY}}$ on $\overline{\text{SMIADS}}$ initiated cycles. This three-state output is floated during HLDA bus cycles.

$\overline{\text{SMIRDY}}$

SMI Ready (Active Low; Synchronous Input)

This input terminates the current bus cycle that $\overline{\text{SMIADS}}$ initiated in the same manner as $\overline{\text{RDY}}$ terminates $\overline{\text{ADS}}$ initiated bus cycles. The system must assert and deassert $\overline{\text{SMIRDY}}$ synchronously to CLK2. The Am486 CPU ignores $\overline{\text{SMIRDY}}$ on $\overline{\text{ADS}}$ initiated cycles. $\overline{\text{SMIRDY}}$ has an internal pull-down resistor. This is different from the Am386[®] CPU $\overline{\text{SMIRDY}}$ which has an internal pull-up resistor. $\overline{\text{SMIRDY}}$ should not be physically connected to $\overline{\text{RDY}}$.

TCK

Test Clock (Input)

Test Clock is an input to the Am486SXLV CPU and provides the clocking function required by the JTAG boundary scan feature. TCK is used to clock state information and data into and out of the component. State select information

and data are clocked into the component on the rising edge of TCK on TMS and TDI, respectively. Data is clocked out of the component on the falling edge of TCK on TDO.

TDI

Test Data Input (Input)

TDI is the serial input used to shift JTAG instructions and data into the component. TDI is sampled on the rising edge of TCK, during the SHIFT-IR and the SHIFT-DR TAP controller states. During all other tap controller states, TDI is a "don't care."

TDO

Test Data Output (Output)

TDO is the serial output used to shift JTAG instructions and data out of the component. TDO is driven on the falling edge of TCK during the SHIFT-IR and SHIFT-DR TAP controller states. At all other times, TDO is driven to the high impedance state.

TMS

Test Mode Select (Input)

TMS is decoded by the JTAG TAP (Tap Access Port) to select the operation of the test logic. TMS is sampled on the rising edge of TCK. To guarantee deterministic behavior of the TAP controller, TMS is provided with an internal pull-up resistor.

$\overline{\text{UP}}$

Upgrade Present (Input)

The Upgrade Present pin forces the CPU to three-state all its outputs and enter the power-down mode. When the Upgrade Present pin is sampled asserted by the CPU in the clock before the falling edge of RESET, the power-down mode is enabled. $\overline{\text{UP}}$ has no effect on the power-down status except during this edge. The CPU is also forced to three-state all of its outputs immediately in response to this signal. The $\overline{\text{UP}}$ signal must remain asserted in order to keep the pins three-stated. $\overline{\text{UP}}$ is active Low and is provided with an internal pull-up resistor.

$\overline{\text{W/R}}$

Write/Read (Output)

This bus definition pin distinguishes write cycles from read cycles.

SWITCHING CHARACTERISTICS

The switching characteristics consist of output delays, input set-up requirements, and input hold requirements. All switching characteristics are relative to the rising edge of the CLK2 signal.

Switching characteristics measurement is defined by 3 through 5. Inputs must be driven to the voltage levels indicated by 5 when switching characteristics are measured. Am486SXLV microprocessor output delays are speci-

fied with minimum and maximum limits, measured as shown. The minimum Am486SXLV microprocessor delay times are hold times provided to external circuitry. Am486SXLV microprocessor input setup and hold times are specified as minimums, defining the smallest acceptable sampling windows. Within the sampling windows, a synchronous input signal must be stable for correct Am486SXLV microprocessor operation.





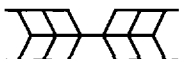
SWITCHING CHARACTERISTICS over COMMERCIAL operating rangesSwitching Characteristics at 33 MHz: 3.3 V \pm 0.3 V; $T_{CASE} = 0^{\circ}\text{C}$ to $+85^{\circ}\text{C}$; $C_L = 50$ pF unless otherwise specified.

Symbol	Parameter Description	Notes	Figure	Preliminary		Unit
				Min	Max	
	Operating Frequency	Half CLK2 Frequency		0	33.3	MHz
t_1	CLK2 Period		3	15		ns
t_2	CLK2 High Time	@ 2.0 V	3	5		ns
t_3	CLK2 Low Time	@ 0.8 V	3	5		ns
t_4	CLK2 Fall Time		3		5	ns
t_5	CLK2 Rise Time		3		5	ns
t_6	A31–A2, PWT, PCD, M/ $\overline{\text{IO}}$, $\overline{\text{BE3}}\text{--}\overline{\text{BE0}}$, D/ $\overline{\text{C}}$, W/ $\overline{\text{R}}$, $\overline{\text{ADS}}$, $\overline{\text{LOCK}}$, BREQ, HLDA Valid Delay		4	3	19	ns
t_{6s}	$\overline{\text{SMIADS}}$ Valid Delay	$C_L = 50$ pF	4	3	19	ns
t_7	A31–A2, PWT, PCD, M/ $\overline{\text{IO}}$, $\overline{\text{BE3}}\text{--}\overline{\text{BE0}}$, D/ $\overline{\text{C}}$, W/ $\overline{\text{R}}$, $\overline{\text{ADS}}$, $\overline{\text{LOCK}}$ Float Delay	(Note 1)	4		20	ns
t_{7s}	$\overline{\text{SMIADS}}$ Float Delay	(Note 1)	4		20	ns
t_8	$\overline{\text{PCHK}}$ Valid Delay		4	3	22	ns
t_{8a}	$\overline{\text{BLAST}}$, $\overline{\text{PLOCK}}$ Valid Delay		4	3	20	ns
t_9	$\overline{\text{BLAST}}$, $\overline{\text{PLOCK}}$ Float Delay	(Note 1)	4		20	ns
t_{10}	D31–D0, DP3–DP0 Write Data Valid Delay		4	3	18	ns
t_{11}	D31–D0, DP3–DP0 Write Data Float Delay	(Note 1)	4		20	ns
t_{12}	$\overline{\text{EADS}}$ Setup Time		5	5		ns
t_{13}	$\overline{\text{EADS}}$ Hold Time		5	4		ns
t_{14}	KEN, $\overline{\text{BS16}}$, $\overline{\text{BS8}}$ Setup Time		5	5		ns
t_{15}	KEN, $\overline{\text{BS16}}$, $\overline{\text{BS8}}$ Hold Time		5	4		ns
t_{16}	$\overline{\text{RDY}}$, $\overline{\text{BRDY}}$ Setup Time		5	5		ns
t_{16s}	$\overline{\text{SMIRDY}}$ Setup Time		5	5		ns
t_{17}	$\overline{\text{RDY}}$, $\overline{\text{BRDY}}$ Hold Time		5	4		ns
t_{17s}	$\overline{\text{SMIRDY}}$ Hold Time		5	4		ns
t_{18}	HOLD, $\overline{\text{AHOLD}}$ Setup Time		5	6		ns
t_{18a}	$\overline{\text{BOFF}}$ Setup Time		5	8		ns
t_{19}	HOLD, $\overline{\text{AHOLD}}$, $\overline{\text{BOFF}}$ Hold Time		5	4		ns
t_{20}	RESET, FLUSH, $\overline{\text{A20M}}$, NMI, INTR Setup Time		2, 5	5		ns
t_{20s}	$\overline{\text{SMI}}$ Setup Time		2, 5	5		ns
t_{21}	RESET, FLUSH, $\overline{\text{A20M}}$, NMI, INTR Hold Time		2, 5	4		ns
t_{21s}	$\overline{\text{SMI}}$ Hold Time		2, 5	4		ns
t_{22}	D31–D0, DP3–DP0, A31–A4 Read Setup Time		5	5		ns
t_{23}	D31–D0, DP3–DP0, A31–A4 Read Hold Time		5	6		ns

Note:

1. Not 100% tested. Guaranteed by design characterization.

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010

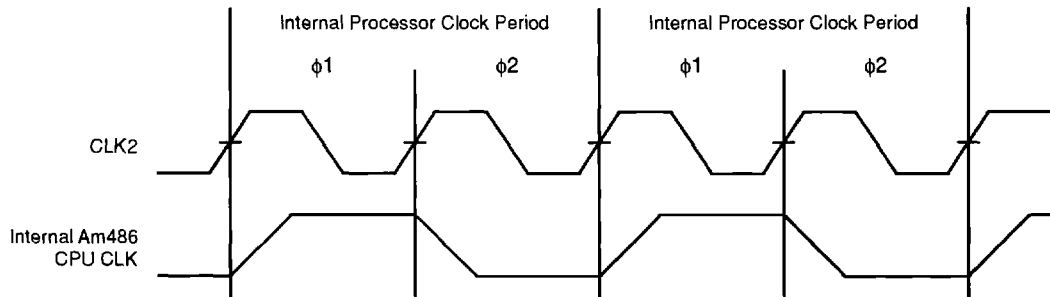
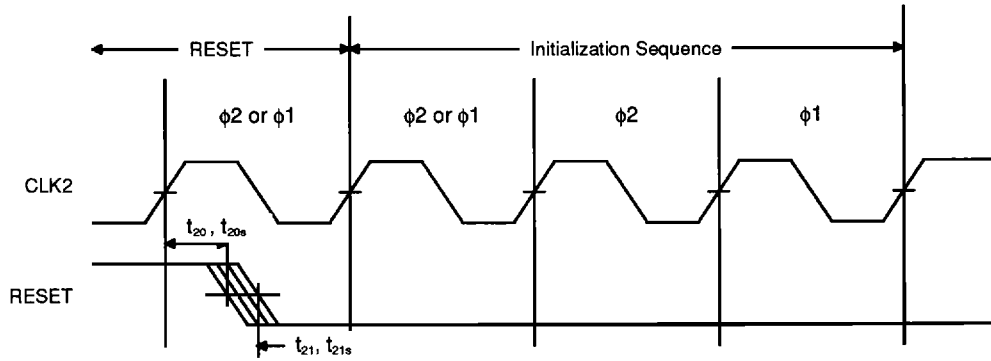


Figure 1. CLK2 Signal and Internal Processor Clock



Note:
 The second internal processor phase following RESET High-to-Low transition (provided t_{20} and t_{21} are met) is $\phi 2$.

Figure 2. RESET Setup and Hold Timing, and Internal Phase

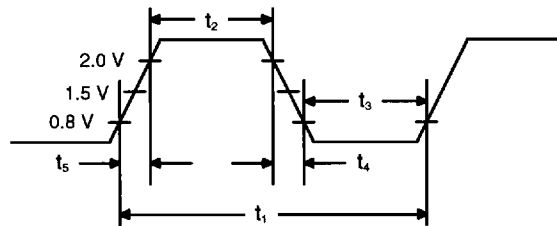


Figure 3. CLK2 Waveforms

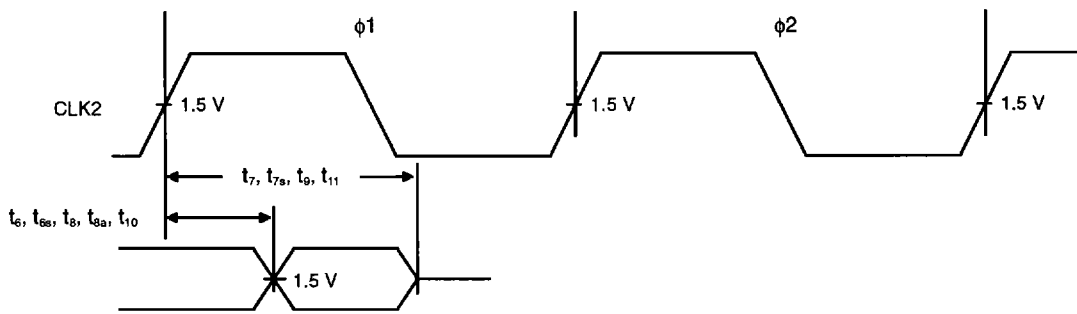
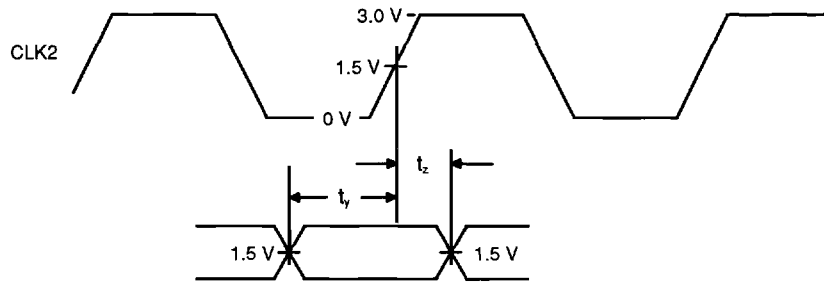


Figure 4. Output Waveforms



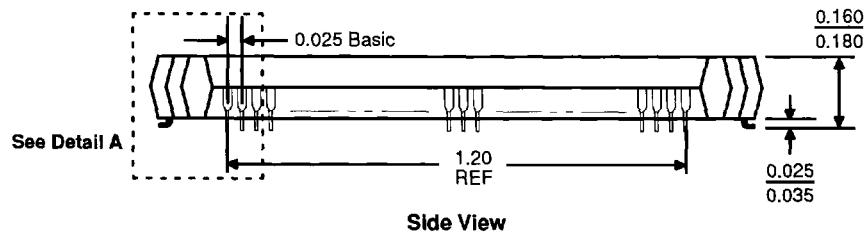
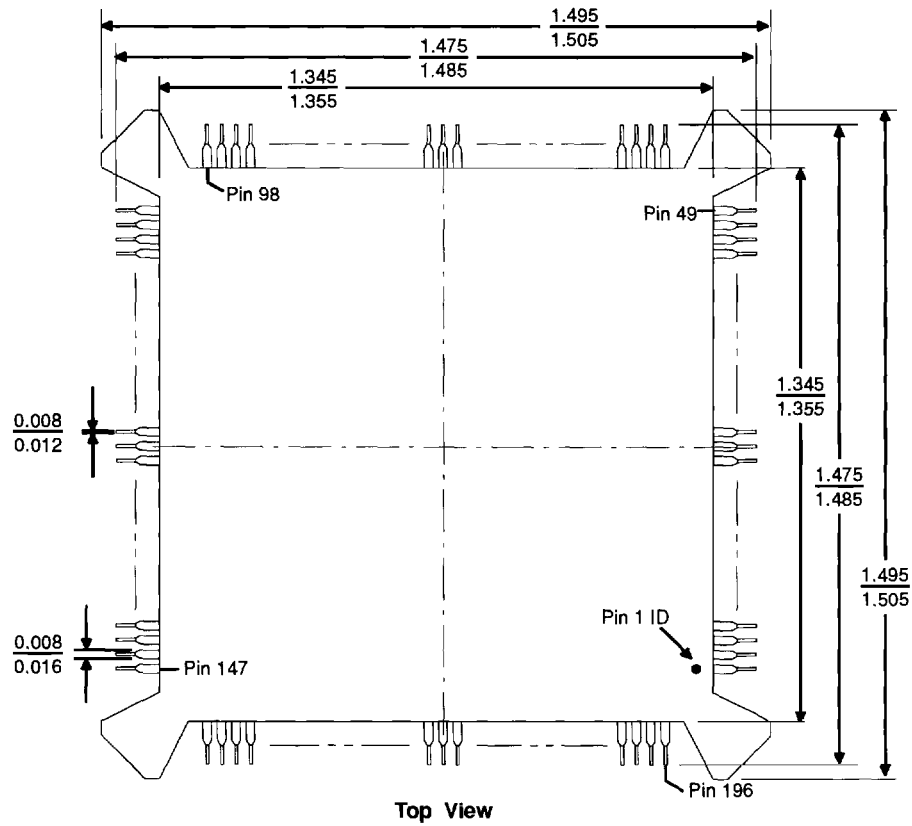
$t_y = t_{12}, t_{14}, t_{16}, t_{16a}, t_{18}, t_{18a}, t_{20}, t_{20a}, t_{22}$
 $t_z = t_{13}, t_{15}, t_{17}, t_{17a}, t_{19}, t_{21}, t_{21a}, t_{23}$

Figure 5. Input Waveforms

PHYSICAL DIMENSIONS

PQB 196

Plastic Quad Flat Pack; Trimmed and Formed (Measured in Inches)

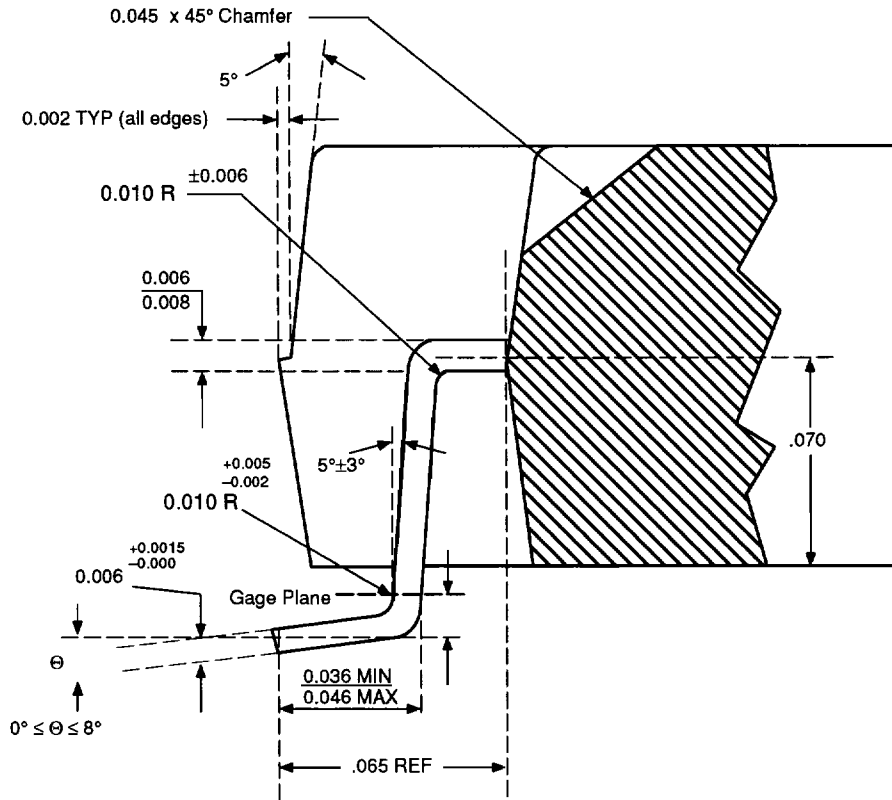


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CL85
04/9/93 MB

1.
For reference only. BSC is an ANSI standard for Basic Space Centering.

PHYSICAL DIMENSIONS (continued)

PQB 196—Plastic Quad Flat Pack; Trimmed and Formed (continued)



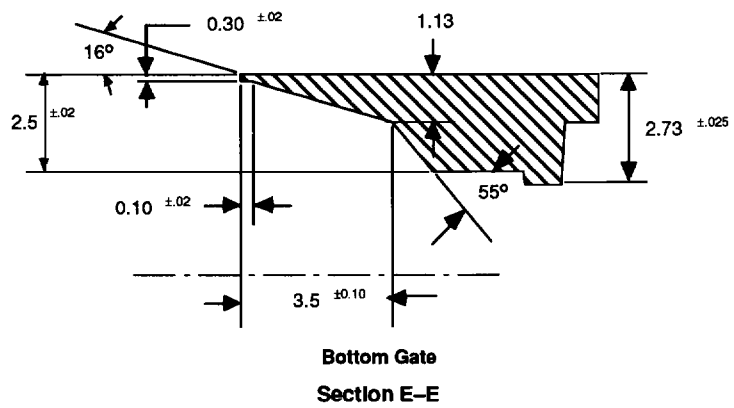
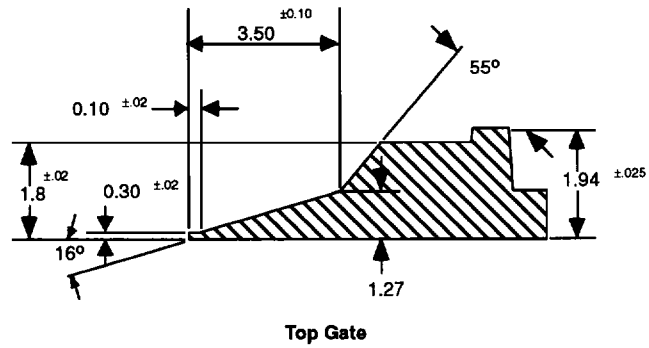
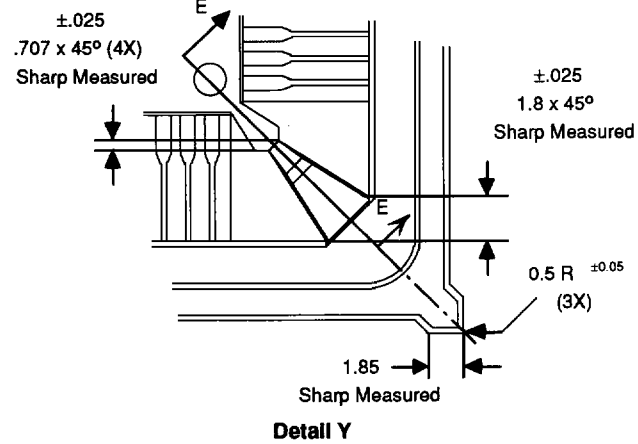
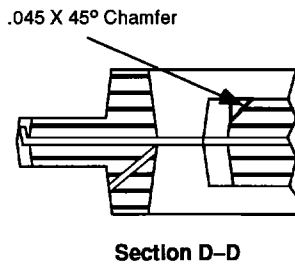
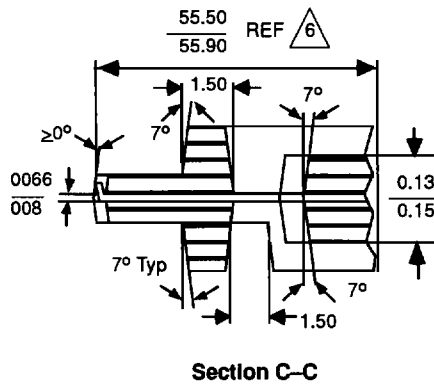
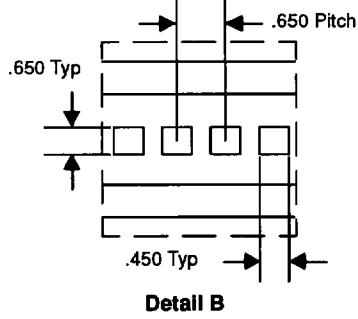
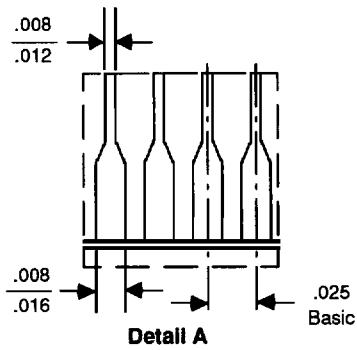
Detail A

Notes:

1. All dimensions are in inches.
2. Dimensions do not include mold protrusion.
3. Coplanarity of all leads will be within 0.004 inches measured from the seating plan. Coplanarity is measured per specification 06-500.
4. Deviation from lead-tip true position shall be within ± 0.003 inches.
5. Half span (center of package to lead-tip) shall be within ± 0.0085 inches.

PHYSICAL DIMENSIONS (continued)

PQB 196—Plastic Quad Flat Pack with Molded Carrier Ring (continued)



PHYSICAL DIMENSIONS (continued)
PQB 196—Plastic Quad Flat Pack with Molded Carrier Ring (continued)**Notes:**

1. All dimensions and tolerances conform to ANSI Y14.5M-1982.
2. Controlling dimensions: package is measured in inches and ring is measured in millimeters.
3. These dimensions do not include mold protrusion. Allowable mold protrusion is 0.2 mm per side.
4. These dimensions include mold mismatch and are measured at the parting line.
5. Dimensions are centered about centerline of lead material.
6. These dimensions are from the outside edge to the outside edge of the test points.
7. There are six locating holes in the ring. -B- and -C- datum holes are used for trim form and excise of the molded package only. Holes Z1 and Z2 are used for electrical testing only.
8. This area is reserved for vacuum pickup on each of the four corners of the ring and must be flat within 0.025 mm. No ejector pins in this area.
9. Datum -A- surface for seating in socket applications.
10. Pin one orientation with respect to carrier ring as indicated.